

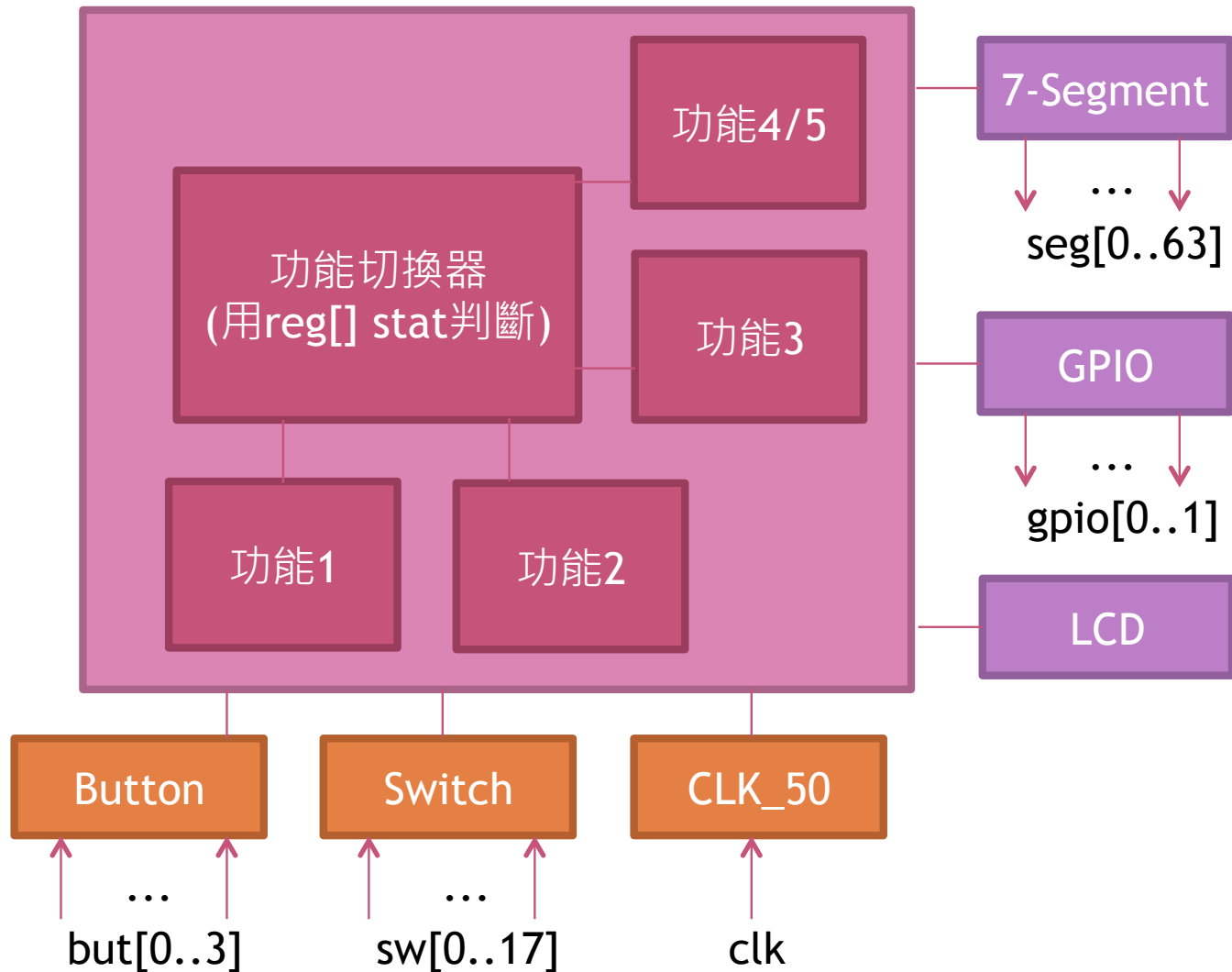
# DSL EXPERIMENT 2

Team B9

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# HARDWARE BLOCK DIAGRAM



# PORT NAMING

Signal	Naming
*INPUT	
Seven Segment Digit	seg[63:0]
GPIO	gpio[1:0]
CLK_50	clk
Pushdown Switch	sw[17:0]
*OUTPUT	
Button	but[3:0]
LCD Data	lcdd[7:0]
LCD RW/EN/RS	lcdc[2:0]

# PIN MAPPING DESCRIPTION(1/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
but[3]	Input	PIN_U29	6	B6_N0		
but[2]	Input	PIN_U30	6	B6_N0		
but[1]	Input	PIN_T28	6	B6_N0		
but[0]	Input	PIN_T29	6	B6_N0		
clk	Input	PIN_AD15	7	B7_N3		
gpio[1]	Output	PIN_G27	5	B5_N1		
gpio[0]	Output	PIN_C30	5	B5_N0		
lcdc[2]	Output	PIN_F3	2	B2_N0		
lcdc[1]	Output	PIN_E2	2	B2_N1		
lcdc[0]	Output	PIN_F2	2	B2_N2		
lcdd[7]	Output	PIN_B2	2	B2_N0		
lcdd[6]	Output	PIN_C3	2	B2_N0		

# PIN MAPPING DESCRIPTION(2/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
lcdd[5]	Output	PIN_C2	2	B2_N0		
lcdd[4]	Output	PIN_C1	2	B2_N0		
lcdd[3]	Output	PIN_D3	2	B2_N1		
lcdd[2]	Output	PIN_D2	2	B2_N1		
lcdd[1]	Output	PIN_E3	2	B2_N0		
lcdd[0]	Output	PIN_E1	2	B2_N1		
seg[63]	Output	PIN_AF12	8	B8_N1		
seg[62]	Output	PIN_AD12	8	B8_N1		
seg[61]	Output	PIN_AD11	8	B8_N2		
seg[60]	Output	PIN_AF10	8	B8_N2		
seg[59]	Output	PIN_AD10	8	B8_N2		
seg[58]	Output	PIN_AH9	8	B8_N1		

# PIN MAPPING DESCRIPTION(3/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
seg[57]	Output	PIN_AF9	8	B8_N2		
seg[56]	Output	PIN_AE8	8	B8_N3		
seg[55]	Output	PIN_AC17	7	B7_N2		
seg[54]	Output	PIN_AD17	7	B7_N2		
seg[53]	Output	PIN_AF17	7	B7_N2		
seg[52]	Output	PIN_AE17	7	B7_N3		
seg[51]	Output	PIN_AG16	7	B7_N3		
seg[50]	Output	PIN_AF16	7	B7_N3		
seg[49]	Output	PIN_AE16	7	B7_N3		
seg[48]	Output	PIN_AG13	8	B8_N0		
seg[47]	Output	PIN_AC19	7	B7_N1		
seg[46]	Output	PIN_AE19	7	B7_N1		

# PIN MAPPING DESCRIPTION(4/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
seg[45]	Output	PIN_AB19	7	B7_N1		
seg[44]	Output	PIN_AB18	7	B7_N1		
seg[43]	Output	PIN_AG4	8	B8_N3		
seg[42]	Output	PIN_AH5	8	B8_N3		
seg[41]	Output	PIN_AF7	8	B8_N3		
seg[40]	Output	PIN_AE7	8	B8_N3		
seg[39]	Output	PIN_M4	2	B2_N3		
seg[38]	Output	PIN_M6	2	B2_N2		
seg[37]	Output	PIN_M7	2	B2_N2		
seg[36]	Output	PIN_M8	2	B2_N1		
seg[35]	Output	PIN_N7	2	B2_N2		
seg[34]	Output	PIN_N10	2	B2_N2		

# PIN MAPPING DESCRIPTION(5/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
seg[33]	Output	PIN_P4	2	B2_N3		
seg[32]	Output	PIN_P6	2	B2_N3		
seg[31]	Output	PIN_L6	2	B2_N1		
seg[30]	Output	PIN_M2	2	B2_N3		
seg[29]	Output	PIN_M1	2	B2_N3		
seg[28]	Output	PIN_N3	2	B2_N3		
seg[27]	Output	PIN_N2	2	B2_N3		
seg[26]	Output	PIN_P3	2	B2_N3		
seg[25]	Output	PIN_P2	2	B2_N3		
seg[24]	Output	PIN_P1	2	B2_N3		
seg[23]	Output	PIN_K6	2	B2_N1		
seg[22]	Output	PIN_K5	2	B2_N1		



# PIN MAPPING DESCRIPTION(6/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
seg[21]	Output	PIN_K4	2	B2_N2		
seg[20]	Output	PIN_K1	2	B2_N2		
seg[19]	Output	PIN_L3	2	B2_N2		
seg[18]	Output	PIN_L2	2	B2_N3		
seg[17]	Output	PIN_L1	2	B2_N3		
seg[16]	Output	PIN_M3	2	B2_N3		
seg[15]	Output	PIN_K2	2	B2_N2		
seg[14]	Output	PIN_E4	2	B2_N0		
seg[13]	Output	PIN_F4	2	B2_N0		
seg[12]	Output	PIN_G4	2	B2_N0		
seg[11]	Output	PIN_H8	2	B2_N0		
seg[10]	Output	PIN_H7	2	B2_N0		

# PIN MAPPING DESCRIPTION(7/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
seg[9]	Output	PIN_H4	2	B2_N1		
seg[8]	Output	PIN_H6	2	B2_N0		
seg[7]	Output	PIN_G2	2	B2_N2		
seg[6]	Output	PIN_G1	2	B2_N2		
seg[5]	Output	PIN_H3	2	B2_N1		
seg[4]	Output	PIN_H2	2	B2_N2		
seg[3]	Output	PIN_H1	2	B2_N2		
seg[2]	Output	PIN_J2	2	B2_N2		
seg[1]	Output	PIN_J1	2	B2_N2		
seg[0]	Output	PIN_K3	2	B2_N2		
sw[17]	Input	PIN_L8	2	B2_N1		
sw[16]	Input	PIN_L7	2	B2_N1		

# PIN MAPPING DESCRIPTION(8/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
sw[15]	Input	PIN_L4	2	B2_N2		
sw[14]	Input	PIN_L5	2	B2_N1		
sw[13]	Input	PIN_T9	1	B1_N0		
sw[12]	Input	PIN_U9	1	B1_N0		
sw[11]	Input	PIN_V10	1	B1_N1		
sw[10]	Input	PIN_W5	1	B1_N1		
sw[9]	Input	PIN_AE27	6	B6_N2		
sw[8]	Input	PIN_AD24	6	B6_N3		
sw[7]	Input	PIN_AD25	6	B6_N3		
sw[6]	Input	PIN_AC23	6	B6_N3		
sw[5]	Input	PIN_AC24	6	B6_N3		
sw[4]	Input	PIN_AC26	6	B6_N3		

# PIN MAPPING DESCRIPTION(9/9)

To	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
sw[3]	Input	PIN_AC27	6	B6_N2		
sw[2]	Input	PIN_AB25	6	B6_N2		
sw[1]	Input	PIN_AB26	6	B6_N2		
sw[0]	Input	PIN_AA23	6	B6_N2		

# TIPS TO REDUCE RESOURCE UTILIZATION(1/3)

## ◎ Tip1:

- 盡量少用除法
- 例如功能1中，計數器是用兩個4-bit-register紀錄，如此顯示時完全不會應用到除法
- 證明: 除法是個非常複雜的操作，需要使用到相當大的resource數目，當我們把功能1中的除法器改成兩個4-bit-register，整個resource數目減少了約莫1000。

# TIPS TO REDUCE RESOURCE UTILIZATION(2/3)

## ◎ Tip2:

- 不要把太複雜的東西用For迴圈
- 例如說在功能3中，LCD顯示的延遲便是直接把Code展開，而不是用迴圈進行
- 證明: 因為For迴圈需要把整個Block包起來，若For內的東西過於複雜可能會造成許多resource的浪費；另外編譯器也可能會把For迴圈展開，如此和直接條列並無差別

# TIPS TO REDUCE RESOURCE UTILIZATION(3/3)

## ◎ Tip3:

- 減少給硬體做的計算量
- 例如說在功能4/5中，要計算active的duration，本可以用頻率/100\*(duty cycle)，但是選擇直接使用8個if來進行判斷
- 證明: 給硬體做計算是很複雜的，例如說上面要用到一個除法器跟一個乘法器，雖然if看起來很多但實際上resource少很多。