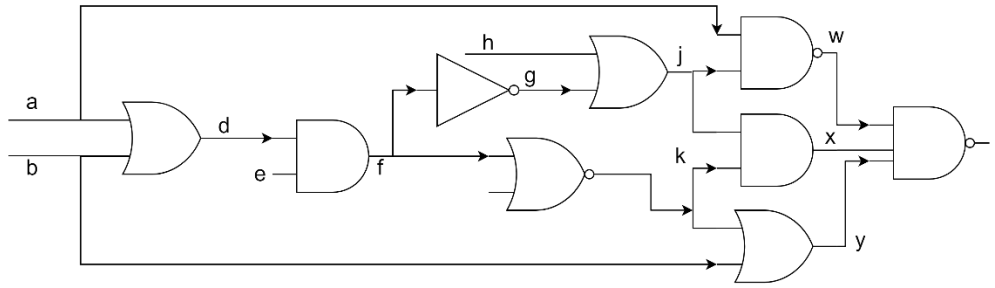
DFT Assignment-2

Instructions:

- Consider the Combinational Logic and write a Verilog/VHDL gate level code and testbench.
- Generate a table for all the test vectors and output patterns for all the stuck-at-faults (s-a-f) at the checkpoints.
- See if you could bypass any test vector to have a minimum number of vectors to detect all the faults. State the reasons for bypassing the vectors.
- Submit all codes and reports on Moodle.
- This is a team assignment; each team(4 students per team) is assigned one circuit (kindly check the Moodle post for Question No.)
- **Deadline: 6th Oct 2022 11:59 PM**

1.



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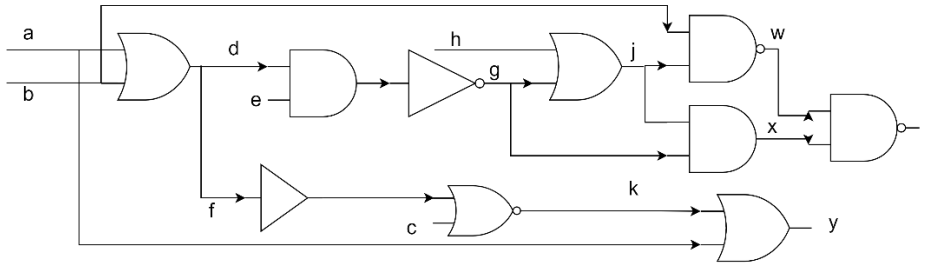

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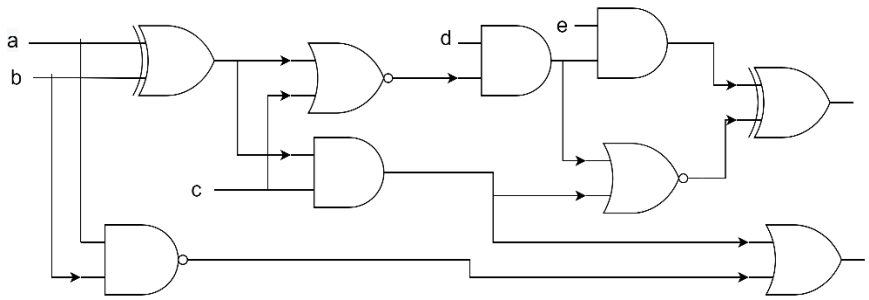

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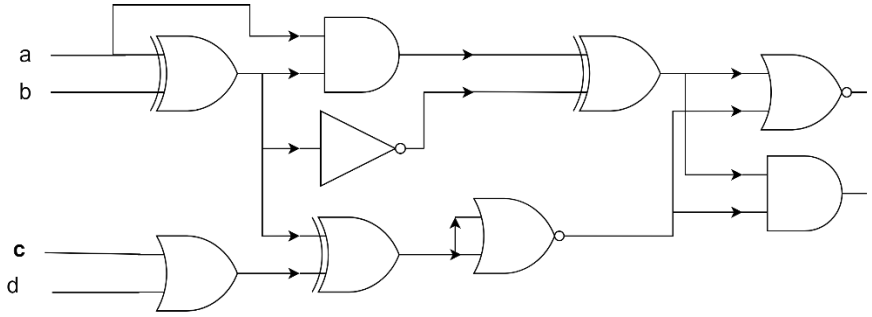

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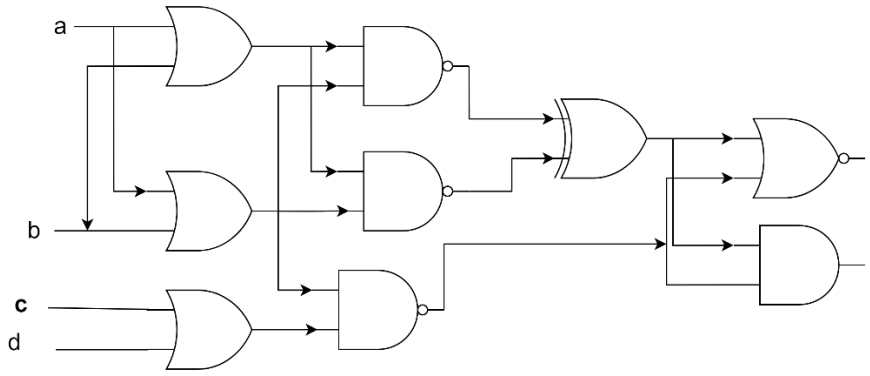

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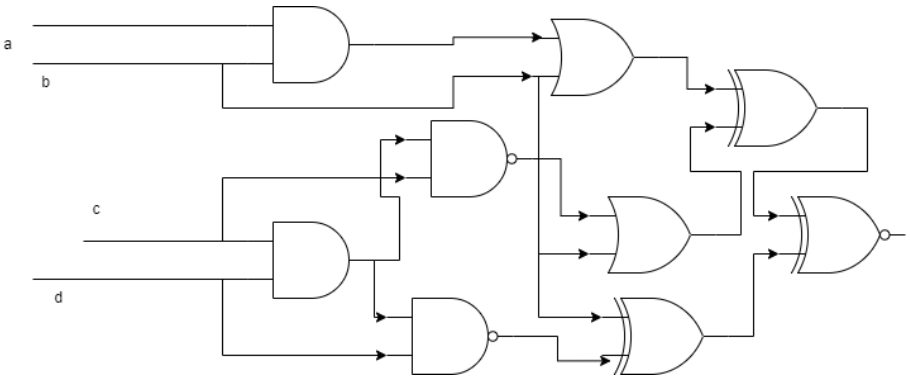

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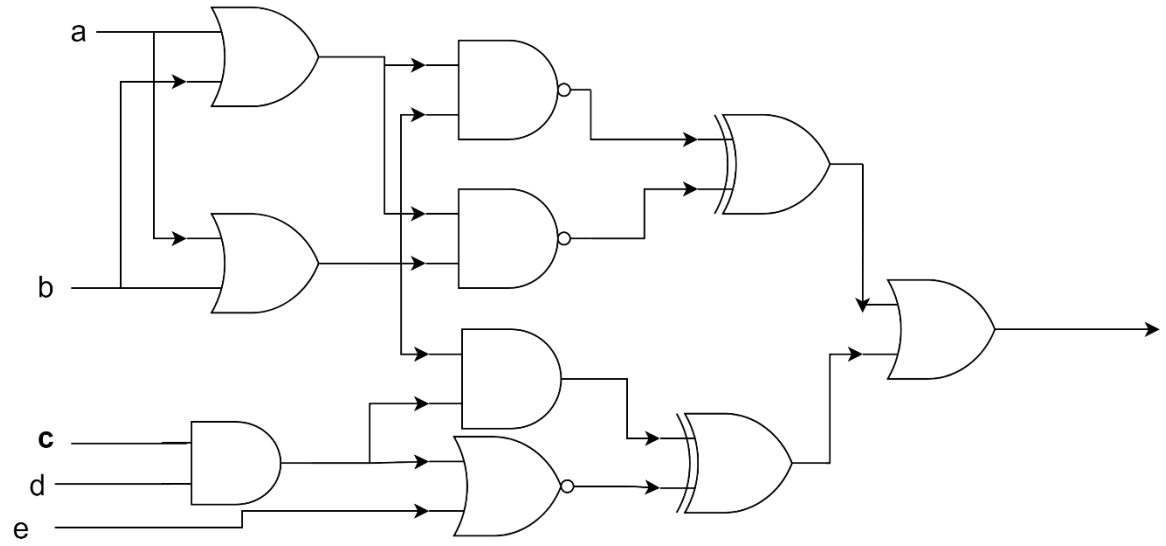

8.