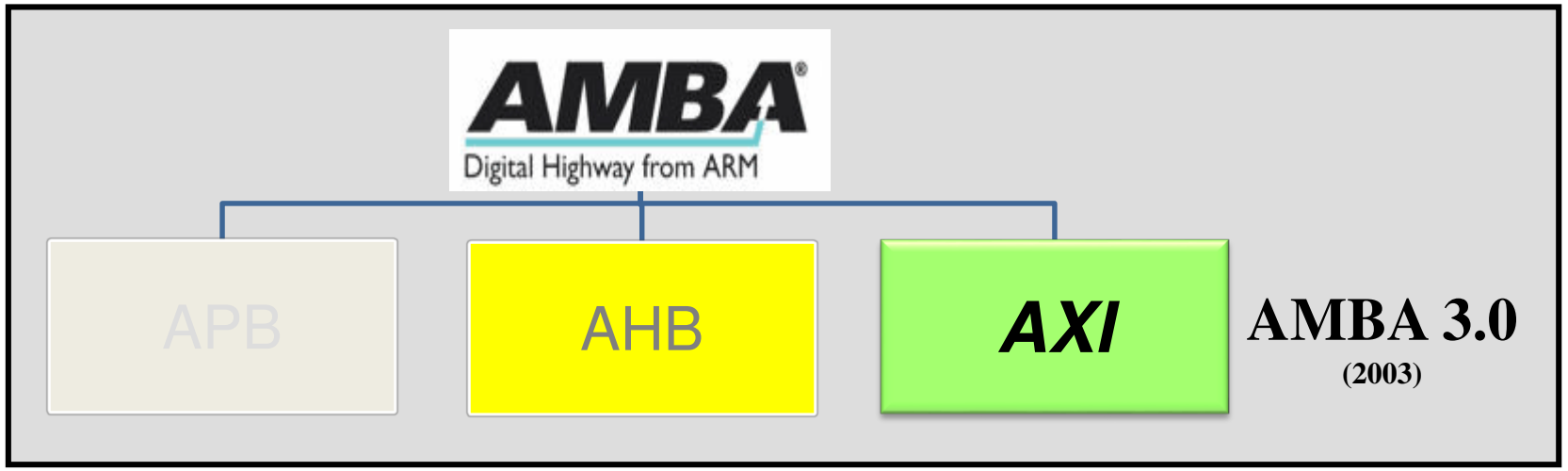
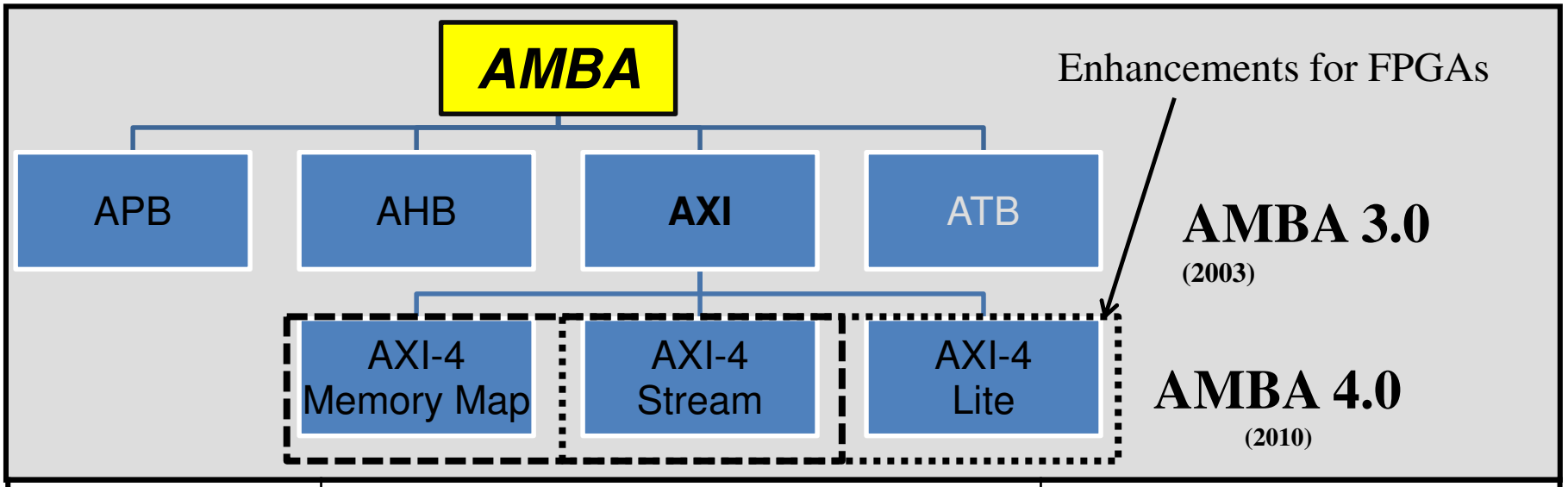
AXI is Part of ARM's AMBA



AMBA: Advanced Microcontroller Bus Architecture
AXI: Advanced Extensible Interface

AXI-4 (Full, Lite and Stream)



Interface	Features	Similar to
Memory Map / Full (AXI4)	Traditional Address/Data Burst (single address, multiple data)	PLBv46, PCI
Streaming (AXI4-Stream)	Data-Only, Burst	Local Link / DSP Interfaces / FIFO / FSL
Lite (AXI4-Lite)	Traditional Address/Data—No Burst (single address, single data)	PLBv46-single OPB

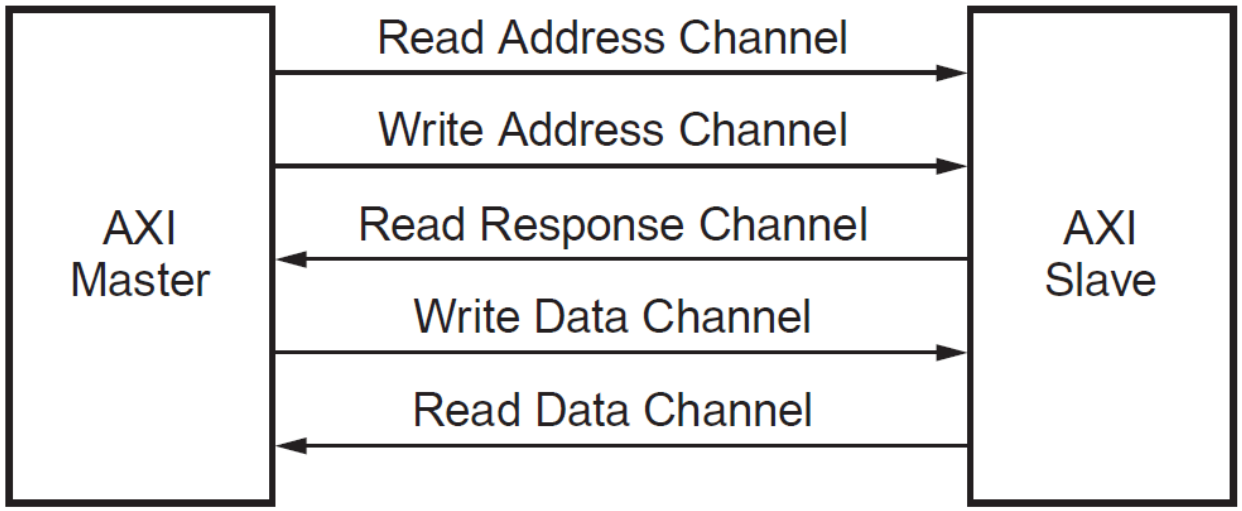
Types of AXI4 interfaces

- AXI4 (a.k.a. AXI4-full)
  - For high-performance memory-mapped requirements.
- AXI4-Lite
  - For simple, low-throughput memory-mapped communication (for example, to and from control and status registers).
- AXI4-Stream
  - For high-speed streaming data.

AXI4 Protocols

- Memory Mapped Protocols: AXI3, AXI4, AXI4-Lite
  - All transactions involve the concept of a target address within a system memory space and data to be transferred.
  - Example: A typical peripheral or memory bank
- Stream Protocol: AXI4-Stream
  - It's used for applications that typically focus on a data-centric and data-flow paradigm where the concept of an address is not present or not required
  - Example: data coming from an Ethernet controller

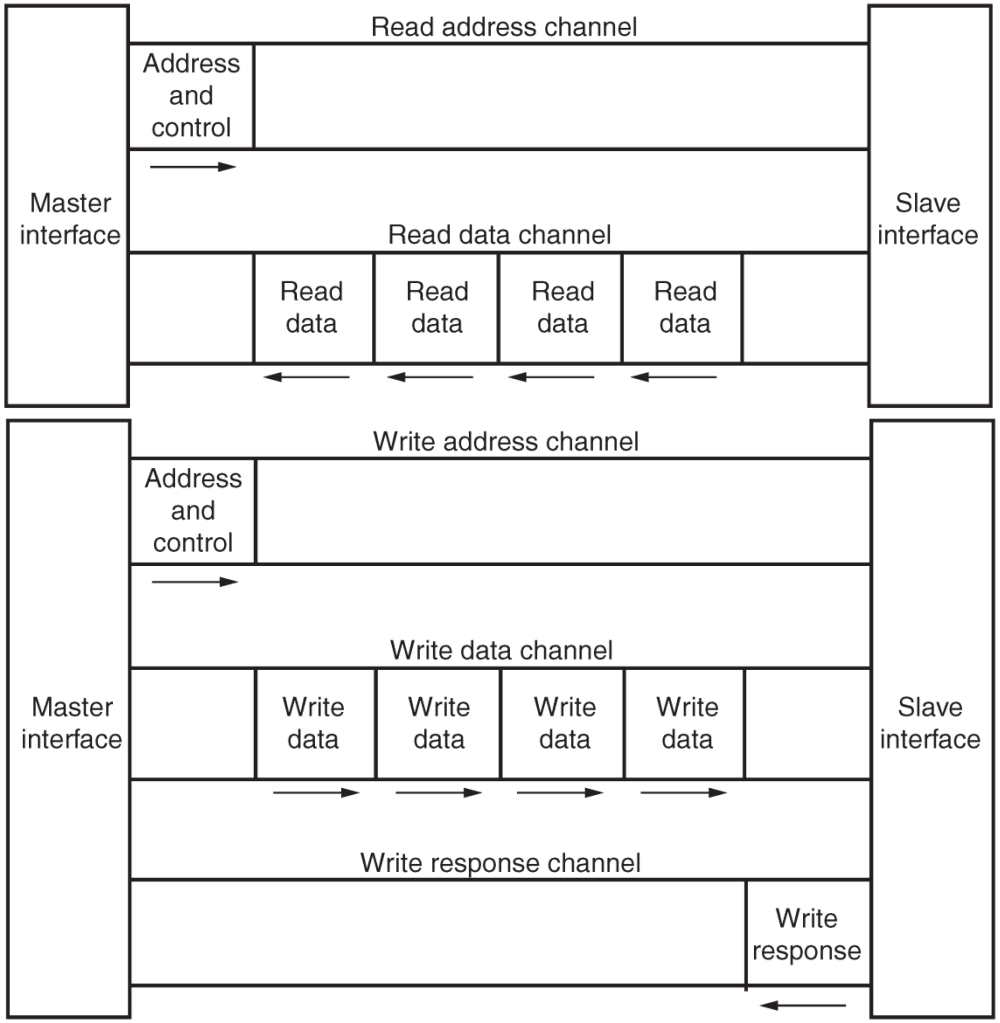
- A typical MM master-slave connections



AXI4 MM Protocol

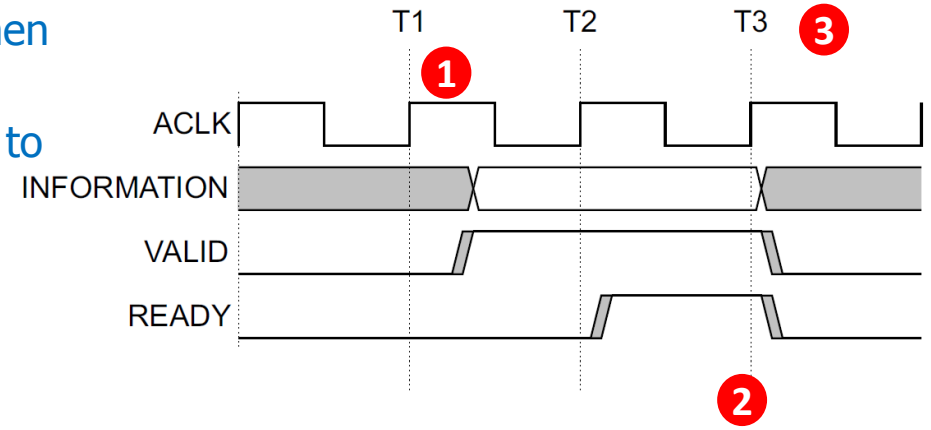
- Read address channel
- Read data channel

- Write address channel
- Write data channel
- Write response channel
  - Non-posted write model
  - There will always be a "write response"



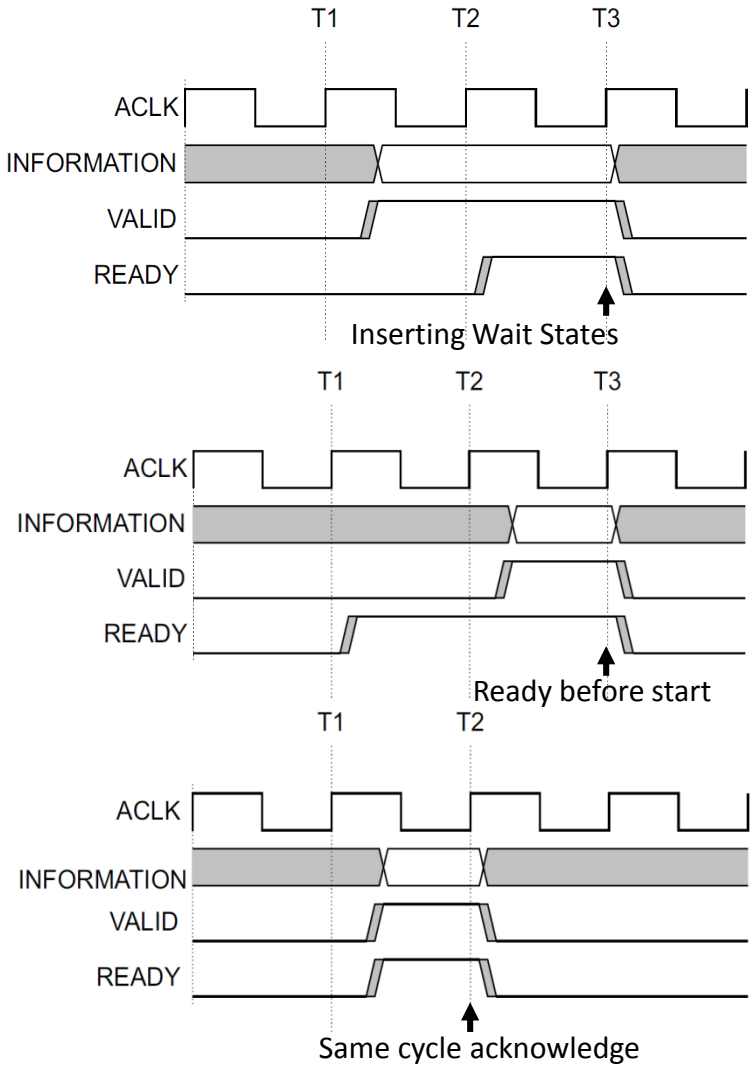
AXI: Channel handshaking

- All AXI channels use a basic VALID/READY handshaking:
  - SOURCE asserts and holds VALID when DATA is available
  - DESTINATION asserts READY if able to accept DATA
  - DATA transferred when VALID and READY = 1
  - SOURCE sends next DATA (if an actual data channel) or deasserts VALID
  - DESTINATION deasserts READY if no longer able to accept DATA



AXI: Channel handshaking

- AXI uses a valid/ready handshake acknowledge
- Each channel has its own valid/ready
  - Address (read/write)
  - Data (read/write)
  - Response (write only)
- Flexible signaling functionality
  - Inserting wait states
  - Always ready
  - Same cycle acknowledge



AXI MM signals

	AXI4	AXI4-Lite
Glbl	ACLK	
	ARESETN	
Write Address	AWID	
	AWADDR	
	AWLEN	
	AWSIZE	
	AWBURST	
	AWLOCK	
	AWCACHE	
	AWPROT	
	AWQOS	
	AWSIZE	
	AWREGION	
	AWLOCK	
	AWUSER	
	AWVALID	
	AWREADY	

	AXI4	AXI4-Lite
Read Address	ARID	
	ARADDR	
	ARLEN	
	ARSIZE	
	ARBURST	
	ARLOCK	
	ARCACHE	ARCACHE
	ARPROT	ARPROT
	ARQOS	
	ARREGION	
	ARUSER	
	ARVALID	
	ARREADY	

	AXI4	AXI4-Lite
Write Data	WDATA	WDATA
	WSTRB	WSTRB
	WLAST	
	WUSER	
	WVALID	
	WREADY	
Write Resp.	BID	
	BRESP	BRESP
	BUSER	
	BVALID	
	BREADY	

	AXI4	AXI4-Lite
Read Data	RID	
	RDATA	RDATA
	RRESP	RRESP
	RLAST	
	RUSER	
	RVALID	
	WREADY	

AXI MM signals: Address channels

- AWADDR (ARADDR): Write (read) address.
  - The write (read) address gives the address of the first transfer in a write (read) burst transaction
- AWVALID (ARVALID): Write (read) address valid
  - This signal indicates that the channel is signaling valid write (read) address and control information.
- AWREADY (ARREADY): Write (read) address ready
  - This signal indicates that the slave is ready to accept an address and associated control signals.

AXI MM signals: Address channels

- AWID (ARID): Write address ID (*multi-thread support*)
  - This signal is the identification tag for the write address group of signals
- AWLEN (ARLEN): Burst length
  - The burst length gives the exact number of transfers in a burst (number of transfers)
  - (length = N+1)
- AWSIZE (ARSIZE): Burst size
  - This signal indicates the size of each transfer in the burst (size = 2^N)
- AWBURST (ARBURST): Burst type
  - The burst type and the size information, determine how the address for each transfer within the burst is calculated. FIXED, INCR, WRAP
- AWLOCK (ARLOCK): Lock type
  - Provides additional information about the atomic characteristics of the transfer.
- AWPROT (ARPROT): Protection type
  - This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.

AXI MM signals: Address channels

- AWCACHE (ARCACHE): Memory type
  - This signal indicates how transactions are required to progress through a system.
- AWQOS (ARQOS): Quality of Service, QoS
  - The QoS identifier sent for each write transaction.
- AWREGION (ARREGION): Region identifier
  - Permits a single physical interface on a slave to be used for multiple logical interfaces
- AWUSER (ARUSER): User signal
  - Optional User-defined signal in the write address channel.

AXI MM signals: Write data channel

- WID: Write ID tag.
  - This signal is the ID tag of the write data transfer.
- WDATA: Write data.
- WSTRB: Write strobes.
  - This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
- WLAST: Write last.
  - This signal indicates the last transfer in a write burst.
- WUSER: User signal.
  - Optional User-defined signal in the write data channel.
- WVALID: Write valid.
  - This signal indicates that valid write data and strobes are available.
- WREADY: Write ready.
  - This signal indicates that the slave can accept the write data.

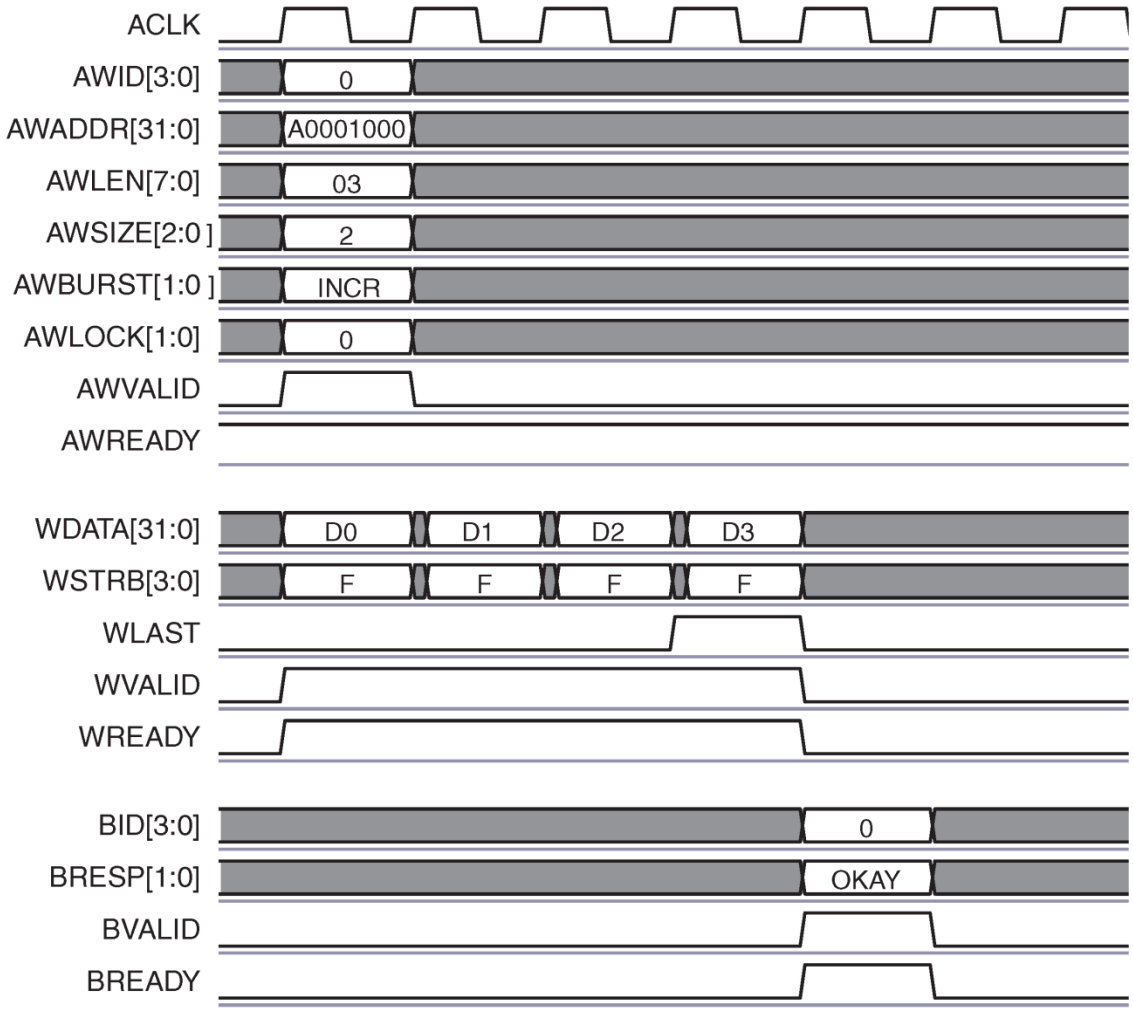
AXI MM signals: Write response channel

- BID: Response ID tag.
  - This signal is the ID tag of the write response.
- BRESP: Write response.
  - This signal indicates the status of the write transaction.
  - OKAY, EXOKAY, SLVERR, DECERR
- BUSER: User signal.
  - Optional User-defined signal in the write response channel.
- BVALID: Write response valid.
  - This signal indicates that the channel is signaling a valid write response.
- BREADY: Response ready.
  - This signal indicates that the master can accept a write response.

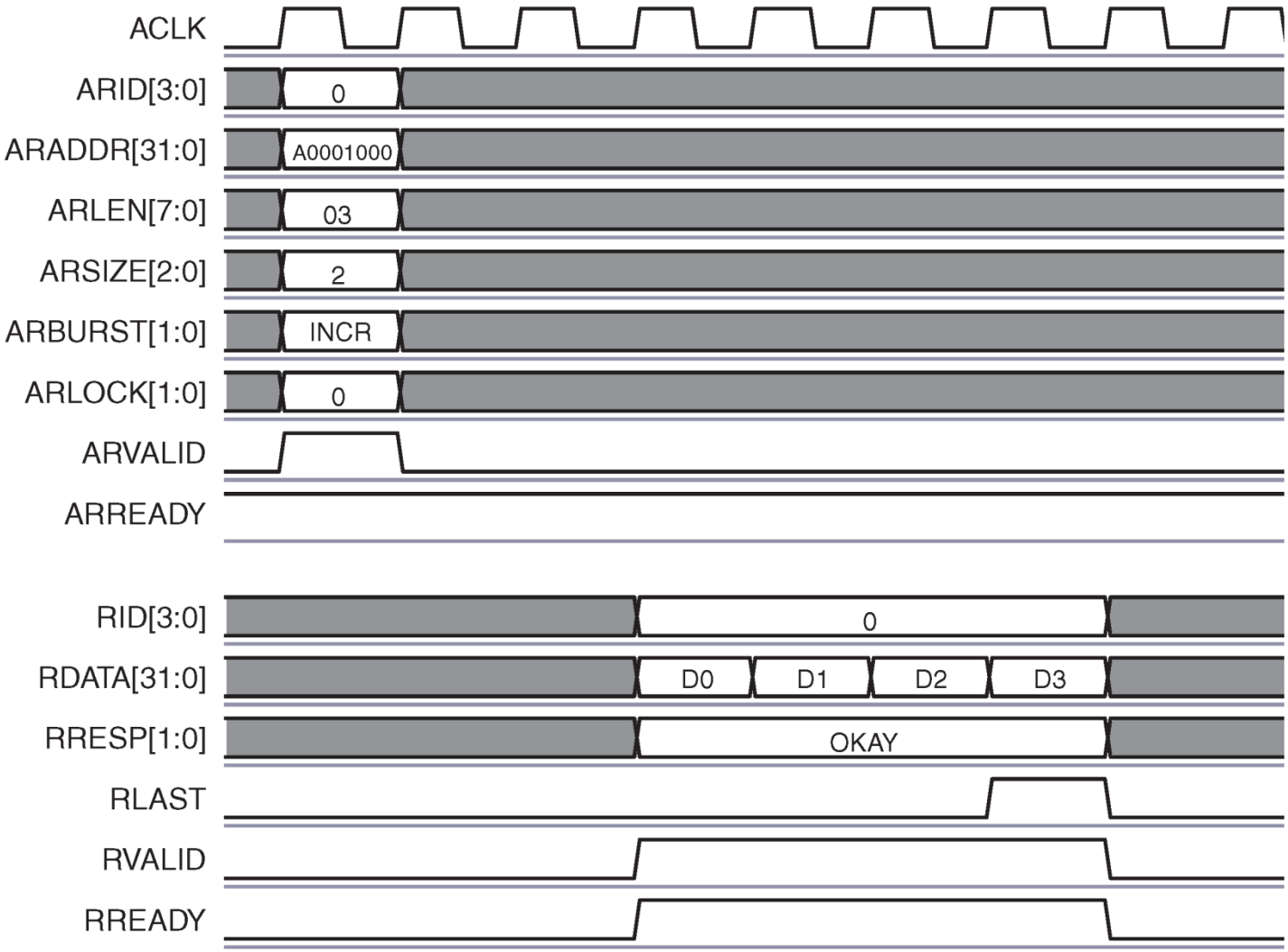
AXI MM signals: Read data channel

- RID: Read ID tag.
  - This signal is the identification tag for the read data group of signals generated by the slave.
- RDATA: Read data.
- RRESP: Read response.
  - This signal indicates the status of the read transfer.
  - OKAY, EXOKAY, SLVERR, DECERR
- RLAST: Read last.
  - This signal indicates the last transfer in a read burst.
- RUSER: User signal.
  - Optional User-defined signal in the read data channel.
- RVALID Read valid.
  - This signal indicates that the channel is signaling the required read data.
- RREADY Read ready.
  - This signal indicates that the master can accept the read data and response information.

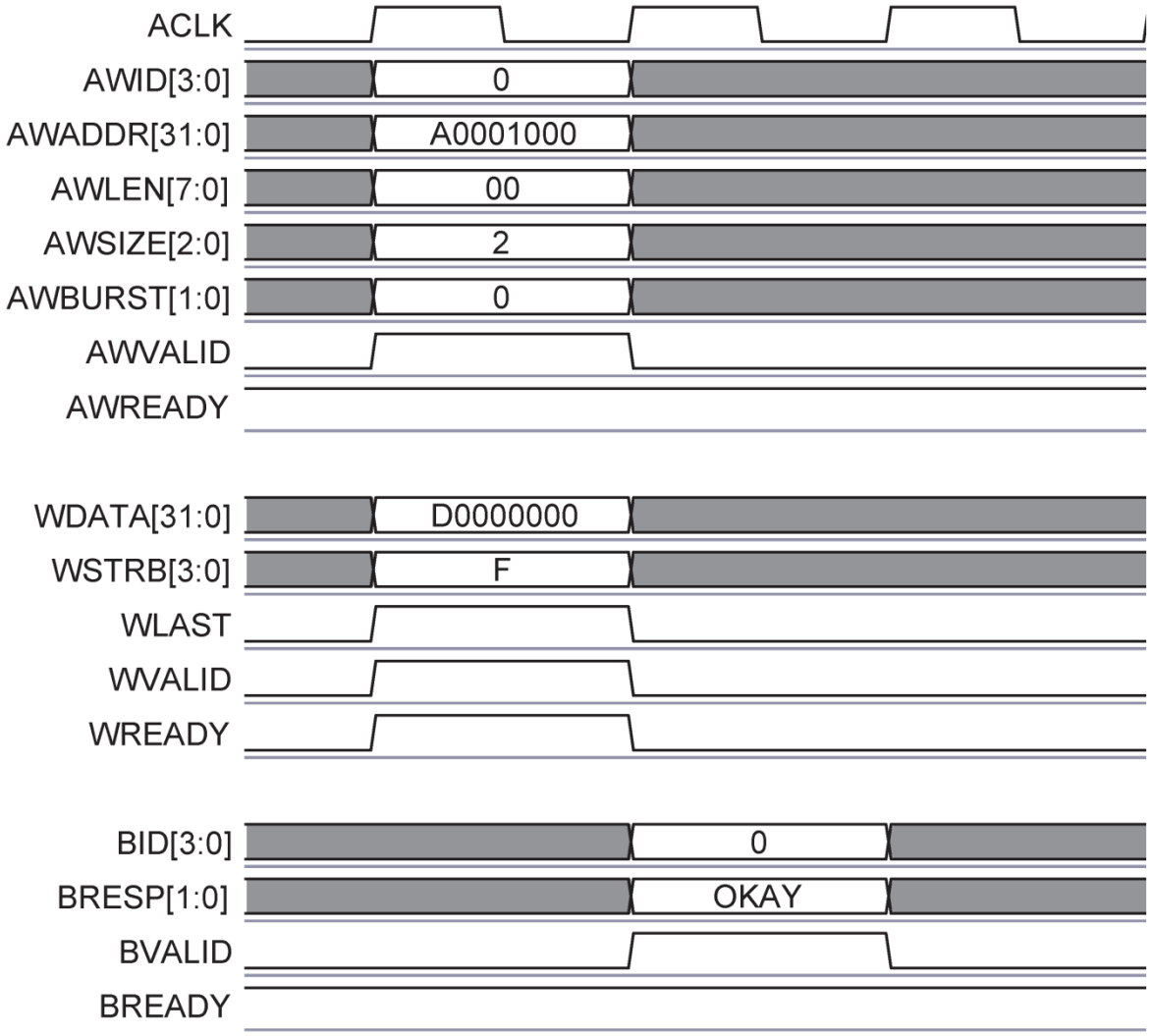
AXI4 Burst Write transaction



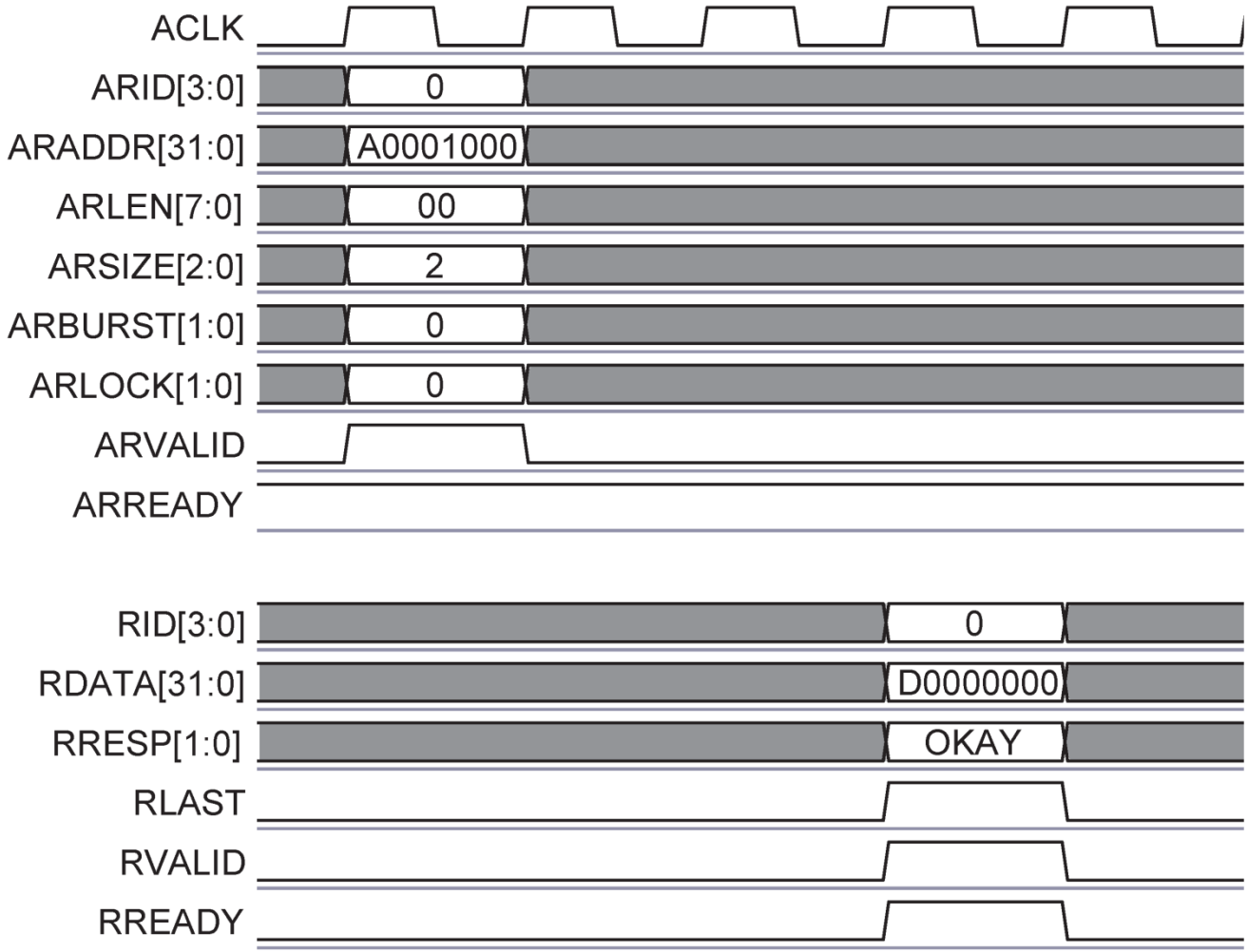
AXI4 Burst Read transaction



AXI4 Single Write transaction



AXI4 Single Read transaction



AXI LITE

- AXI-lite is subset of AXI4 for communication with simpler control register style interfaces within components.
  - all transactions are of burst length 1
  - all data accesses use the full width of the data bus
  - AXI4-Lite supports a data bus width of 32-bit or 64-bit.
  - all accesses are Non-modifiable, Non-bufferable
  - Exclusive accesses are not supported.

AXI LITE: Signals

Required signals:

Global	Write address channel	Write data channel	Write response channel	Read address channel	Read data channel
ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETn	AWREADY	WREADY	BREADY	ARREADY	RREADY
–	AWADDR	WDATA	BRESP	ARADDR	RDATA
–	AWPROT	WSTRB	–	ARPROT	RRESP

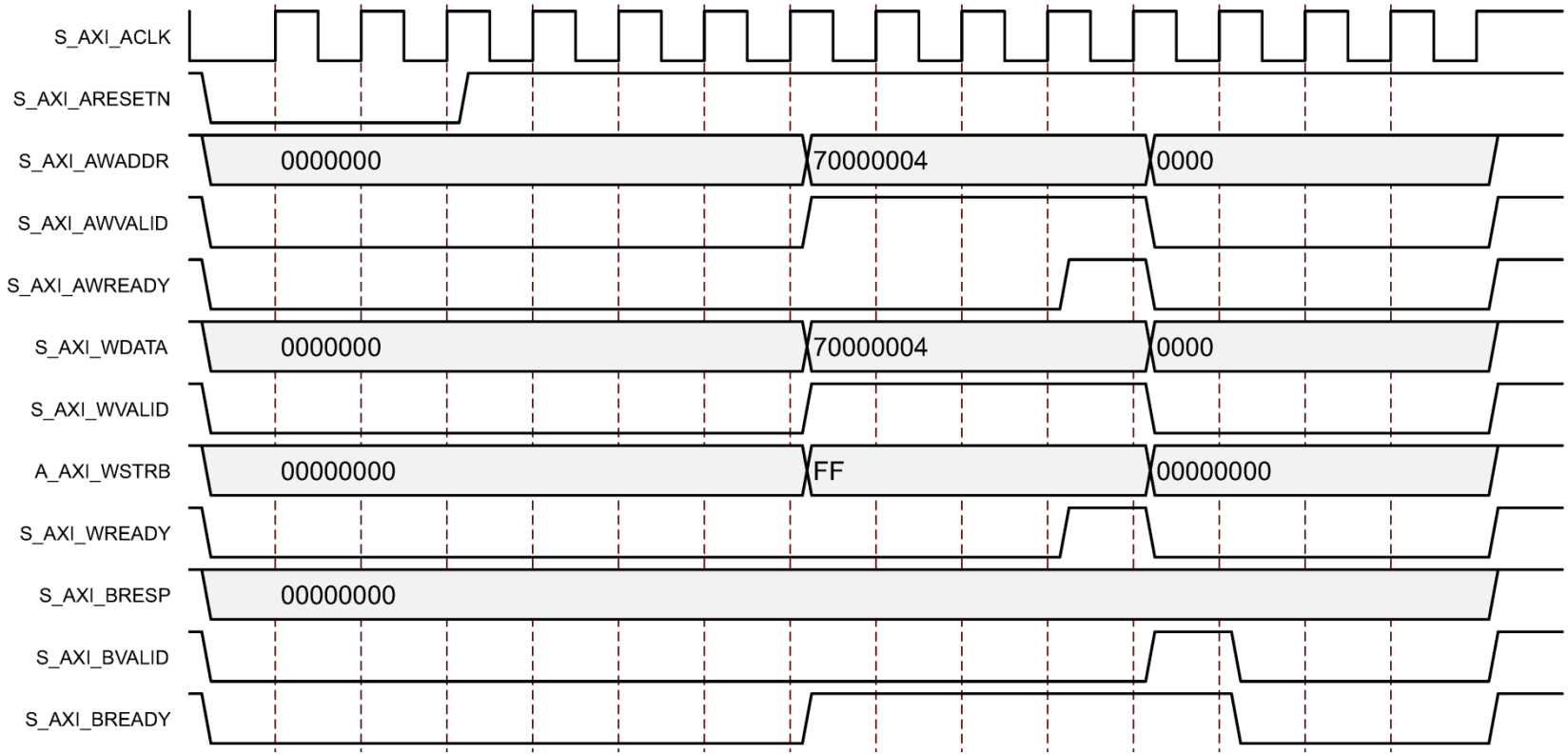
Modified signals:

- RRESP, BRESP
  - The EXOKAY response is not supported on the read data and write response channels.

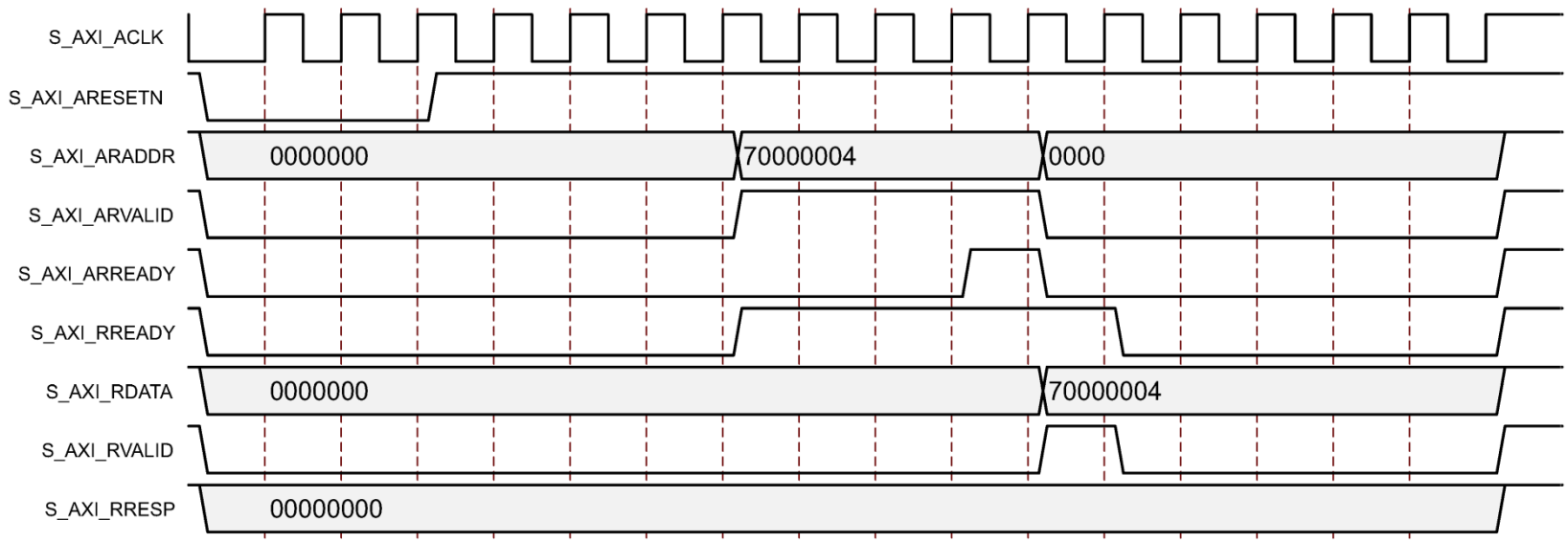
AXI LITE: Not supported signals

- AWLEN, ARLEN
  - The burst length is defined to be 1, equivalent to an AxLEN value of zero.
- AWSIZE, ARSIZE
  - All accesses are defined to be the width of the data bus.
  - AXI4-Lite requires a fixed data bus width of either 32-bits or 64-bits.
- AWBURST, ARBURST:
  - The burst type has no meaning because the burst length is 1.
- AWLOCK, ARLOCK
  - All accesses are defined as Normal accesses, equivalent to an AxLOCK=0.
- AWCACHE, ARCACHE
  - All accesses are defined as Non-modifiable, Non-bufferable, equivalent to an AxCACHE=0b0000.
- WLAST, RLAST
  - All bursts are defined to be of length 1, equivalent to a WLAST or RLAST value of 1.

AXI LITE: Single Write transfer

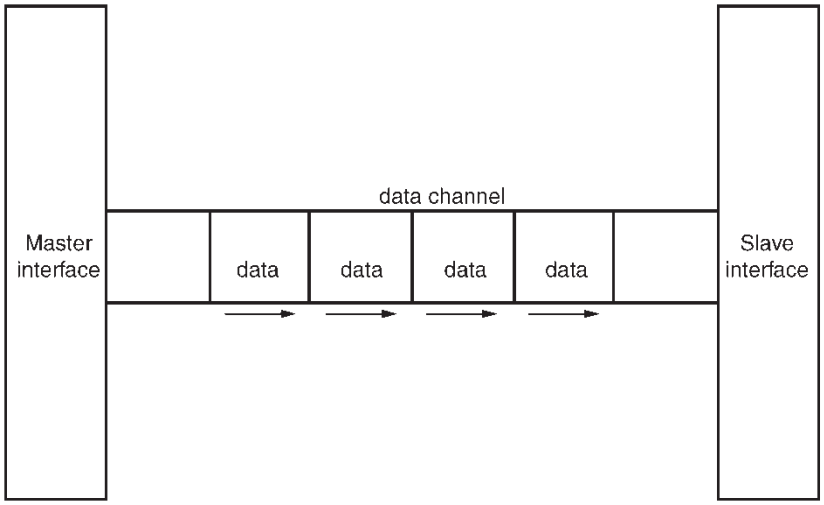


AXI LITE: Single Read transfer



AXI STREAM

- Data moves in a single direction from a master to a slave
  - Simplex communication
  - Dual direction would be dual simplex
    - individual channels in each direction
- Data only
  - No address bus
  - Minimum control lines
- Data interpretation
  - Packet or no packet
  - Master and slave must have prior knowledge of data format
  - Optional use of hardware signaling



AXI STREAM: Signals

- More signals defined than typically required
- Required signals
  - ACLK
  - TDATA
- Special, user-defined sideband signals consist of TUSER
- Other popular and useful signals are
  - TVALID
  - TREADY
  - TLAST

Used for AXIS-interconnect →

Signal	Source	Description
ACLK	Clock source	The global clock signal. All signals are sampled on the rising edge of **ACLK**.
ARESETn	Reset source	The global reset signal. **ARESETn** is active-LOW.
TVALID	Master	**TVALID** indicates that the master is driving a valid transfer. A transfer takes place when both **TVALID** and **TREADY** are asserted.
TREADY	Slave	**TREADY** indicates that the slave can accept a transfer in the current cycle.
TDATA[(8n-1):0]	Master	**TDATA** is the primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
TSTRB[(n-1):0]	Master	**TSTRB** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as a data byte or a position byte.
TKEEP[(n-1):0]	Master	**TKEEP** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as part of the data stream. Associated bytes that have the **TKEEP** byte qualifier deasserted are null bytes and can be removed from the data stream.
TLAST	Master	**TLAST** indicates the boundary of a packet.
TID[(i-1):0]	Master	**TID** is the data stream identifier that indicates different streams of data.
TDEST[(d-1):0]	Master	**TDEST** provides routing information for the data stream.
TUSER[(u-1):0]	Master	**TUSER** is user defined sideband information that can be transmitted alongside the data stream.

AXI STREAM: Basic protocol