A Memristor Based Image Sensor Exploiting Compressive Measurement For Low-power Video Streaming

A Seminar Report

Submitted by

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This is to Certify that this Seminar report on A Memristor Based Image Sensor Exploiting Compressive Measurement For Low-power Video Streaming is a bonafide record of the seminar done by **HOLMES JOSEPH(13153815)** of Seventh semester B.Tech in Electrical and Electronics Engineering, towards the partial fulfilment of the requirement as a part of the curriculum for the award of degree of Bachelor of Technology by Cochin University of Science and Technology.

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ABSTRACT

Image sensor is a commonly used electronic device in various applications. With the increasing requirement for resolution and frame rates, the power consumption is getting significant, which limits the use of image sensors in mobile device sand IoT applications. Compressive sensing (CS) techniques can achieve sub-Nyquist sampling rate to reduce the power consumption in hardware circuits. Currently, most compressive measurements are implemented in digital CMOS circuits, leading to high hardware complexity and power consumption as well as the limited sampling speed. These drawbacks cannot support the rapid growth in performance requirement of image sensor applications. The proposed technique is a memristor-based image sensor exploiting compressive measurement to achieve high performance with low power consumption and hardware overheads. Simulation results demonstrate the advantages of the proposed technique.

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LIST OF ABBREVIATIONS

CS	Compressive sensing
CMOS	Complementary metal-oxide-Semiconductor
IoT	Internet of things
AI	Artificial Intelligence
VLC	Visible light communications
ADC	Analog to digital converter
RIP	Restricted isometric property
CSSF	Compressive sensor sampling factor
HRS	High resistance state
LRS	Low resistance state
PPD	Pinned photodiode
MSE	Mean square Error
PSNR	Peak signal to noise ration
SSIM	Structural similarity
WB	Worst block

CHAPTER 1

INTRODUCTION

Image sensors are widely utilized in various applications, such as cameras, personal electronics, surveillance systems, and artificial intelligent (AI) robotic systems. Many emerging applications, such as visible light communications (VLC) and Internet of Things (IoT) also propose the intensive usage of image sensors. However, with the ever-increasing demand for high performance, large power consumption and high data quality requirement have become a critical issue in the circuit design. Studies have revealed that the dominant power consumption and speed restrictions are caused by the ADC operation. It could be a bottleneck when image sensors are applied to the resource limited systems, such as mobile devices and wireless sensor networks. To solve this problem, an effective compressive measurement technique is needed. Traditional codec methods such as H.264/MPEG4-AVC are post-sampling; they could not provide improvement during the sampling operation. Recently, a new research area called compressive sensing (CS) has drawn lots of attention, since it allows more efficient signal acquisition with fewer measurements. Physical resources needed for data acquisition, computation and transmission can be significantly reduced, which makes it very appealing for image sensor applications. However, implementing compressive measurement in digital CMOS circuits leads to high hardware complexity and low processing speed due to the intensive matrix operations .More advanced compressive Sensing implementations are desired to advance image sensor applications. The key element of the compressive measurement is the randomly generated measurement matrix. As the size of the target signal grows, to generate and store the corresponding measurement matrix is difficult. In our previous work, we developed a technique that uses memristors to build the measurement matrix by utilizing the inherent process variations during the

fabrication process. The memristor array allows analog matrix computations, which greatly save the resources during the compressive measurement and also reduce the hardware complexity and increases the processing speed. To apply the CS techniques, the target signals need to be sparse in order to conduct the compressive measurement. Wireless video streaming, with the nature that its differential outputs are sparse, can easily benefit from the CS techniques, as it could be directly applied without extra signal manipulation. Based on these features, I propose a memristor-based compressive measurement scheme in this paper for image sensor design targeting wireless video streaming applications. The proposed technique significantly improves energy efficiency with small hardware overheads.

CHAPTER 2

BACKGROUNDS

This section reviews the CS theory and memristor physical models. We also explain how CS can be applied to wireless video streaming.

2.1 Compressive Sensing

Compressive sensing process consists of two parts, namely compressive measurement and reconstruction. Compressive measurement has the advantage of reducing the input signal to fewer measurements. It can be simply expressed as

$$Y = \Phi \times X \quad \text{.....(1)}$$

where X is the N dimensional input signal, Y is the resulted compressed data of length M, and $\Phi \in R^{M \times N}$ is the measurement matrix. If Φ is chosen carefully so that (1) satisfies the restricted isometry property (RIP), X can be reconstructed non-destructively. To meet the restricted isometry property, two major conditions must be fulfilled based on the basic of CS theory. First of all, the measurement matrix Φ needs to be sufficiently random, so that it is capable of preserving the original message after sampling. Bernoulli or Gaussian distributed matrices are usually chosen to build the measurement matrix. Since Gaussian matrices offer a higher precision, they could provide better signal conservation than the binary Bernoulli matrices. Second, X has to be sparse by itself or when it is projected onto some different spaces. For example, images represented by the Discrete Cosine Transform or Wavelet Transform will only have a few non-zero (or significant) elements. The number of the measurements M is directly related to the sparsity of X. Hence, we define the CS sampling factor (CSSF), which is the ratio between M and the sparsity of a signal, to get a better quantitative evaluation in Chapter 4. On the other hand, in the case of video streaming, the subsequent frames usually have a high temporal

correlation, so that their differential vectors are sparse signals that can be exploited for CS implementations. Since M<N, there exist infinite solutions that satisfy (1). To reliably recover X, various signal reconstruction algorithms have been proposed. Our past work also developed some algorithms for high-speed and energy-efficient signal reconstruction. In this paper, a standard l1 norm optimization method will be utilized to reconstruct the original signal from the compressive measurements.

2.2 Memristor

A memristor device typically has a sandwich structure with two metal electrodes at each end and a stack of functional nano-materials in the middle. Consider a classic Pt/TiO2/Pt type memristor. When a positive or negative voltage is applied over the electrodes, the Titanium material will convert between TiO2 and Ti2O3, which are high resistivity insulator and conducting material, respectively. Based on this mechanism, memristor devices are able to be switched between the stable high resistance states (HRS) and the low resistance state (LRS). However, the fabrication of these nanoscale devices will inevitably introduce significant process variations, which hinder its adoption in memory applications. But according to our analysis in, this inherent non-deterministic property could be leveraged to generate true random matrix used by compressive sensing applications. Under these applications, the measurement matrix Φ can be constructed through writing a M×N memristor array using a short pulse, with the width of tens of nanoseconds. Then, the matrix multiplication operation is reduced to a simple analog process, where the input signals go through all these memristive devices in parallel and being accumulated at the end of each row. The process can be represented as:

$$Y_i(t) = I_i(t) = \sum_{j=1}^{N} \phi(i,j) \times V_j(t);\ i = 1, 2, 3, \cdots, M \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where Y_i is the 'i'th output in terms of current I_i, V_j is the voltage of the 'j'th input signal, and ϕ (i, j) stands for the conductance of memristor in 'i'th row and 'j'th column. Both the matrix generation and multiplication processes can be done within one clock cycle.

CHAPTER 3

CMOS BASED IMAGE SENSORS

Advent of CMOS technology in eighties led to the phenomenal growth in semiconductor industry. Transistors have become smaller, faster, consume less power, and are cheaper to manufacture. It is CMOS technology which has enabled very high integration on the chips leading to modern high performance, miniaturized integrated circuits.

Apart from the valuable contribution in miniaturization of integrated circuits, CMOS technology found applications in sensing applications.

CMOS technology has been adopted to design sensors, especially in the field of imaging. Due to the wide usage of CMOS based image sensors, CMOS sensors are often considered to be a synonym of CMOS based image sensors and have emerged as a competitor to CCD based image sensors. Until recently, charge coupled devices (CCDs) dominated most of the image sensing systems, i.e. , cameras ,camcoders,etc. CCDs have been in use in astronomical cameras, video camcorders and scanners. However of late, CMOS imaging have emerged as an alternative to CCD imagers and it also offers better features.

Subsequent sections will discuss both CCD and CMOS sensor based imagers, their pros and cons, and also their applications .Further, other applications of CMOS technology in the field of sensing will be discussed

3.1 CMOS Vs CCD

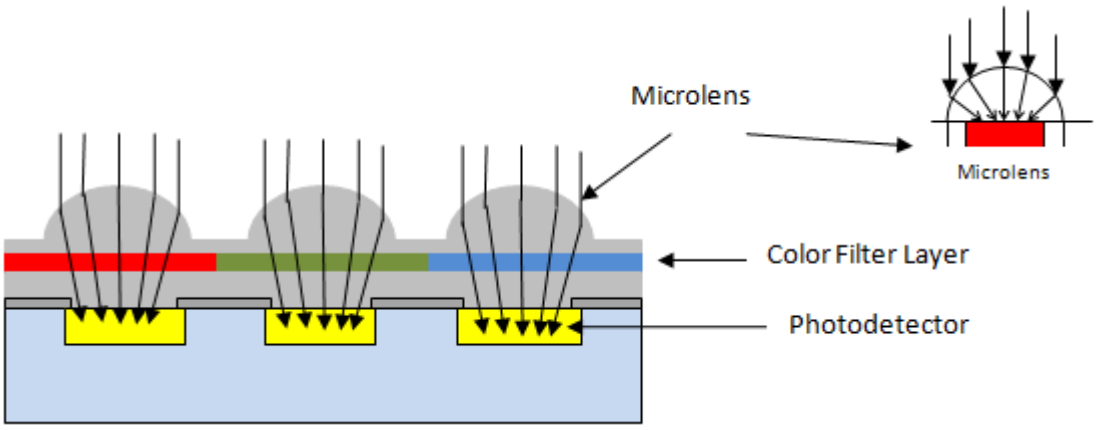
Invention of CCD marked the end of vacuum tube imagers used in television cameras as it overcame the disadvantages of vacuum tubes like chronic picture artifacts as lag and burn-in, fragility of large glass tubes or the sensitivity to shock, vibration and electromagnetic radiation, painstaking periodic alignment of tubes, etc. It also marked the beginning of a new era in imaging systems and for decades, it enjoyed quality advantages over the rival CMOS sensors. Wherever image quality was paramount, CCDs were preferred, CMOS were used mainly in applications where small size and low power were prime requirements.

With the technological development in CMOS technology, gap between CCD and CMOS sensors has narrowed; CMOS sensors can also achieve competitive quality. Choice amongst CCD and CMOS sensors has become increasingly difficult.

Both CCD and CMOS image sensors use large arrays of thousands (sometimes millions) of photo-sites, commonly called pixels. Both carry out same steps

3.1.1. Light-to-charge conversion

Incident light is directed by the microlens (a tiny lens placed over the pixel to increase its effective size and thereby fill factor) onto the photo-sensitive area of each pixel where it is converted into electrons that collect in a semiconductor "bucket."



Light to charge conversion
Figure 3.1

The bigger the pixel, the more light it can collect. Thus, big pixel sensors work best under low-light conditions. For the same number of pixels, bigger pixels results in bigger chip, this means higher cost. Conversely, smaller pixels enable smaller chip sizes and lower chip prices, as well as lower lens costs. But there are limitations on pixel size reduction. Smaller pixels are less sensitive to light, the optics required to resolve the pixels becomes expensive and requires expensive fabrication possesses.

3.1.2. Charge accumulation

As more light enters, more electrons accumulate into the bucket.

3.1.3. Transfer

Accumulated charge must be transferred to the signal conditioning and processing circuitry.

3.1.4. Charge-to-voltage conversion

The accumulated charge must be output as the voltage signal.

3.1.5. Amplification

Voltage signal is then amplified before it is fed to the camera circuitry.

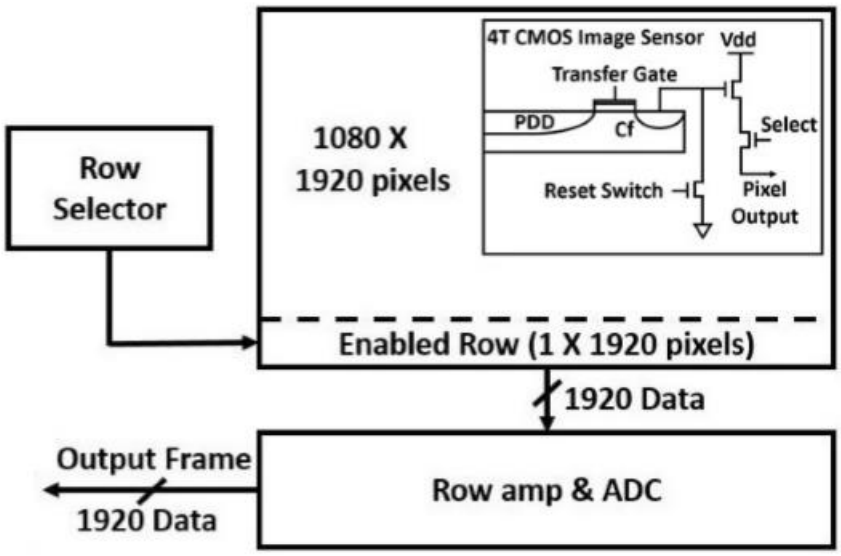
Both CMOS and CCD perform all these tasks; however the aspect in which they differ is the order of execution of these tasks.

CHAPTER 4

MEMRISTOR BASED IMAGE SENSOR DESIGN

4.1 Proposed Architecture

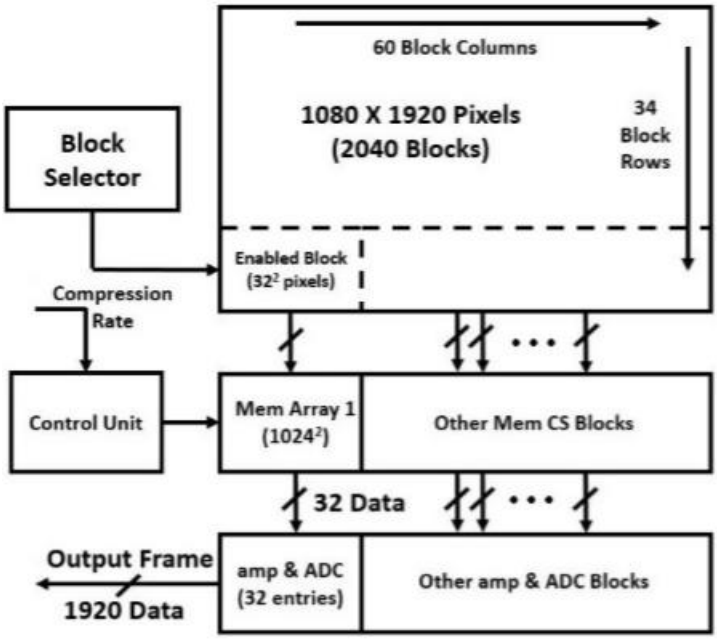
Figure 4.1 is the conventional design of a 1920 × 1080 pixels CMOS-based image sensor, and the inserted sub-figure shows a typical pixel structure with one pinned photodiode (PPD) and three transistors. The CMOS-based image sensor contains three major blocks: row selector, pixel array, amplifier and analog-to-digital converter (amp & ADC). The pixel array is the main unit which converts the incident image to electrical signals. In most designs, amp & ADC are not implemented in every single pixel to avoid large hardware overheads and power consumption. The number of the amp & ADC is determined by the number of columns so that each amp & ADC is shared by multiple rows. A row selector is needed to enable different pixel rows for each ADC time period.



Traditional CMOS image sensor architecture.

Figure 4.1

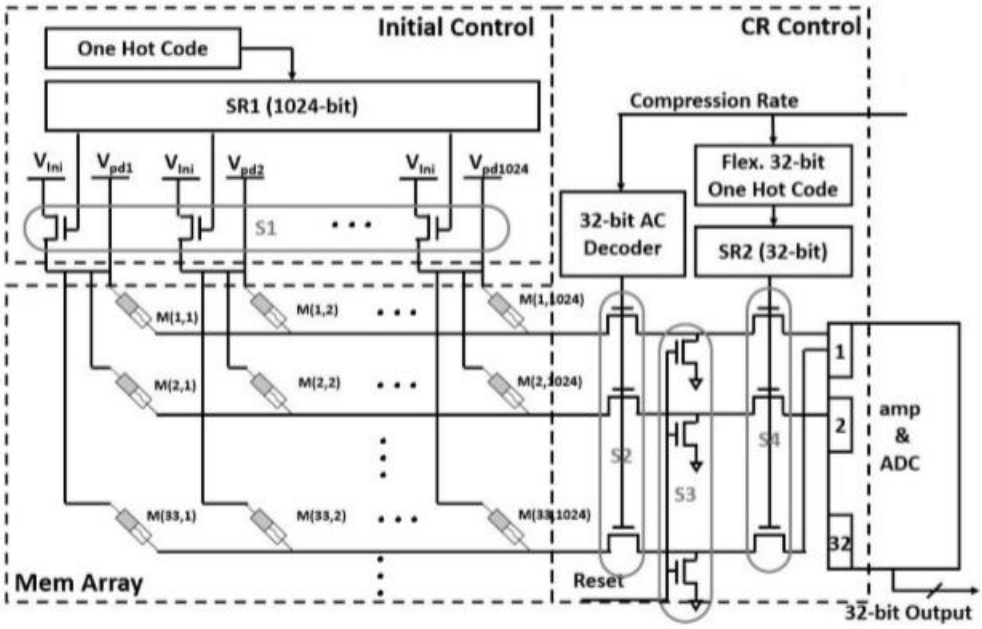
In this paper, we propose a new block-based compressive sensing image sensor design as shown in Figure 4.2. Through the compressive measurement, the proposed design will greatly reduce the volume of the data for digitalization, so that the power consumption of amp & ADC operations can be



Proposed design
Figure 4.2

Significantly reduced. The pixel array is divided into 34×60 blocks because the block-based structure helps to improve signal recovery quality. Hence, the original 1⁄1088 row selector is modified to the 1⁄34 block selector. Each vertical 34 blocks are combined together into a pixel bank, shared with one CS module. For each pixel bank, a 1024×1024 memristor array is utilized to conduct compressive measurement with the help of the corresponding control unit. During one frame operation, all the blocks will operate 34 times to finish the compressive measurement for the entire frame. In addition, different level of data compression can be achieved through the communication with receiver end.

4.2 Implementation and Detailed Operations



Single memristor based CS block
Figure 4.3

Figure 4.3 shows the detailed circuit implementation of a single memristor based CS block. For illustration purpose, only three rows are displayed. In addition to the the memristor array and amp & ADC unit, the reminder of the logic consists of four sets of switches, S1 to S4, as well as their control logic. All these transistor sets are in the size of 1k. S1 is the initial process control linked to a 1024bit shift register. S2 manages how many memristor rows should be activated based on the accepting rate so that different compression levels can be applied. In S2, every 32 switches are bounded together and adjusted by a 32bit incremental decoder where a higher input will turn on more switches. S3 is used to reset the overall status after one block finishes its operation and prepare the device for the next block. Since there are 1024 rows but only 32 amp & ADC entries within one block, multiplexing is necessary. Each individual amp & ADC unit is linked to 32 separated rows and controlled by S4 with a flexible 32bit one hot code. Detailed operations are described as the follows.

4.2.1 Initialization process

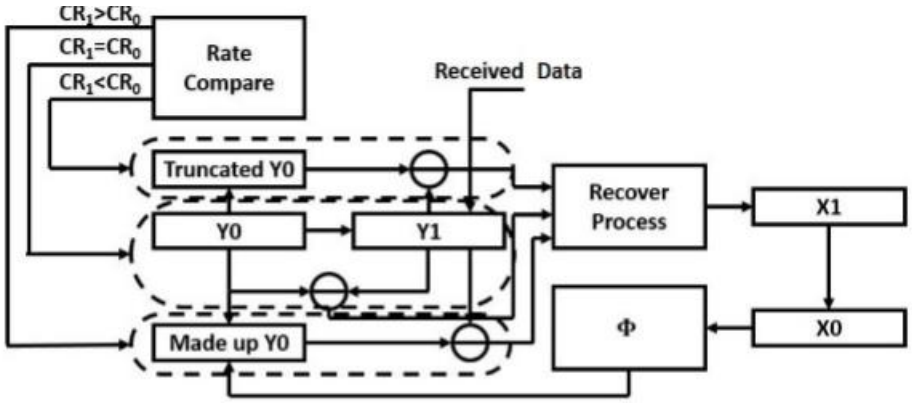
Before the sampling, the memristor array needs to be initialized to generate the measurement matrix Φ. Due to the nonvolatility of memristor devices, the values of Φ will stay for a long time without requiring any refresh operation. To perform the initialization, all CMOS pixels are deactivated through the block selector at the beginning. S1, S2 and S3 are all turned to “1s” while S4 is disabled. A writing voltage with a value of 2Vdd is applied to all the memristor units so that they are tuned to a certain resistance region with the desired randomness. Afterwards, S1 is controlled by the 1k−bit one hot code, S2 is all enabled, S3 is disabled, and S4 is managed by another 32−bit one hot code. Through 1k’s iteration, the matrix values can be sent to the receiver end column by column. Finally, a reset operation is applied.

4.2.2 Normal Image Read-out

During the normal image read operation, S1 is turned to “0s” to terminate the initialization module. The selector connects data in 1024 pixels to every CS block. At the same time, operations of S2 and S4 are controlled by compression rate (CR) to perform different level of compressive sensing for each pixel block. For example, CR “00010” can let S2 to enable first 64 rows and generate 2bit one hot code for S4 while the related compression level is 6.25% (64⁄1024) for this block. After the modification of switch signals, all those 1024 pixels’ voltage (Vpd) flow over the specific rows and are fed into the ADC module. Then, a reset operation is used to prepare for the next block read-out.

4.2.3 Recovery Process of Receiver Side

As mentioned in the previous section, the sampling and recovery processes are conducted based on the differential vector of two subsequent image frame. The subtraction is actually carried out on the receiver side to save the resources in the image sensor. Since the CR is adjustable, different strategies are applied to the reconstruction process as shown in Figure 4.4,



Reconstruction process
Figure 4.4

where X1, Y1 and CR1 stand for the data of current status, while X0, Y0 and CR0 are related to the previous iteration. If CR1=CR0, the receiver goes through the normal recover process and compute X1 from (Y 1−Y 0) and X0. IfCR1 < CR0, which means Y0 is smaller than Y1, then Y1 needs to be truncated to the same dimension as Y1 before the recovery. On the other hand, if CR1 > CR 0, the missing measurements of Y0 (compare to Y1) need be complemented through multiplying Y 0 with certain rows of Φ. After the recovery, the current X1, Y 1 and CR1 are updated as the new X0, Y0 and CR0, respectively, and become the base information for the next iteration. Since the error is accumulative, image frames without compression should be transmitted periodically. This post-sampling subtraction mechanism can reduce the compression rate and make the proposed system much more efficient.

CHAPTER 5

EVALUATION

The proposed memristor-based image sensor is simulated in a standard 90nm CMOS process, with the parametric memristor model based on the fabricated paradigm in. To guarantee the effective switching of S1−S4, memristor rows are tuned to 10kΩ on average during the initialization. In these simulations, 4F2 (“F” refers to the feature size of technology process and here it is 90nm) is utilized to calculate the area for each memristor component. Table 5.1 summarizes the implementation of 60 CS blocks while the power is the average value of multiple iterations.

CS BLOCK IMPLEMENTATION

No. of CS Blocks	60	
Total Area	$5.366mm^2$	
Clock Frequency	200kHz	
Initialization	34k Clk	309.74mW
Normal Read-out	1156 Clk	32.64mW

Table 5.1

The proposed circuit is designed to meet the requirement of 120fps. Thus, the clock frequency is assigned as 200 kHz. It is slow enough to allow the ADC to complete data conversion with in one cycle. In comparison with a fabricated image sensor chip, all the CS blocks will only introduce1.8%areaoverheads. However, our design saves more power from the amp & ADC and data transmission. To verify the compression rate and recovery performance, a case study is evaluated between two surveillance frames. The overall sparsity level over their subtraction is around 8% while the frame rate is only 15fps.

RECONSTRUCTION PERFORMANCE UNDER DIFFERENT COMPRESSION LEVELS

CSSF	Overall CR	Overall MSE	Overall PSNR	Overall SSIM	WB MSE	WB PSNR	WB SSIM	No. of Distortion
4	27.09	0.0454	58.55	0.9997	1.2119	-0.83	0.2889	425
5	30.12	0.0062	67.02	1	0.5732	2.42	0.4849	106
6	32.73	0.0012	73.93	1	0.4395	3.57	0.5438	31
7	35.01	1.12E-4	83.65	1	0.1875	7.27	0.779	5
8	36.82	6.57E-5	86.02	1	0.1064	9.73	0.8506	4
9	38.86	2.70E-5	91.99	1	0.0654	11.84	0.8959	1
Note: CSSF = CS sampling factor; WB = worst block's; Frame size is 1920 × 1088; Total number of pixel blocks is 2040.								

Table 5.2

Table 5.2 shows the qualities of the recovered image frames under different CS sampling factors . Mean square error(MSE), peak signal to noise ration (PSNR) and structural similarity(SSIM)are observed both in terms of overall scheme and worst block's (WB) view. In general, better compressive recovery leads to lower MSE, higher PSNR and SSIM approaching to 1. The number of distorted blocks is also a very important criterion as it stands for the sustainable ability of CS iterations. Based on the results, we can see that a higher sampling factor will increase the overall compression rate, but also achieve better recovery performance. It is worth noting that the 4th case can be regarded as having a very high quality recovery with only 5 blocks of distortion, which is good enough to serve as the base frame for the next sampling. About 65% power consumption of amp & ADC and data transmission can be saved through the proposed CS process. Thus, it is evident that the proposed memristor based image sensor can achieve significant power savings for video streaming without affecting the real-time performance

CHAPTER 6

CONCLUSION

In this paper, we proposed a memristive based image sensor that exploits compressive measurement to reduce the power consumption of video streaming. High speed and low power analog CS operations have been achieved through the memristor array Simulation results demonstrate high-level data compression and significant energy savings, as well as good reconstruction quality. Future work is being directed towards further power/performance improvement and the fabrication of the proposed design.

CHAPTER 7

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