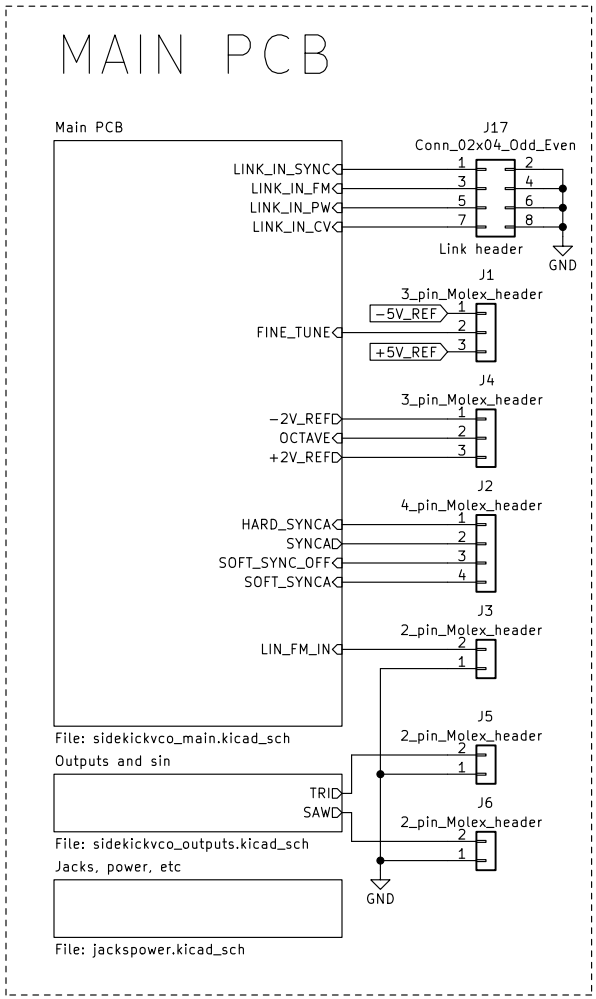

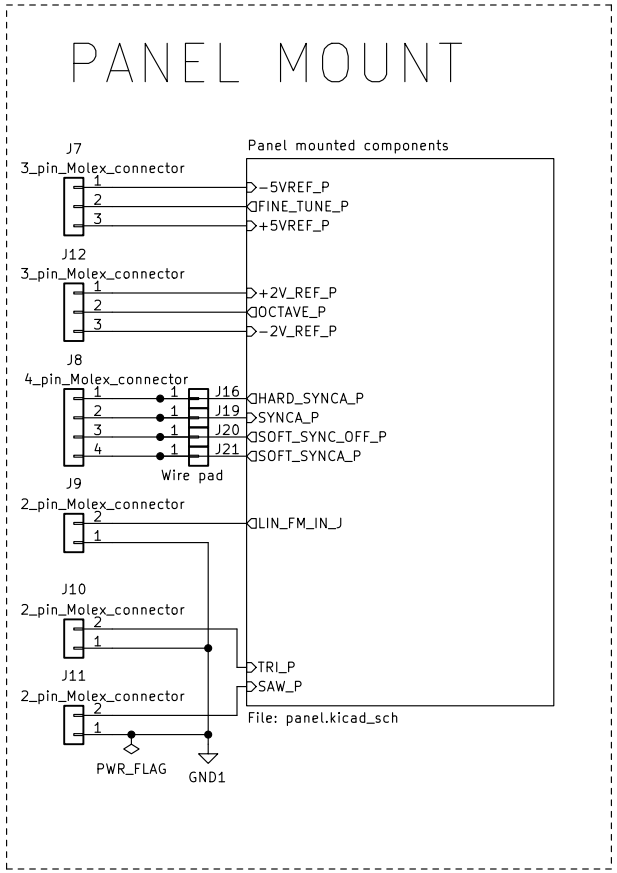

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Sheet: /
File: sidekickvco.kicad_sch

Title: Sidekick VCO

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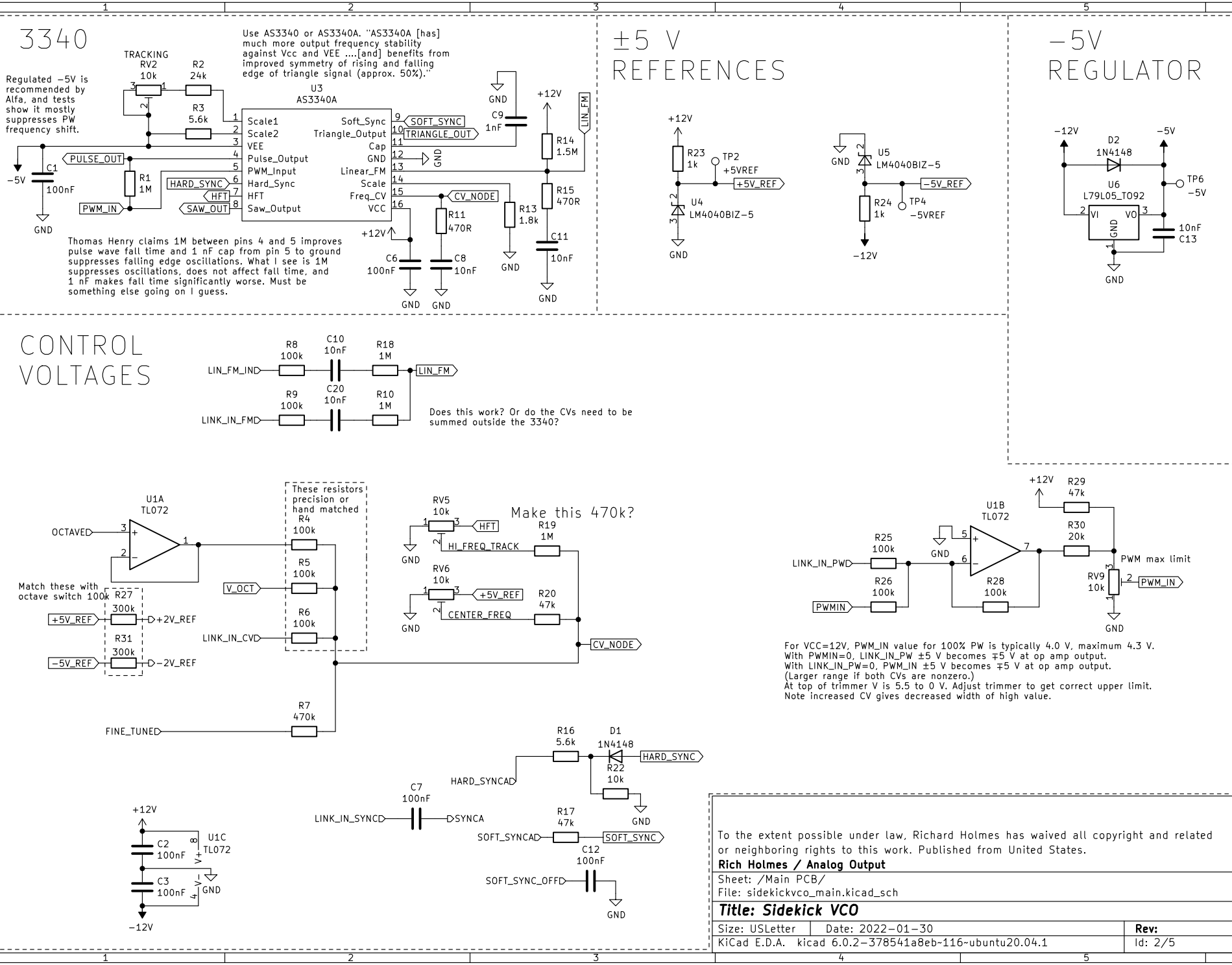
3340
Use AS3340 or AS3340A. "AS3340A [has] much more output frequency stability against Vcc and VEE ....[and] benefits from improved symmetry of rising and falling edge of triangle signal (approx. 50%)."
Regulated −5V is recommended by Alfa, and tests show it mostly suppresses PW frequency shift.
TRACKING
RV2 10k
R2 24k
R3 5.6k
U3 AS3340A
Scale1
Scale2
VEE
Pulse_Output
PWM_Input
Hard_Sync
HFT
Saw_Output
Soft_Sync
Triangle_Output
Cap
GND
Linear_FM
Scale
Freq_CV
VCC
SOFT_SYNC
TRIANGLE_OUT
CV_NODE
LIN_FM
PULSE_OUT
HARD_SYNC
HFT
SAW_OUT
PWM_IN
C1 100nF
R1 1M
C9 1nF
R14 1.5M
R15 470R
R11 470R
R13 1.8k
C11 10nF
C6 100nF
C8 10nF
Thomas Henry claims 1M between pins 4 and 5 improves pulse wave fall time and 1 nF cap from pin 5 to ground suppresses falling edge oscillations. What I see is 1M suppresses oscillations, does not affect fall time, and 1 nF makes fall time significantly worse. Must be something else going on I guess.
±5 V REFERENCES
R23 1k
TP2 +5VREF
U4 LM4040BIZ−5
U5 LM4040BIZ−5
R24 1k
TP4 −5VREF
−5V REGULATOR
D2 1N4148
U6 L79L05_TO92
TP6 −5V
C13 10nF
CONTROL VOLTAGES
R8 100k
C10 10nF
R18 1M
LIN_FM_IN
LIN_FM
R9 100k
C20 10nF
R10 1M
LINK_IN_FM
Does this work? Or do the CVs need to be summed outside the 3340?
U1A TL072
OCTAVE
These resistors precision or hand matched
R4 100k
R5 100k
R6 100k
V_OCT
LINK_IN_CV
Match these with octave switch 100k
R27 300k
R31 300k
+5V_REF
−5V_REF
+2V_REF
−2V_REF
RV5 10k
RV6 10k
HI_FREQ_TRACK
CENTER_FREQ
Make this 470k?
R19 1M
R20 47k
CV_NODE
R7 470k
FINE_TUNED
U1B TL072
R29 47k
R30 20k
R25 100k
R26 100k
R28 100k
LINK_IN_PW
PWMIN
PWM max limit
RV9 10k
PWM_IN
For VCC=12V, PWM_IN value for 100% PW is typically 4.0 V, maximum 4.3 V.
With PWMIN=0, LINK_IN_PW ±5 V becomes ∓5 V at op amp output.
With LINK_IN_PW=0, PWM_IN ±5 V becomes ∓5 V at op amp output.
(Larger range if both CVs are nonzero.)
At top of trimmer V is 5.5 to 0 V. Adjust trimmer to get correct upper limit.
Note increased CV gives decreased width of high value.
U1C TL072
C2 100nF
C3 100nF
R16 5.6k
D1 1N4148
R22 10k
HARD_SYNCA
C7 100nF
LINK_IN_SYNC
SYNCA
R17 47k
SOFT_SYNCA
C12 100nF
SOFT_SYNC_OFF
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Sheet: /Main PCB/
File: sidekickvco_main.kicad_sch
Title: Sidekick VCO
Size: USLetter
Date: 2022−01−30
Rev:
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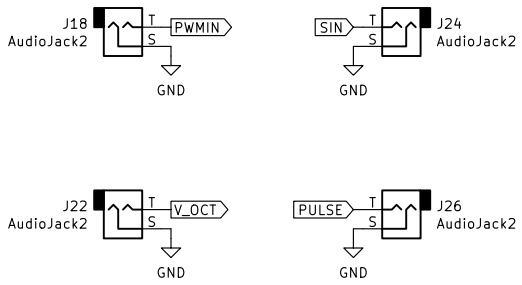
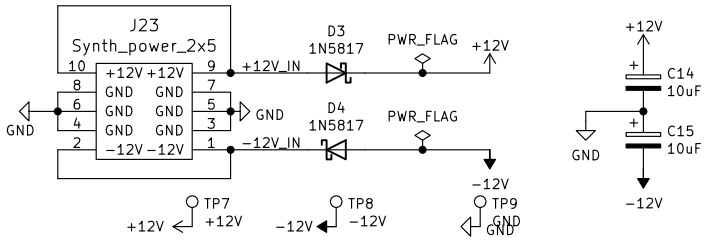
Id: 2/5

BOARD MOUNTED JACKS



POWER



ACME GRAF2 Holes

ACME GRAF3 AO logo

ACME GRAF4 CC0 logo

B1 Board

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Sheet: /Jacks, power, etc/

File: jackspower.kicad_sch

Title: Sidekick VCO

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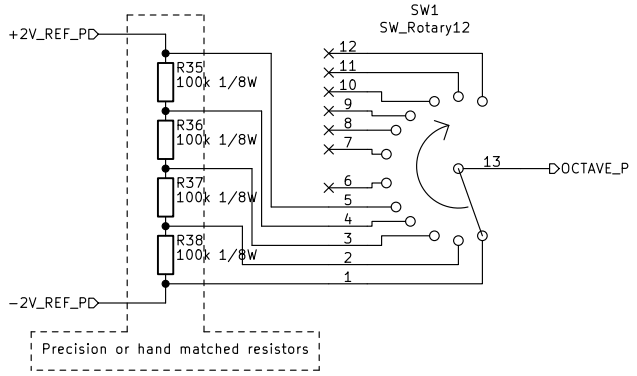
OCTAVE SWITCH



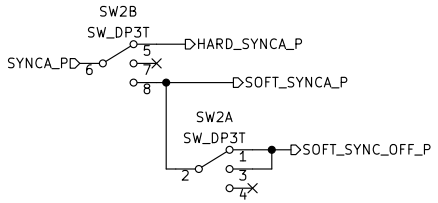
SYNC SWITCH

B2
Board

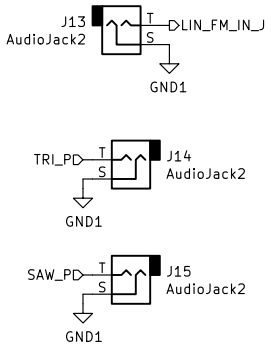
ACME GRAF1
board

H1
MountingHole

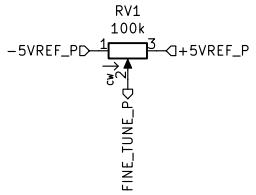
H2
MountingHole



JACKS



POT



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Sheet: /Panel mounted components/
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Title: Sidekick VCO

Size: USLetter	Date: 2022−01−30	**Rev:**
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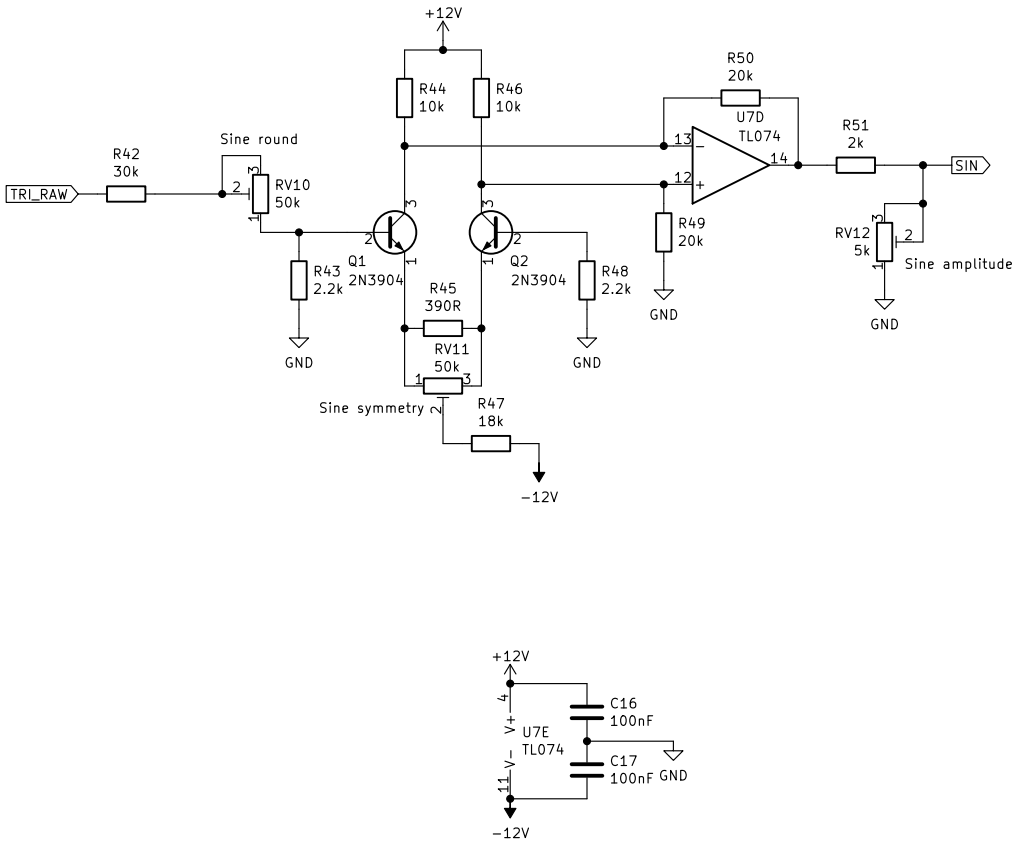
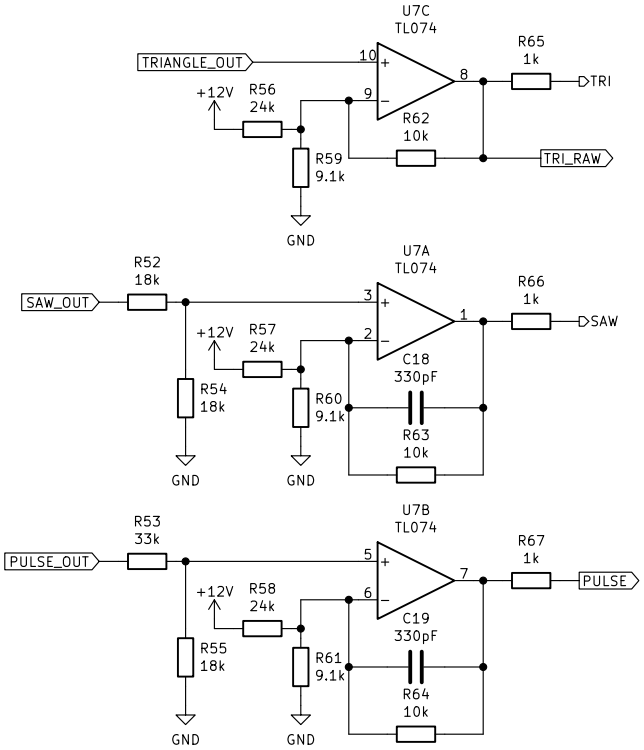
SINE SHAPING



OUTPUT CONDITIONING



Kassutronics used 100k feedback resistors and similarly large values for voltage divider resistors. AS3340 datasheet calls for a 51k pulldown on pin 4, so I reduced the voltage divider resistances by a factor ~ (51k/(180k+100k)). Op amp resistances were reduced by a factor of 10. Then stabilization caps were increased more to make 1/(2πRC) ~ 50kHz.

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Sheet: /Outputs and sin/
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