



»» **DATA SHEET**

( DOC No. HX8309-A-DS )

»» **HX8309-A**

176RGB x 220 dot,  
262,144-Color TFT Controller  
Driver with Internal RAM  
*Version 02 November, 2005*

***List of Contents***

November, 2005

<b>General Description</b> .....	7
<b>Features</b> .....	8
<b>1. Device Overview</b> .....	9
1.1 Block Diagram .....	9
1.2 Pin Description.....	10
1.3 Pin assignment .....	15
1.4 BUMP Arrangement.....	20
<b>2. Interface</b> .....	21
2.1 System Interface.....	21
2.1.1 80-System.....	22
2.1.2 Serial Data Transfer Interface .....	31
2.2 Vsync Interface .....	34
2.3 RGB Interface .....	37
<b>3. Function Description</b> .....	44
3.1 Graphics RAM .....	44
3.1.1 Window Address Function.....	52
3.1.2 High-Speed Burst RAM Write Function .....	53
3.2 Graphics Operation Function .....	58
3.3 Display Function .....	64
3.3.1 Scan Mode Setting.....	64
3.3.2 Partial Screen Display .....	65
3.3.3 8-Color Display.....	68
3.3.4 N-line Inversion LCD Drive .....	70
3.3.5 Interlaced Driving Function.....	71
3.3.6 AC Driving Alternating Timing.....	72
3.4 Frame-Frequency Adjustment Function.....	73
3.5 γ-Correction Function .....	74
3.6 Oscillator.....	84
<b>4. Introduction</b> .....	85
<b>5. Power Generation</b> .....	124
5.1 Specification.....	124
5.2 Power supply Circuit.....	125
5.3 Voltage Setting.....	126
5.4 Register Setting .....	127
5.5 Power Supply Setting .....	129
<b>6. Electrical Characteristic</b> .....	130
6.1 Absolute Maximum Ratings .....	130
6.2 AC Characteristic .....	131
6.3 DC Characteristic.....	137
<b>7. System Configuration</b> .....	142
7.1 System Diagram .....	142
7.2 Layout Recommendation .....	143
<b>8. Ordering information</b> .....	144
<b>9. Revision History</b> .....	144

***List of Figures***

November, 2005

Figure 2. 1 Example of 80 System 18-bit bus Interface .....	22
Figure 2. 2 Data Format of 18-bit bus System Interface .....	22
Figure 2. 3 Example of 80 System 16-bit bus Interface .....	23
Figure 2. 4 Data Format of 16-bit bus System Interface .....	24
Figure 2. 5 Example of 80 System 9-bit bus Interface .....	25
Figure 2. 6 Data Format of 9-bit bus System Interface .....	25
Figure 2. 7 Example of 80 System 8-bit bus Interface .....	26
Figure 2. 8 Data Format of 8-bit bus System Interface .....	27
Figure 2. 9 18 / 16-bit Parallel Bus Interface Timing ( for i80 series MPU ) .....	28
Figure 2. 10 9 / 8-bit Parallel Bus Interface Timing ( for i80 series MPU ) .....	29
Figure 2. 11 8-bit Parallel Bus Interface Timing ( for i80 series MPU ) .....	30
Figure 2. 12 Data Format of Serial Data Transfer Interface GRAM .....	32
Figure 2. 13 Data Transfer through Serial Data Transfer Interface .....	33
Figure 2. 14 VSYNC Interface to MPU .....	34
Figure 2. 15 VSYNC Interface with Internal Clock and System Interface with Internal Clock .....	36
Figure 2. 16 Example of Update Still and Moving Picture .....	38
Figure 2. 17 Transition between System Interface Mode and RGB Interface Mode .....	39
Figure 2. 18 RAM Data Write Sequence through System Interface or RGB Interface during RGB .....	40
Figure 2. 19 18-bit RGB Interface .....	41
Figure 2. 20 Data Format for 18-bit Interface .....	41
Figure 2. 21 16-bit RGB Interface .....	42
Figure 2. 22 Data Format for 16-bit Interface .....	42
Figure 2. 23 6-bit RGB Interface .....	43
Figure 2. 24 Data Format for 6-bit Interface .....	43
Figure 3. 1 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "0", BGR = "0") .....	45
Figure 3. 2 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "0", BGR = "0") .....	45
Figure 3. 3 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = "0", BGR = "0") .....	46
Figure 3. 4 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = "0", BGR = "0") .....	46
Figure 3. 5 GRAM Data and Display Data of RGB Interface (SS = "0", BGR = "0") .....	47
Figure 3. 6 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "1", BGR = "1") .....	49
Figure 3. 7 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "1", BGR = "1") .....	49
Figure 3. 8 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = "1", BGR = "1") .....	50
Figure 3. 9 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = "1", BGR = "1") .....	50
Figure 3. 10 GRAM Data and Display Data of RGB Interface (SS = "1", BGR = "1") .....	51
Figure 3. 11 Address Update Direction Settings .....	52
Figure 3. 12 The Operation of High-speed Burst RAM Function .....	53
Figure 3. 13 Example of the Operation of High-Speed Consecutive Writing to RAM .....	54
Figure 3. 14 Example of the High-Speed RAM Write with a Window Address-Range Specification .....	57
Figure 3. 15 Graphics Operations .....	58
Figure 3. 16 Write Data Mask Function .....	59
Figure 3. 17 Example1 of Write Mode Operation .....	60
Figure 3. 18 Example2 of Write Mode Operation .....	61
Figure 3. 19 Example3 of Write Mode Operation .....	62
Figure 3. 20 Example4 of Write Mode Operation .....	63
Figure 3. 21 SCAN Mode Setting .....	64
Figure 3. 22 Partial Screen Display Example in 2-Windows Driving .....	65
Figure 3. 23 Partial Display Setting Flow .....	67
Figure 3. 24 Grayscale Control in 8-Color Mode .....	68
Figure 3. 25 Switch Sequence between 262,144-color Mode and 8-color Mode .....	69
Figure 3. 26 N-line Inversion Driving Diagram .....	70
Figure 3. 27 Output Timing for Interlaced Gate Signals (Three-Field is selected) .....	71
Figure 3. 28 AC Driving Alternating Timing Diagram .....	72
Figure 3. 29 Grayscale Control .....	74

***List of Figures***

November, 2005

Figure 3. 30 Structure of Grayscale Voltage Generator .....	75
Figure 3. 31 Gamma Resister Stream and Gamma Reference Voltage .....	77
Figure 3. 32 Relationship between Source Output and Vcom .....	83
Figure 3. 33 Relationship between GRAM Data and Output Level .....	83
Figure 3. 34 Oscillation Circuit .....	84
Figure 4. 1 80-System Interface Mode .....	87
Figure 4. 2 Index Register .....	88
Figure 4. 3 Status Read Register .....	88
Figure 4. 4 Start Oscillation Register (R00h) .....	88
Figure 4. 5 Driver Output Control Register (R01h) .....	88
Figure 4. 6 LCD-Driving-Waveform Control Register (R02h) .....	90
Figure 4. 7 Entry Mode Register (R03h) .....	90
Figure 4. 8 Address Direction Settings .....	91
Figure 4. 9 The Setting of DFM and TRI (80-system 16-bit Interface) .....	92
Figure 4. 10 The Setting of DFM and TRI (80-system 8-bit Interface) .....	93
Figure 4. 11 The Setting of DFM and TRI (Serial Data Transfer Interface) .....	93
Figure 4. 12 Compare Register 1 (R04h) .....	94
Figure 4. 13 Compare Register 2 (R05h) .....	94
Figure 4. 14 Bit Operation .....	94
Figure 4. 15 Display Control Register 1 (R07h) .....	95
Figure 4. 16 Display Control Register 2 (R08h) .....	97
Figure 4. 17 BP/FP .....	98
Figure 4. 18 Display Control Register 3 (R09h) .....	99
Figure 4. 19 Frame Cycle Control Register (R0Bh) .....	99
Figure 4. 20 Equalized Period and Source Output Delay .....	101
Figure 4. 21 Non-overlap Time between Two Adjacent Gate Output Pulses .....	102
Figure 4. 22 External Display Interface Control Register (R0Ch) .....	102
Figure 4. 23 Power Control Register 1 (R10h) .....	103
Figure 4. 24 Power Control Register 2 (R11h) .....	105
Figure 4. 25 Power Control Register 3 (R12h) .....	107
Figure 4. 26 Power Control Register 4 (R13h) .....	107
Figure 4. 27 RAM Address Register (R21h) .....	109
Figure 4. 28 Write Data Register (R22h) .....	109
Figure 4. 29 Input Data Written to GRAM through Write Data Register in 18-bit Interface Mode .....	110
Figure 4. 30 Input Data Written to GRAM through Data Register in 16-bit Interface Mode .....	110
Figure 4. 31 Input Data Written to GRAM through Data Register in 9-bit Interface Mode .....	111
Figure 4. 32 Input Data Written to GRAM through Write Data Register in 8-bit Interface Mode .....	111
Figure 4. 33 Input Data Written to GRAM through Write Data Register in 18-/16-/6-bit RGB .....	112
Figure 4. 34 Read Data Register (R22h) .....	114
Figure 4. 35 Output Data Read from GRAM through Read Data Register in 18-bit Interface .....	114
Figure 4. 36 Output Data Read from GRAM through Read Data Register in 16-/9-/8-bit Interface .....	115
Figure 4. 37 Flow Chart of GRAM Read Data .....	116
Figure 4. 38 Write Data Mask Register 1 (R23h) .....	116
Figure 4. 39 Write Data Mask Register 1 (R24h) .....	116
Figure 4. 40 GRAM Write Data Mask .....	117
Figure 4. 41 Gamma Control Register 1~10 (R30h~R39h) .....	117
Figure 4. 42 Gate Scan Position Register (R40h) .....	118
Figure 4. 43 SCN Bits and Scanning Start Position for Gate Driver .....	118
Figure 4. 44 Vertical Scroll Control Register (R41h) .....	119
Figure 4. 45 First Screen Driving Position Register (R42h) .....	120
Figure 4. 46 Second Screen Driving Position Register (R43h) .....	120
Figure 4. 47 Horizontal RAM Address Position Register (R44h) .....	120
Figure 4. 48 Vertical RAM Address Position Register (R45h) .....	120
Figure 4. 49 Window Address Setting Range .....	121

# >> HX8309-A

176RGB x 220 dot, 262,144-Color TFT  
Controller Driver with Internal RAM



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## List of Figures

November, 2005

Figure 5. 1 Block Diagram of Power Supply Circuit .....	125
Figure 5. 2 Voltage Setting Diagram .....	126
Figure 5. 3 Applied Voltage of TFT Display .....	126
Figure 5. 4 Register Setting Sequence .....	127
Figure 5. 5 Standby Mode and Sleep Mode Setting Sequence.....	128
Figure 5. 6 Power Supply Setting Flow .....	129
Figure 6. 1 80-system Bus Timing .....	138
Figure 6. 2 Clock Synchronized Serial Data Transfer Interface Timing.....	139
Figure 6. 3 RGB Interface Operation .....	140
Figure 6. 4 LCD Driving Output.....	141
Figure 6. 5 Reset Timing.....	141
Figure 7. 1 System Diagram of HX8309-A.....	142

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-P.4-  
November 2005

***List of Tables***

November, 2005

Table 2. 1 Register Selection (18-/16-/9-/8- Bit System Interface) .....	21
Table 2. 2 Register Selection (Serial Data Transfer Interface) .....	21
Table 2. 3 The Function of RS and R/W Bit bus.....	31
Table 2. 4 DIM Bit Set .....	34
Table 2. 5 EPL and ENABLE Set .....	37
Table 3. 1 GRAM Address and Display Panel Position (SS = "0", BGR = "0") .....	44
Table 3. 2 GRAM Address and Display Panel Position (SS = "1", BGR="1") .....	48
Table 3. 3 Comparisons between Normal and High-Speed RAM Write Operation.....	55
Table 3. 4 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits) .....	56
Table 3. 5 Number of Dummy Write Operation in High-Speed RAM Write (HEA Bits) .....	56
Table 3. 6 Bit Set of Graphics Operation Function .....	58
Table 3. 7 Conditions on One Screen Driving (STP = 0).....	66
Table 3. 8 Condition on Two Screen Driving (STP = 1).....	66
Table 3. 9 Source and Gate Output in Non-Display Area during Partial Display Function .....	66
Table 3. 10 Combined with GS and FLD Setting.....	71
Table 3. 11 Gamma-Adjustment Registers.....	76
Table 3. 12 Offset Adjustment 0    Table 3. 13 Offset Adjustment 1    Table 3. 14 Center Adjustment....	78
Table 3. 15 Output Voltage of 8 to 1 Selector.....	78
Table 3. 16 Voltage Calculation Formula (Positive Polarity).....	79
Table 3. 17 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity) .....	80
Table 3. 18 Voltage Calculation Formula (Negative Polarity) .....	81
Table 3. 19 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity) .....	82
Table 3. 20 External Resistance Value and R-C Oscillation Frequency (Temporally Define) .....	84
Table 4. 1 List Table of Register Set .....	86
Table 4. 2 NL bits and Scan Line .....	89
Table 4. 3 EPL Bit and Enable Pin .....	89
Table 4. 4 FLD Bits and Interlaced Field .....	90
Table 4. 5 D Bits and Operation .....	95
Table 4. 6 Display Control Instruction .....	95
Table 4. 7 CL Bit for 8-Color Display .....	96
Table 4. 8 GON and DTE Bits .....	96
Table 4. 9 VLE Bits .....	96
Table 4. 10 PT Bits for Source and Gate Output in Non-Display Area of Partial Display.....	97
Table 4. 11 BP/FP Bits Setting .....	98
Table 4. 12 BP3-0, FP3-0 Setting Dependent on Operation Mode .....	98
Table 4. 13 PTG Bits Setting.....	99
Table 4. 14 ISC Bit2 Setting .....	99
Table 4. 15 RTN Bits and Clock Cycles .....	100
Table 4. 16 DIV Bits and Clock Frequency.....	100
Table 4. 17 CE Bits for Equalized Period .....	101
Table 4. 18 SDT Bits for Source Output Delay .....	101
Table 4. 19 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulses.....	102
Table 4. 20 Clock Source for Interface Mode .....	102
Table 4. 21 RIM Bits for Transfer Mode of RGB interface .....	103
Table 4. 22 DM Bits for Operation Mode of LCD display.....	103
Table 4. 23 RM Bit for Access Interface of GRAM .....	103
Table 4. 24 DK Bit for Operation of Step-up Circuit 1 .....	104
Table 4. 25 AP Bits and Amount of Current in Operational Amplifier .....	104
Table 4. 26 BT Bits and VLCD and VGH Outputs .....	105
Table 4. 27 SAP Bits and Amount of Current in Operational Amplifier .....	105
Table 4. 28 VC Settings and Internal Reference Voltage .....	106
Table 4. 29 Operation Frequency of Step-up Circuit 1 .....	106
Table 4. 30 Operation Frequency of Step-up Circuit 2 .....	106

***List of Tables***

November, 2005

Table 4. 31 VRH Bits and VGAM1OUT Voltage .....	107
Table 4. 32 VCM4-0 Bits and VcomH Voltage.....	108
Table 4. 33 VDV4-0 Bits and Vcom Amplitude .....	108
Table 4. 34 GRAM Address Mapping .....	109
Table 4. 35 GRAM Data and Grayscale Level .....	113
Table 4. 36 SCN bits and Scanning Start Position for Gate Driver.....	118
Table 4. 37 VL Bits and Scrolling Length .....	119
Table 5. 1 Adoptability of Capacitor.....	124
Table 5. 2 Adoptability of Schottkey diode.....	124
Table 5. 3 Adoptability of Variable resistor .....	124
Table 6. 1 Absolute Maximum Rating.....	130
Table 6. 2 Clock Characteristics (Vcc = 2.4 ~ 3.3V).....	131
Table 6. 3 Normal Write Mode (HWM = 0) / (IOVcc = 1.65 ~ 2.4V) / (Vcc=2.4~3.3V) .....	131
Table 6. 4 Normal Write Mode (HWM = 0) / (IOVcc = 2.4 ~ 3.3V) / (Vcc=2.4~3.3V) .....	131
Table 6. 5 High-Speed Write Mode (HWM = 1) / (IOVcc = 1.65 ~ 2.4V) / (Vcc=2.4~3.3V) .....	132
Table 6. 6 High-Speed Write Mode (HWM = 1) / (IOVcc = 2.4 ~ 3.3V) / (Vcc=2.4~3.3V) .....	132
Table 6. 7 Normal Write Mode (HWM = 0) / (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V) .....	133
Table 6. 8 Normal Write Mode (HWM = 0) / (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V) .....	133
Table 6. 9 (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V) .....	134
Table 6. 10 (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V) .....	134
Table 6. 11 18-/16-bit Bus RGB Interface Mode and High-Speed Write Mode ( HWM = 1 ) / .....	135
Table 6. 12 18-/16-bit Bus RGB Interface Mode and High-Speed Write Mode ( HWM = 1 ) / .....	135
Table 6. 13 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1) / (IOVcc=1.65~2.4V) /136	136
Table 6. 14 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1) / (IOVcc=2.4~3.3V) / 136	136
Table 6. 15 Driver output delay timing.....	136
Table 6. 16 (IOVcc=1.65~3.3V) / (Vcc = 2.4 ~ 3.3V) .....	136
Table 6. 17 DC Characteristic (Vcc = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C) .....	137

## >> HX8309-A

176RGB x 220 dot, 262,144-Color TFT  
Controller Driver with Internal RAM



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*Version 02*

*November, 2005*

## General Description

This manual describes the Himax's HX8309-A 176RGB\*220 dots resolution driving controller. The HX8309-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 176RGB\*220 dots at maximum.

The HX8309-A can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8309-A also supports various functions to reduce the power consumption of a LCD system via software control, such as an standby mode, sleep mode and 8-color display mode, The HX8309-A has four system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, VSYNC interface (internal clock, DB17-0), serial data transfer interface and RGB18-/16-/6-bit bus interface (DOTCLOCK, VSYNC, HSYNC, ENABLE, PD17-0). In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write mode and widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers.

The HX8309-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

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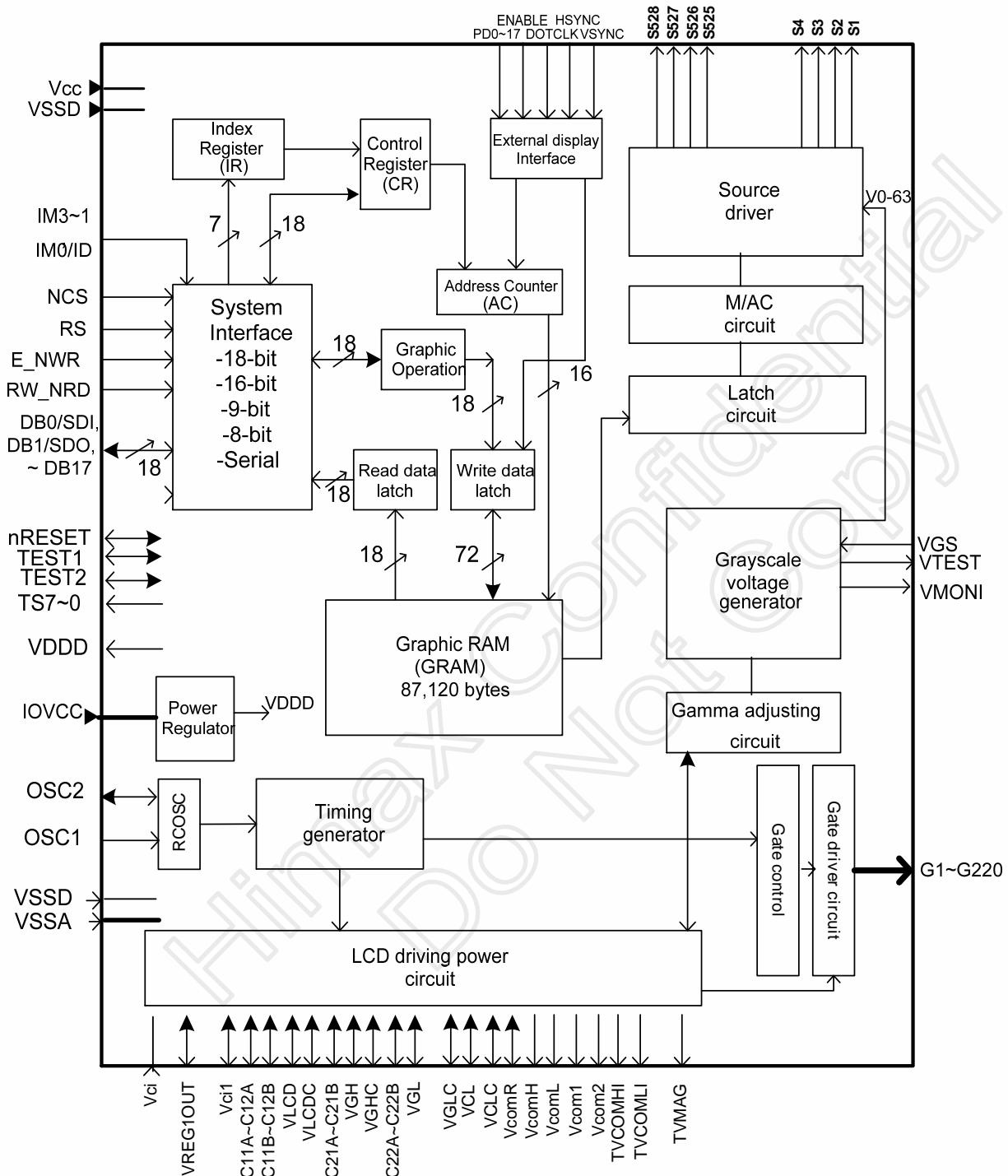
*-P.7-*  
November 2005

## Features

- ~ Single chip solution to drive a TFT panel
- ~ 176RGB x 220-dot graphics display LCD controller/driver and 262,144 TFT colors
- ~ Support interface:
  - 80 System interface (8-/9-/16-/18-bit bus)
  - Serial Data Transfer Interface
  - RGB interface (6-/16-/18-bit bus)
  - VSYNC data transfer interface
- ~ Internal graphics RAM capacity: 87,120 bytes
- ~ The 262,144 colors can be displayed at the same time with gamma correction
- ~ The vertical scroll display function in line units
- ~ Internal operation circuit of liquid crystal display:
  - Source channel: 528
  - Gate line: 220
- ~ To write data in a window-RAM address area by using a window-address function
- ~ Bit-operation functions for graphics transaction:
  - The write data mask function in bit unit
  - The logical operation in pixel unit and conditional write function
- ~ Low-power consumption architecture supports:
  - $V_{ci}$  = 2.5 to 3.3 V (internal reference voltage)
  - $V_{cc}$  = 2.4 to 3.3 V (corresponding low-voltage operation)
  - $I_{OVcc}$  = 1.65 to 3.3 V (Interface I/O operation)
  - $V_{LCD}$  = 4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - Standby mode
    - Sleep mode
- ~ N-line inversion AC liquid-crystal drive
- ~ Partial liquid crystal drive to display two screens at arbitrary positions
- ~ Internal oscillator and hardware reset function

## 1. Device Overview

### 1.1 Block Diagram



## 1.2 Pin Description

Input Parts																											
Signals	I/O	Pin Number	Connected with	Description																							
IM3-1, IMO	I	4	VSSD/ IOVcc	Select the MPU interface mode as listed below																							
				IM0 (ID)	IM1	IM2	IM3	MPU interface mode	DB pins																		
				0	0	0	0	Setting invalid	-																		
				1	0	0	0	Setting invalid	-																		
				0	1	0	0	16-bit bus interface, 80-system	DB17-10, 8-1																		
				1	1	0	0	8-bit bus interface, 80-system	DB17-10																		
				ID	0	1	0	Serial data transfer interface	DB1-0																		
				*	1	1	0	Setting invalid	-																		
				0	0	0	1	Setting invalid	-																		
				1	0	0	1	Setting invalid	-																		
				0	1	0	1	18-bit bus interface, 80-system	DB17-0																		
				1	1	0	1	9-bit bus interface, 80-system	DB17-9																		
				*	*	1	1	Setting invalid	-																		
Note: If the serial data transfer interface was selected, IMO pin is used like the ID setting for the device code in transfer data.																											
NCS	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. Must be connected to VSSD if not in use.																							
RS	I	1	MPU	The signal for register index or register command select. Low: Register index or internal status (in read operation); High: Register command. Connect to IOVcc or VSSD level when serial data transfer interface is selected.																							
VLD	I	1	MPU	Fix to VSSD																							
E_NWR/SCL	I	1	MPU	Serves as a write signal and writes data at the rising edge in i80 system interface. Serves as the synchronous clock signal in serial data transfer interface.																							
RW_NRD	I	1	MPU	Low: Write ; High: Read) Serves as a read signal and reads data at the low level in i80 system interface. Fix it to IOVcc or VSSD level when using serial data transfer interface.																							
ENABLE	I	1	MPU	A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVcc level. Low: Selected (access enabled) The polarity of the ENABLE signal is inverted by the EPL bit.																							
				<table border="1"> <tr> <th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr> <tr> <td>0</td><td>0</td><td>Enable</td><td>Update</td></tr> <tr> <td>0</td><td>1</td><td>Disable</td><td>Keep</td></tr> <tr> <td>1</td><td>0</td><td>Disable</td><td>Keep</td></tr> <tr> <td>1</td><td>1</td><td>Enable</td><td>Update</td></tr> </table>				EPL	ENABLE	RAM write	RAM address	0	0	Enable	Update	0	1	Disable	Keep	1	0	Disable	Keep	1	1	Enable	Update
EPL	ENABLE	RAM write	RAM address																								
0	0	Enable	Update																								
0	1	Disable	Keep																								
1	0	Disable	Keep																								
1	1	Enable	Update																								
VSYNC	I	1	MPU	Frame synchronizing signal. The polarity of the VSYNC signal is selected by VSPL bit. 0: Start in the low level, 1: Start in the high level Fix to the IOVcc level when not used.																							
HSYNC	I	1	MPU	Frame synchronizing signal. The polarity of the HSYNC signal is selected by HSPL bit. 0: Start in the low level, 1: Start in the high level. Fix to the IOVcc level when not used.																							
DOTCLK	I	1	MPU	Dot clock signal. Fix to the IOVcc level when not used. If DPL=0: Data are latched on the rising edge of DOTCLK. If DPL=1: Data are latched on the falling edge of DOTCLK.																							
PD0~17	I	18	MPU	An 18-bit bus RGB data bus in 80-system interface mode. Fix the unused pins to either the VSSD level or the IOVcc level. 6-bit bus: use PD17-PD12 16-bit bus: use PD17-PD13 and PD11-PD1 18-bit bus: use PD17-PD0																							

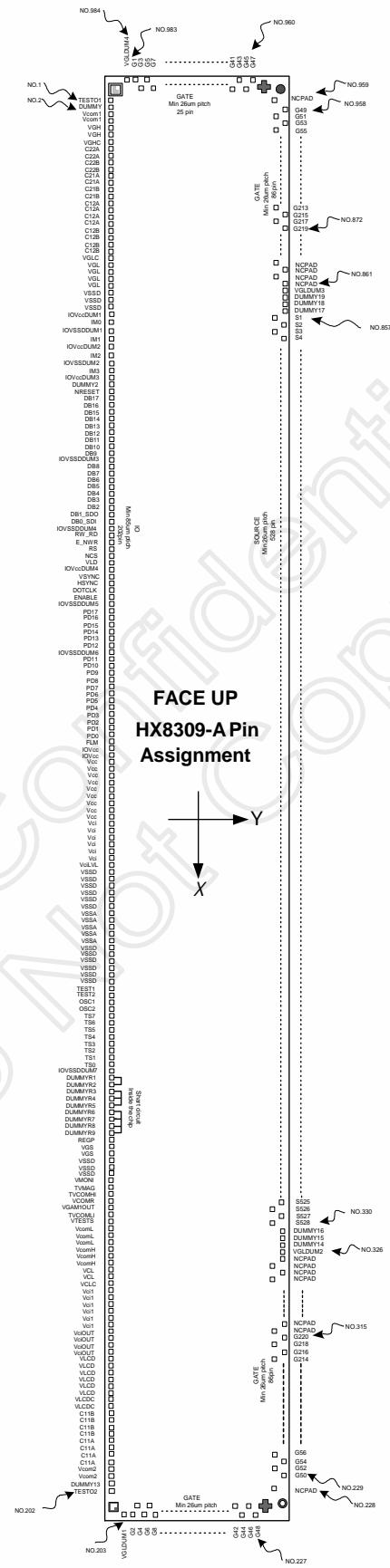
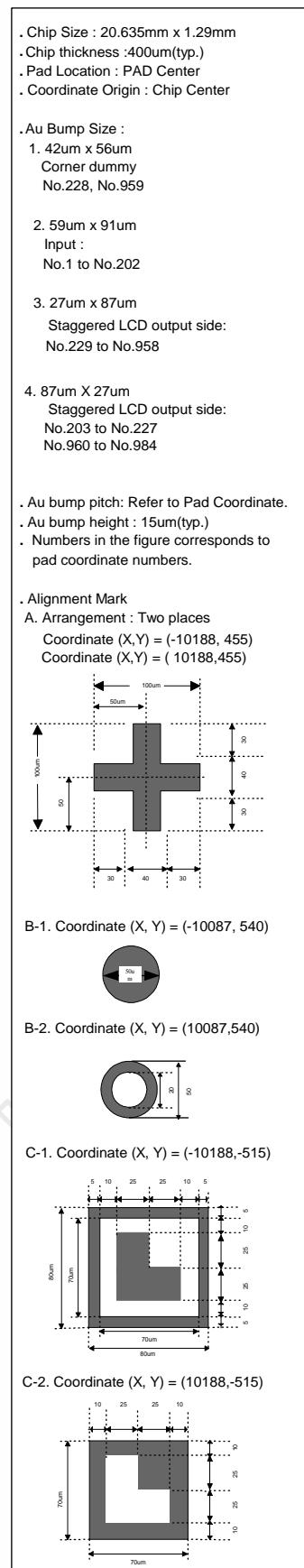
Input Parts				
Signals	I/O	Pin Number	Connected with	Description
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
VcomR	I	1	Variable Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VGAM1OUT and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8309-A.
VLCD	I	1	VLCDC	A power supply for the source driver outputs. A reference voltage for the step-up circuit2
VGH	I	1	VGHC	A power supply for the TFT LCD's gate driver. Connect to VGHC.
VGL	I	1	VGLC	A power supply for the TFT LCD's gate driver. Connect to VGLC.
VCL	I	1	VCLC	A power supply for the VcomL level. Connect to VCLC.
TEST1	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
TEST2	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
Vci	I	1	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VciLVL	I	1	Power Supply	Generates a reference voltage (VciOUT, REGP) from the VciLVL level according to the ratio determined by the VC2-0 BITS. Connect to Vci on the FPC.

Output Part				
Signals	I/O	Pin Number	Connected with	Description
S1~S528	O	528	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0, DATA IN THE ram address "0000" is output from S1. If SS=1, the same data in the ram address "0000" is output from S528. S1, S4, S7...display red (R), S2, S5, S8...display green (G), and S3, S6, S9...display blue (B) (SS=0).
G1~G220	O	220	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
Vcom1, Vcom2,	O	2	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VcomH and VcomL is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel.
VcomH	O	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of Vcom amplitude generated in driving the Vcom alternation.
VcomL	O	1	Stabilizing Capacitor or open	When the Vcom alternation is driven, this pin indicates a low level of Vcom amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
FLM	O	1	MPU or open	A frame head pulse (amplitude: IOVcc-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it.
VciOUT	O	1	Stabilizing Capacitor Vci1	An internal reference voltage. The amplitude between Vci and VSSD is determined by the VC2-0 bits.
VLCDC	O	1	Stabilizing Capacitor, VLCD	An output from the step-up circuit1 of twice is the Vci1 level. Connect to a stabilizing capacitor between VSSD and VLCDC. Place a schottkey barrier diode. (See "power supply circuit"). VLCDC =4.5 to 5.5V
VGHC	O	1	Stabilizing Capacitor, VGH	An output from the step-up circuit2 or 4 ~ 6 time the Vci1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGHC. Place a schottkey barrier diode between Vci and VGHC. Place a schottkey barrier diode (see "power supply circuit"). VGHC=16.5V
VGLC	O	1	Stabilizing capacitor, VGL	An output from the step-up circuit2 or -3 ~ -5 time the Vci1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGLC. Place a schottkey barrier diode between Vci and VGLC. Place a schottkey barrier diode (see "power supply circuit"). VGLC=min -16.5V
VCLC	O	1	Stabilizing capacitor, VCL	An output from the step-up circuit of 1-time the Vci1 level. Connect to stabilizing capacitor .VCLC=0~ -3.3V
VMONI	O	1	Open	A test pin. Disconnect it.
TS0 ~ 7		8	Open	A test pin. Disconnect it.
VTESTS	O	1	Open	A test pin. Disconnect it.
IOVccDUM1~4	O	4	Input pin	Internal IOVcc level outputs. When adjacent input pins are fixed to the IOVcc level, short-circuit them.
IOVSSDDUM 1~4	O	4	Input pin	Internal VSSD level outputs. When neighboring input pins are fixed to the VSSD level, short-circuit them.

Input/Output Part				
Signals	I/O	Pin Number	Connected with	Description
C11A, C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B, C21A, C21B C22A, C22B	I/O	6	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0_SDI	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Input pin in Serial Data Transfer interface. The input data is latched by the rising edge of the SCL signal on the chip.
DB1_SDO	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Output pin operate in Serial Data Transfer interface, the data is output by the falling edge of the SCL signal on the chip. If operate in Serial Data Transfer interface, do not connect the DB1_SDO pin to VSSD.
DB2~17	I/O	16	MPU	Operates liked a 18-bit bi-directional data bus 8-bit bus: use DB17-DB10 9-bit bus: use DB17-DB9 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 Connected unused pins to the IOVcc or VSSD level.
REGP	I/O	1	Test pin	A test pin for VGAM1OUT. Disconnect it.
Vci1	I/O	1	VciOUT	A reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
VGAM1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM2 between VSSD and VLCD from the reference voltage between Vci and VSSD that is generated internally. VGAM1OUT serves as a source driver grayscale reference voltage VGAM2, a VcomH level reference voltage, and a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT = 3.0 ~ (VLCD - 0.5)V
TVCOMHI	I/O	1	Open	A test pin for VcomH. It must be connected with the capacitor 0.1uF to VSSD.
TVCOMLI	I/O	1	Open	A test pin for VcomL. It must be connected with the capacitor 0.1uF to VSSD.
TVMAG	I/O	1	Open	A test pin for VcomL. It must be connected with the capacitor 0.1uF to VSSD.
TESTO1~4	-	4	-	Test pins. Disconnect them.
DUMMY1,2,13	-	3	-	Test oins. Disconnect them.
DUMMY3-12,14-19	-	16	-	Dummy pads. Can be connected to the wiring to the COG panel.
DUMMYR1-9	-	9	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3, DUMMYR4 and DUMMYR5 are short-circuited within the chip. DUMMYR6, DUMMYR7, DUMMYR8, and DUMMYR9 are short circuited within the chip.
VGLDUM1~4	-	4	-	Outputs the internal VGL level. Use as dummy gate output pins.
NCPAD	-	20	Open	No connected pad. Disconnected it.

Power Part				
Signals	I/O	Pin Number	Connected with	Description
Vcc	-	1	Power supply	A power supply for the internal logic. Vcc = 2.4 ~ 3.3V
IOVcc	-	1	Power supply	A power supply for the interface pins. When using the COG method, usually connect to Vcc on the FPC to prevent noise. Voltage range: 1.65 ~ 3.3V
VSSA	-	1	Power supply	Analogy ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSD	-	1	Power supply	Ground for the internal RAM. VSSD = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.

### 1.3 Pin assignment



**PAD Coordinate**

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	TEST01	-9828	-524.5	66	NCS	-3689	-524.5	131	OSC1	2703	-524.5	196	C11A	9266	-524.5
2	DUMMY1	-9743	-524.5	67	VLD	-3604	-524.5	132	OSC2	2788	-524.5	197	C11A	9351	-524.5
3	Vcom1	-9658	-524.5	68	IOVCCDUM4	-3519	-524.5	133	TS7	2944	-524.5	198	C11A	9436	-524.5
4	Vcom1	-9573	-524.5	69	VSYNC	-3434	-524.5	134	TS6	3029	-524.5	199	VCOM2	9521	-524.5
5	VGH	-9488	-524.5	70	HSYNC	-3349	-524.5	135	TS5	3114	-524.5	200	VCOM2	9606	-524.5
6	VGH	-9403	-524.5	71	DOTCLK	-3264	-524.5	136	TS4	3199	-524.5	201	DUMMY13	9691	-524.5
7	VGHC	-9318	-524.5	72	ENABLE	-3179	-524.5	137	TS3	3284	-524.5	202	TEST02	9776	-524.5
8	C22A	-9070	-524.5	73	IOVSSDDUM5	-3094	-524.5	138	TS2	3369	-524.5	203	VGLDUM1	10199	-305
9	C22A	-8985	-524.5	74	PD17	-3009	-524.5	139	TS1	3454	-524.5	204	G2	10077	-279
10	C22B	-8900	-524.5	75	PD16	-2924	-524.5	140	TS0	3539	-524.5	205	G4	10199	-253
11	C22B	-8815	-524.5	76	PD15	-2839	-524.5	141	IOVSSDDUM7	3624	-524.5	206	G6	10077	-227
12	C21A	-8730	-524.5	77	PD14	-2754	-524.5	142	DUMMYR1	3709	-524.5	207	G8	10199	-201
13	C21A	-8645	-524.5	78	PD13	-2669	-524.5	143	DUMMYR2	3794	-524.5	208	G10	10077	-175
14	C21B	-8560	-524.5	79	PD12	-2584	-524.5	144	DUMMYR3	3879	-524.5	209	G12	10199	-149
15	C21B	-8475	-524.5	80	IOVSSDDUM6	-2499	-524.5	145	DUMMYR4	3964	-524.5	210	G14	10077	-123
16	C12A	-8390	-524.5	81	PD11	-2414	-524.5	146	DUMMYR5	4049	-524.5	211	G16	10199	-97
17	C12A	-8305	-524.5	82	PD10	-2329	-524.5	147	DUMMYR6	4134	-524.5	212	G18	10077	-71
18	C12A	-8220	-524.5	83	PD9	-2244	-524.5	148	DUMMYR7	4219	-524.5	213	G20	10199	-45
19	C12A	-8135	-524.5	84	PD8	-2159	-524.5	149	DUMMYR8	4304	-524.5	214	G22	10077	-19
20	C12B	-8050	-524.5	85	PD7	-2074	-524.5	150	DUMMYR9	4389	-524.5	215	G24	10199	7
21	C12B	-7965	-524.5	86	PD6	-1989	-524.5	151	REGP	4474	-524.5	216	G26	10077	33
22	C12B	-7880	-524.5	87	PD5	-1904	-524.5	152	VGS	4559	-524.5	217	G28	10199	59
23	C12B	-7795	-524.5	88	PD4	-1819	-524.5	153	VGS	4644	-524.5	218	G30	10077	85
24	VGLC	-7547	-524.5	89	PD3	-1734	-524.5	154	VSSD	4917	-524.5	219	G32	10199	111
25	VGL	-7462	-524.5	90	PD2	-1649	-524.5	155	VSSD	5002	-524.5	220	G34	10077	137
26	VGL	-7377	-524.5	91	PD1	-1564	-524.5	156	VSSD	5087	-524.5	221	G36	10199	163
27	VGL	-7292	-524.5	92	PD0	-1479	-524.5	157	VMONI	5360	-524.5	222	G38	10077	189
28	VGL	-7207	-524.5	93	FLM	-1394	-524.5	158	TVMAG	5445	-524.5	223	G40	10199	215
29	VSSD	-6959	-524.5	94	IOVcc	-1175	-524.5	159	TVCOMHI	5530	-524.5	224	G42	10077	241
30	VSSD	-6874	-524.5	95	IOVcc	-1090	-524.5	160	VcomR	5615	-524.5	225	G44	10199	267
31	VSSD	-6789	-524.5	96	Vcc	-879	-524.5	161	VRGAM1OUT	5700	-524.5	226	G46	10077	293
32	IOVCCDUM1	-6579	-524.5	97	Vcc	-794	-524.5	162	TVCOMLI	5817	-524.5	227	G48	10199	319
33	IM0	-6494	-524.5	98	Vcc	-709	-524.5	163	VTESTS	5934	-524.5	228	NCPAD	9899	404.5
34	IOVSSDDUM1	-6409	-524.5	99	Vcc	-624	-524.5	164	VcomL	6051	-524.5	229	G50	9873	526.5
35	IM1	-6324	-524.5	100	Vcc	-539	-524.5	165	VcomL	6136	-524.5	230	G52	9847	404.5
36	IOVCCDUM2	-6239	-524.5	101	Vcc	-454	-524.5	166	VcomL	6221	-524.5	231	G54	9821	526.5
37	IM2	-6154	-524.5	102	Vcc	-369	-524.5	167	VcomH	6306	-524.5	232	G56	9795	404.5
38	IOVSSDDUM2	-6069	-524.5	103	Vcc	-284	-524.5	168	VcomH	6391	-524.5	233	G58	9769	526.5
39	IM3	-5984	-524.5	104	Vcc	-199	-524.5	169	VcomH	6476	-524.5	234	G60	9743	404.5
40	IOVCCDUM3	-5899	-524.5	105	Vci	-51	-524.5	170	VCL	6686	-524.5	235	G62	9717	526.5
41	DUMMY2	-5814	-524.5	106	Vci	34	-524.5	171	VCL	6771	-524.5	236	G64	9691	404.5
42	NRESET	-5729	-524.5	107	Vci	119	-524.5	172	VCLC	6856	-524.5	237	G66	9665	526.5
43	DB17	-5644	-524.5	108	Vci	204	-524.5	173	Vci1	6997	-524.5	238	G68	9639	404.5
44	DB16	-5559	-524.5	109	Vci	289	-524.5	174	Vci1	7082	-524.5	239	G70	9613	526.5
45	DB15	-5474	-524.5	110	Vci	374	-524.5	175	Vci1	7167	-524.5	240	G72	9587	404.5
46	DB14	-5389	-524.5	111	VciLVL	459	-524.5	176	Vci1	7252	-524.5	241	G74	9561	526.5
47	DB13	-5304	-524.5	112	VSSD	669	-524.5	177	Vci1	7337	-524.5	242	G76	9535	404.5
48	DB12	-5219	-524.5	113	VSSD	754	-524.5	178	Vci1	7422	-524.5	243	G78	9509	526.5
49	DB11	-5134	-524.5	114	VSSD	839	-524.5	179	VciOUT	7633	-524.5	244	G80	9483	404.5
50	DB10	-5049	-524.5	115	VSSD	924	-524.5	180	VciOUT	7718	-524.5	245	G82	9457	526.5
51	DB9	-4964	-524.5	116	VSSD	1009	-524.5	181	VciOUT	7803	-524.5	246	G84	9431	404.5
52	IOVSSDDUM3	-4879	-524.5	117	VSSD	1094	-524.5	182	VciOUT	7888	-524.5	247	TESTO3	9405	526.5
53	DB8	-4794	-524.5	118	VSSA	1274	-524.5	183	VLCD	8161	-524.5	248	G86	9379	404.5
54	DB7	-4709	-524.5	119	VSSA	1359	-524.5	184	VLCD	8246	-524.5	249	G88	9353	526.5
55	DB6	-4624	-524.5	120	VSSA	1444	-524.5	185	VLCD	8331	-524.5	250	G90	9327	404.5
56	DB5	-4539	-524.5	121	VSSA	1529	-524.5	186	VLCD	8416	-524.5	251	G92	9301	526.5
57	DB4	-4454	-524.5	122	VSSA	1614	-524.5	187	VLCD	8501	-524.5	252	G94	9275	404.5
58	DB3	-4369	-524.5	123	VSSD	1794	-524.5	188	VLCD	8586	-524.5	253	G96	9249	526.5
59	DB2	-4284	-524.5	124	VSSD	1879	-524.5	189	VLCDC	8671	-524.5	254	G98	9223	404.5
60	DB1_SDO	-4199	-524.5	125	VSSD	1964	-524.5	190	VLCDC	8756	-524.5	255	G100	9197	526.5
61	DB0_SDI	-4114	-524.5	126	VSSD	2049	-524.5	191	C11B	8841	-524.5	256	G102	9171	404.5
62	IOVSSDDUM4	-4029	-524.5	127	VSSD	2134	-524.5	192	C11B	8926	-524.5	257	G104	9145	526.5
63	RW_NRD	-3944	-524.5	128	VSSD	2219	-524.5	193	C11B	9011	-524.5	258	G106	9119	404.5
64	E_NWR	-3859	-524.5	129	TEST1	2429	-524.5	194	C11B	9096	-524.5	259	G108	9093	526.5
65	RS	-3774	-524.5	130	TEST2	2514	-524.5	195	C11A	9181	-524.5	260	G110	9067	404.5





No.	Pad name	X	Y
781	S77	-4898	404.5
782	S76	-4924	526.5
783	S75	-4950	404.5
784	S74	-4976	526.5
785	S73	-5002	404.5
786	S72	-5028	526.5
787	S71	-5054	404.5
788	S70	-5080	526.5
789	S69	-5106	404.5
790	S68	-5132	526.5
791	S67	-5158	404.5
792	S66	-5184	526.5
793	S65	-5210	404.5
794	S64	-5236	526.5
795	S63	-5262	404.5
796	S62	-5288	526.5
797	S61	-5314	404.5
798	S60	-5340	526.5
799	S59	-5366	404.5
800	S58	-5392	526.5
801	S57	-5418	404.5
802	S56	-5444	526.5
803	S55	-5470	404.5
804	S54	-5496	526.5
805	S53	-5522	404.5
806	S52	-5548	526.5
807	S51	-5574	404.5
808	S50	-5600	526.5
809	S49	-5626	404.5
810	S48	-5652	526.5
811	S47	-5678	404.5
812	S46	-5704	526.5
813	S45	-5730	404.5
814	S44	-5756	526.5
815	S43	-5782	404.5
816	S42	-5808	526.5
817	S41	-5834	404.5
818	S40	-5860	526.5
819	S39	-5886	404.5
820	S38	-5912	526.5
821	S37	-5938	404.5
822	S36	-5964	526.5
823	S35	-5990	404.5
824	S34	-6016	526.5
825	S33	-6042	404.5
826	S32	-6068	526.5
827	S31	-6094	404.5
828	S30	-6120	526.5
829	S29	-6146	404.5
830	S28	-6172	526.5
831	S27	-6198	404.5
832	S26	-6224	526.5
833	S25	-6250	404.5
834	S24	-6276	526.5
835	S23	-6302	404.5
836	S22	-6328	526.5
837	S21	-6354	404.5
838	S20	-6380	526.5
839	S19	-6406	404.5
840	S18	-6432	526.5
841	S17	-6458	404.5
842	S16	-6484	526.5
843	S15	-6510	404.5
844	S14	-6536	526.5
845	S13	-6562	404.5

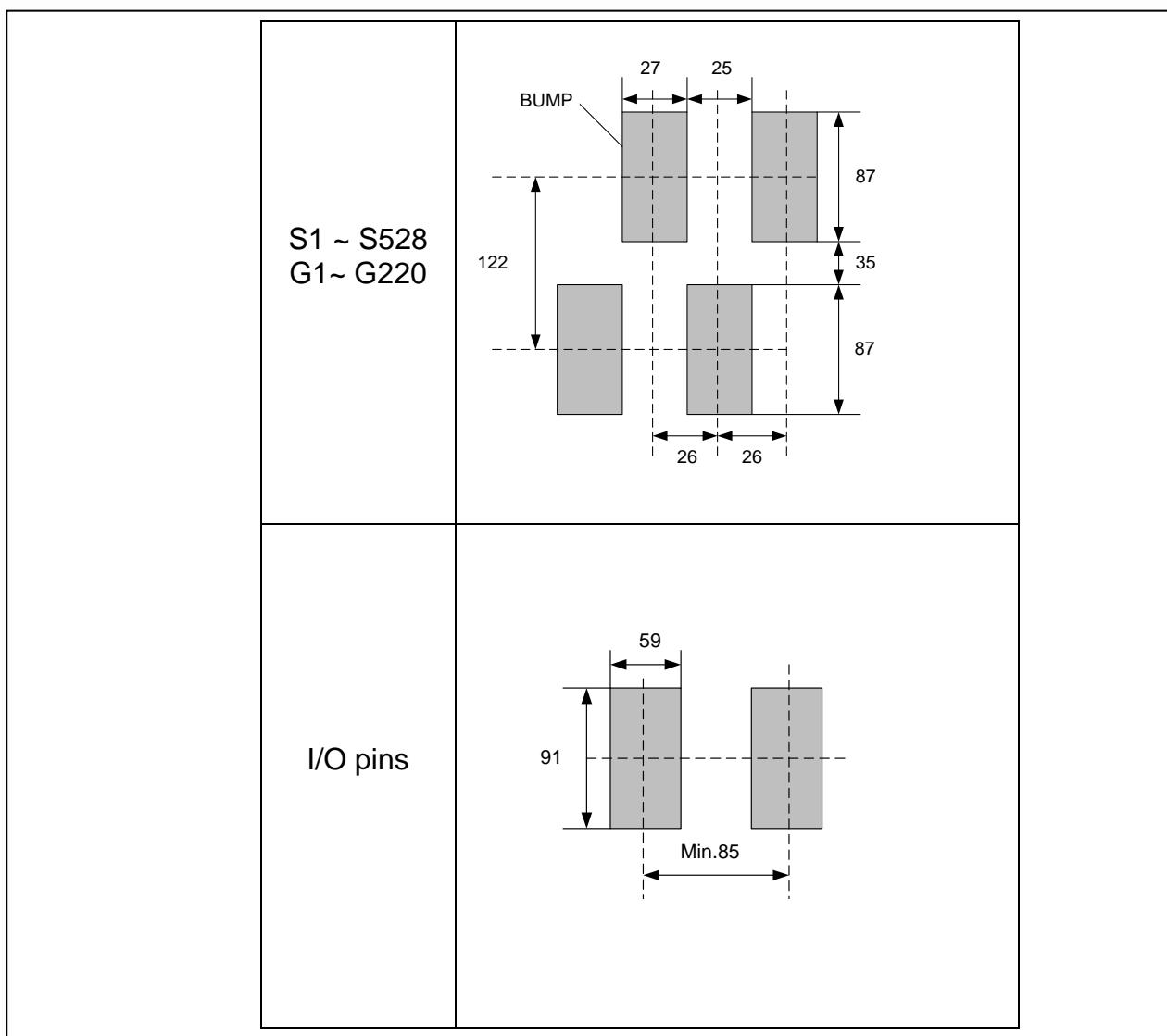
No.	Pad name	X	Y
846	S12	-6588	526.5
847	S11	-6614	404.5
848	S10	-6640	526.5
849	S9	-6666	404.5
850	S8	-6692	526.5
851	S7	-6718	404.5
852	S6	-6744	526.5
853	S5	-6770	404.5
854	S4	-6796	526.5
855	S3	-6822	404.5
856	S2	-6848	526.5
857	S1	-6874	404.5
858	DUMMY17	-7000	526.5
859	DUMMY18	-7052	526.5
860	DUMMY19	-7104	526.5
861	VGLDUM3	-7156	526.5
862	NCPAD	-7377	526.5
863	NCPAD	-7403	404.5
864	NCPAD	-7429	526.5
865	NCPAD	-7455	404.5
866	NCPAD	-7481	526.5
867	NCPAD	-7507	404.5
868	NCPAD	-7533	526.5
869	NCPAD	-7559	404.5
870	NCPAD	-7585	526.5
871	NCPAD	-7611	404.5
872	G219	-7637	526.5
873	G217	-7663	404.5
874	G215	-7689	526.5
875	G213	-7715	404.5
876	G211	-7741	526.5
877	G209	-7767	404.5
878	G207	-7793	526.5
879	G205	-7819	404.5
880	G203	-7845	526.5
881	G201	-7871	404.5
882	G199	-7897	526.5
883	G197	-7923	404.5
884	G195	-7949	526.5
885	G193	-7975	404.5
886	G191	-8001	526.5
887	G189	-8027	404.5
888	G187	-8053	526.5
889	G185	-8079	404.5
890	G183	-8105	526.5
891	G181	-8131	404.5
892	G179	-8157	526.5
893	G177	-8183	404.5
894	G175	-8209	526.5
895	G173	-8235	404.5
896	G171	-8261	526.5
897	G169	-8287	404.5
898	G167	-8313	526.5
899	G165	-8339	404.5
900	G163	-8365	526.5
901	G161	-8391	404.5
902	G159	-8417	526.5
903	G157	-8443	404.5
904	G155	-8469	526.5
905	G153	-8495	404.5
906	G151	-8521	526.5
907	G149	-8547	404.5
908	G147	-8573	526.5
909	G145	-8599	404.5
910	G143	-8625	526.5

No.	Pad name	X	Y
911	G141	-8651	404.5
912	G139	-8677	526.5
913	G137	-8703	404.5
914	G135	-8729	526.5
915	G133	-8755	404.5
916	G131	-8781	526.5
917	G129	-8807	404.5
918	G127	-8833	526.5
919	G125	-8859	404.5
920	G123	-8885	526.5
921	G121	-8911	404.5
922	G119	-8937	526.5
923	G117	-8963	404.5
924	G115	-8989	526.5
925	G113	-9015	404.5
926	G111	-9041	526.5
927	G109	-9067	404.5
928	G107	-9093	526.5
929	G105	-9119	404.5
930	G103	-9145	526.5
931	G101	-9171	404.5
932	G99	-9197	526.5
933	G97	-9223	404.5
934	G95	-9249	526.5
935	G93	-9275	404.5
936	G91	-9301	526.5
937	G89	-9327	404.5
938	G87	-9353	526.5
939	G85	-9379	404.5
940	TESTO4	-9405	526.5
941	G83	-9431	404.5
942	G81	-9457	526.5
943	G79	-9483	404.5
944	G77	-9509	526.5
945	G75	-9535	404.5
946	G73	-9561	526.5
947	G71	-9587	404.5
948	G69	-9613	526.5
949	G67	-9639	404.5
950	G65	-9665	526.5
951	G63	-9691	404.5
952	G61	-9717	526.5
953	G59	-9743	404.5
954	G57	-9769	526.5
955	G55	-9795	404.5
956	G53	-9821	526.5
957	G51	-9847	404.5
958	G49	-9873	526.5
959	NCPAD	-9899	404.5
960	G47	-10199	319
961	G45	-10077	293
962	G43	-10199	267
963	G41	-10077	241
964	G39	-10199	215
965	G37	-10077	189
966	G35	-10199	163
967	G33	-10077	137
968	G31	-10199	111
969	G29	-10077	85
970	G27	-10199	59
971	G25	-10077	33
972	G23	-10199	7
973	G21	-10077	-19
974	G19	-10199	-45
975	G17	-10077	-71

No.	Pad name	X	Y
976	G15	-10199	-97
977	G13	-10077	-123
978	G11	-10199	-149
979	G9	-10077	-175
980	G7	-10199	-201
981	G5	-10077	-227
982	G3	-10199	-253
983	G1	-10077	-279
984	VGLDUM4	-10199	-305

No.	Alignment mark	X	Y
(1-a)	(1-a)	-10188	455
(1-b)	(1-b)	10188	455
(2-a)	(2-a)	-10087	540
(2-b)	(2-b)	10087	540
(3-a)	(3-a)	-10188	-515
(3-b)	(3-b)	10188	-515

## 1.4 BUMP Arrangement



## 2. Interface

### 2.1. System Interface

The HX8309-A supports two system interfaces: an 80-system 18-/16-/9-/8-bit bus interface and a serial data transfer bus interface. The interface mode is selected by the IM3-0 pins setting. The system interface enables instruction setting and RAM access.

The HX8309-A includes an index register (IR) be stored index data of internal control register and RAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting RS=0. Furthermore, There are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. The IR will be indexed to these two control registers through data bus by setting RS=1. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

Operations	E_NWR	RW_NRD	RW	RS
Writes Indexes into IR	0	1	0	0
Reads internal status	1	0	1	0
Writes data into control register or GRAM	0	1	0	1
Reads control register or GRAM data	1	0	1	1

Table 2. 1 Register Selection (18-/16-/9-/8- Bit System Interface)

Start Bytes		
Operations	R/W Bit	RS
Writes Indexes into IR	0	0
Reads internal status	1	0
Writes data into control register or GRAM	0	1
Reads data from control register or GRAM	1	1

Table 2. 2 Register Selection (Serial Data Transfer Interface)

## 2.1.1 80-System

### 80 system 18-bit bus Interface

The 80-system 18-bit parallel data transfer can be used by setting IM3-0 pins to "1010". The Figure2.1 is the example of interface with i80Microcomputer and the Figure2.2 is the data format of 18-bit system interface.

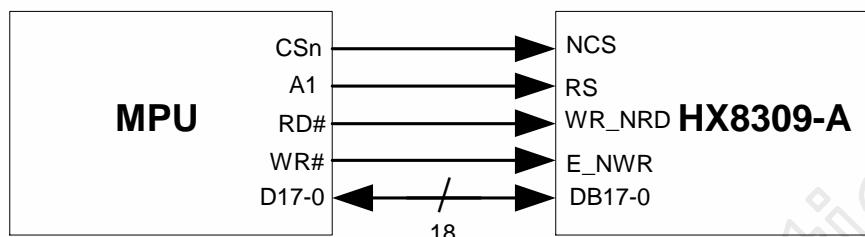
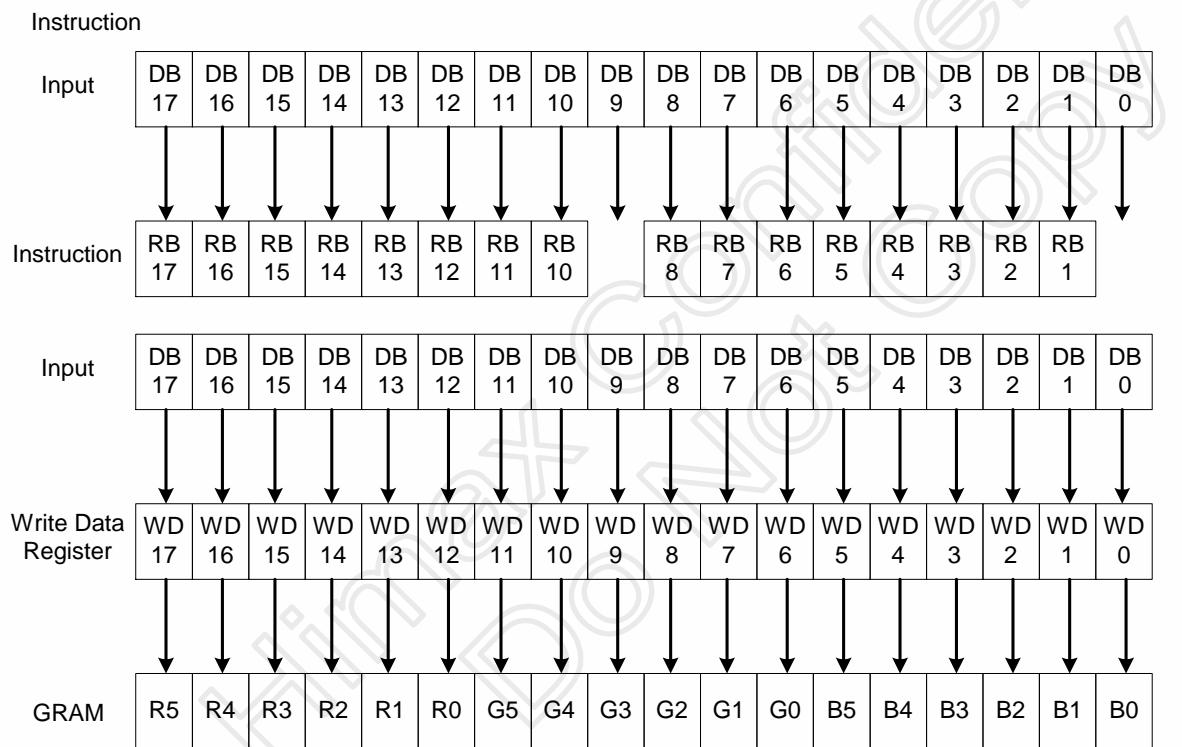


Figure 2. 1 Example of 80 System 18-bit bus Interface

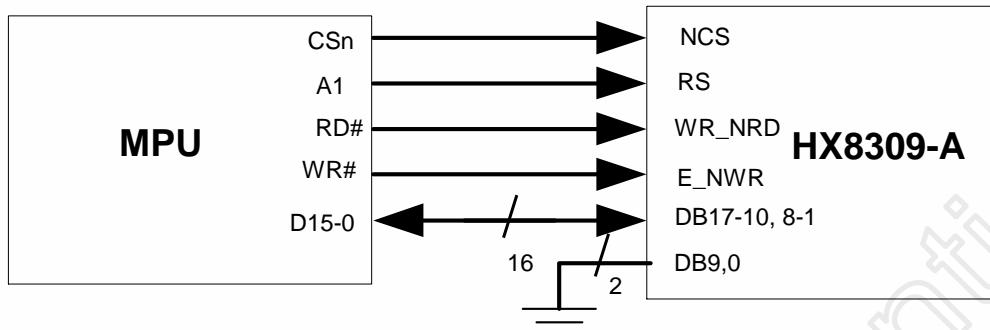


262,144 colors are available

Figure 2. 2 Data Format of 18-bit bus System Interface

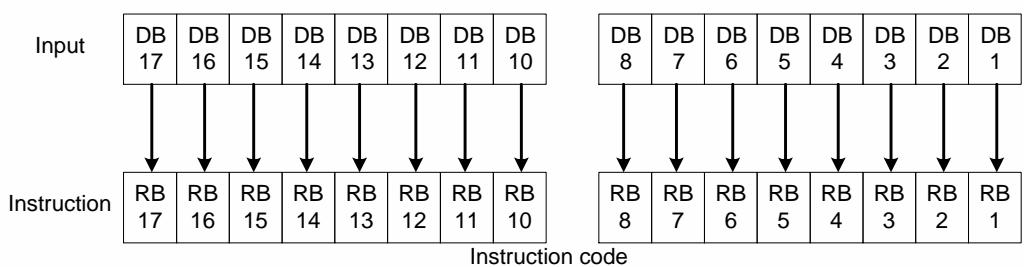
**80 system 16-bit bus Interface**

The 80-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to "0010". The data written to GRAM is expanded to 18-bit bus data automatically in the LSI. Unused pins (DB9, DB0) must be fixed to the IOVcc or VSSD level. The Figure2.3 is the example of interface with 16-bit bus i80Microcomputer and the Figure2.4 is the data format of 16-bit bus system interface.

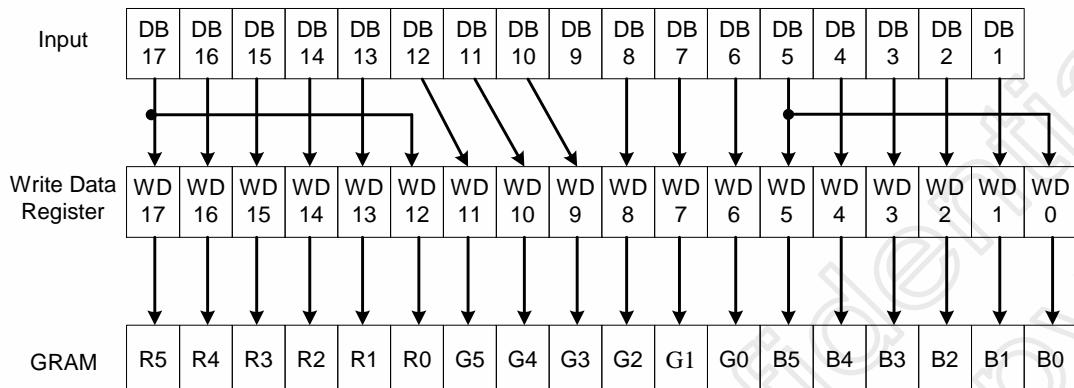


**Figure 2. 3 Example of 80 System 16-bit bus Interface**

## Instruction

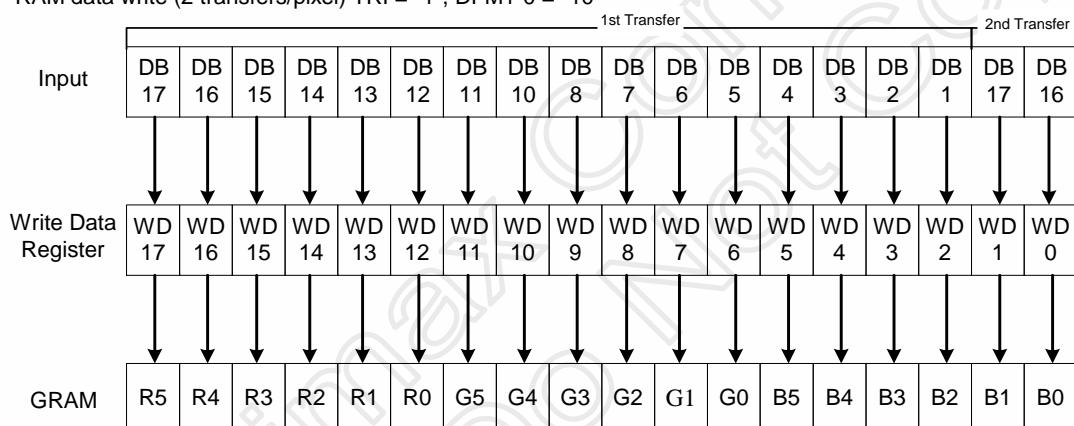


RAM data write (1 transfer/pixel) TRI = "0"



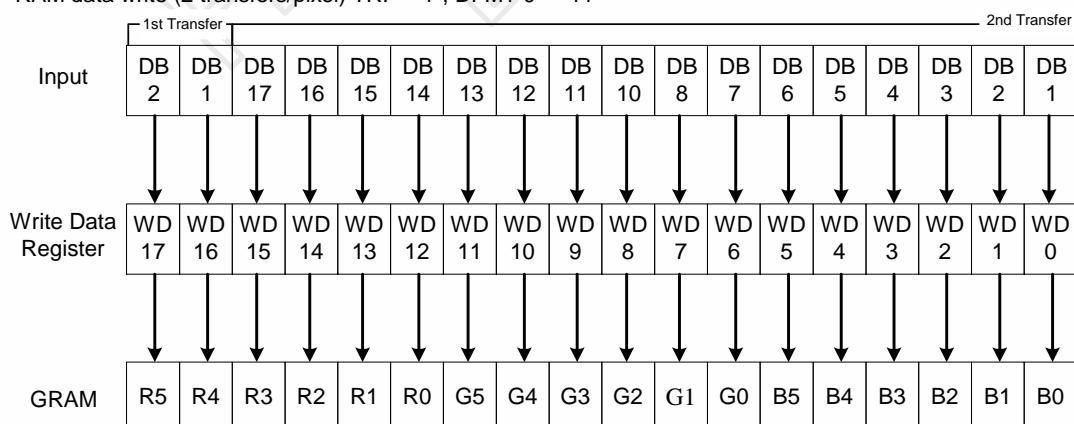
65,536 colors

RAM data write (2 transfers/pixel) TRI = "1", DFM1-0 = "10"



266,144 colors

RAM data write (2 transfers/pixel) TRI = "1", DFM1-0 = "11"



266,144 colors

Figure 2. 4 Data Format of 16-bit bus System Interface

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-P.24-

November 2005

**80-system 9-bit bus Interface**

The 80-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to "1011". In 80-system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper nine bits, and then the upper nine bits are transferred first. Unused pins (DB8-0) must be fixed to the IOVcc or VSSD level. Ensure that upper bytes have to be written when writing the index register.

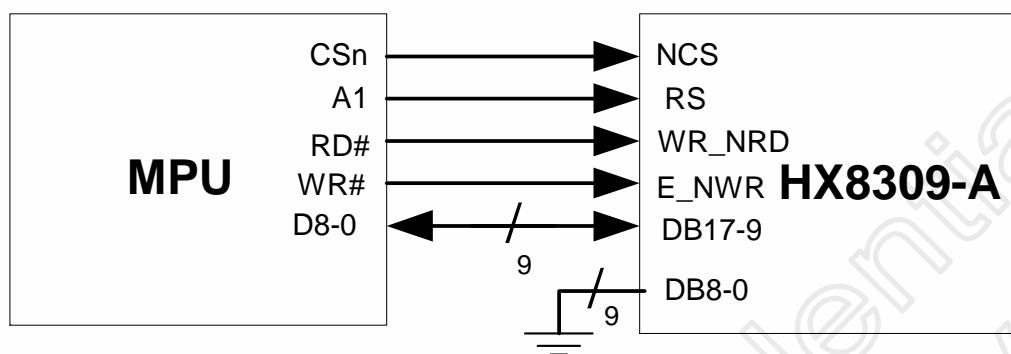
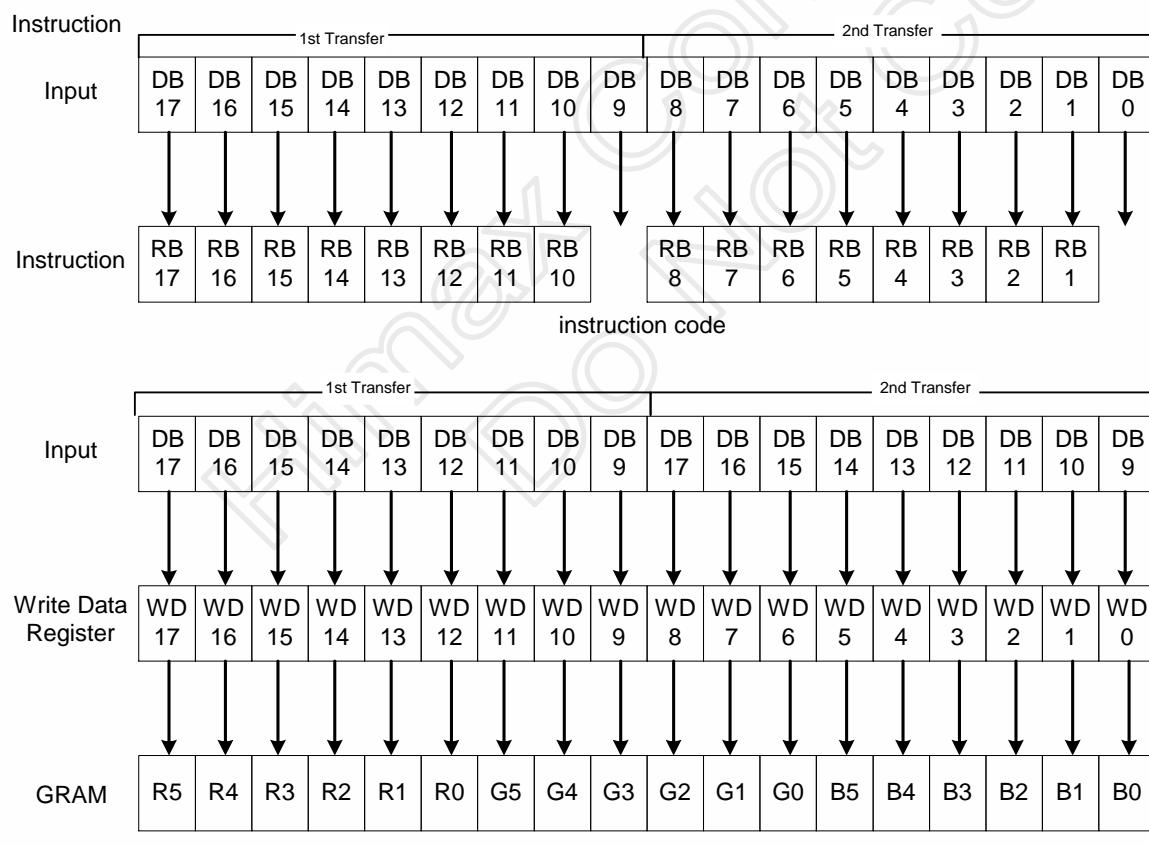


Figure 2.5 Example of 80 System 9-bit bus Interface



262,144 colors are available

Figure 2.6 Data Format of 9-bit bus System Interface

**80 System 8-bit bus Interface**

The 80-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to "0011". In 80-system 8-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper eight bits, and then the upper eight bits are transferred first. Furthermore, the GRAM write data can be expanded into 16-bit bus automatically in internal process. Unused pins (DB9-0) must be fixed to the IOVcc or VSSD level.

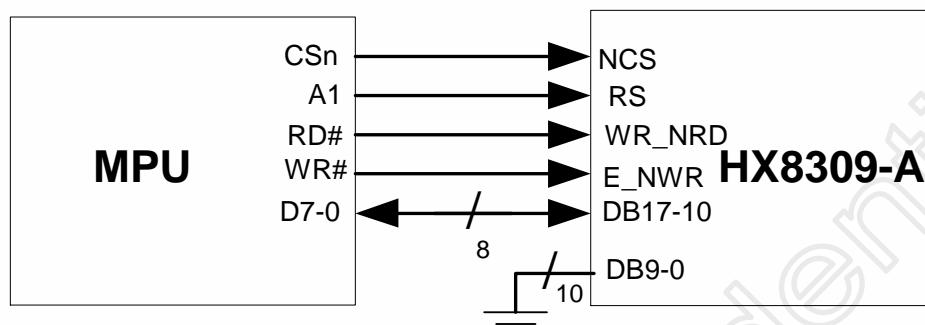
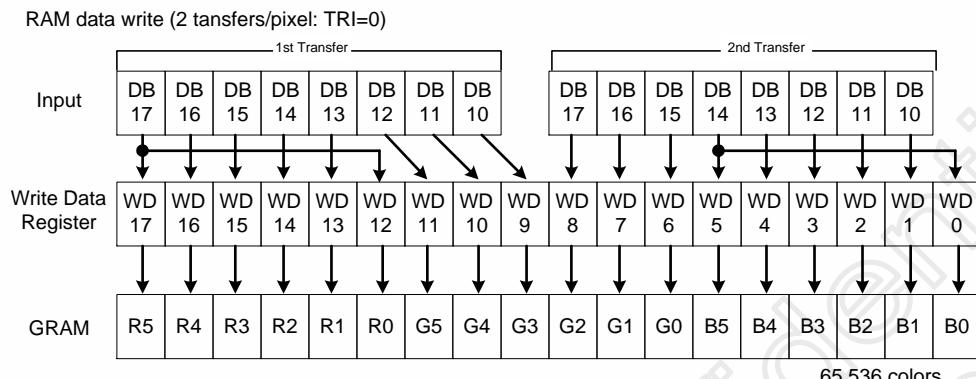
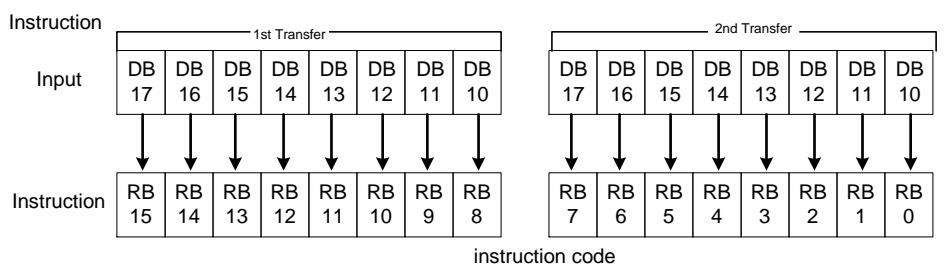
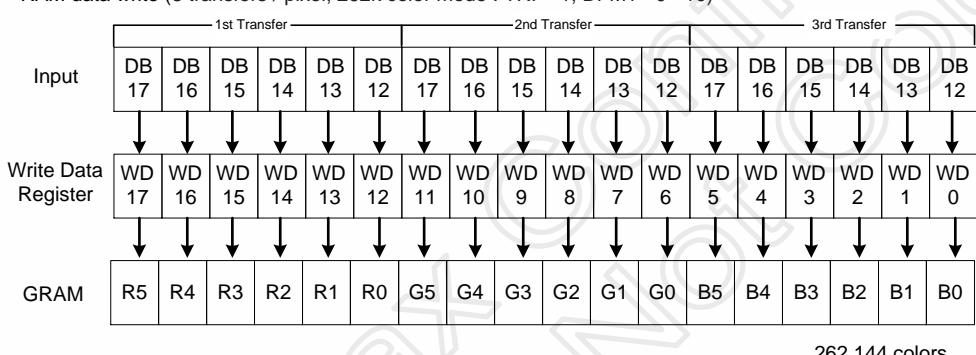


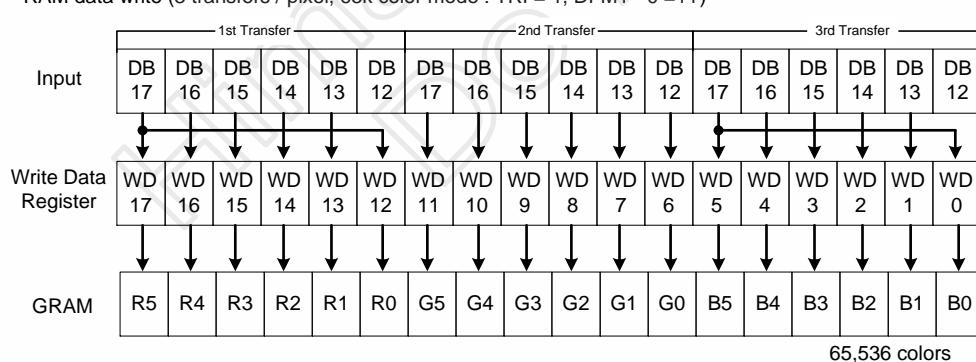
Figure 2. 7 Example of 80 System 8-bit bus Interface

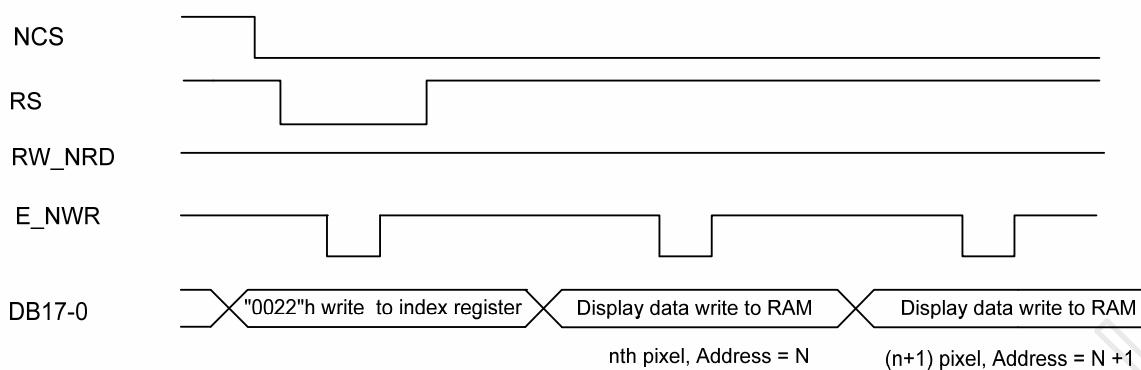
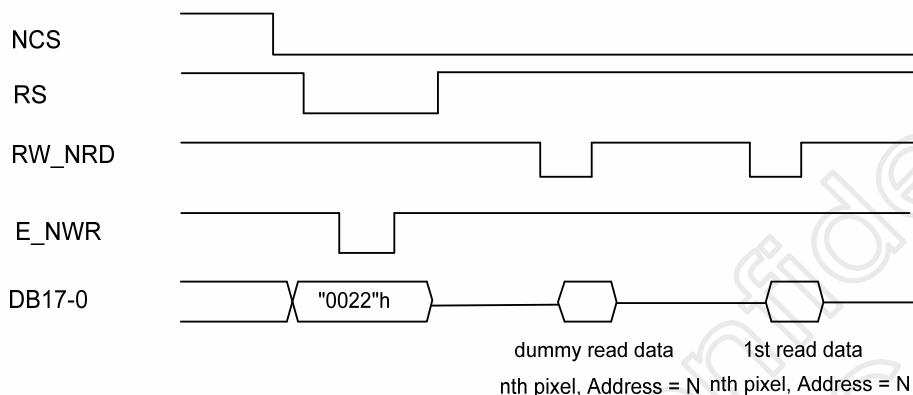
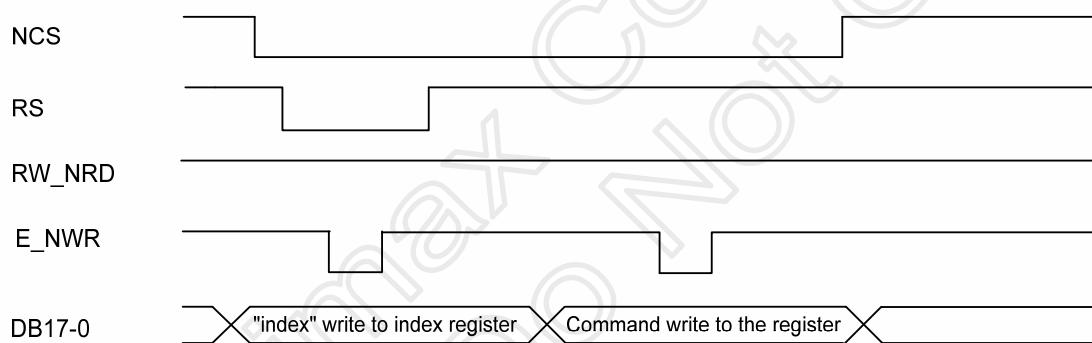
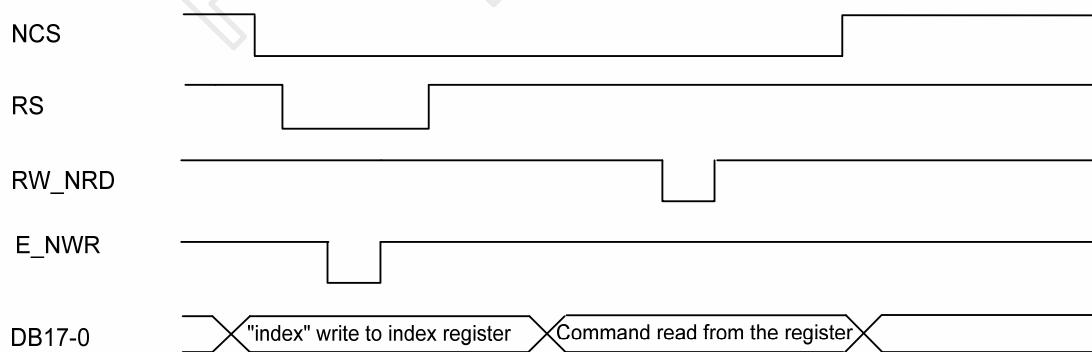


RAM data write (3 transfers / pixel, 262k color mode : TRI = 1, DFM1 - 0 =10)



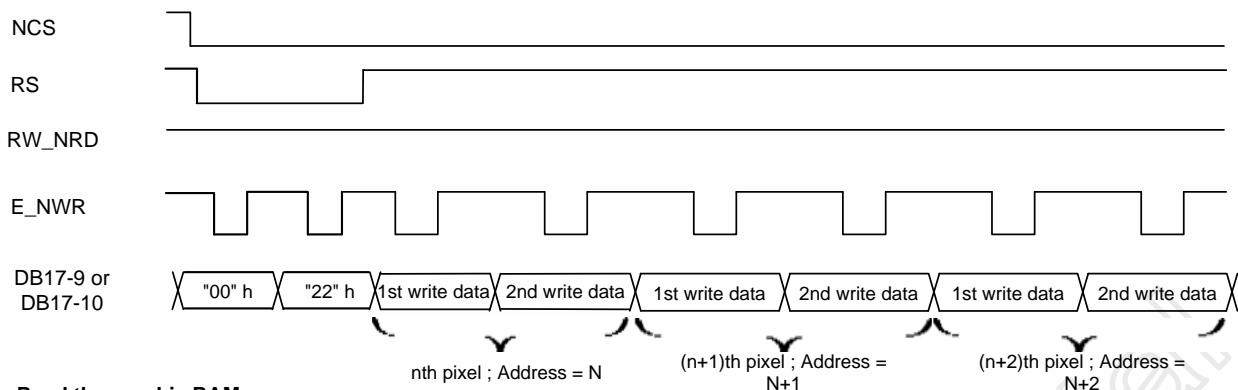
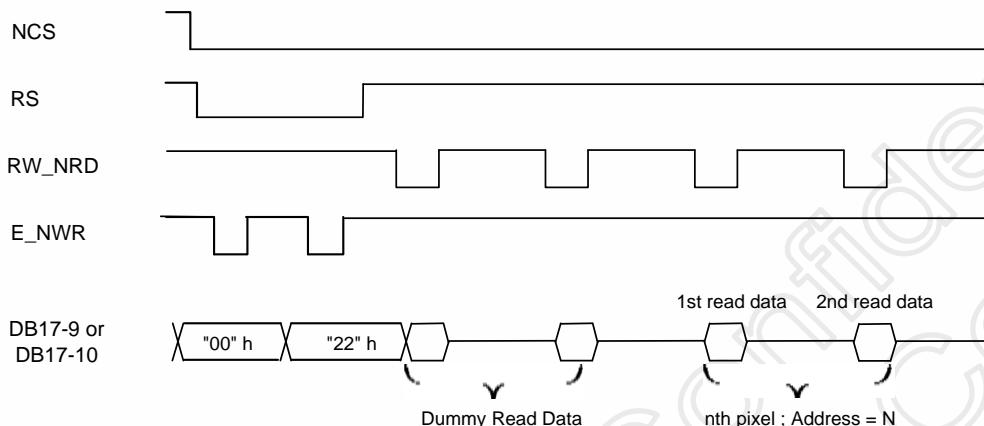
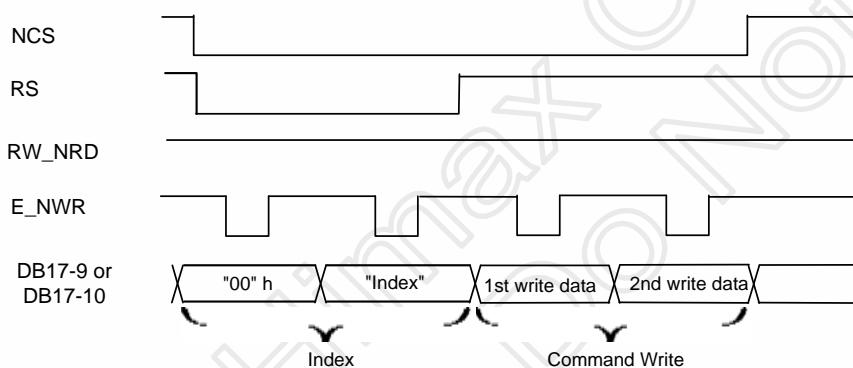
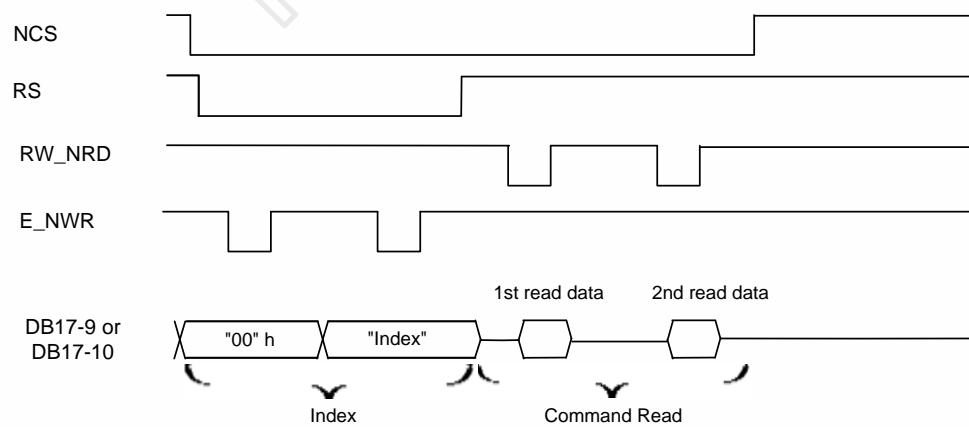
RAM data write (3 transfers / pixel, 65k color mode : TRI = 1, DFM1 - 0 =11)

**Figure 2. 8 Data Format of 8-bit bus System Interface**

**Write to the graphic RAM****Read the graphic RAM****Write to the register****Read the register**

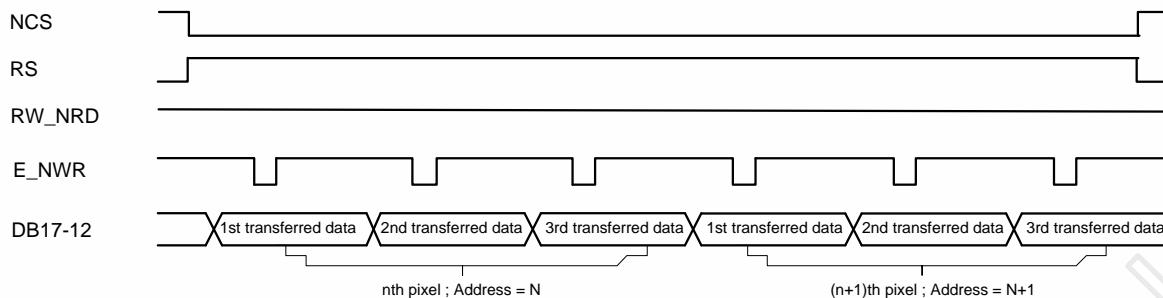
I80 - 18/16 bit interface : D17~D10 = 00h, D8~D1 = Index value

**Figure 2. 9 18 / 16-bit Parallel Bus Interface Timing ( for i80 series MPU )**

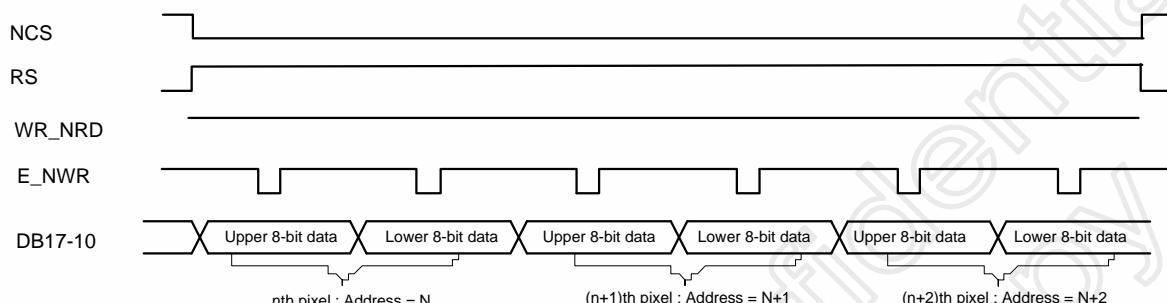
**Write to the graphic RAM****Read the graphic RAM****Write to the register****Read the register****Figure 2. 10 9 / 8-bit Parallel Bus Interface Timing ( for i80 series MPU )**

**Write to the display data RAM**

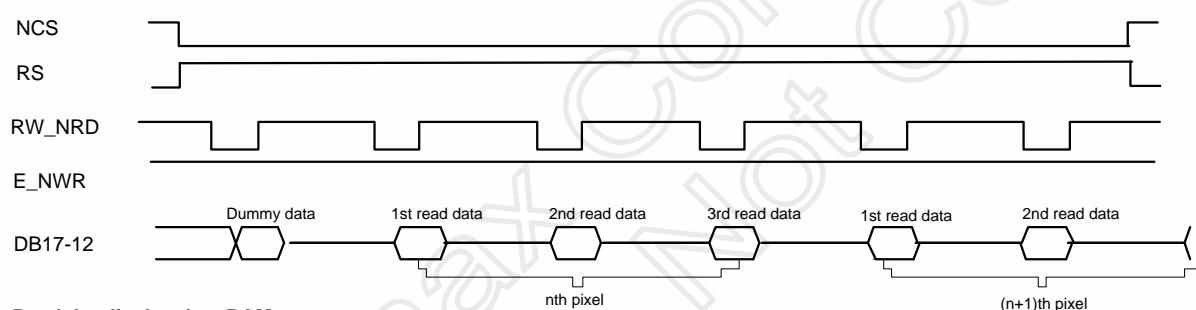
18/16-bit display data (6-bit x 3 transfers transfers)

**Write to the display data RAM**

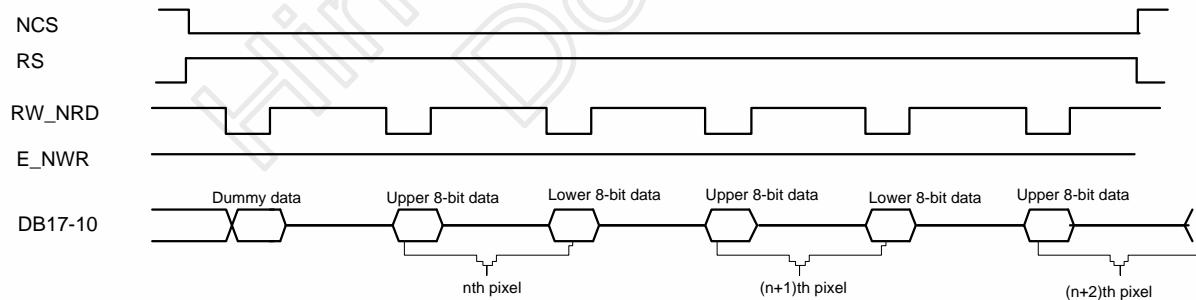
16-bit display data (8-bit x 2 transfers, TRI=0)

**Read the display data RAM**

18/16-bit display data (6-bit x 3 transfers, TRI=1)

**Read the display data RAM**

16-bit display data (8-bit x 2 transfers, TRI=0)

**Figure 2. 11 8-bit Parallel Bus Interface Timing ( for i80 series MPU )**

## 2.1.2 Serial Data Transfer Interface

The HX8309-A supports the serial data transfer interface by setting IM3-1 pins to "010". The serial data transfer interface mode is enabled through the chip select line (NCS), and accessed via a three-wire control consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock line (SCL). When HX8309-A is set up for serial data transfer interface mode, the IMO (ID) pin is used as an ID pin.

In serial data transfer interface mode, the HX8309-A can transfer initially with the start byte at the falling edge of NCS input and finish the transfer at the rising edge of a NCS input.

When the chip select line (NCS) of HX8309-A is set active low, the start byte will be transferred first. The start byte is made up of 6-bit bus device identification code, register select (RS) bit and read /write operation (R/W) bit. The five upper bits of 6-bit bus device identification code must be set 01110 and the least significant bit bus of the identification code can be determined by the IMO/ID pin. Furthermore, two different internal addresses of HX8309-A can be assigned to the register select bit (RS) that is the seventh bit bus of the start byte. The cases of write data to the index register or read the status must be setting RS = 0, and then the cases of write or read an instruction or GRAM data must be setting RS = 1. The read or write function is selected according to the eighth bit bus of the start byte (R/W bit). The data is received when R/W = 0, and is transmitted when R/W = 1. Table2.3 is list different conditions when change the RS and R/W bit.

When the serial data transfer interface is enabled, the HX8309-A starts taking in start byte and subsequent data that is transferred with the MSB first. Further, the registers of 16-bit bus format can be divided to the upper eight bits as the first byte and lower eight bits as second byte when HX8309-A are executed from the MSB after transferring two bytes. The HX8309-A executes the write data operation to the GRAM after two-byte and then automatically expanded to the 18-bit bus format (Figure2.9). When the read status/register operation is executed, the prior byte after start byte is invalid, and then the HX8309-A starts to read correct status/register data from second byte. As well as, when the read GRAM data operation, the prior five bytes of GRAM read data after the start byte are invalid. The HX8309-A starts to read correct GRAM data from the sixth byte.

RS	R/W	Function
0	0	Index register set
0	1	Status read
1	0	Register or GRAM data write
1	1	Register or GRAM data read

Table 2. 3 The Function of RS and R/W Bit bus

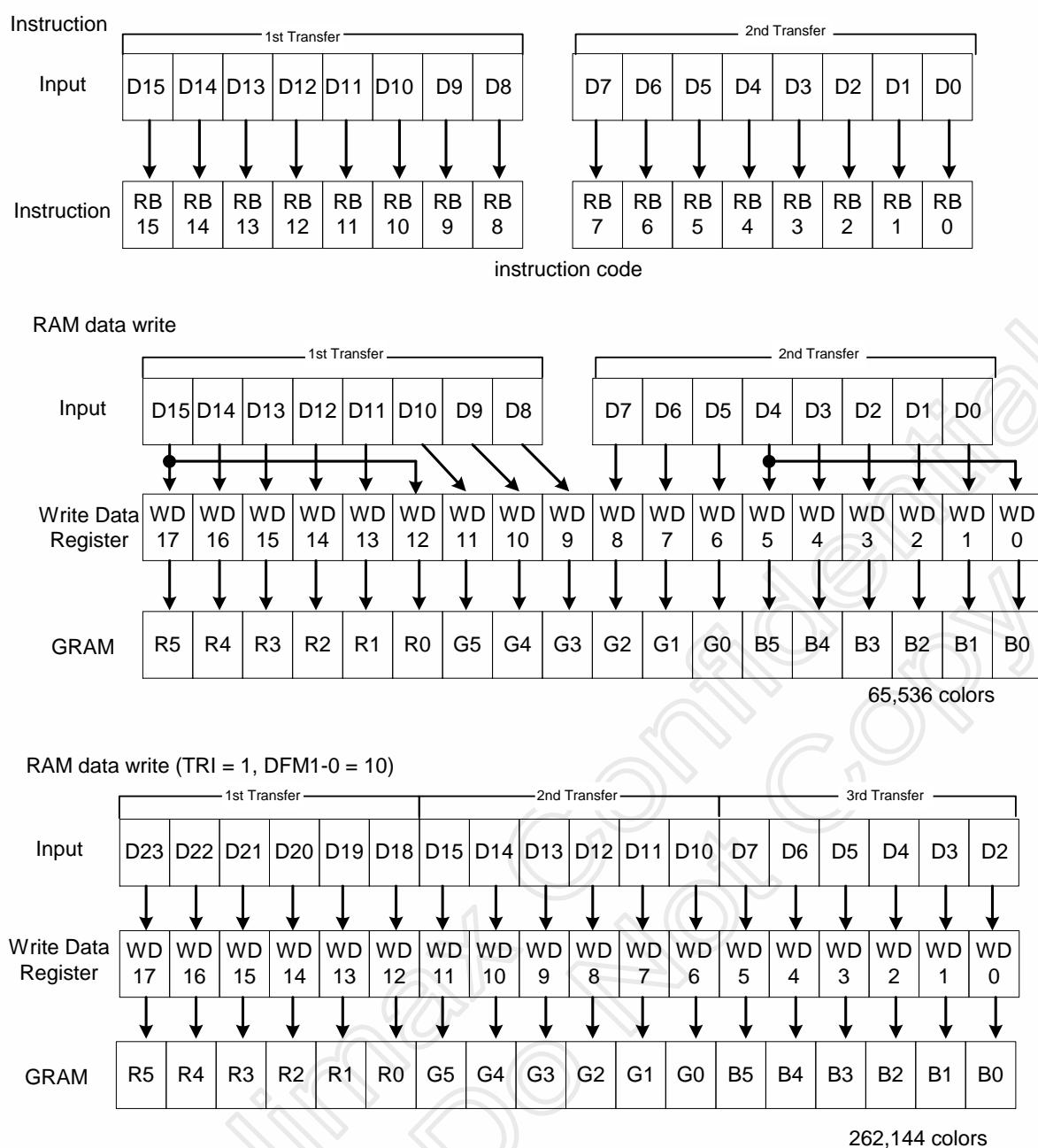
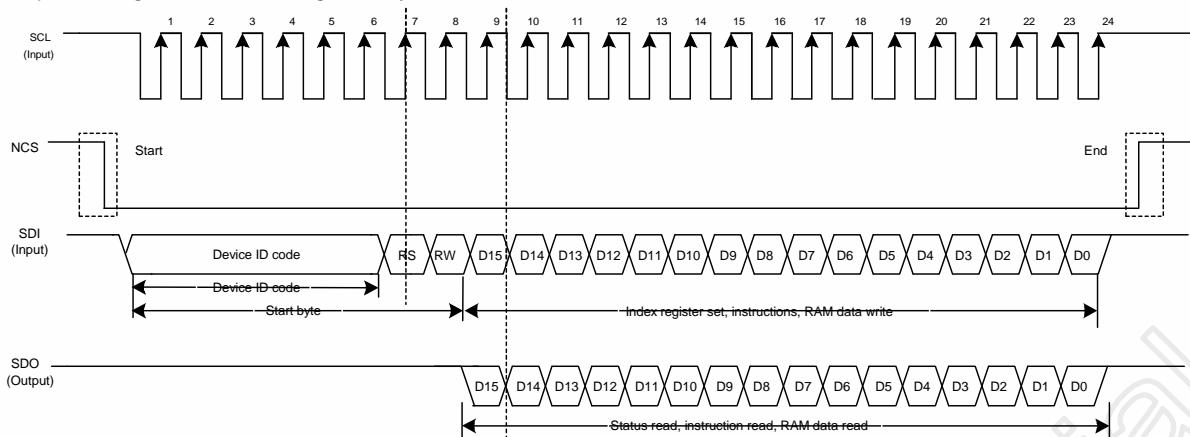
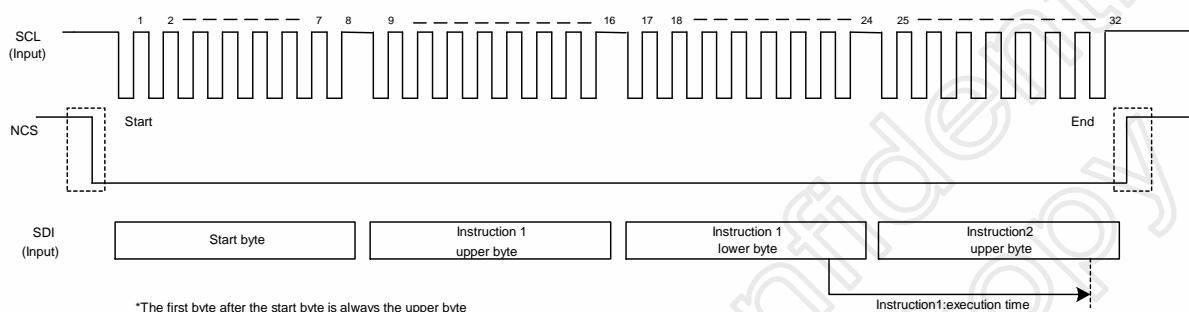
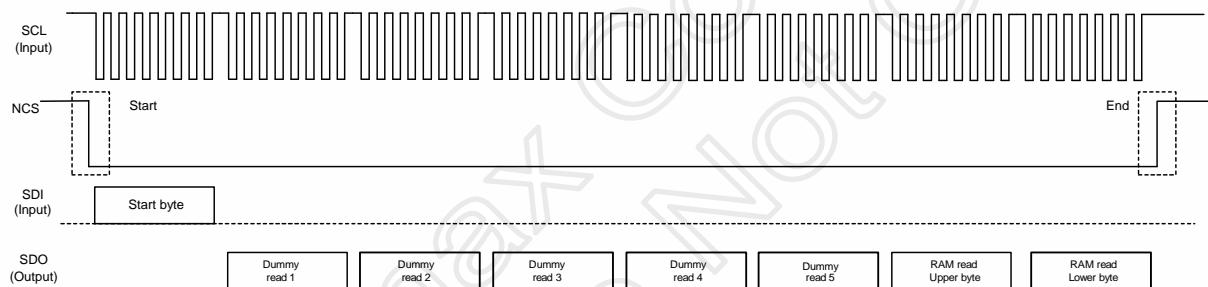
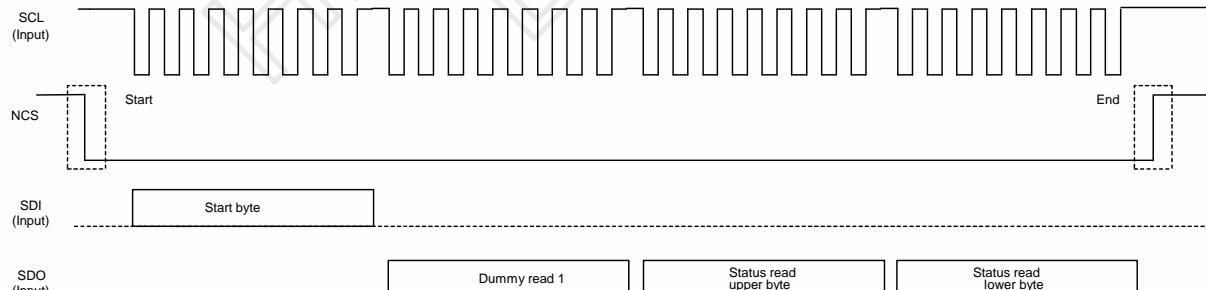


Figure 2. 12 Data Format of Serial Data Transfer Interface GRAM

**A) Basic Timing Transfer Format through Clock-Synchronized Serial Data Transfer Interface****B) Timing of Consecutive Data-write through Clock-synchronized Serial Data Transfer Interface****C) Timing Format of GRAM-Data Read**

Note: A RAM data read operation follows 5-byte dummy read operations.

**D) Timing Format of Status Read/ Instruction Read**

Note: One byte of the read data after the start byte are invalid. The HX8309-A starts to read the correct status or instruction data from the second byte

**Figure 2. 13 Data Transfer through Serial Data Transfer Interface**

## 2.2 Vsync Interface

The HX8309-A supports the VSYNC interface mode that executes the display operation by the internal clocks. The internal clocks is generated from internal oscillators and synchronized with the frame synchronization signal VSYNC. When the VSYNC interface mode is selected, the interface display a moving picture through system interface with minimum modification that re-writes display data to the internal GRAM in a high speed RAM function. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

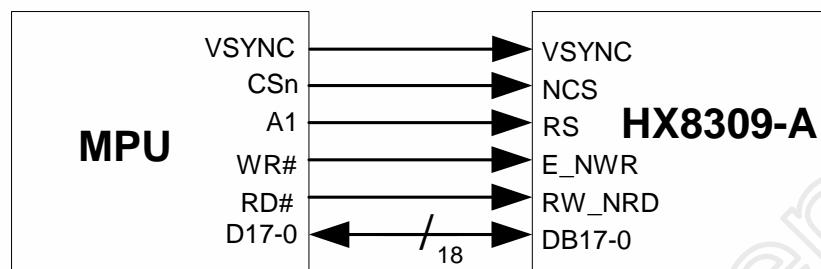


Figure 2. 14 VSYNC Interface to MPU

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 2. 4 DIM Bit Set

When the HX8309-A is set up in VSYNC interface mode, the interface is used high speed write function (HWM=1) to display a moving picture when writing data to GRAM in high speed with low power consumption. Therefore, the VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It requires GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP, BP and display lines duration (NL):

$$\text{Internal oscillator clock } (f_{osc}) [\text{Hz}] = \text{Frame Frequency} \times [\text{Display Lines}(NL) + FP + BP] \times RTN \\ \times \text{frequency fluctuation}$$

The parameter of frequency fluctuation is ascribed to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

The minimum speed for RAM can be computed by the following formula:

$$\text{The Min. RAM Write Speed [Hz]} \geq \frac{176 \times \text{DisplayLines}(NL) \times f_{osc}}{[\text{Back Proch}(BP) + \text{DisplayLines}(NL) - \text{margin lines}] \times RTN}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the HX8309-A start the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting a internal oscillator clock (fosc) first.

An example of internal oscillator clock (fosc) and minimum speed for RAM writing set up in VSYNC interface mode is as follows.

#### Example

Display size: 176RGB\*200 lines

Lines of be used: 200 lines (11000)

FP: 2 lines (0010)

BP: 14 lines (1110)

Frequency fluctuation: 5%

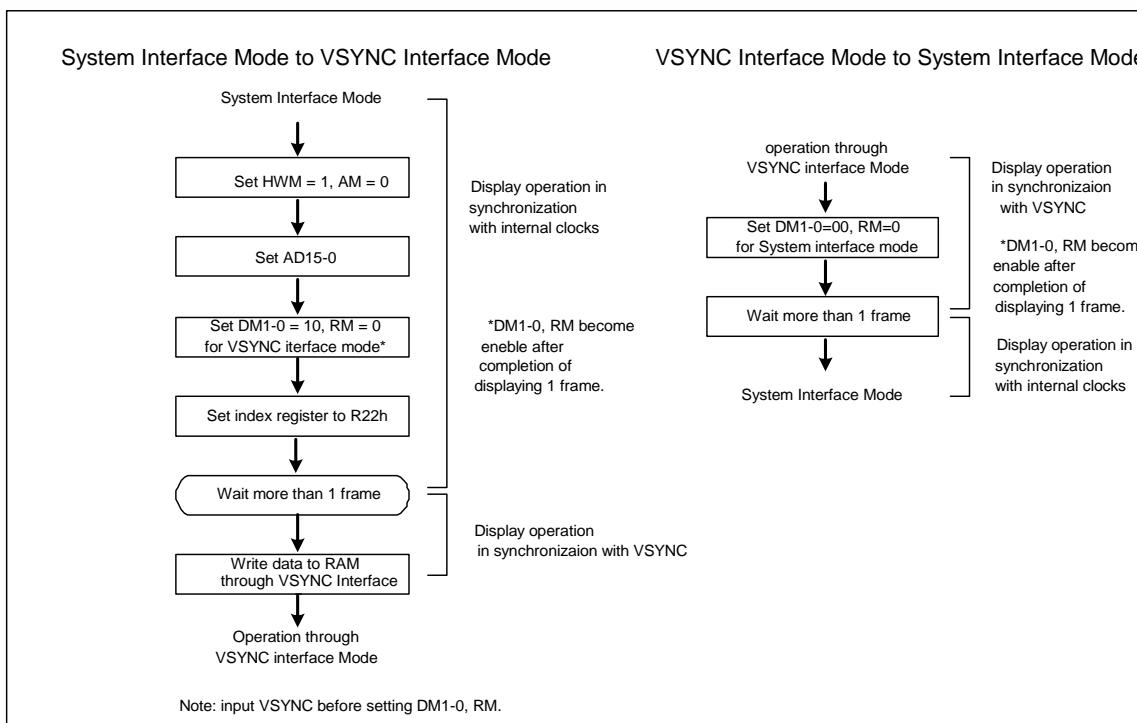
Frame frequency: 60Hz

**Internal oscillator clock (fosc) [Hz] =  $60 \times [200 + 2 + 14] \times 16 \times (1.05/0.95) \approx 229 \text{ kHz}$**

**The Min. RAM Write Speed [Hz]  $\geq 176 \times 200 \times 229 / ([14 + 200 - 2] \times 16) \approx 2.37\text{MHz}$**

In this example, the minimum RAM write speed of VSYNC interface is 2.37MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the HX8309-A initiate the display operation and make it possible to re-write the display area set previously. Further, if the display area were different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.

When the HX8309-A make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 2.15 illustrates the process of VSNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.



**Figure 2. 15 VSYNC Interface with Internal Clock and System Interface with Internal Clock Mode Transition**

When HX8309-A is set up on VSYNC interface mode, use the high-speed RAM write mode (HWM=1) to access RAM in high speed with low power consumption when display a moving picture. But the partial display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

## 2.3 RGB Interface

The HX8309-A supports the RGB interface that display operations that executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE) be described on Table 2.5. The RGB interface can be used by setting DM1-0=01 and RM=1. In RGB interface mode, with use of high-speed RAM write mode (HWM=1) and a window address function, enables to display data in a moving picture area and makes it possible to transfer the display only by re-writing a screen with minimum data transfers.

EPL	ENABLE	RAM Write	RAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

Table 2. 5 EPL and ENABLE Set

When the HX8309-A set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continues until the next input of the VSYNC signal.

The HX8309-A supports two types of RGB interface mode; the difference between them is the RAM access using the RGB interface (PD17-0) or system interface (DB17-0). The data written to the internal GRAM were synchronized with DOTCLK inputs when ENABLE is setting low. Contrary to set ENABLE high, the data written to the GRAM would be entered to the process of using the system interface. Further, when select to use system interface, set ENABLE high to stop using the RGB interface for writing data, and then set the RAM access setting bit bus (RM) low to invert RAM access operation by using system interface. After that, set address AD15-0 on falling edge of VSYNC and then set the index field of register (R22h) to access RAM via the system interface. The HX8309-A allows rewriting data in the still picture area by using the system interface when displaying a moving picture in RGB interface mode. When return to use RGB interface to access RAM, set address AD 15-0, RAM access setting bit bus (RM=1) and the index field of register (R22h) before accessing RAM via RGB interface.

The Figure2.16 is shown the process of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

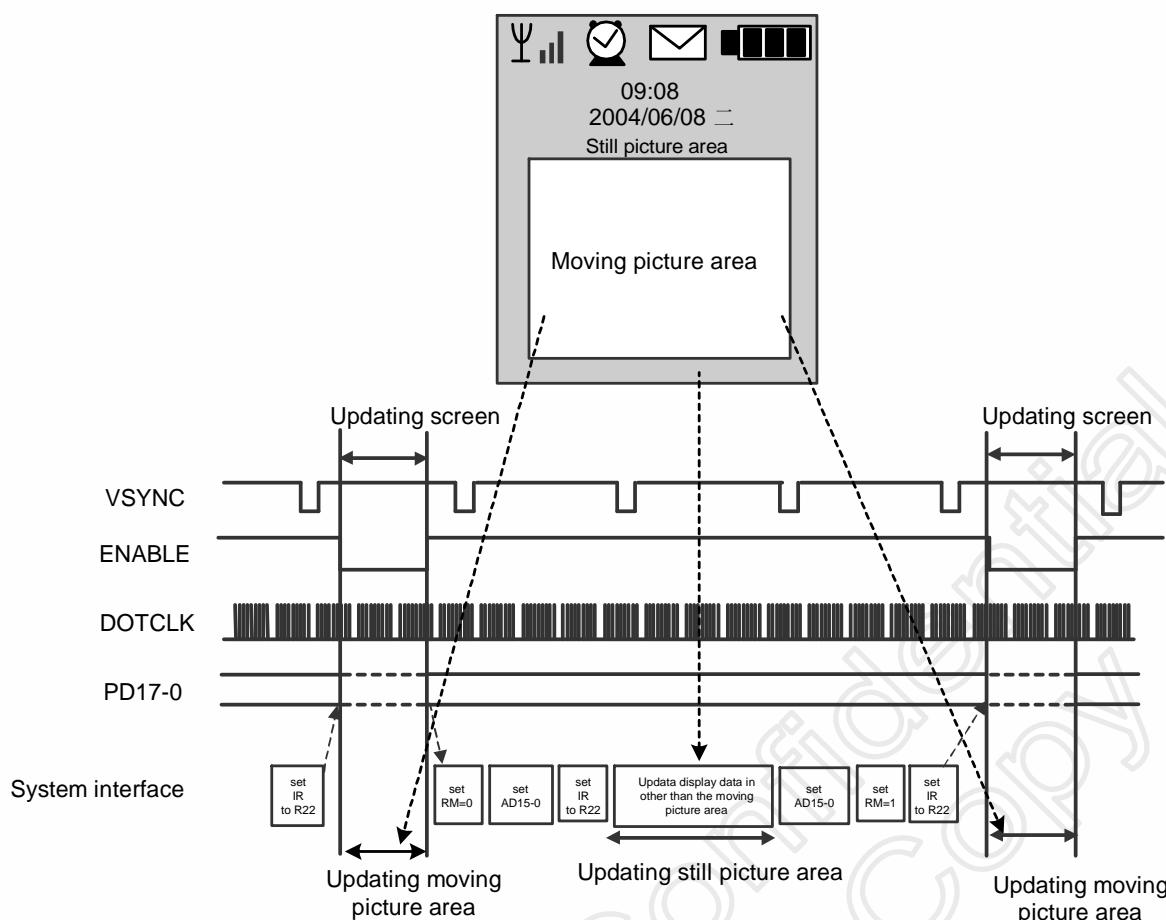


Figure 2. 16 Example of Update Still and Moving Picture

When set up in RGB interface mode, the used of high speed RAM write mode to write data to the internal GRAM and GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal. Such as VSYNC interface mode, partial screen display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

When the HX8309-A make the transition with system interface mode and RGB interface mode, the sequence of switching process must be following as Figure2.17.

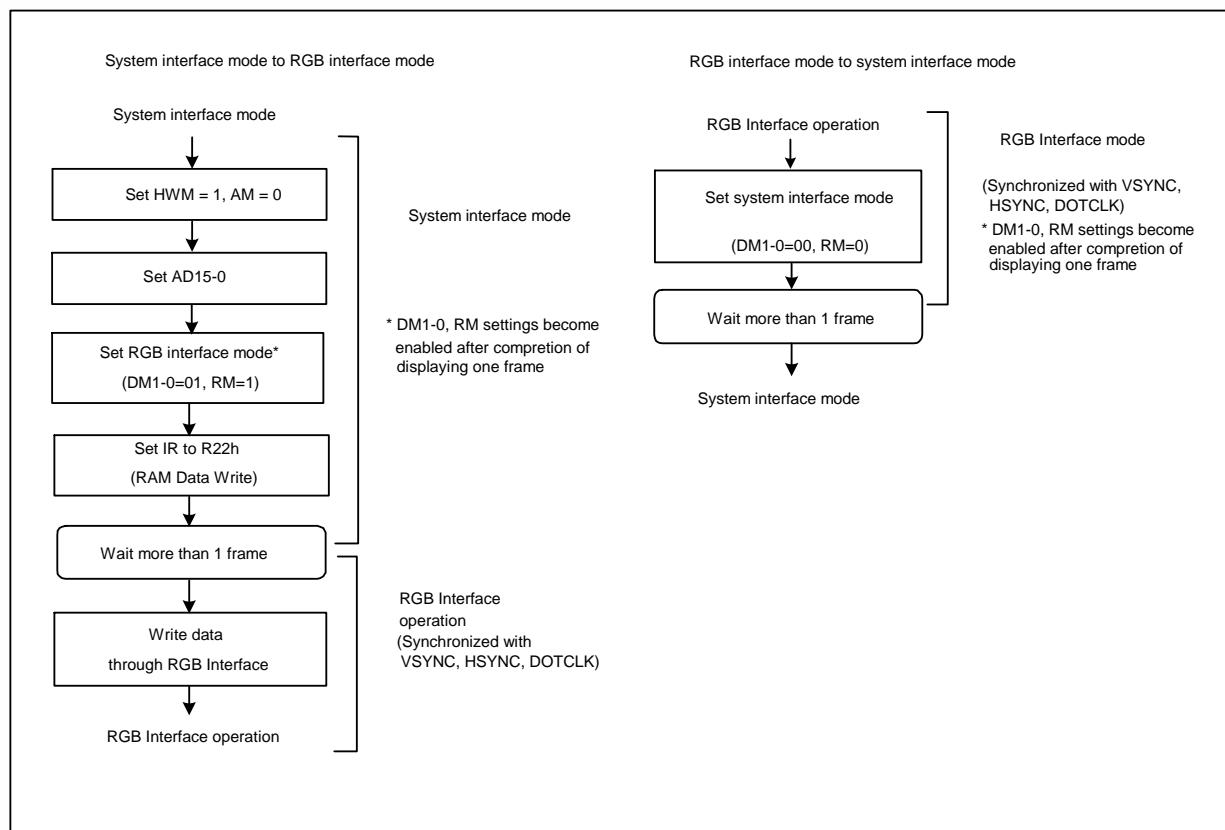
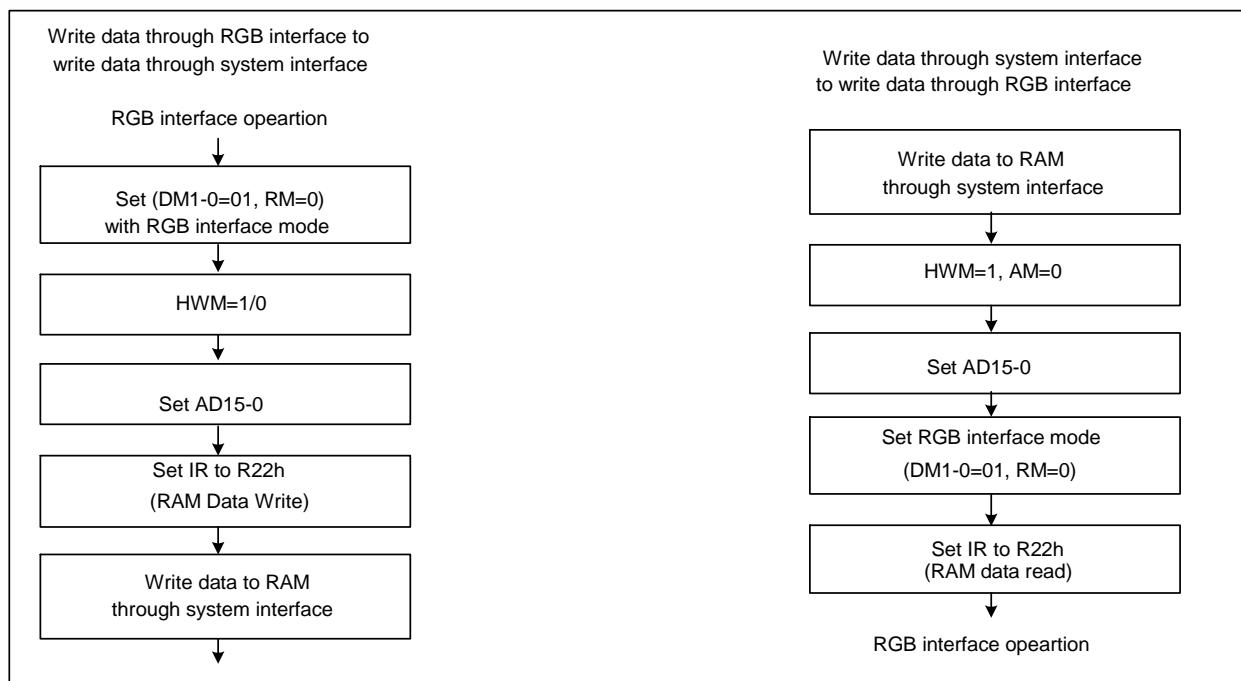


Figure 2.17 Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure2.18.

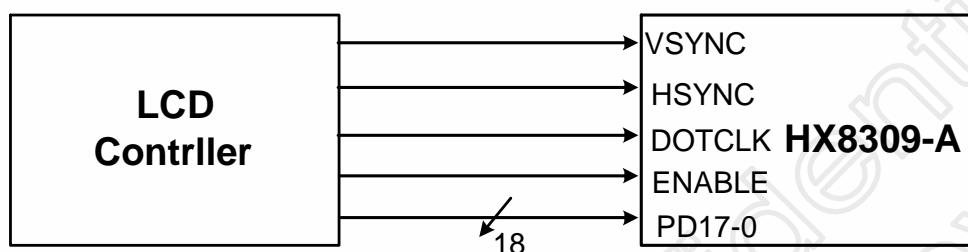


**Figure 2. 18 RAM Data Write Sequence through System Interface or RGB Interface during RGB Interface Mode**

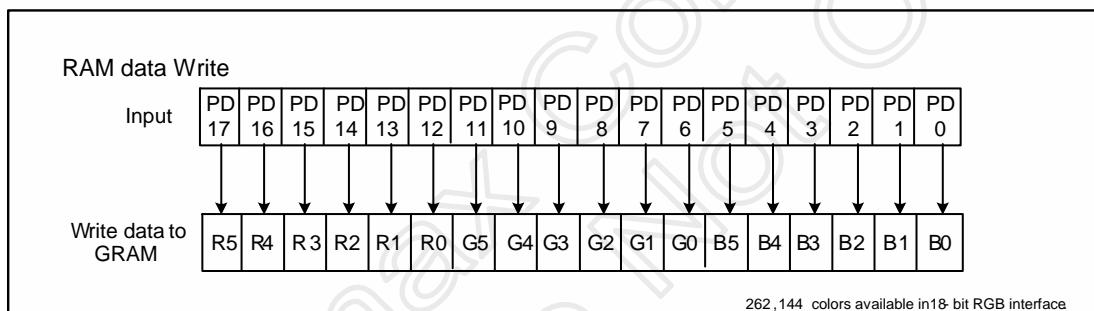
The HX8309-A supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

### 18-bit bus RGB interface

The 18-bit interface can be used by setting RIM1-0 bits to "00". The Figure 2.19 is the example of 18-bit RGB interface with LCD Controller and HX8309-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE). The Figure 2.20 is the data format of 18-bit RGB interface.



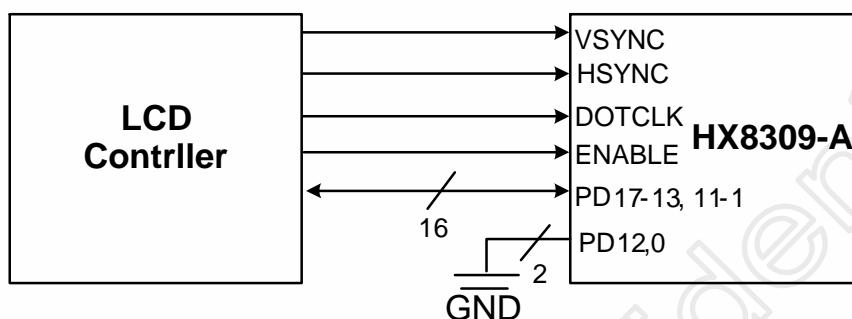
**Figure 2. 19 18-bit RGB Interface**



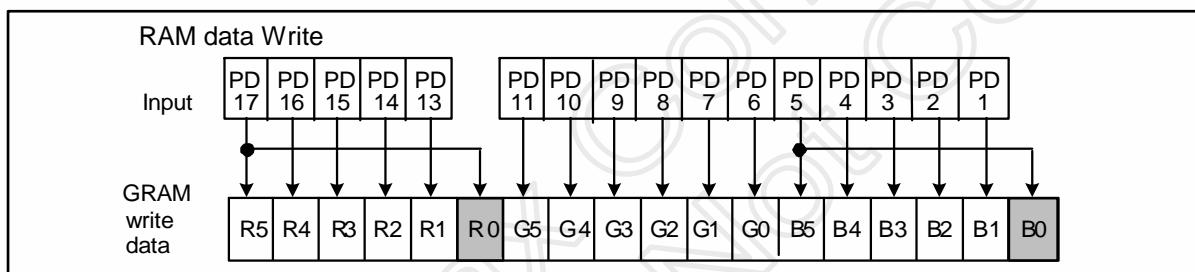
**Figure 2. 20 Data Format for 18-bit Interface**

## 16-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “01”. The Figure 2.21 is the example of 16-bit bus RGB interface with LCD Controller and HX8309-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-13, PD11-1 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (PD12, PD0) must be fixed to the IOVcc or VSSD level. The Figure2.22 is the data format of 16-bit RGB interface.



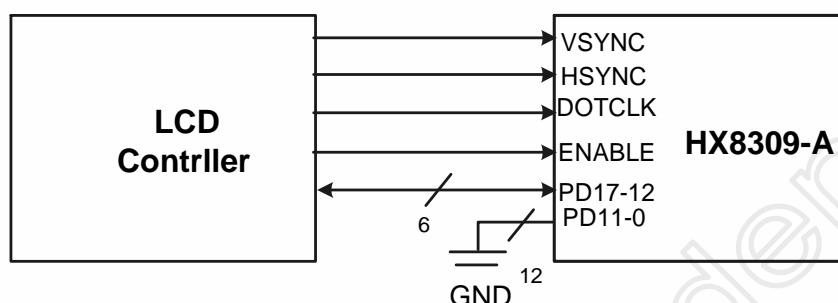
**Figure 2. 21 16-bit RGB Interface**



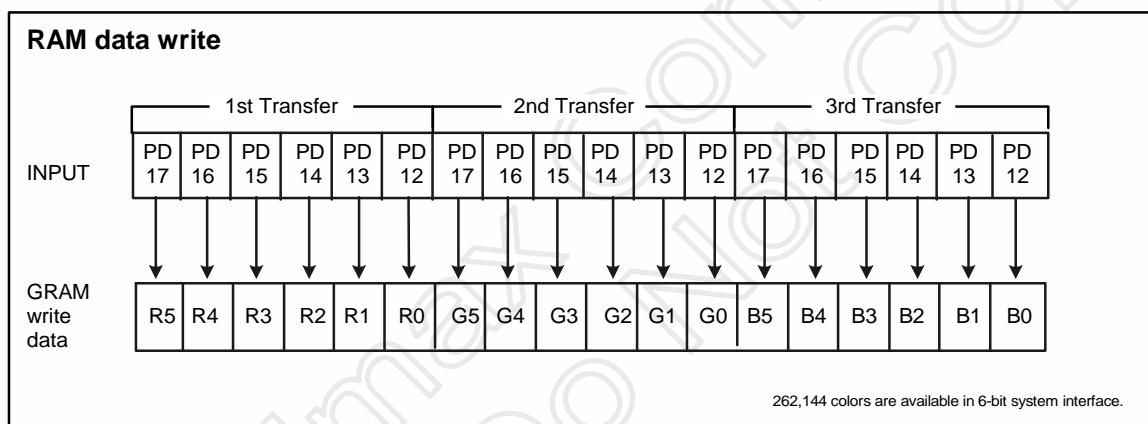
**Figure 2. 22 Data Format for16-bit Interface**

### 6-bit bus RGB interface

The 6-bit bus interface can be used by setting RIM1-0 bits to "10". The Figure2.23 is the example of 6-bit bus RGB interface with LCD Controller and HX8309-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-12 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (PD11-0) must be fixed to the IOVcc or VSSD level. The Figure2.24 is the data format of 6-bit bus RGB interface.



**Figure 2. 23 6-bit RGB Interface**



**Figure 2. 24 Data Format for 6-bit Interface**

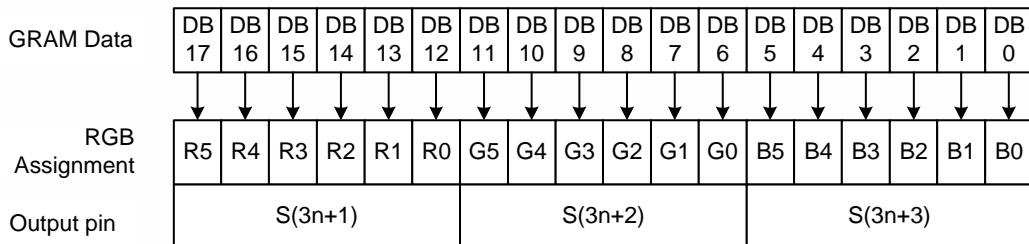
### 3. Function Description

#### 3.1 Graphics RAM

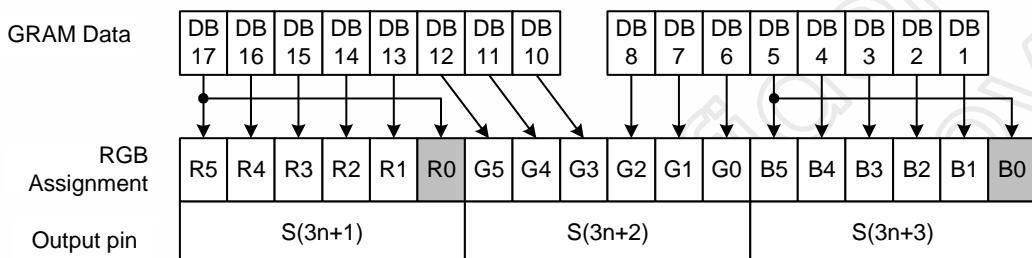
The HX8309-A have an internal graphics RAM that stores 87,120 bytes bit-pattern data, where one pixel is expressed by 18 bits. The GRAM address map is listed as follow:

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	-----	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=1	GS=0	DB--DB 17 --0		DB--DB 17 --0		DB--DB 17 --0		-----		-----	DB--DB 17 --0	DB--DB 17 --0											
G220	G1	0000H	0001H	0002H	-----	-----	-----	00AACH	00ADH	00AEH	00AFH												
G219	G2	0100H	0101H	0102H	-----	-----	-----	01AACH	01ADH	01AEH	01AFH												
G218	G3	0200H	0201H	0202H	-----	-----	-----	02AACH	02ADH	02AEH	02AFH												
G217	G4	0300H	0301H	0302H	-----	-----	-----	03AACH	03ADH	03AEH	03AFH												
G216	G5	0400H	0401H	0402H	-----	-----	-----	04AACH	04ADH	04AEH	04AFH												
G215	G6	0500H	0501H	0502H	-----	-----	-----	05AACH	05ADH	05AEH	05AFH												
G214	G7	0600H	0601H	0602H	-----	-----	-----	06AACH	06ADH	06AEH	06AFH												
G213	G8	0700H	0701H	0702H	-----	-----	-----	07AACH	07ADH	07AEH	07AFH												
G212	G9	0800H	0801H	0802H	-----	-----	-----	08AACH	08ADH	08AEH	08AFH												
G211	G10	0900H	0901H	0902H	-----	-----	-----	09AACH	09ADH	09AEH	09AFH												
G210	G11	0A00H	0A01H	0A02H	-----	-----	-----	0AAACH	0AADH	0AAEH	0AAFH												
G209	G12	0B00H	0B01H	0B02H	-----	-----	-----	0BACH	0BADH	0BAEH	0BAFH												
G208	G13	0C00H	0C01H	0C02H	-----	-----	-----	0CACH	0CADH	0CAEH	0CAFH												
G207	G14	0D00H	0D01H	0D02H	-----	-----	-----	0DACH	0DADH	0DAEH	0DAFH												
G206	G15	0E00H	0E01H	0E02H	-----	-----	-----	0EACH	0EADH	0EAEH	0EAFH												
G10	G211	D200H	D201H	D202H	-----	-----	-----	D2AACH	D2ADH	D2AEH	D2AFH												
G9	G212	D300H	D301H	D302H	-----	-----	-----	D3AACH	D3ADH	D3AEH	D3AFH												
G8	G213	D400H	D401H	D402H	-----	-----	-----	D4AACH	D4ADH	D4AEH	D4AFH												
G7	G214	D500H	D501H	D502H	-----	-----	-----	D5AACH	D5ADH	D5AEH	D5AFH												
G6	G215	D600H	D601H	D602H	-----	-----	-----	D6AACH	D6ADH	D6AEH	D6AFH												
G5	G216	D700H	D701H	D702H	-----	-----	-----	D7AACH	D7ADH	D7AEH	D7AFH												
G4	G217	D800H	D801H	D802H	-----	-----	-----	D8AACH	D8ADH	D8AEH	D8AFH												
G3	G218	D900H	D901H	D902H	-----	-----	-----	D9AACH	D9ADH	D9AEH	D9AFH												
G2	G219	DA00H	DA01H	DA02H	-----	-----	-----	DAACH	DAADH	DAAEH	DAAFH												
G1	G220	DB00H	DB01H	DB02H	-----	-----	-----	DBACH	DBADH	DBAEH	DBAFH												

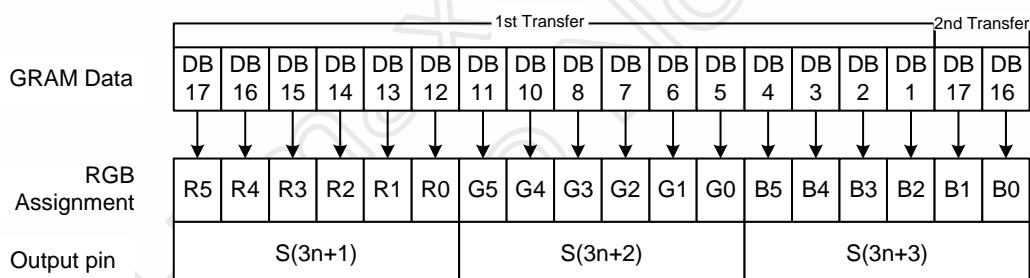
Table 3. 1 GRAM Address and Display Panel Position (SS = "0", BGR = "0")

**80-System 18-bit bus Interface**

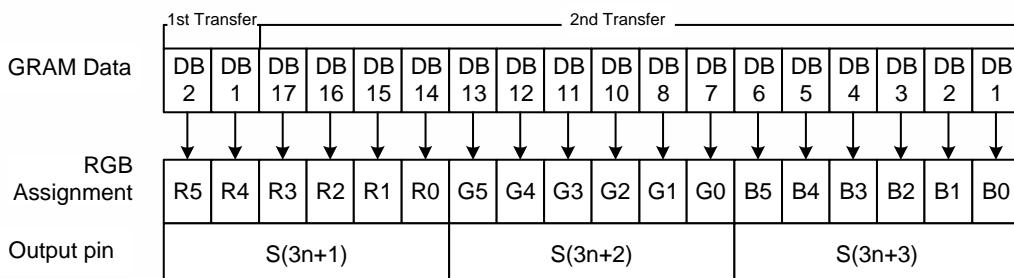
Note: n = lower eight bits of address (0 to 175)

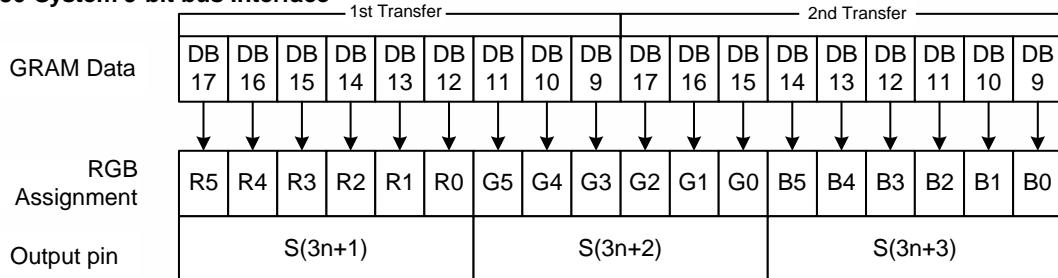
**Figure 3. 1 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "0", BGR = "0")****80-System 16-bit bus Interface**

Note: n = lower eight bits of address (0 to 175)

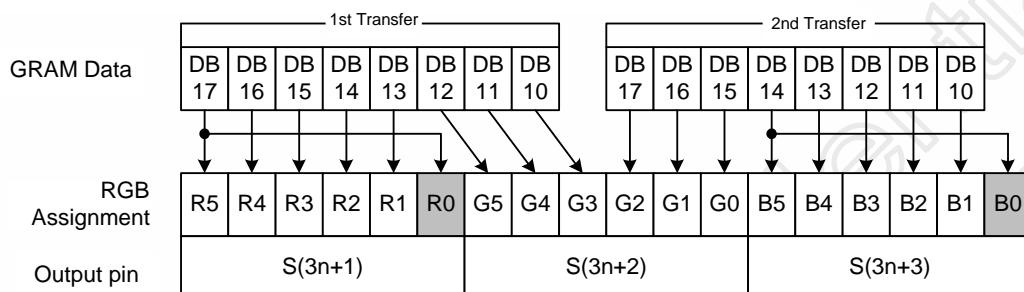
**80-System 16-bit Interface MSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "10"**

Note: n = lower eight bits of address (0 to 175)

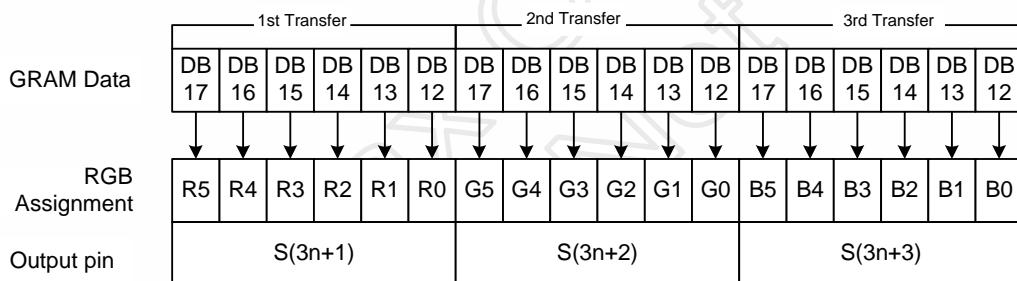
**80-System 16-bit Interface LSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "11"****Figure 3. 2 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "0", BGR = "0")**

**80-System 9-bit bus Interface**

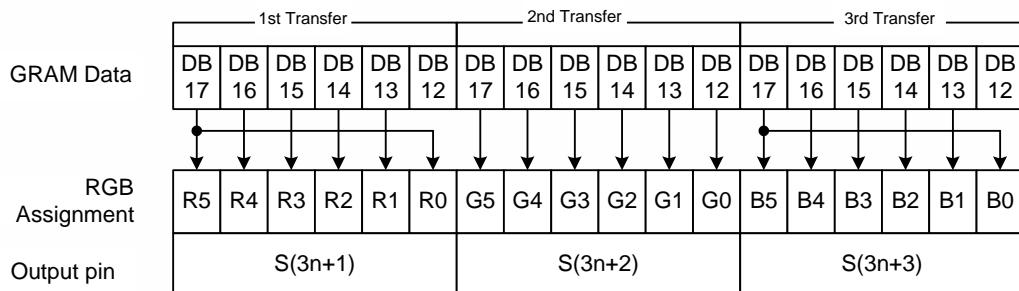
Note: n = lower eight bits of address (0 to 175)

**Figure 3. 3 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = "0", BGR = "0")****80-System 8-bit Interface/Serial Data Transfer Interface (2 transfers/ pixel)**

Note: n = lower eight bits of address (0 to 175)

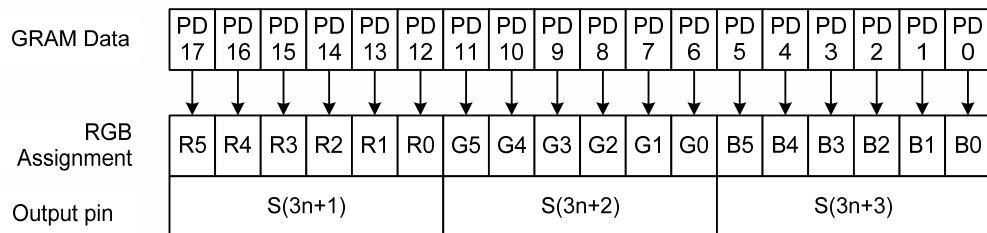
**80-System 8-bit Interface (3 transfers/pixel, 262k colors: TRI=1, DFM1-0=10)**

Note: n = lower eight bits of address (0 to 175)

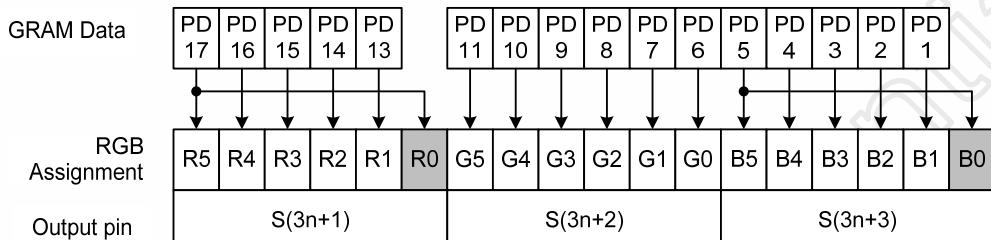
**80-System 8-bit Interface (3 transfers/pixel, 65k colors: TRI=1, DFM1-0=11)**

Note: n = lower eight bits of address (0 to 175)

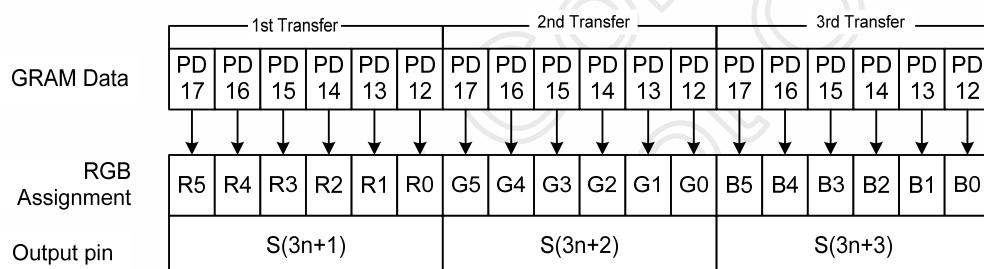
**Figure 3. 4 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = "0", BGR = "0")**

**18-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

**16-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

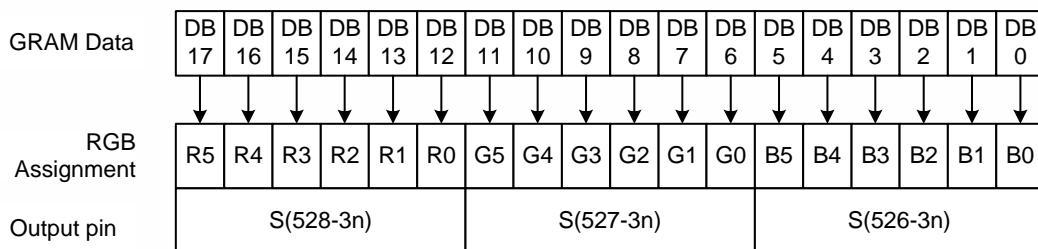
**6-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

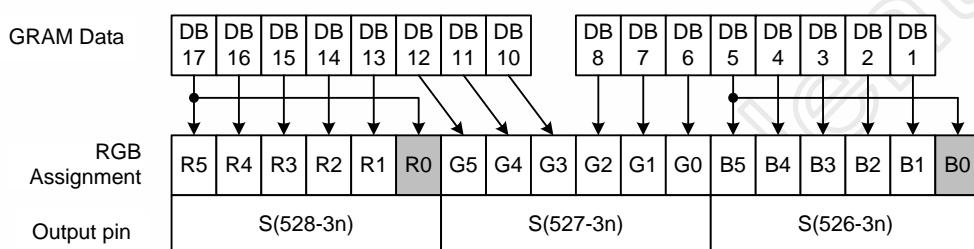
**Figure 3. 5 GRAM Data and Display Data of RGB Interface (SS = "0", BGR = "0")**

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	-----	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB--DB 17---0		DB--DB 17---0		DB---DB 17---0		DB--DB 17---0		-----		DB--DB 17---0											
G1	G220	00AFH	00AEH	00ADH	00ACH	-----	-----	0002H	0001H	-----	-----	0000H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G2	G219	01AFH	01AEH	01ADH	01ACH	-----	-----	0102H	0101H	-----	-----	0100H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G3	G218	02AFH	02AEH	02ADH	02ACH	-----	-----	0202H	0201H	-----	-----	0200H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G4	G217	03AFH	03AEH	03ADH	03ACH	-----	-----	0302H	0301H	-----	-----	0300H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G5	G216	04AFH	04AEH	04ADH	04ACH	-----	-----	0402H	0401H	-----	-----	0400H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G6	G215	05AFH	05AEH	05ADH	05ACH	-----	-----	0502H	0501H	-----	-----	0500H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G7	G214	06AFH	06AEH	06ADH	06ACH	-----	-----	0602H	0601H	-----	-----	0600H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G8	G213	07AFH	07AEH	07ADH	07ACH	-----	-----	0702H	0701H	-----	-----	0700H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G9	G212	08AFH	08AEH	08ADH	08ACH	-----	-----	0802H	0801H	-----	-----	0800H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G10	G211	09AFH	09AEH	09ADH	09ACH	-----	-----	0902H	0901H	-----	-----	0900H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G11	G210	0AAFH	0AAEH	0AADH	0AACB	-----	-----	0A02H	0A01H	-----	-----	0A00H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G12	G209	0BAFH	0BAEH	0BADH	0BACB	-----	-----	0B02H	0B01H	-----	-----	0B00H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G13	G208	0CAFH	0CAEH	0CADH	0CACH	-----	-----	0C02H	0C01H	-----	-----	0C00H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G213	G8	D4AFH	D4AEH	D4ADH	D4ACH	-----	-----	D402H	D401H	-----	-----	D400H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G214	G7	D5AFH	D5AEH	D5ADH	D5ACH	-----	-----	D502H	D501H	-----	-----	D500H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G215	G6	D6AFH	D6AEH	D6ADH	D6ACH	-----	-----	D602H	D601H	-----	-----	D600H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G216	G5	D7AFH	D7AEH	D7ADH	D7ACH	-----	-----	D702H	D701H	-----	-----	D700H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G217	G4	D8AFH	D8AEH	D8ADH	D8ACH	-----	-----	D802H	D801H	-----	-----	D800H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G218	G3	D9AFH	D9AEH	D9ADH	D9ACH	-----	-----	D902H	D901H	-----	-----	D900H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G219	G2	DAAFH	DAAEH	DAADH	DAACH	-----	-----	DA02H	DA01H	-----	-----	DA00H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
G220	G1	DBAFH	DBAEH	DBADH	DBACH	-----	-----	DB02H	DB01H	-----	-----	DB00H	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	

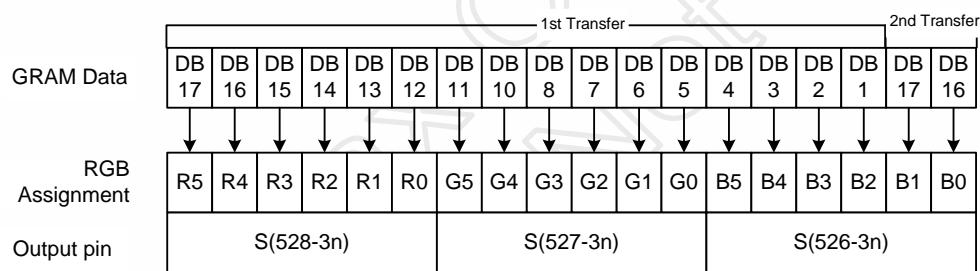
Table 3. 2 GRAM Address and Display Panel Position (SS = "1", BGR="1")

**80-System 18-bit bus Interface**

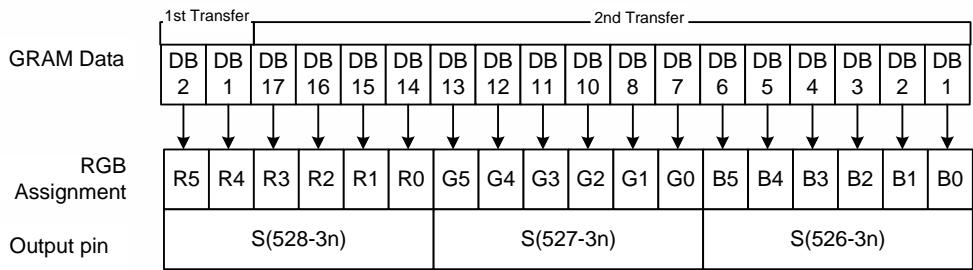
Note: n = lower eight bits of address (0 to 175)

**Figure 3. 6 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "1", BGR = "1")****80-System 16-bit bus Interface**

Note: n = lower eight bits of address (0 to 175)

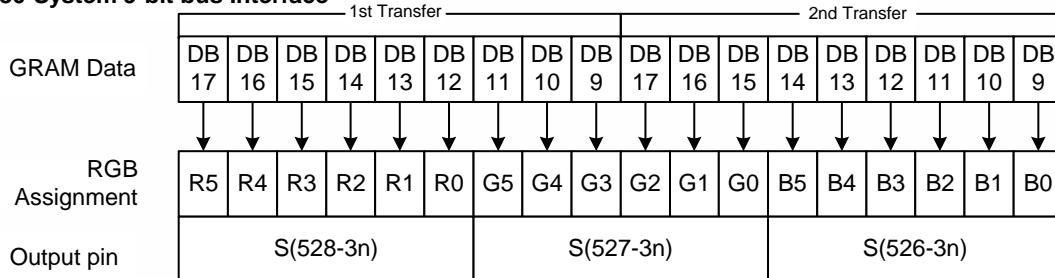
**80-System 16-bit Interface MSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "10"**

Note: n = lower eight bits of address (0 to 175)

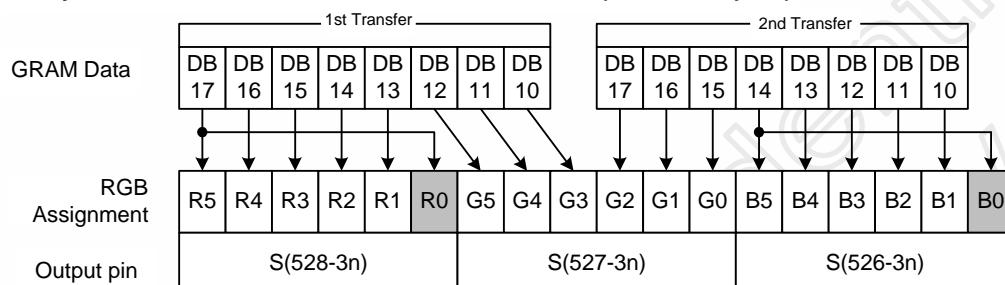
**80-System 16-bit Interface LSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "11"**

Note: n = lower eight bits of address (0 to 175)

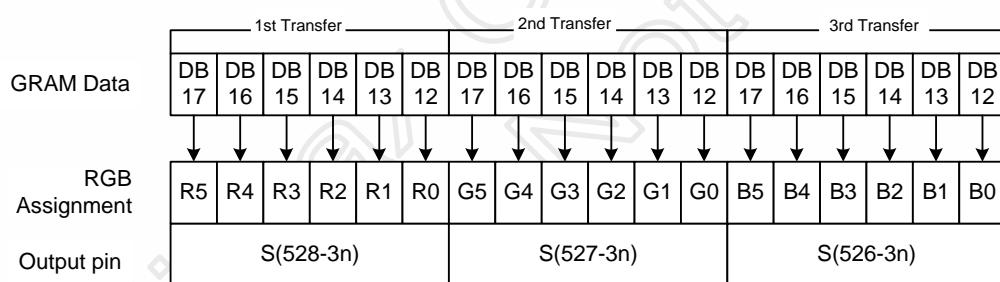
**Figure 3. 7 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "1", BGR = "1")**

**80-System 9-bit bus Interface**

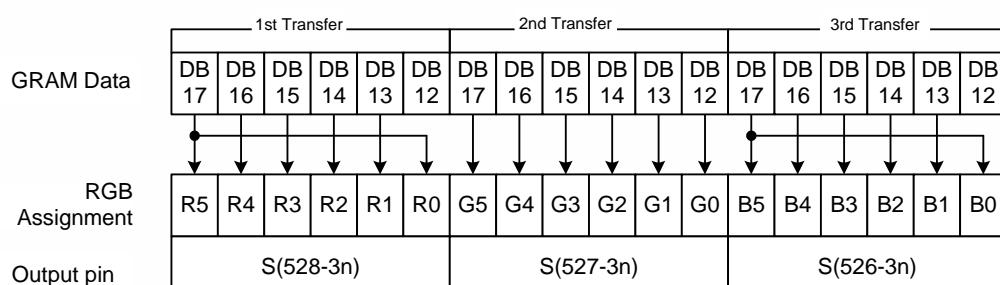
Note: n = lower eight bits of address (0 to 175)

**Figure 3. 8 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = “1”, BGR = “1”)****80-System 8-bit Interface/Serial Data Transfer Interface (2 transfers/ pixel)**

Note: n = lower eight bits of address (0 to 175)

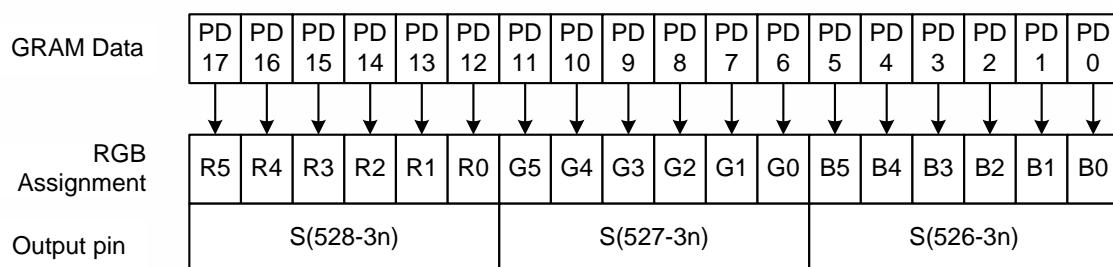
**80-System 8-bit Interface (3 transfers/pixel, 262k colors: TRI=1, DFM1-0=10)**

Note: n = lower eight bits of address (0 to 175)

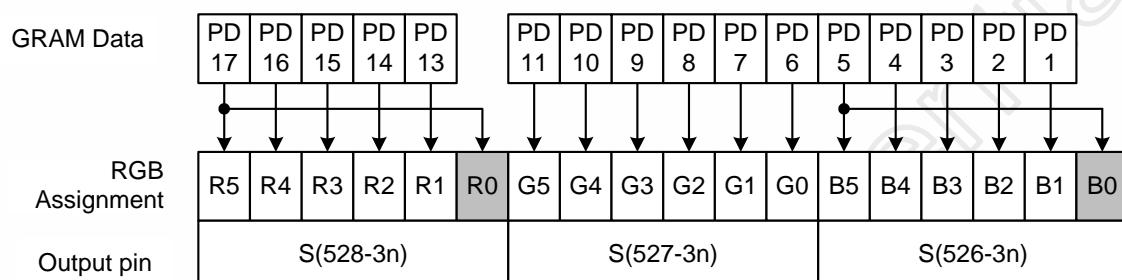
**80-System 8-bit Interface (3 transfers/pixel, 65k colors: TRI=1, DFM1-0=11)**

Note: n = lower eight bits of address (0 to 175)

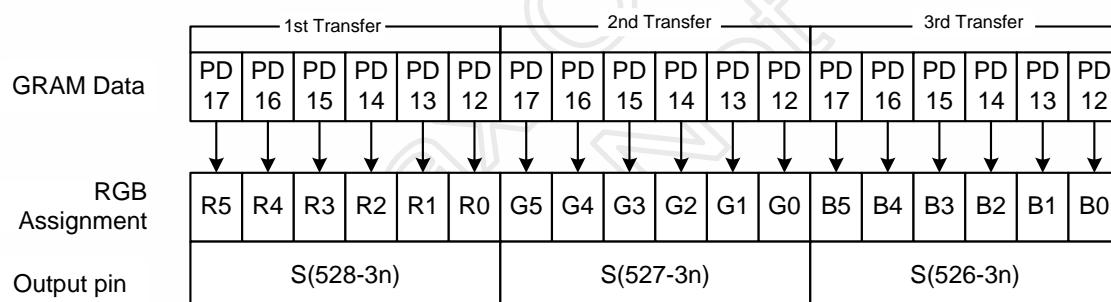
**Figure 3. 9 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = “1”, BGR = “1”)**

**18-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

**16-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

**6-Bit RGB Interface**

Note: n = lower eight bits of address (0 to 175)

**Figure 3. 10 GRAM Data and Display Data of RGB Interface (SS = "1", BGR = "1")**

### 3.1.1 Window Address Function

The HX8309-A contains a GRAM 16-bit bus address counter (AC), which assigns address for writing pixel data to GRAM. The high eight bits of AC are expressed Y address (line address) and the lower eight bits of AC are expressed X address (pixel address). Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (AM bit and I/D bits) setting. However, the AC will be not updated after reading from GRAM.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0). Therefore, data can be written consecutively without thinking a data wrap by those bit function. The address setting of window and GRAM are listed as following:

#### The window address setting range:

$$00H \leq HSA7-0 \leq HEA7-0 \leq AFH$$

$$00H \leq VSA7-0 \leq VEA7-0 \leq DBH$$

#### GRAM address setting range:

$$HSA7-0 \leq AD7-0 \leq HEA7-0$$

$$VSA7-0 \leq AD15-8 \leq VEA7-0$$

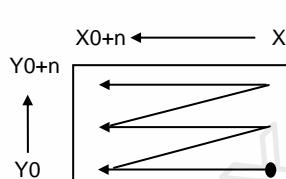
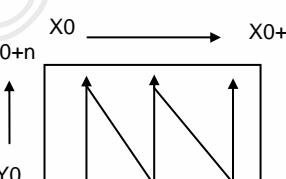
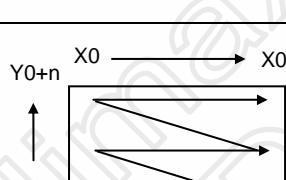
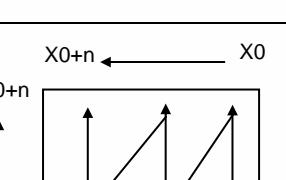
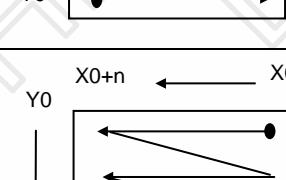
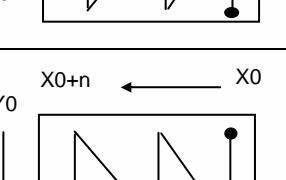
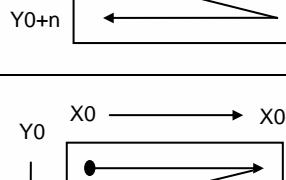
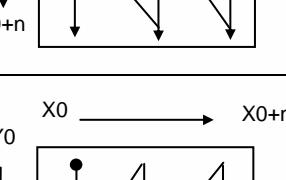
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

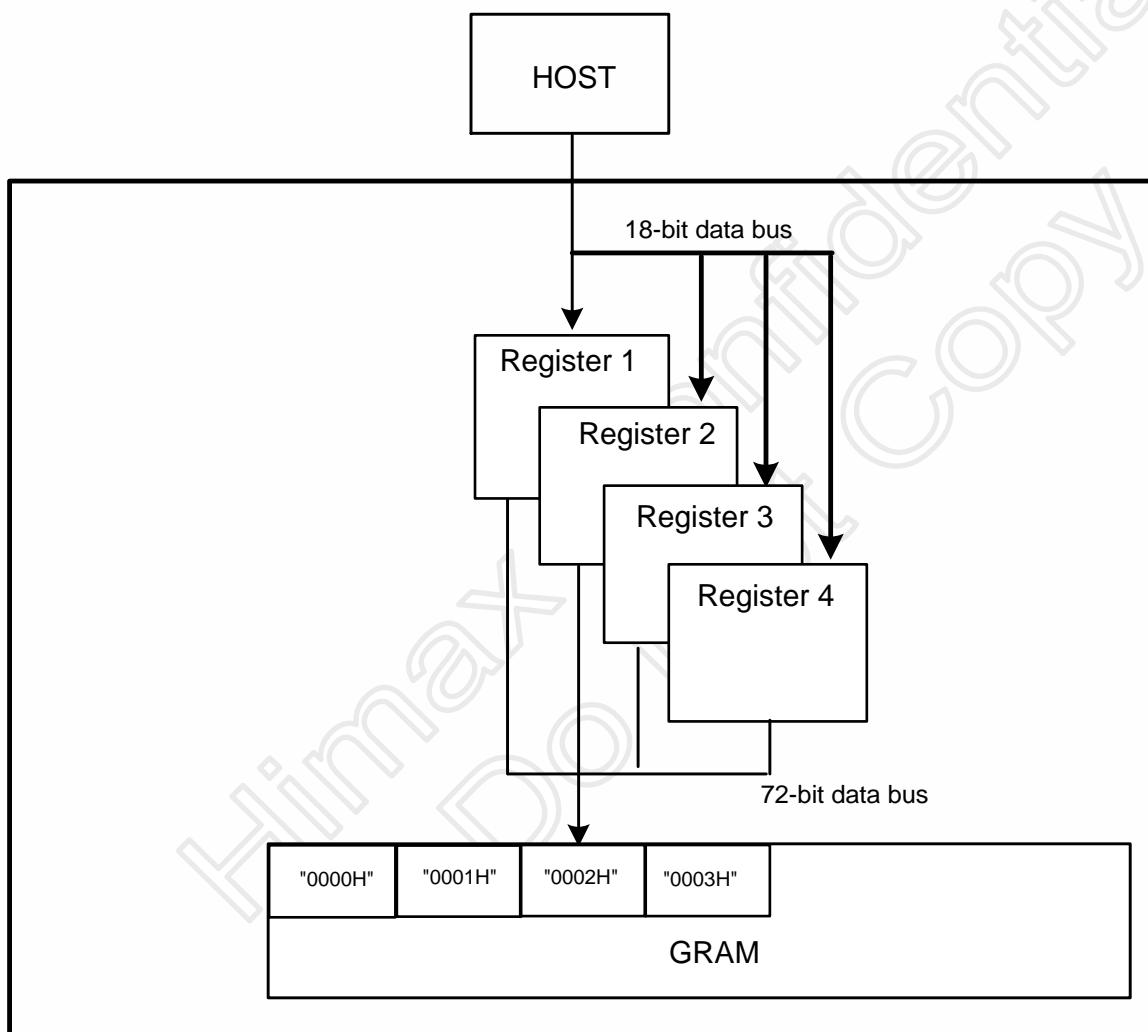
Figure 3. 11 Address Update Direction Settings

### 3.1.2 High-Speed Burst RAM Write Function

The HX8309-A incorporates high-speed burst RAM function that writes data to the internal GRAM about one forth the time of the normal RAM write operation. This function is very useful in high-speed displaying applications such as animation, motion picture and so on.

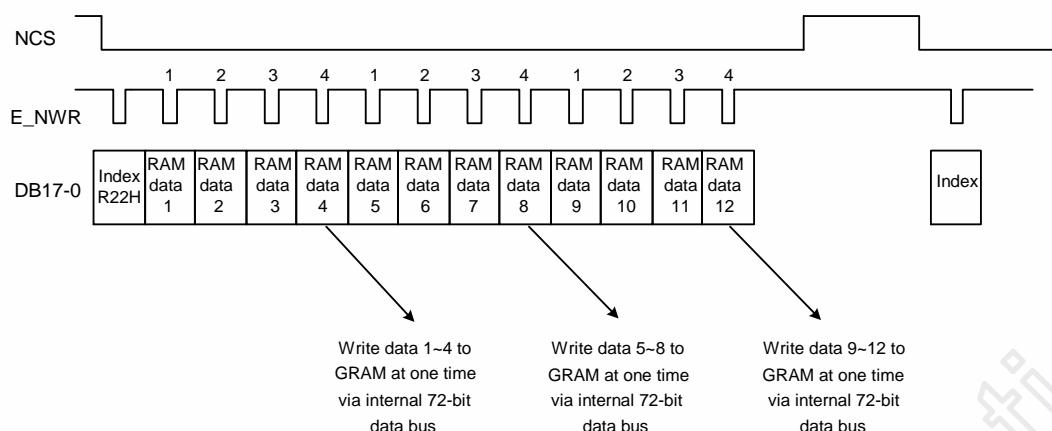
When the high-speed burst RAM write function is selected (setting HWM=1), data are temporarily stored to the internal registers by executing four times write operation merged with one word and then written to the GRAM at once.

When four-word data (72-bits) is written to the on-chip GRAM, the next four-word data can be written to an internal registers so that high-speed and consecutive RAM writing can be executed.



**Figure 3. 12 The Operation of High-speed Burst RAM Function**

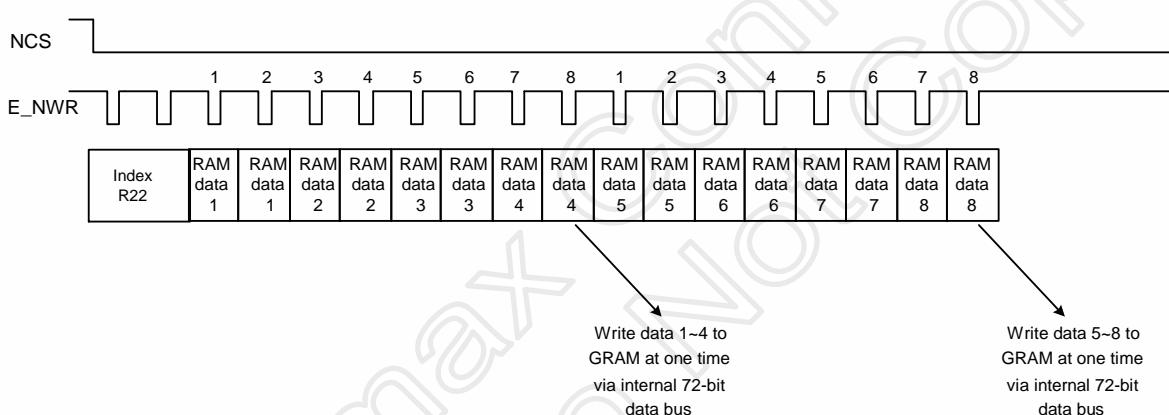
**(a) Example of the Operation of High-speed Consecutive Writing to RAM  
(16-bit bus interface)**



## NOTE:

- Table4. When high-speed RAM write is canceled, the next instruction can be executed only after the RAM write execution time has elapsed.  
 2. When I/D=0, the lower two bits of the start address must be set to 11.  
 3. When I/D=1, the lower two bits of the start address must be set to 00.

**(b) Example of the Operation of High-speed Consecutive Writing to RAM  
(9-bit bus system interface)**



## NOTE:

- Table4. Since data is written to GRAM every four words in high-speed RAM write function, data will be stored eight times to internal register before written to GRAM when using 9-bit bus interface.  
 2. When I/D=0, the lower two bits of the start address must be set to 11.  
 3. When I/D=1, the lower two bits of the start address must be set to 00.

**Figure 3. 13 Example of the Operation of High-Speed Consecutive Writing to RAM**

When use the high-speed RAM write mode, the following items should be note:

	<b>Normal RAM write (HWM=0)</b>	<b>High-Speed RAM Write (HWM=1)</b>
RAM address set	Specified by word	I/D0 bit =0: Set lower two bits to 11 I/D0 bit =1: Set lower two bits to 00
RAM read	Read by word	×
RAM write	Written by word	Dummy write operations may have to be inserted according to a window address range specification.
Write mask function	⌚	⌚
Graphics operation function	⌚	×
Window address	Set by word unit	Set by four-word unit
AM setting	AM =1/0	AM = 0

**Table 3. 3 Comparisons between Normal and High-Speed RAM Write Operation**

⌚ : Can be used

× : Cannot be used

Note1. The Graphic operations cannot be used.

Note2. When using the high-speed RAM write mode. The data are written to RAM each 4 words. And the address is set; the lower two bits of the address must be set to the values as below.

Set the lower two bits of the address to 11, If I/D0 = 0.

Set the lower two bits of the address to 00, If I/D0 = 1.

Note3. The data are written to RAM based on each 4 words. The last RAM writhed

Operation will not be done. If the number of writing to RAM less than four words.

Note4. The RAM can not be read. If HWM bit had been set to 1. Anyway, HWM bit must be set to 0, if want to read data from RAM.

Note5. The high-speed RAM write and normal RAM write can not be operated at the same time.

Note6. If the high-speed RAM write had been used and a window address-range had been set, dummy write operations may be necessary to match the window address setting.

## High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become  $4 \times N$  as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1-0, HEA1-0). Number of total writing operations includes dummy writes each row must be  $4 \times N$ .

Number of Dummy Write Operations Inserted at the Start of a Row	HSA1	HSA0
0	0	0
1	0	1
2	1	0
3	1	1

Table 3. 4 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

Number of Dummy Write Operations Inserted at the End of a Row	HEA1	HEA0
3	0	0
2	0	1
1	1	0
0	1	1

Table 3. 5 Number of Dummy Write Operation in High-Speed RAM Write (HEA Bits)

The access of each row must consist of  $4 \times N$  operations, including the dummy writes

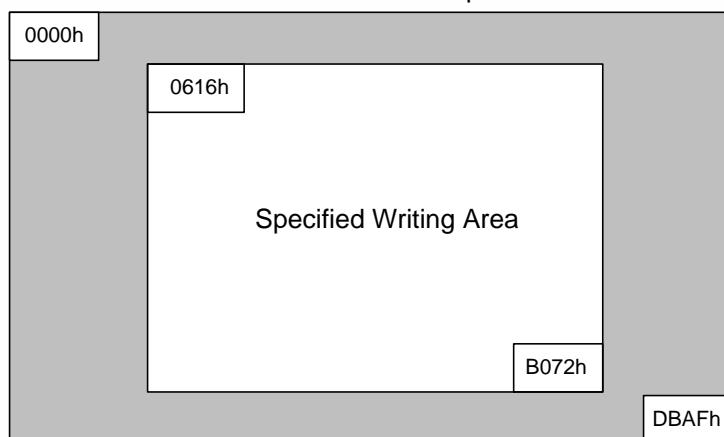
Horizontal access count =  $4 \times N$

$$= \text{First dummy write count} + \text{write data count} + \text{last dummy write count}$$

An example of high-speed RAM write with a window address-range specified:

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writing operations at the start of a row and three dummy writing operations at the end of a row, as determined by using the window address-range specification bits (HSA = 16h, HEA = 72h).

## GRAM address map



## Set window address-range

HSA=16h, HEA=72h

VSA=06h, VEA=B0h

Setting horizontal direction  
while writing :  
AM = 0, I/D0 = 1

Setting window address-range  
HSA = 16h, HEA = 72h  
VSA = 06h, VEA = B0h

Setting to high-speed RAM  
write mode HWM = 1

Set address = 0614h\*

Dummy RAM write x 2

RAM write x 63

Dummy RAM write x 3

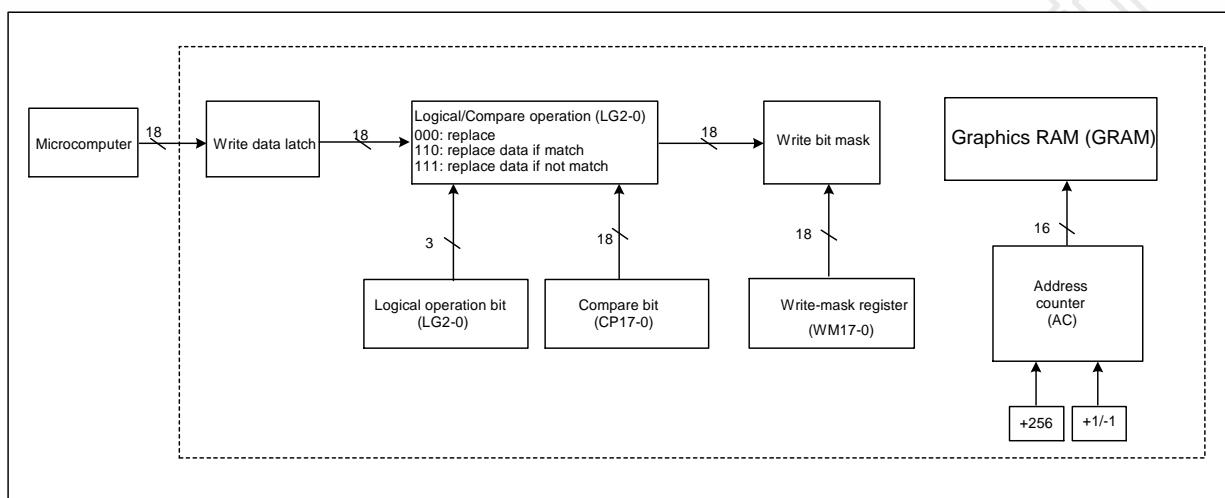
x171

Note: The address set for high speed GRAM write must be 00 or 11 according to I/D bit. Dummy write would not write any data into GRAM.

**Figure 3. 14 Example of the High-Speed RAM Write with a Window Address-Range Specification**

### 3.2 Graphics Operation Function

The graphics bit operations of the HX8309-A are executed with setting ID1-0, AM and LG2-0 and RAM write data mask register bits whenever do the read or write operations from MCU. The significant concept of graphics bit operation function is reduced the graphics processing load on software of the MCU with 18-bit bus architecture. The graphics bit operation function includes the write data mask function that rewrites some bits of 18-write data via write-mask register (WM17-0). Furthermore, the graphics bit operations function can do the conditional rewrite operation that compares the write data sent from the MCU and the data in the compare register and rewrites the data before write mask enable when the bits in logical/compare register be satisfied the condition.



**Figure 3. 15 Graphics Operations**

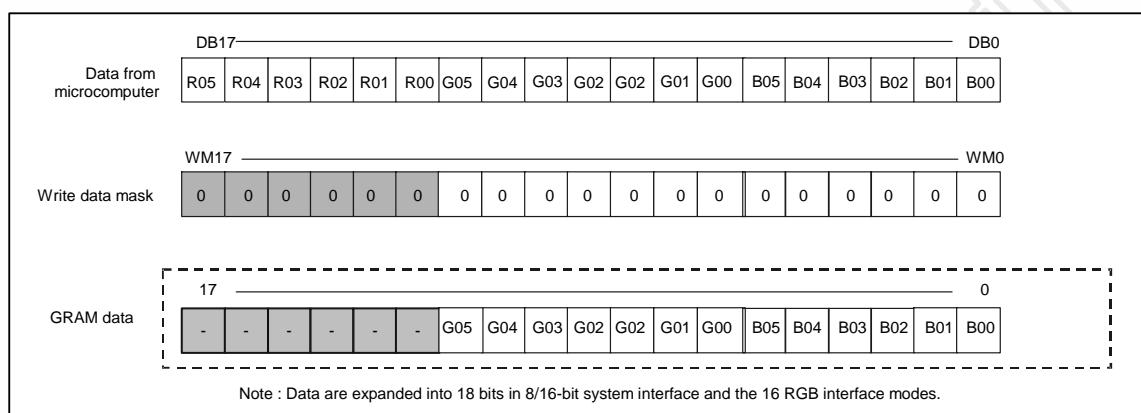
No.	Operation Mode	Bit Setting			Operation and Usage
		I/D	AM	LG2-0	
1	Write mode 1	0/1	0	000	Horizontal data replacement
2	Write mode 2	0/1	1	000	Vertical data replacement
3	Write mode 3	0/1	0	110	Conditional horizontal data replacement (match to write)
4	Write mode 4	0/1	1	110	Conditional vertical data replacement (mismatch to write)

**Table 3. 6 Bit Set of Graphics Operation Function**

## Enable write-data Mask function

The write-data mask function executes the operation of writing the corresponding bits to GRAM when the corresponding bits of the write data mask register (WM17-0) are given "0" and out of writing the corresponding bits of GRAM when the corresponding bits of the write data mask register (WM17-0) are given "1" contrary. Furthermore, the data sent from microcomputer are expanded into 18 bits internally in the 8/16-bit bus system interface, and 16-bit bus RGB interface. But in 18-bit bus system or RGB interface, data are not expanded.

When executes the write-data mask function, the GRAM data are not overwritten but retained. This function is usually used when only corresponding bits of one specific pixel is rewritten or a designated display color is changed separately.



**Figure 3. 16 Write Data Mask Function**

### Graphics Operation Function Examples:

#### 1. Example1 of write mode operation:

The registers are set as following:

I/D = "1", AM = "1", LG2-0 = "000"

WM17-0 (Write-data mask) = "0003F" H

AC (Address Counter) = "0000" H

In this example, the write-data function write mask "B" plan of pixel. The data are expanded into 18 bits when not set at 18-bit bus interface. The data are vertically written in high-speed mode when set AM=1 and the address counter will be automatically increments or decrement by setting I/D1-0.

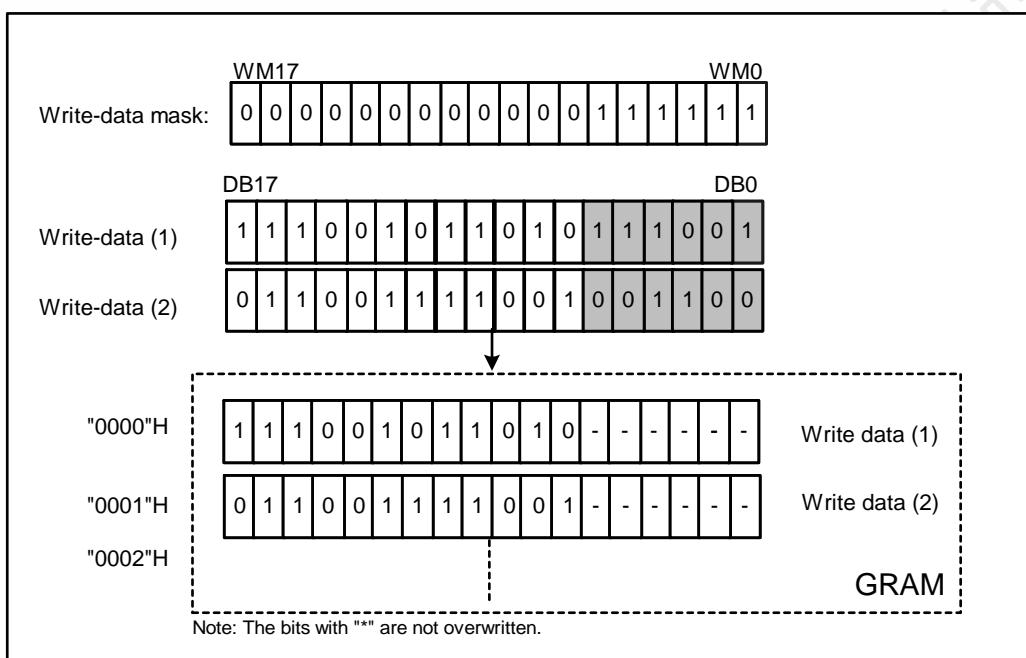


Figure 3. 17 Example1 of Write Mode Operation

## 2. Example2 of write mode operation:

The registers are set as following:

I/D = "1", AM = "0", LG2-0 = "000"

WM17-0 (Write-data mask) = "0003F" H

AC (Address Counter) = "0000" H

In this example, the write-data function write mask "B" plan of pixel. The data are expanded into 18 bits when not set at 18-bit bus interface. The data are horizontally written in high-speed mode when set AM=0 and the address counter will be automatically increments or decrement by setting I/D1-0.

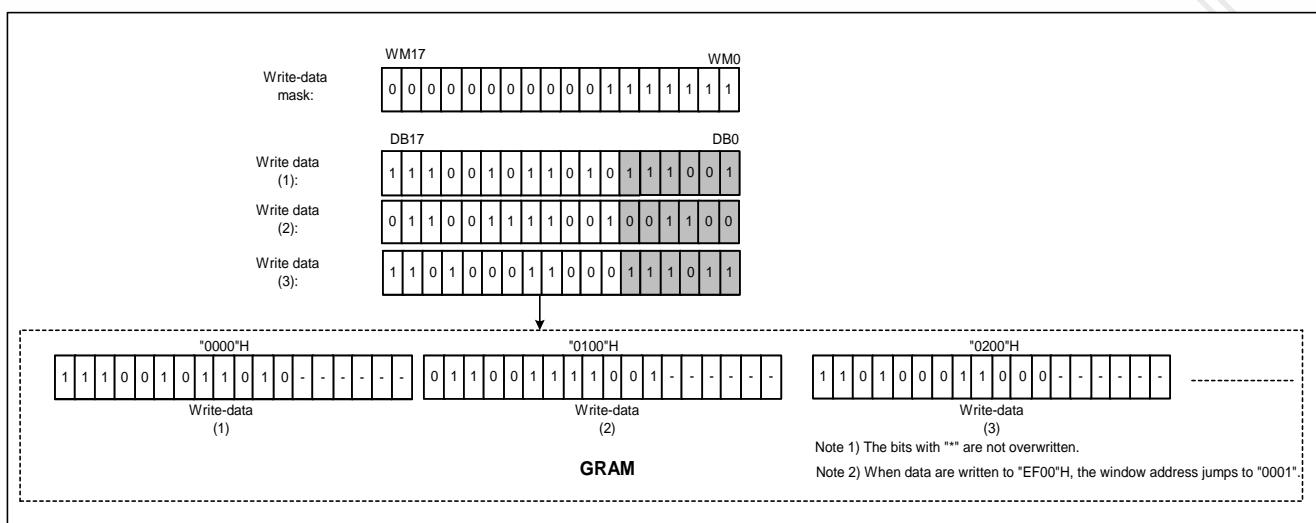


Figure 3. 18 Example2 of Write Mode Operation

## 3. Example3 of write mode operation:

The registers are set as following:

I/D = "1", AM = "1", LG2-0 = "110"

CP17-0 (Compare register) = "070F0" H

WM17-0 (Write-data mask) = "00000" H

AC (Address Counter) = "0000" H

In this example, the data is expanded into 18 bits when not set at 18-bit bus interface. The data are vertically written (AM=1) in high-speed mode that comparing the write data with the data in the compare register (CP17-0). When the result of comparison match up a condition, the data sent from microcomputer would be written to GRAM and then the address counter will be automatically increments or decrement by setting I/D1-0.

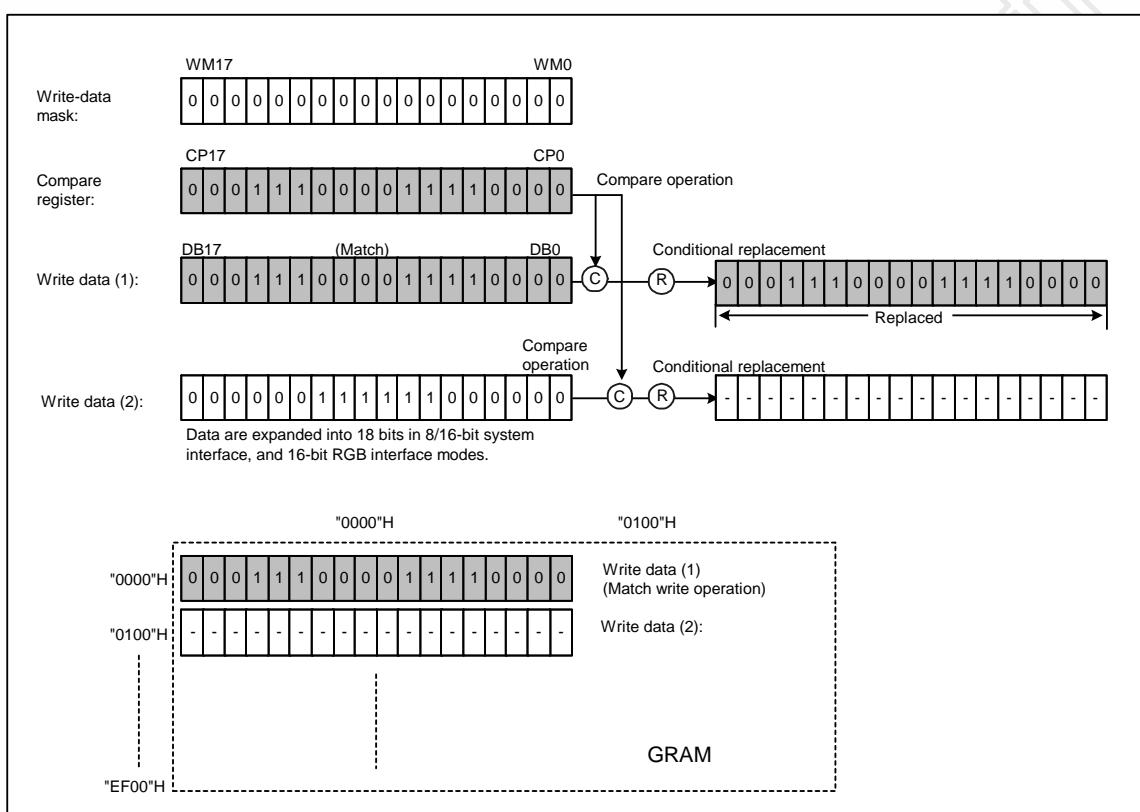


Figure 3. 19 Example3 of Write Mode Operation

#### 4. Example4 of write mode operation:

The registers are set as following:

I/D = "0", AM = "0", LG2-0 = "111"

CP17-0 (Compare register) = "070F0" H

WM17-0 (Write-data mask) = "00000" H

AC (Address Counter) = "0000" H

In this example, the data are expanded into 18 bits when not set at 18-bit bus interface. The data are horizontally written (AM=0) in high speed mode that comparing the write data with the data in the compare register (CP17-0). When the result of comparison match up a condition, the data sent from microcomputer would be written to GRAM and then the address counter will be automatically increments or decrement by setting I/D1-0. The logical operation register (LG2-0) is set about match or mismatch to write.

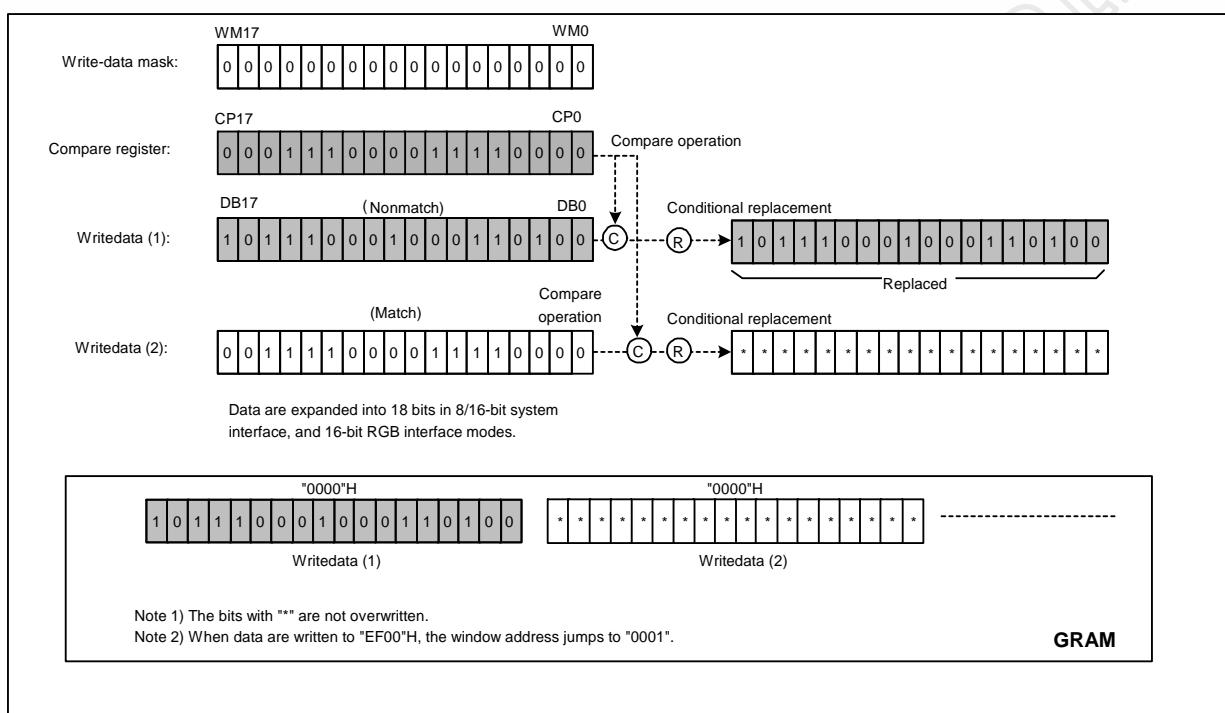
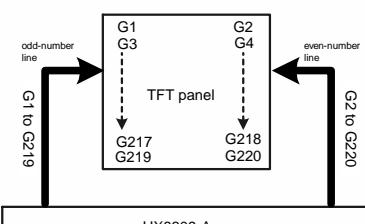
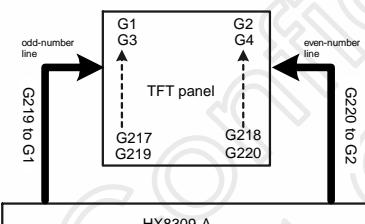
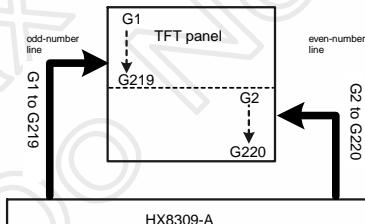
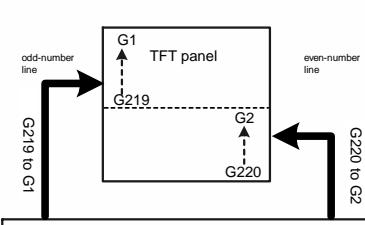


Figure 3. 20 Example4 of Write Mode Operation

### 3.3 Display Function

#### 3.3.1 Scan Mode Setting

The HX8309-A can set SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8309-A.

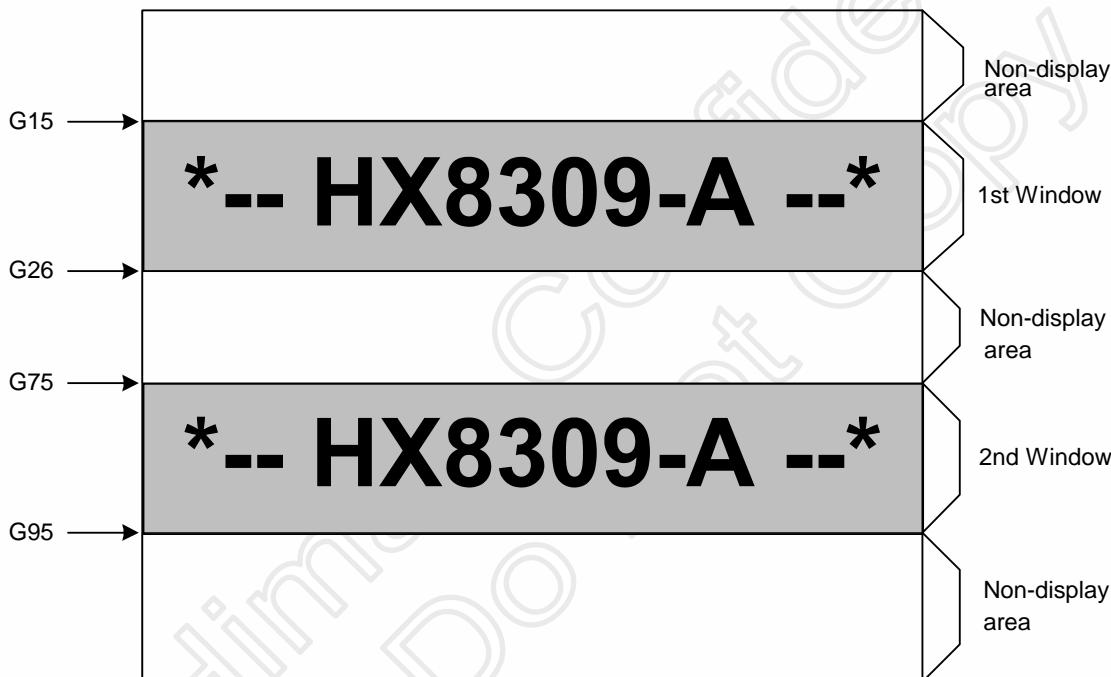
SM	GS	Scan direction
0	0	 <p style="text-align: center;">HX8309-A G1, G2, G3, G4,..., G217, G218, G219, G220</p>
0	1	 <p style="text-align: center;">HX8309-A G220, G219, G218, G217,..., G4, G3, G2, G1</p>
1	0	 <p style="text-align: center;">HX8309-A G1, G3, G5,..., G217, G219, G2, G4, G6,..., G218, G220</p>
1	1	 <p style="text-align: center;">HX8309-A G220, G218, G216,..., G4, G2, G219, G217, G215,..., G3, G1</p>

**Note:** Scan mode setting depend on the design and layout of glass on panel.  
**Figure 3. 21 SCAN Mode Setting**

### 3.3.2 Partial Screen Display

The HX8309-A has one or two screens driving functions. The position of display screen register (R42h and R43h) can display at any position of the whole screen. The numbers of display lines that display on the first and second windows must be less than total LCD-driving lines setting (NL4-0). The rest display area in the screen should be white display if the type of LCD is normally white and should be black display if the type of LCD is normally black. Therefore, the partial display can reduce the power consumption.

As the below, the first window start line from the SS1 (7-0) and end line at SE1 (7-0), that are specified by the 1<sup>st</sup> Display Window Driving Position Register (R42h). The second window start line from SS2 (7-0) and end line at SE2 (7-0), that are specified by 2<sup>nd</sup> Display Window Driving Position Register (R43h). And the second display window is availed when the SPT bit is set to 1. The number of the total selection driving lines included the 1<sup>st</sup> and 2<sup>nd</sup> display window must be equal to or less than the LCD Drive Line (NL).



Number of Scan Line : NL(4-0) = "10101" (176 lines)

1st Screen Setting : SS1(7-0) = "0E"h , SE1(7-0) = "19"h

2nd Screen Setting : SS2(7-0) = "4A"h , SE2(7-0) = "5E"h , SPT=1

**Figure 3. 22 Partial Screen Display Example in 2-Windows Driving**

## The conditions of 1<sup>st</sup> and 2<sup>nd</sup> Display Window Driving Position Register Setting

The conditions as following must be contented when setting the start line SS1 (7-0) and end line SE1 (7-0) of the 1<sup>st</sup> display window at register (R42h) and the start line SS2 (7-0) and end line SE2 (7-0) of the 2<sup>nd</sup> display window at register (R42).

Note: That incorrect display may occur if the condition setting is not contented.

**Condition:  $0 \leq SS1(7-0) \leq SE1(7-0) \leq NL$**

Register Settings	Display Operation
$SE1(7-0) - SS1(7-0) + 1 = NL$	Whole-Screen Display The area of SE1 (7-0)-SS1 (7-0) is normally displayed
$0 < SE1(7-1) - SS1(7-0) + 1 < NL$	Partial screen display The area of SE1 (7-0)-SS1 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

**Table 3. 7 Conditions on One Screen Driving (STP = 0)**

Note: The SS2 (7-0) and SE2 (7-0) settings are ignored.

**Condition:  $0 \leq SS1(7-0) \leq SE1(7-0) < SS2(7-0) \leq SE2(7-0) \leq NL$**

Register Settings	Display Operation
$(SE1(7-0) - SS1(7-0) + 1) + (SE2(7-0) - SS2(7-0) + 1) = NL$	Whole-Screen Display The area of SE2 (7-0) - SS1 (7-1) is normally displayed
$(SE1(7-0) - SS1(7-0) + 1) + (SE2(7-0) - SS2(7-0) + 1) < NL$	Partial Screen Display The area of SE1 (7-0) - SS1 (7-0) and SE2 (7-0) - SS2 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

**Table 3. 8 Condition on Two Screen Driving (STP = 1)**

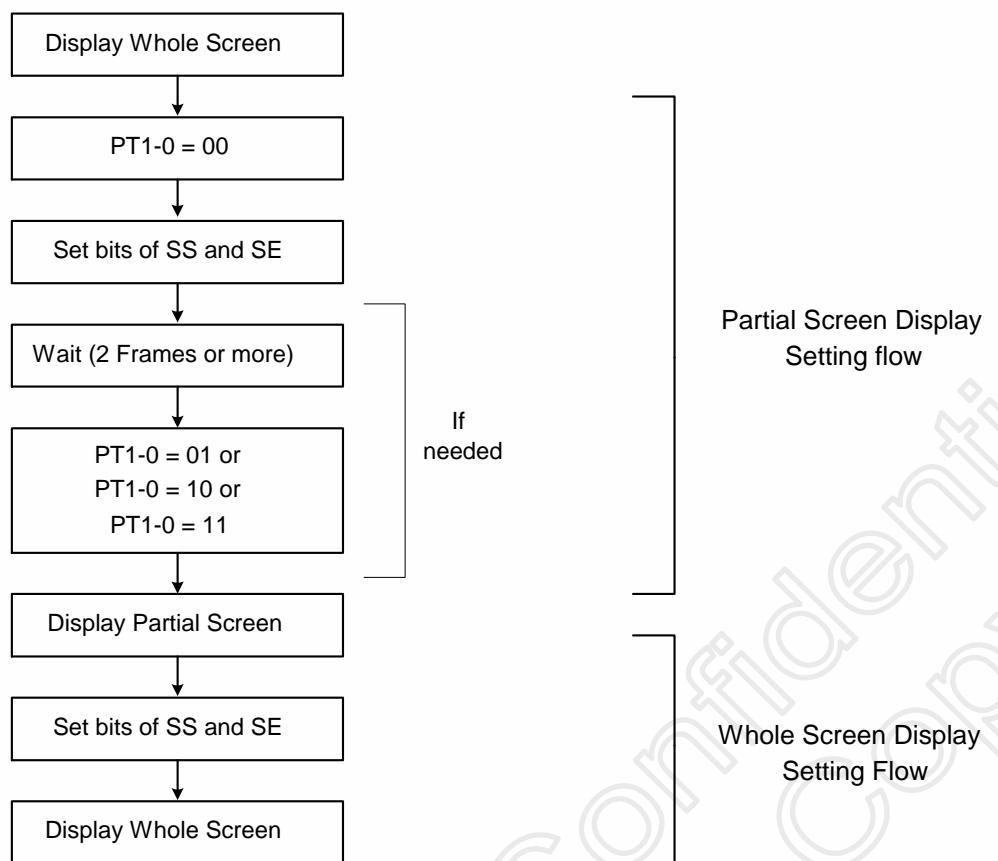
The driver outputs for non-display area on partial display can be specified. Set the values to match the characteristics for the panel.

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	Vcom output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VcomH↔VcomL
0	1	Ignore	Ignore	Reference to PTG1-0	VcomH↔VcomL
1	0	VSSD	VSSD	Reference to PTG1-0	VcomH↔VcomL
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

**Table 3. 9 Source and Gate Output in Non-Display Area during Partial Display Function**

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

Setting of the partial display should follow the flow shown as below



**Figure 3. 23 Partial Display Setting Flow**

### 3.3.3 8-Color Display

The HX8309-A supports an 8-color display mode. The grayscale level to be used is V0 and V63 with R5, G5, B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

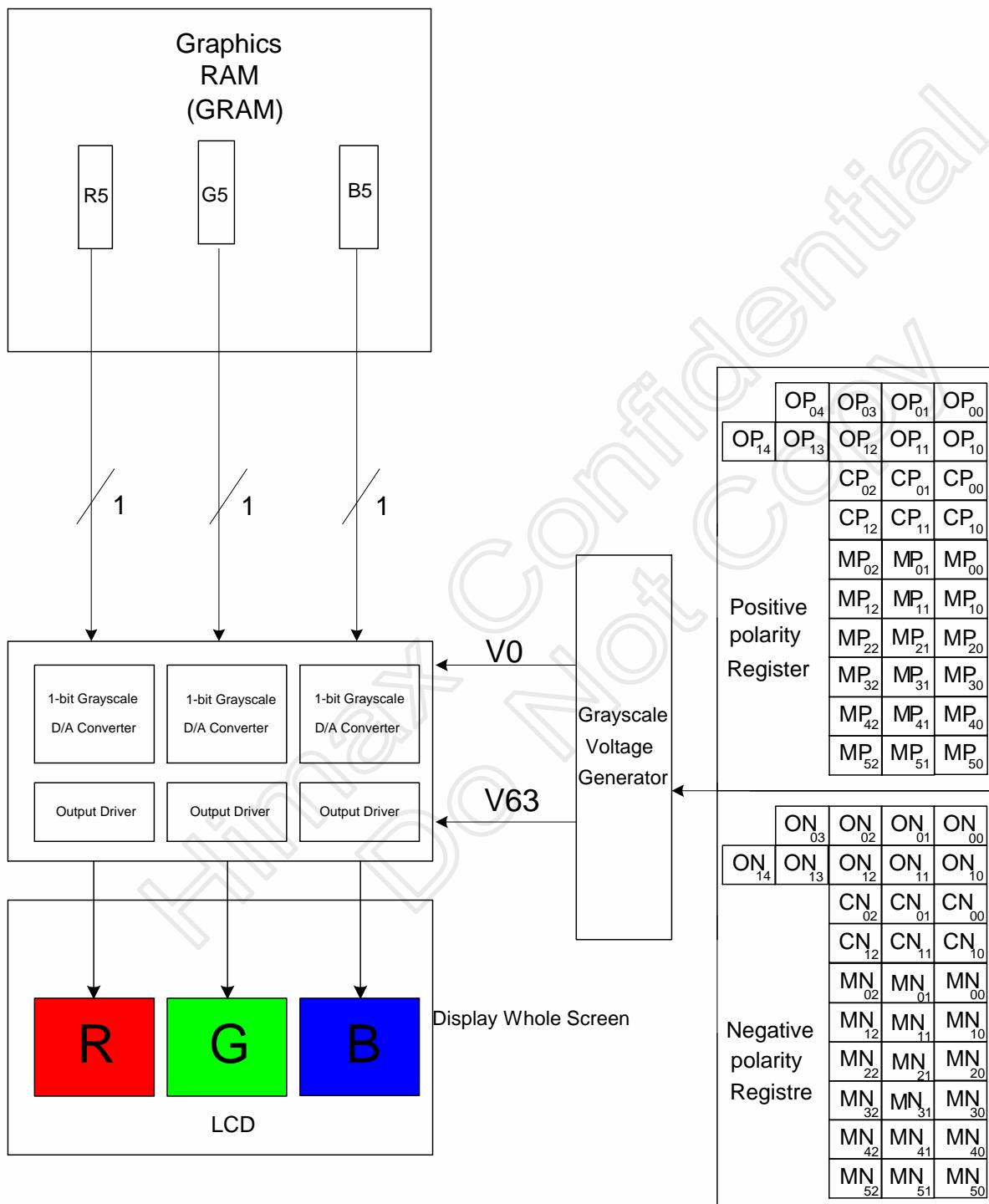
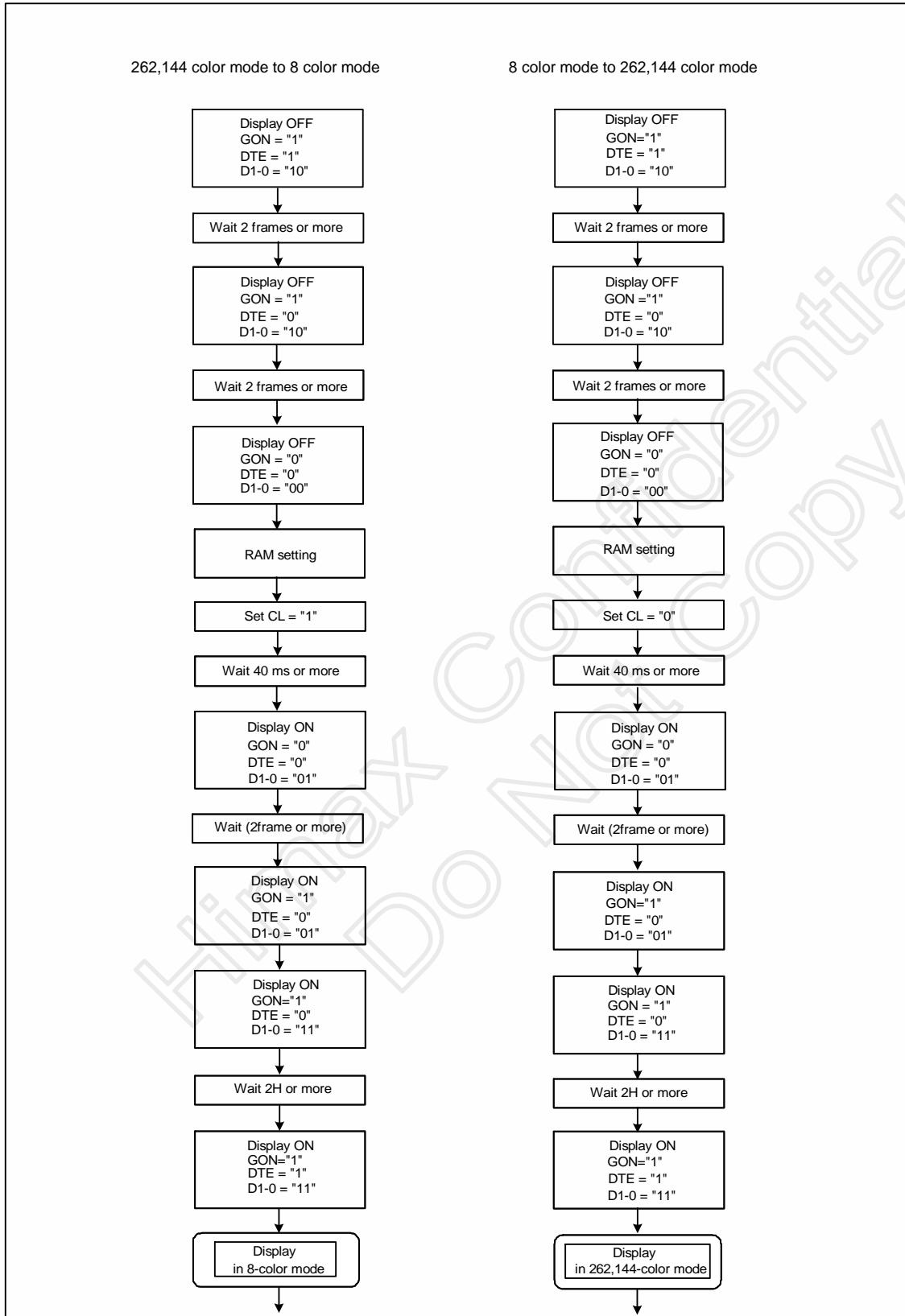


Figure 3. 24 Grayscale Control in 8-Color Mode

The follow figure is the switch sequence between the 262,144-color mode and 8-color mode:

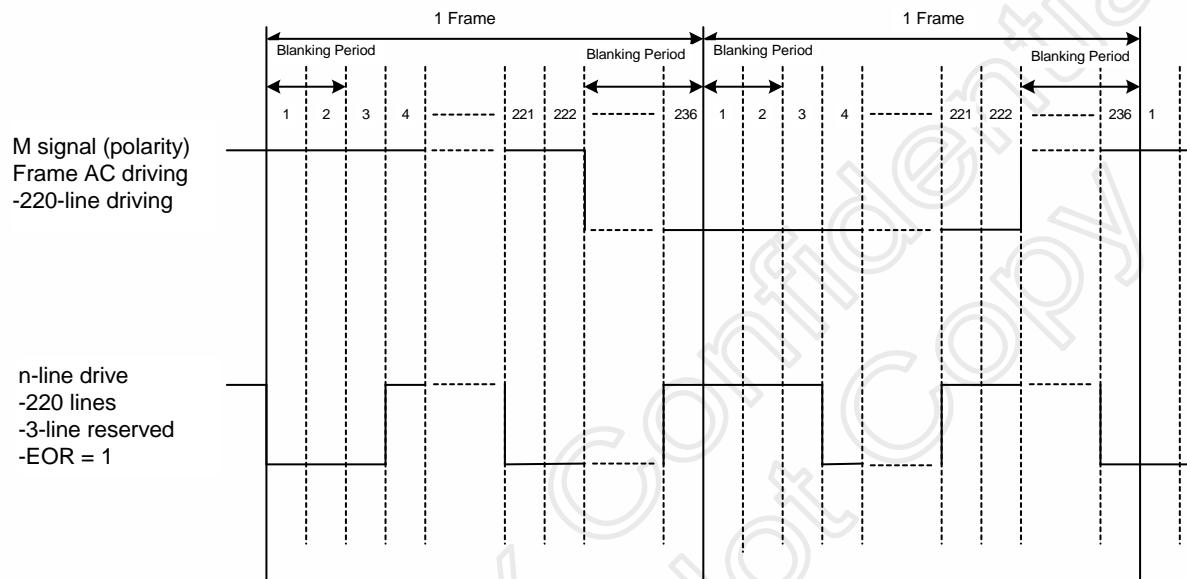


**Figure 3. 25 Switch Sequence between 262,144-color Mode and 8-color Mode**

### 3.3.4 N-line Inversion LCD Drive

The HX8309-A supports frame inversion and n-line inversion LCD current driving, which n chooses 1~64. The inversion operation is controlled by POL (Polarity of Liquid Crystal) signal which interval is set by NW5-0 bits in R02h register. The HX8309-A internally transfers POL signal for alternating the VCOM voltage and alternates source output voltage according to gamma register with POL signal, which changes the polarity of LCD driving voltage. When a display quality problem occurs, the n-line inversion LCD drive can improve the quality by setting proper n value.

The value of n also represented by the NW bits+1, which represented LCD alternating frequency becomes high when the number of inversion lines were setting a smaller value, hence, in the LCD cells, the charge or discharge current is increased.



**Figure 3. 26 N-line Inversion Driving Diagram**

### 3.3.5 Interlaced Driving Function

The HX8309-A has an interlaced function that divided one frame into 3 fields to drive. The LCD to avoid flicker to confirm the display quality with the actual LCD display then determined the number of fields. As following table, the gate selection where the number of field is 3 (setting FLD1-0 = 11) and as following figure the output waveform when 3 field interlaced driving is performed is shown.

GS = 0			GS = 1		
FLD1-0	11		FLD1-0	11	
Gate	Field	1	Gate	Field	1
G1	*		G220	*	
G2		*	G219		*
G3			G218		*
G4	*		G217	*	
G5		*	:		*
G6		*	G9		*
G7	*		G8	*	
G8		*	G7		*
G9		*	G6		*
:	:	:	G5	:	:
G217			G4		
G218	*		G3	*	
G219		*	G2		*
G220		*	G1		*

Table 3. 10 Combined with GS and FLD Setting

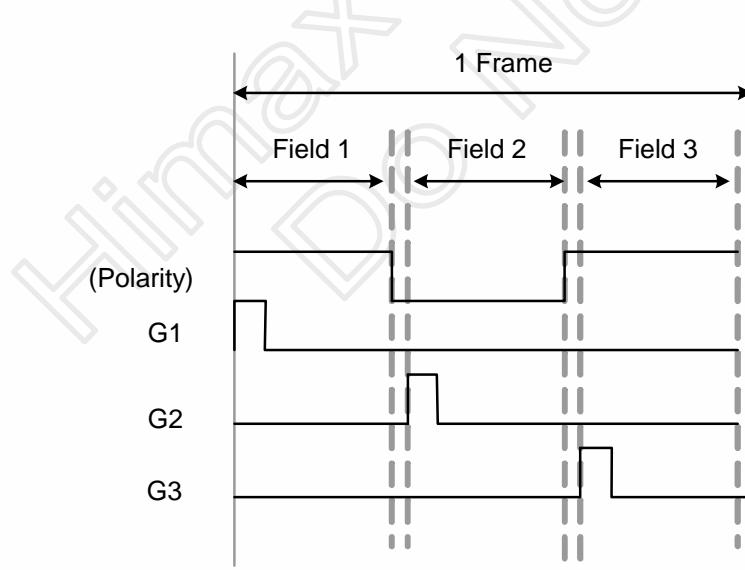


Figure 3. 27 Output Timing for Interlaced Gate Signals (Three-Field is selected)

### 3.3.6 AC Driving Alternating Timing

LCD must be driven by alternating voltage polarity between liquid crystal layers. The operation of AC drive timing in each type is shown below. The period of AC drive timing is the same as the period of POL signal, which is controlled by the value in register R02h (NW).

In frame-inversion AC drive, LCD-driving signal alternates after one frame finishing display and then a FP or back-porch blanking period are inserted. During the blanking period all gate outputs are remain Vgoff. In interlaced drive, LCD-driving signal alternates after one field finishing display and then a blanking period is inserted. The sum of blanking periods in three fields is equal to the sum of BP and FP blanking period set in a frame. For n-line inversion AC drive, LCD-driving signal alternates before every n-line display starts. Back-porch blanking period is inserted before all display operations starting and front-porch blanking period is inserted after the completion of all display operations.

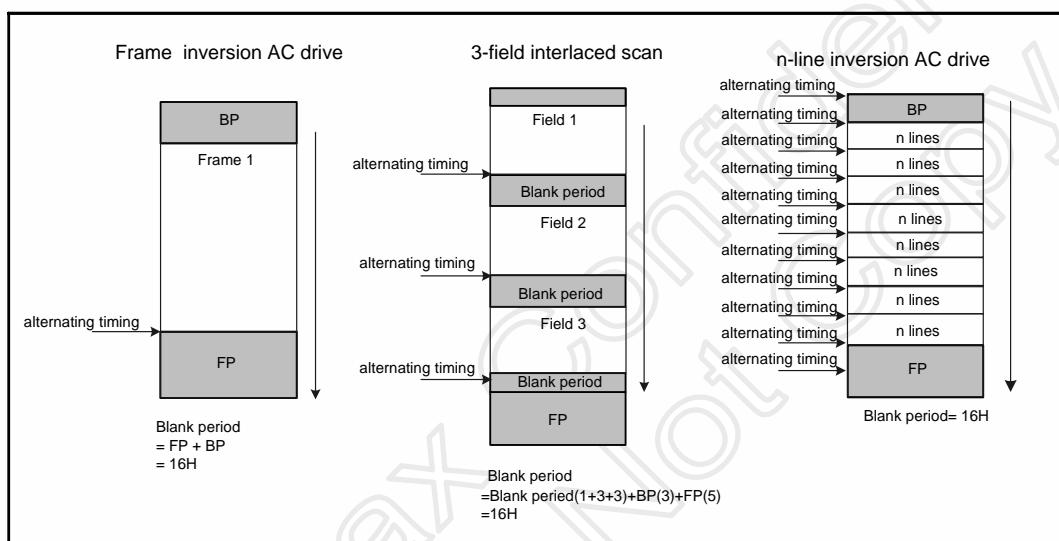


Figure 3.28 AC Driving Alternating Timing Diagram

### 3.4 Frame-Frequency Adjustment Function

The HX8309-A supports frequency adjustment function of frame frequency stably that can adjust the frame frequency via the register (DIV, RTN bits) setting in R0Bh during the oscillation frequency.

An animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching (an animated display) is required, the frame frequency can be set higher.

### Relationship between LCD Drive Duty and Frame Frequency

The LCD driving duty and the frame frequency is obtained by the following calculation. The frame frequency can be adjusted in the 1-H line period bit (RTN) and in the operation clock division bit (DIV) by write the instruction to the relative register.

#### Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL}+\text{BP}+\text{FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency

RTN bit: Clocks per line

DIV bit: Division ratio

NL: The number of lines

FP: Number of lines for front porch

BP: Number of lines for back porch

$\text{BP}+\text{FP} \leq 16$

#### Example Calculation: To set the maximum frame frequency to 60 Hz

Number of drive lines: 200 lines

line period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1 Division

$\text{fosc} = 60 \text{ Hz} \times (0 + 16) \text{ clock} \times 1 \text{ division} \times (200+16) \text{ lines} = 207 \text{ (KHz)}$

In this case, the R-C oscillation frequency becomes 207 KHz. The external resistance value of the R-C oscillator must be adjusted so that the frequency of internal R-C oscillator is equal to 207 KHz. The display duty can be changed by the partial display with the same frequency setting as above.

### 3.5 γ-Correction Function

The HX8309-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

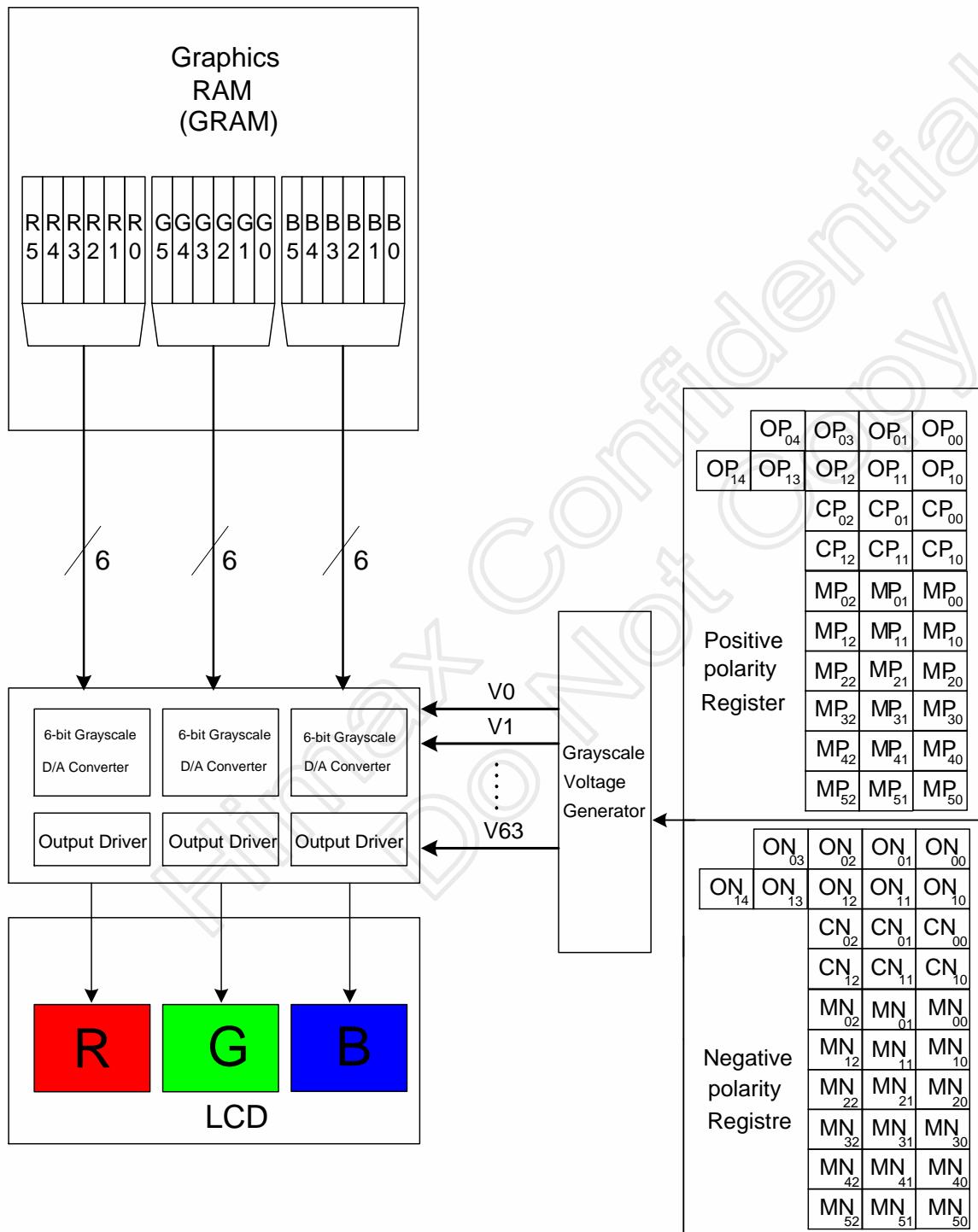
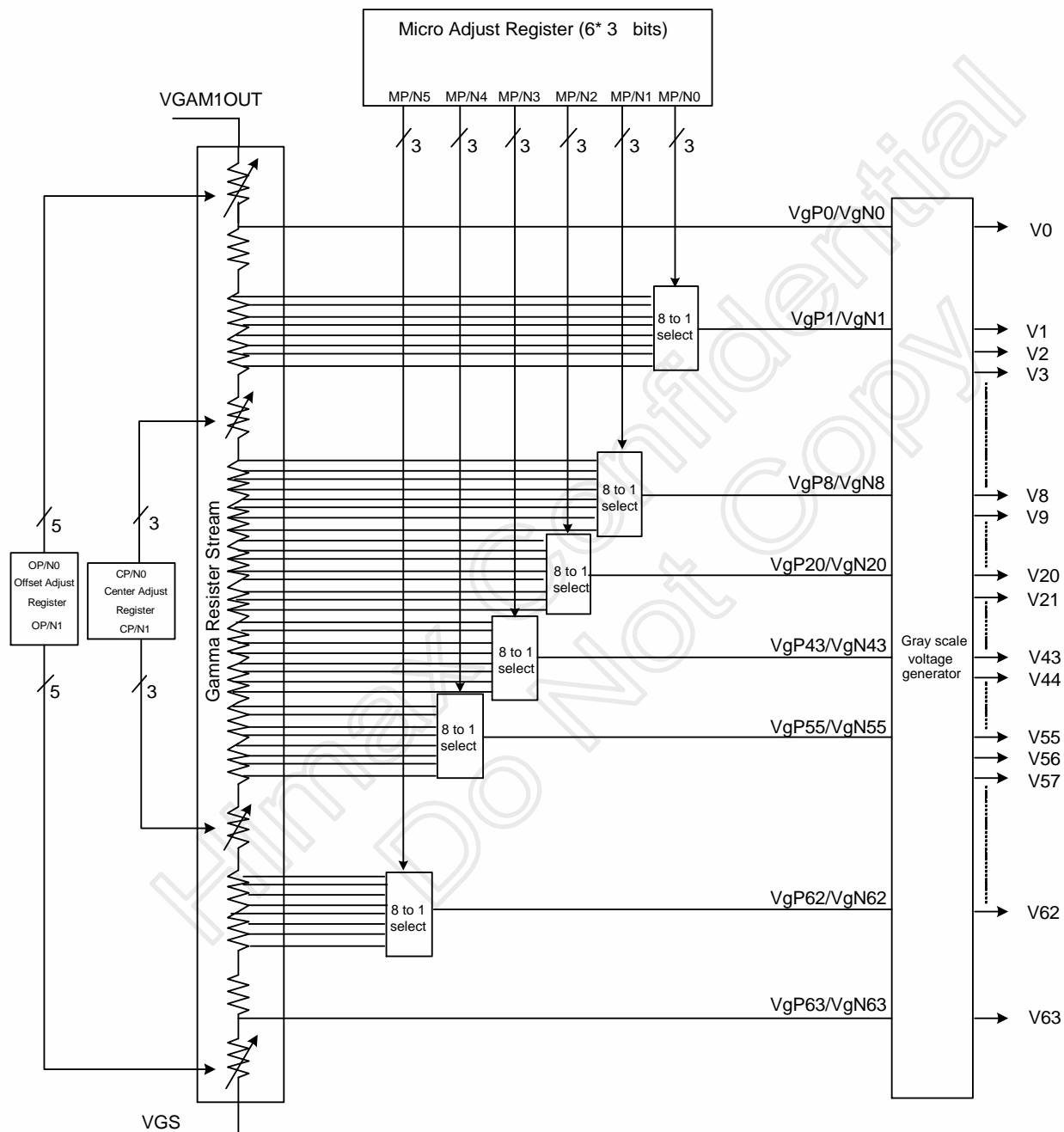


Figure 3. 29 Grayscale Control

## Structure of Grayscale Voltage Generator

Eight reference gamma voltages  $VgP/N(0, 1, 8, 20, 43, 55, 62, 63)$  for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages ( $V0-V63$ ) can be generated from grayscale amplifier for LCD panel used.



**Figure 3.30 Structure of Grayscale Voltage Generator**

## Gamma-Characteristics Adjustment Register

This HX8309-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

### 1. Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

### 2. Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

### 3. Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0) for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1) for offset adjustment

Table 3. 11 Gamma-Adjustment Registers

## Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. ( $V_{gP/N}$ ) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

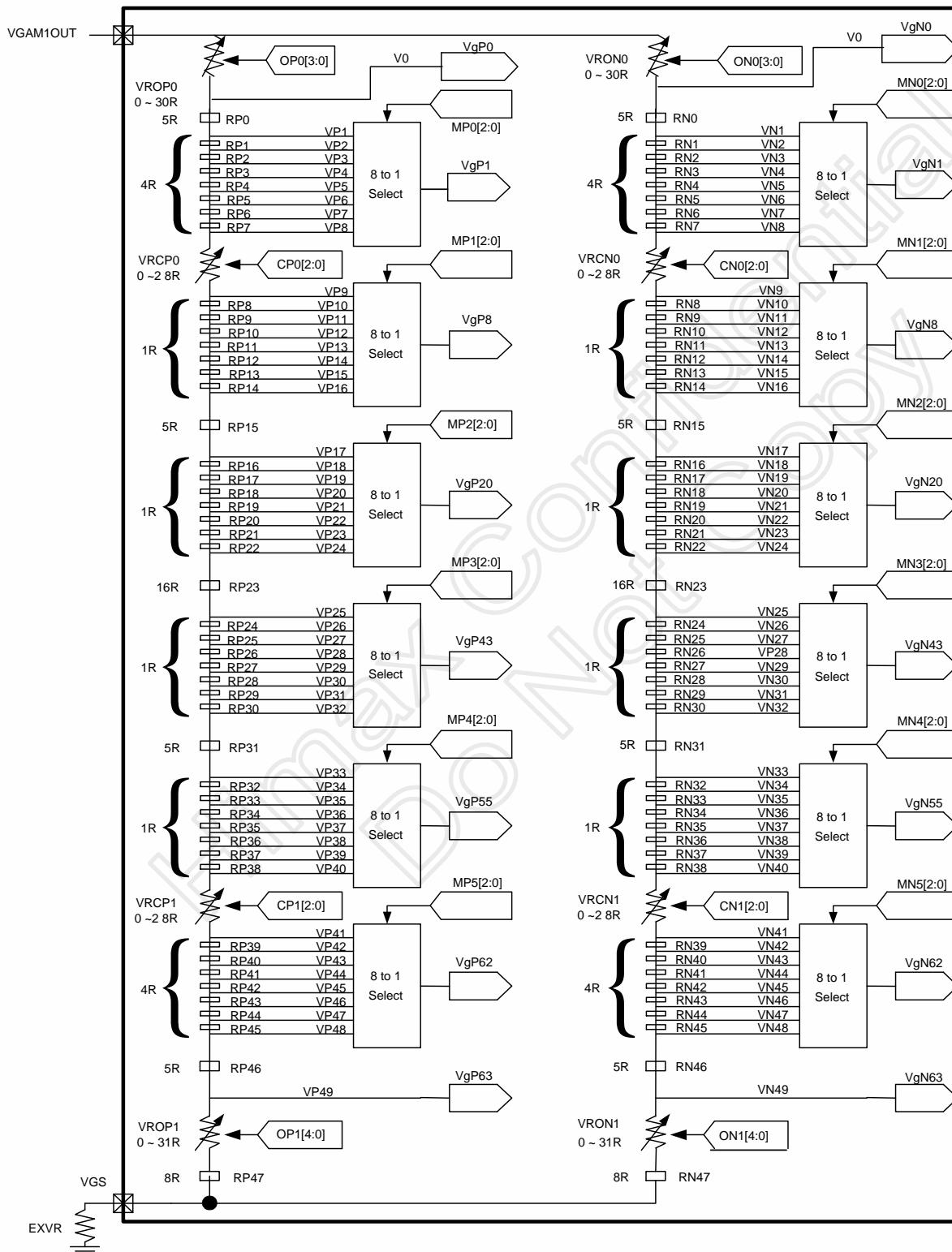


Figure 3.31 Gamma Resister Stream and Gamma Reference Voltage

## Variable resistor

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register O(P/N) 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
1101	26R
1110	28R
1111	30R

Table 3. 12 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
11101	29R
11110	30R
11111	31R

Table 3. 13 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 3. 14 Center Adjustment

## 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register M(P/N) 2-0	Voltage level					
	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 3. 15 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	-	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	VP28
	MP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	-	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R + VROP0+ VROP1+ VRCP0+ VRCP1;

SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1

VD=(VGAM1OUT-VGS)

[sumRPx (sumRN/ (sumRP+sumRN))]/ [sumRPxsumRN/ (sumRP+sumRN) +EXVR]

Table 3. 16 Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula
V0	VINP0
V1	VINP1
V2	$V8+(V1-V8)*(30/48)$
V3	$V8+(V1-V8)*(23/48)$
V4	$V8+(V1-V8)*(16/48)$
V5	$V8+(V1-V8)*(12/48)$
V6	$V8+(V1-V8)*(8/48)$
V7	$V8+(V1-V8)*(4/48)$
V8	VINP2
V9	$V20+(V8-V20)*(22/24)$
V10	$V20+(V8-V20)*(20/24)$
V11	$V20+(V8-V20)*(18/24)$
V12	$V20+(V8-V20)*(16/24)$
V13	$V20+(V8-V20)*(14/24)$
V14	$V20+(V8-V20)*(12/24)$
V15	$V20+(V8-V20)*(10/24)$
V16	$V20+(V8-V20)*(8/24)$
V17	$V20+(V8-V20)*(6/24)$
V18	$V20+(V8-V20)*(4/24)$
V19	$V20+(V8-V20)*(2/24)$
V20	VINP3
V21	$V43+(V20-V43)*(22/23)$
V22	$V43+(V20-V43)*(21/23)$
V23	$V43+(V20-V43)*(20/23)$
V24	$V43+(V20-V43)*(19/23)$
V25	$V43+(V20-V43)*(18/23)$
V26	$V43+(V20-V43)*(17/23)$
V27	$V43+(V20-V43)*(16/23)$
V28	$V43+(V20-V43)*(15/23)$
V29	$V43+(V20-V43)*(14/23)$
V30	$V43+(V20-V43)*(13/23)$
V31	$V43+(V20-V43)*(12/23)$
V32	$V43+(V20-V43)*(11/23)$
V33	$V43+(V20-V43)*(10/23)$
V34	$V43+(V20-V43)*(9/23)$
V35	$V43+(V20-V43)*(8/23)$
V36	$V43+(V20-V43)*(7/23)$
V37	$V43+(V20-V43)*(6/23)$
V38	$V43+(V20-V43)*(5/23)$
V39	$V43+(V20-V43)*(4/23)$
V40	$V43+(V20-V43)*(3/23)$
V41	$V43+(V20-V43)*(2/23)$
V42	$V43+(V20-V43)*(1/23)$
V43	VINP4
V44	$V55+(V43-V55)*(22/24)$
V45	$V55+(V43-V55)*(20/24)$
V46	$V55+(V43-V55)*(18/24)$
V47	$V55+(V43-V55)*(16/24)$
V48	$V55+(V43-V55)*(14/24)$
V49	$V55+(V43-V55)*(12/24)$
V50	$V55+(V43-V55)*(10/24)$
V51	$V55+(V43-V55)*(8/24)$
V52	$V55+(V43-V55)*(6/24)$
V53	$V55+(V43-V55)*(4/24)$
V54	$V55+(V43-V55)*(2/24)$
V55	VINP5
V56	$V62+(V55-V62)*(44/48)$
V57	$V62+(V55-V62)*(40/48)$
V58	$V62+(V55-V62)*(36/48)$
V59	$V62+(V55-V62)*(32/48)$
V60	$V62+(V55-V62)*(25/48)$
V61	$V62+(V55-V62)*(18/48)$
V62	VINP6
V63	VINP7

Table 3. 17 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VGAM1OUT-VD*VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VGAM1OUT-VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VGAM1OUT-VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VGAM1OUT-VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VGAM1OUT-VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VGAM1OUT-VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VGAM1OUT-VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VGAM1OUT-VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VGAM1OUT-VD((VRON0+33R) /sumRN	VN8
	MN1 2-0=000	VGAM1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
VgN8	MN1 2-0=001	VGAM1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VGAM1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VGAM1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VGAM1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VGAM1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VGAM1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VGAM1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
	MN2 2-0=000	VGAM1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VGAM1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
VgN20	MN2 2-0=010	VGAM1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VGAM1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VGAM1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VGAM1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VGAM1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VGAM1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
	MN3 2-0=000	VGAM1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VGAM1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VGAM1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
VgN43	MN3 2-0=011	VGAM1OUT-VD((VRON0+71R+VRCN0) /sumRN	VNP8
	MN3 2-0=100	VGAM1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VGAM1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VGAM1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VGAM1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
	MN4 2-0=000	VGAM1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VGAM1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VGAM1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VGAM1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
VgN55	MN4 2-0=100	VGAM1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VGAM1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VGAM1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VGAM1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
	MN5 2-0=000	VGAM1OUT-VD((VRON0+87R+VRCN0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VGAM1OUT-VD((VRON0+91R+VRCN0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VGAM1OUT-VD((VRON0+95R+VRCN0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VGAM1OUT-VD((VRON0+99R+VRCN0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VGAM1OUT-VD((VRON0+103R+VRCN0+VRCN1) /sumRN	VN45
VgN62	MN5 2-0=101	VGAM1OUT-VD((VRON0+107R+VRCN0+VRCN1) /sumRN	VN46
	MN5 2-0=110	VGAM1OUT-VD((VRON0+111R+VRCN0+VRCN1) /sumRN	VN47
	MN5 2-0=111	VGAM1OUT-VD((VRON0+115R+VRCN0+VRCN1) /sumRN	VN48
	VgN63	-	VGAM1OUT-VD((VRON0+120R+VRCN0+VRCN1) /sumRN

SumRP = 128R + VRP0+ VRP1+ VRCP0+ VRCP1;

SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1

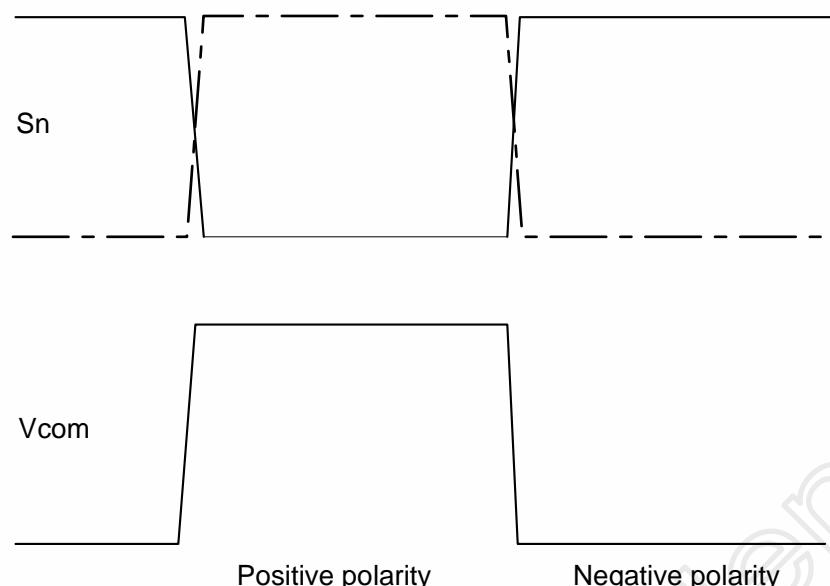
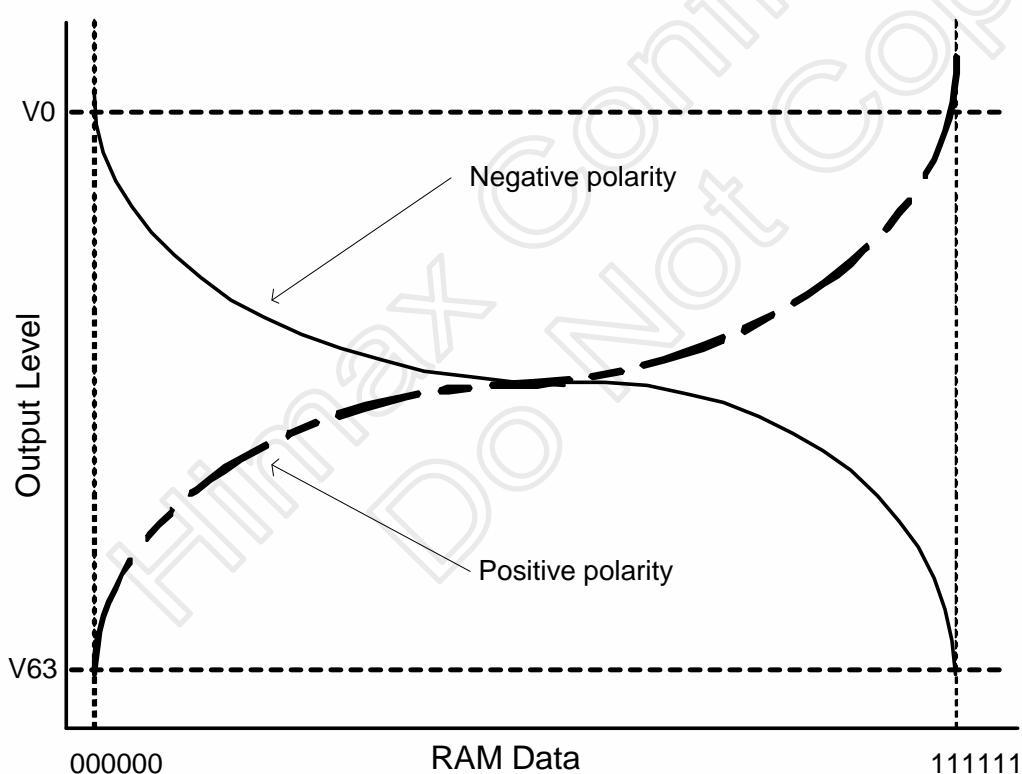
VD = (VGAM1OUT-VGS)

[sumRP(sumRN/(sumRP+sumRN))]/[ sumRP(sumRN/(sumRP+sumRN)+EXVR)

**Table 3. 18 Voltage Calculation Formula (Negative Polarity)**

Grayscale Voltage	Formula
V0	VINN0
V1	VINN1
V2	$V8+(V1-V8)*(30/48)$
V3	$V8+(V1-V8)*(23/48)$
V4	$V8+(V1-V8)*(16/48)$
V5	$V8+(V1-V8)*(12/48)$
V6	$V8+(V1-V8)*(8/48)$
V7	$V8+(V1-V8)*(4/48)$
V8	VINN2
V9	$V20+(V8-V20)*(22/24)$
V10	$V20+(V8-V20)*(20/24)$
V11	$V20+(V8-V20)*(18/24)$
V12	$V20+(V8-V20)*(16/24)$
V13	$V20+(V8-V20)*(14/24)$
V14	$V20+(V8-V20)*(12/24)$
V15	$V20+(V8-V20)*(10/24)$
V16	$V20+(V8-V20)*(8/24)$
V17	$V20+(V8-V20)*(6/24)$
V18	$V20+(V8-V20)*(4/24)$
V19	$V20+(V8-V20)*(2/24)$
V20	VINN3
V21	$V43+(V20-V43)*(22/23)$
V22	$V43+(V20-V43)*(21/23)$
V23	$V43+(V20-V43)*(20/23)$
V24	$V43+(V20-V43)*(19/23)$
V25	$V43+(V20-V43)*(18/23)$
V26	$V43+(V20-V43)*(17/23)$
V27	$V43+(V20-V43)*(16/23)$
V28	$V43+(V20-V43)*(15/23)$
V29	$V43+(V20-V43)*(14/23)$
V30	$V43+(V20-V43)*(13/23)$
V31	$V43+(V20-V43)*(12/23)$
V32	$V43+(V20-V43)*(11/23)$
V33	$V43+(V20-V43)*(10/23)$
V34	$V43+(V20-V43)*(9/23)$
V35	$V43+(V20-V43)*(8/23)$
V36	$V43+(V20-V43)*(7/23)$
V37	$V43+(V20-V43)*(6/23)$
V38	$V43+(V20-V43)*(5/23)$
V39	$V43+(V20-V43)*(4/23)$
V40	$V43+(V20-V43)*(3/23)$
V41	$V43+(V20-V43)*(2/23)$
V42	$V43+(V20-V43)*(1/23)$
V43	VINN4
V44	$V55+(V43-V55)*(22/24)$
V45	$V55+(V43-V55)*(20/24)$
V46	$V55+(V43-V55)*(18/24)$
V47	$V55+(V43-V55)*(16/24)$
V48	$V55+(V43-V55)*(14/24)$
V49	$V55+(V43-V55)*(12/24)$
V50	$V55+(V43-V55)*(10/24)$
V51	$V55+(V43-V55)*(8/24)$
V52	$V55+(V43-V55)*(6/24)$
V53	$V55+(V43-V55)*(4/24)$
V54	$V55+(V43-V55)*(2/24)$
V55	VINN5
V56	$V62+(V55-V62)*(44/48)$
V57	$V62+(V55-V62)*(40/48)$
V58	$V62+(V55-V62)*(36/48)$
V59	$V62+(V55-V62)*(32/48)$
V60	$V62+(V55-V62)*(25/48)$
V61	$V62+(V55-V62)*(18/48)$
V62	VINN6
V63	VINN7

Table 3. 19 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

**Relationship between GRAM Data and Output Level (REV = "0")**

**Figure 3.32 Relationship between Source Output and Vcom**


(Same characteristic for each RGB)

**Figure 3.33 Relationship between GRAM Data and Output Level**

### 3.6 Oscillator

The HX8309-A can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor (Rf). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases.

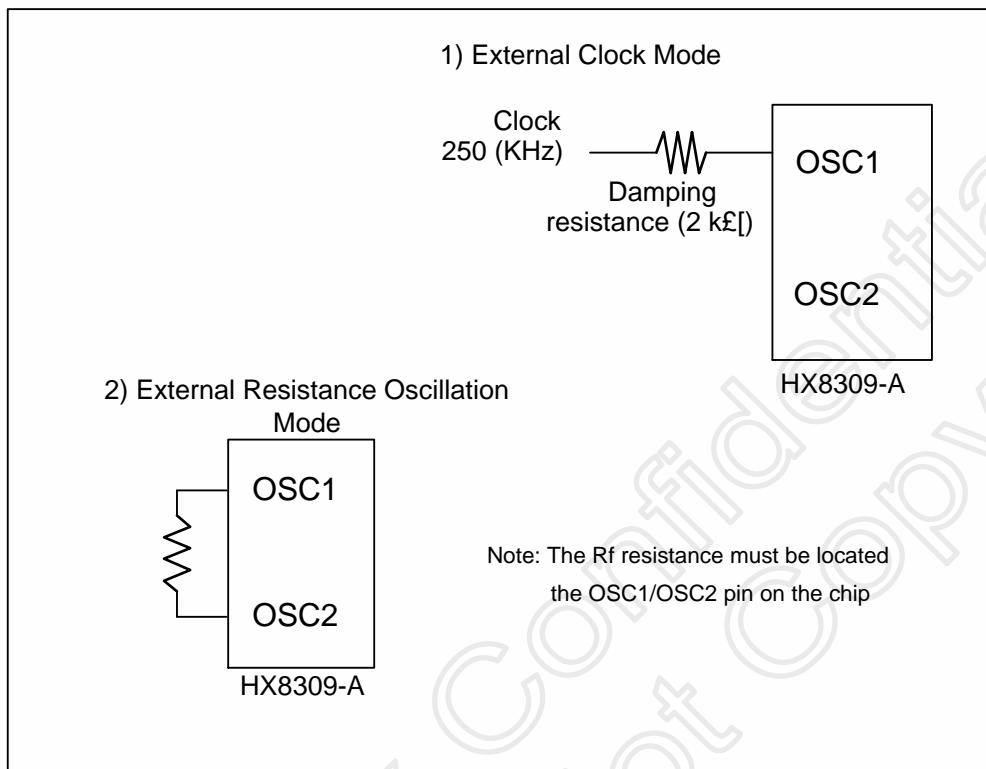


Figure 3.34 Oscillation Circuit

External Resistance (Rf)	R-C Oscillation Frequency : fosc (KHz)		
	Vcc = 2.4V	Vcc = 3V	Vcc = 3.3V
110KΩ	387	427	444
150 KΩ	290	318	329
180 KΩ	246	269	281
200 KΩ	194	211	217
240 KΩ	160	173	179
270 KΩ	142	153	157
300 KΩ	125	134	139
390 KΩ	88	93	95
430 KΩ	79	83	85

Table 3.20 External Resistance Value and R-C Oscillation Frequency (Temporally Define)

## 4. Introduction

The HX8309-A is a single chip with 18-bit bus architecture. When data read from/write to internal GRAM through the 18-bit data format. When the internal operation of the HX8309-A wants to start, first send the control information, which is temporarily stored in the registers, described as below to allow high-speed interface with a high-performance MPU. The internal operation of the HX8309-A is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17-0), control the HX8309-A register.

There are nine categories of registers that follows:

- Select the index
- Read back the status
- Control the display functions
- Control power management and save power function
- Process or operate the graphics data
- Set internal GRAM addresses for partial data updating
- Transfer data to and from the internal GRAM with High Speed Function
- Set grayscale level for the internal embedded grayscale gamma adjustment

The following specify the explanation of registers such as register format and bit function.

Register No.	Register	R/W	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
IR	Index	W	0	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0		
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0		
R00h	Oscillation Start	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
R01h	Device Code Read	R	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	
R02h	Driver Output Control	W	1	0	VSP1 (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (1)	NL0 (1)	
R03h	LCD AC driving Control	W	1	0	0	0	0	FLD (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	
R04h	Entry Mode	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	HWM (0)	0	0	0	I/D1 (1)	I/D0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
R05h	Compare Register (1)	W	1	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	0	OP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	
R06h	Compare Register (2)	W	1	0	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	C/L (0)	REV (0)	D1 (0)	
R07h	Display Control (1)	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
R08h	Display Control (2)	W	1	0	0	0	0	0	0	0	0	0	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	
R09h	Display Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
R0Bh	Frame Cycle Adjustment Control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1 (0)	CE0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
R0Ch	External Display Interface Control	W	1	0	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
R10h	Power Control (1)	W	1	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	AP2 (0)	AP1 (0)	AP0 (0)	0	DK (1)	SLP (0)	STB (0)	
R11h	Power Control (2)	W	1	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VO0 (0)	
R12h	Power Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
R13h	Power Control (4)	W	1	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
R21h	RAM Address Set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
R22h	RAM data Write/Read	W	1	RAM WD17-0 / RAM (RD17-0)																
R23h	RAM Write Data Mask (1)	W	1	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R24h	RAM Write Data Mask (2)	W	1	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
R30h	r Control (1)	W	1	0	0	0	0	0	MP12 (0)	MP11 (0)	MP10 (0)	0	0	0	0	0	MP02 (0)	MP01 (0)	MP00 (0)	
R31h	r Control (2)	W	1	0	0	0	0	0	MP32 (0)	MP31 (0)	MP30 (0)	0	0	0	0	0	MP22 (0)	MP21 (0)	MP20 (0)	
R32h	r Control (3)	W	1	0	0	0	0	0	MP52 (0)	MP51 (0)	MP50 (0)	0	0	0	0	0	MP42 (0)	MP41 (0)	MP40 (0)	
R33h	r Control (4)	W	1	0	0	0	0	0	CP12 (0)	CP11 (0)	CP10 (0)	0	0	0	0	0	CP02 (0)	CP01 (0)	CP00 (0)	
R34h	r Control (5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)	
R35h	r Control (6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)	
R36h	r Control (7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)	
R37h	r Control (8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)	
R38h	r Control (9)	W	1	0	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)				OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)	
R39h	r Control (10)	W	1	0	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)				ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)	
R40h	Gate Scan Start Position	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
R41h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL0 (0)	
R42h	First Screen Driving Position	W	1	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	
R43h	Second Screen Driving Position	W	1	SE27 (1)	SE26 (1)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (0)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
R44h	Horizontal RAM Address Position	W	1	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
R45h	Vertical RAM Address Position	W	1	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	

Table 4.1 List Table of Register Set

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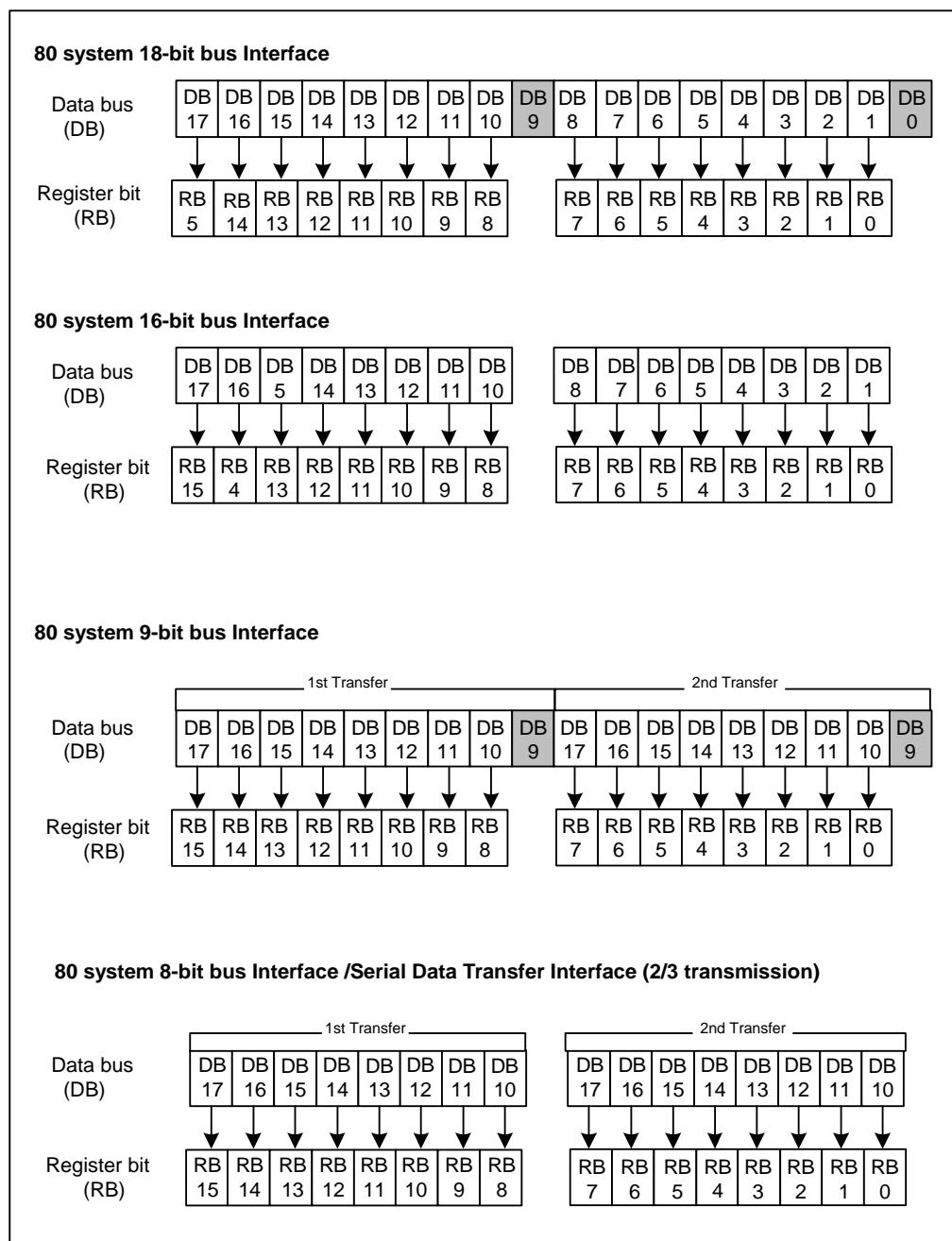


Figure 4. 1 80-System Interface Mode

## 4.1 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 4. 2 Index Register

Index register (IR) specifies Index of the register from R00h to R4Fh. It sets the register number (ID6-0) in the range from 000000b to 1111111b in binary form.

## 4.2 Status Read Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	

Figure 4. 3 Status Read Register

Status Read Register for reading the internal status of the HX8309-A.

**L7–0:** Indicate the position of driving line, where the liquid crystal display is driven at present.

## 4.3 Start Oscillation Register (R00h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1

Figure 4. 4 Start Oscillation Register (R00h)

Start Oscillation Register restarts the oscillator from the suspend state at the standby mode. After setting this register, and wait at least 10 ms for oscillation stabilizing before setting the next register.

When the read command is issued, 8309h is read.

## 4.4 Driver Output Control Register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 4. 5 Driver Output Control Register (R01h)

**NL4–0:** Specify the number of scan lines for the LCD driver can be adjusted by every 8 lines. Select the setting value for the panel size or higher.

NL4	NL3	NL2	NL1	NL0	Gate Driver Used	Number of Scan Line	Display Size
0	0	0	0	0	Ignore	Ignore	Ignore
0	0	0	0	1	G1~G16	16	528*16 dots
0	0	0	1	0	G1~G24	24	528*24dots
0	0	0	1	1	G1~G32	32	528*32 dots
0	0	1	0	0	G1~G40	40	528*40 dots
0	0	1	0	1	G1~G48	48	528*48dots
0	0	1	1	0	G1~G56	56	528*56 dots
0	0	1	1	1	G1~G64	64	528*64 dots
0	1	0	0	1	G1~G72	72	528*72 dots
:	:	:	:	:	:	:	:
1	1	0	0	0	G1~G200	200	528*200 dots
1	1	0	0	1	G1~G208	208	528*208 dots
1	1	0	1	0	G1~G216	216	528*216 dots
1	1	0	1	1	G1~G220	220	528*220 dots
1	1	1	0	0	G1~G220	220	528*220 dots
1	1	1	0	1	G1~G220	220	528*220 dots
1	1	1	1	0	G1~G220	220	528*220 dots
1	1	1	1	1	G1~G220	220	528*220 dots

**Table 4. 2 NL bits and Scan Line**

**SS:** The source driver output shift direction selected. The shift direction from S1 to S528 when SS = 0. And shift direction from S528 to S1 when SS = 1. And if the BGR = 0, <R><G><B> color is assigned from S1. When SS = 1 and BGR = 1, <R><G><B> color is assigned from S528. Re-write to the GRAM after changed the SS bit or BGR bit.

**GS:** Specify the shift direction of gate driver output. When GS = 0, the shift direction from G1 to G220. When GS = 1, the shift direction from G220 to G1.

**SM:** Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

**EPL:** Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to PD17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to PD17-0

**Table 4. 3 EPL Bit and Enable Pin**

**VSPL:** The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

**HSPL:** The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

**DPL:** The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

#### 4.5 LCD Driving Waveform Register (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 4. 6 LCD-Driving-Waveform Control Register (R02h)

**NW5–0:** Specify the number of n lines that will alternate POL signal when B/C = 1. The inversion is occurred every n + 1 line, and the 1st to the 64th lines can be selected.

**EOR:** EOR=1 will force POL signal alternate at the beginning of a frame in n-line inversion driving mode (B/C=1), no matter the last interval of POL signal is over or not in last frame. Therefore, EOR bit is used when the POL signal is not completely alternated in some number of drive lines in LCD display area. For details, see the “N-line Inversion LCD Drive” section.

**B/C:** When B/C = 0, POL signal alternates in every frame for LCD drive. When B/C = 1, POL signal alternates in each n line specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “N-line Inversion LCD Drive” section.

**FLD1–0:** Set the number of n field for interlaced driving mode. For details, see the “Interlaced driving function section”.

FLD1	FLD0	Number of field
0	0	Ignore
0	1	1 field
1	0	Ignore
1	1	3 fields

Table 4. 4 FLD Bits and Interlaced Field

#### 4.6 Entry Mode Register (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM1	DFM0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0

Figure 4. 7 Entry Mode Register (R03h)

**LG2–0:** The compare operation. The data is read from the GRAM by the MPU and is compared with the compare registers (CP17–0) by a compare operation, then write the results to GRAM. For details, see the “Graphics Operation Function section”.

**AM:** The updating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D [1..0].

**I/D[1..0]:** The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the update method with I/D1-0 & AM bit.

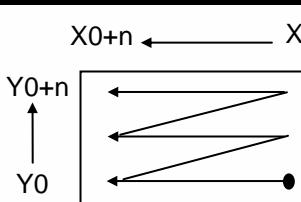
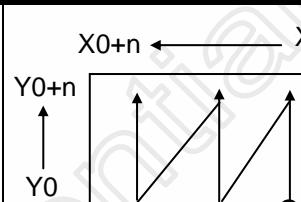
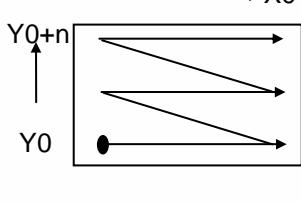
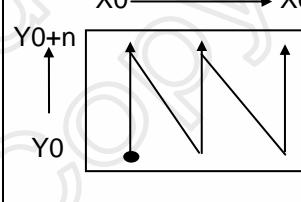
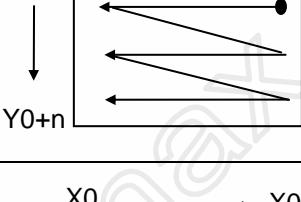
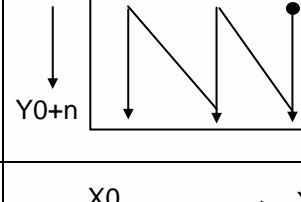
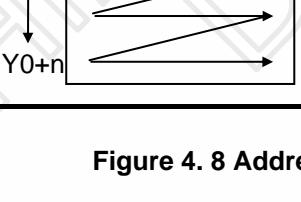
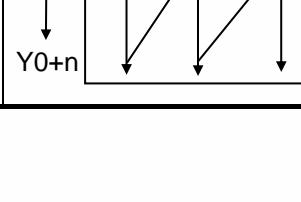
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			0	0	
		1				1	

Figure 4. 8 Address Direction Settings

**HWM:** When HWM=1 (high-speed write mode), four words are written to GRAM in one time. If write operations are terminated less than four times, the last data will not be written.

**BGR:** The order of <R><G><B> dot color. When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order. Setting BGR will change the bit order of (CP17-0) and (WM17-0) in the same way.

**TRI:** When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus interface. When TRI=0, 8-bit bus interface mode is unselected.

**DFM1-0:** Specify the data format when TRI=1, for 8-bit bus interface or serial data transfer interface. DFM1-0=10, 262K color mode. DFM1-0=11, 65K color mode.

DFM1	DFM0	TRI	16-bit interface RAM write data transfer
0	0	0	80-system 16-bit interface (1 transfer/pixel) 65536 colors Available 
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	80-system 16-bit interface MSB mode (2 transfers/pixel) 262,144 colors Available 
1	1	1	80-system 16-bit interface LSB mode (2 transfers/pixel) 65,536 colors Available 

Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

**Figure 4. 9 The Setting of DFM and TRI (80-system 16-bit Interface)**

DFM1	DFM0	TRI	8-bit interface RAM write data transfer
0	0	0	80-system 8-bit interface (2 transfers/pixel) 65,536 colors Available 
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	80-system 8-bit interface (3 transfers/pixel) 262,144 colors Available 
1	1	1	80-system 8-bit interface (3 transfers/pixel) 65,536 colors Available 

Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

**Figure 4. 10 The Setting of DFM and TRI (80-system 8-bit Interface)**

DFM1	DFM0	TRI	Serial Data Transfer Interface RAM write data transfer
0	0	0	Serial Data Transfer (2 transfers/pixel) 65536 colors Available 
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	Serial Data Transfer (3 transfers/pixel) 262,144 colors Available 
1	1	1	Ignore

Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

**Figure 4. 11 The Setting of DFM and TRI (Serial Data Transfer Interface)**

## 4.7 Compare Register Set

The written date is sent from the microprocessor and modified in the HX8309-A, then written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the MPU software processing. For details, see the Graphics Operation Function section.

### 4.7.1 Compare Register 1 (R04h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0

Figure 4. 12 Compare Register 1 (R04h)

### 4.7.2 Compare Register 2 (R05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

Figure 4. 13 Compare Register 2 (R05h)

**CP17-0:** The values of compare register for the compare operation with the data read from the GRAM or written from the MPU.

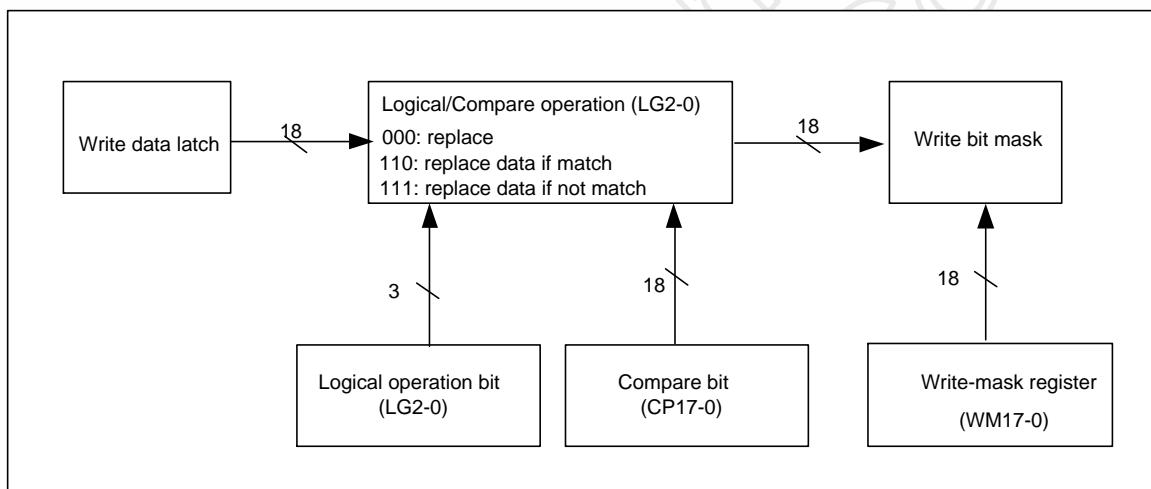


Figure 4. 14 Bit Operation

## 4.8 Display Control Register Set

### 4.8.1 Display Control Register 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	PT2	PT1	PT0	VLE2	VLE1	SPT	0	1	GON	DTE	CL	REV	D1	D0

Figure 4. 15 Display Control Register 1 (R07h)

**D1-0:** When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8309-A can control the charging current for the LCD with AC driving.

Control the display on/off while control GON and DTE. When D1-0 = 01, the internal display of the HX8309-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	Source Output	HX8309-A Internal Display Operations	Gate-Driver Control Signals (CPV, FLM, M) (CPV, STV, POL)
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

Note: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

Table 4. 5 D Bits and Operation

**REV:** REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

REV		Source output level								
		GRAM data		Display area		Non-display area				
				Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity	Positive Polarity
0	18'h00000	V63	V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z	
	18'h3FFFF	V0	V63							
1	18'h00000	V0	V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z	
	18'h3FFFF	V63	V0							

Table 4. 6 Display Control Instruction

**CL:** CL = 1, the display mode is set to the 8-color display mode. For details, see the section on the 8-color display mode section.

CL	Number of Display Colors
0	262,144
1	8

Note: The display 262,144 colors when 18/9 bit bus interface is using, and display 65,536 colors when 16/8 bit bus interface is using.

**Table 4. 7 CL Bit for 8-Color Display**

**DTE, GON:** Specify the output level of gate line. Vcom level is VSSD when GON = 0.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Note: GON bit is used in the gate driver. Control according to the bits' values is executed by the gate driver.  
For details, see the data sheet of the gate driver.

**Table 4. 8 GON and DTE Bits**

**SPT:** When SPT = 1, the 2-division LCD drive is performed so a LCD can be divided 2 split display windows. For details, see the Partial Screen Display Function section.

**VLE2-1:** When VLE1 = 1, a vertical scroll is performed in the 1st display window.  
When VLE2 = 1, a vertical scroll is performed in the 2nd display window.  
Vertical scrolling on the two windows cannot be controlled at the same time.

VLE2	VLE1	1st Display Window	2nd Display Window
0	0	Fixed display	Fixed display
0	1	Scrolled display	Fixed display
1	0	Fixed display	Scrolled display
1	1	Ignore	Ignore

**Table 4. 9 VLE Bits**

**PT1-0:** When partial display is in use, these bits determine the source output in the non-display area. For details, see the Partial Screen Display Function section. The output on the source lines during the periods of the front and BP are also determined by PT1-0.

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	Vcom output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VcomH↔VcomL
0	1	Ignore	Ignore	Reference to PTG1-0	VcomH↔VcomL
1	0	VSSD	VSSD	Reference to PTG1-0	VcomH↔VcomL
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

**Table 4. 10 PT Bits for Source and Gate Output in Non-Display Area of Partial Display**

#### 4.8.2 Display Control Register 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0	

**Figure 4. 16 Display Control Register 2 (R08h)**

**BP3-0:** Specify the amount of scan line for back porch (BP).

**FP3-0:** Specify the amount of scan line for front porch (FP).

The setting vale, ensure that:

**BP + FP ≤ 16 lines**

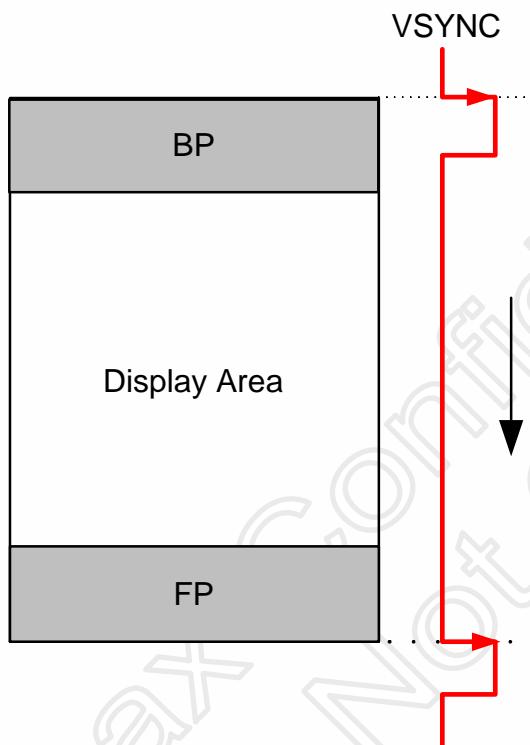
**PB ≥ 2 lines**

**FP ≥ 2 lines**

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by he display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

FP3	FP2	FP1	FP0	Number of FP Line	Number of BP Line
BP3	BP2	BP1	BP0		
0	0	0	0		Ignore
0	0	0	1		Ignore
0	0	1	0		2 lines
0	0	1	1		3 lines
:	:	:	:		:
1	1	0	1		13 lines
1	1	1	0		14 lines
1	1	1	1		Ignore

Table 4. 11 BP/FP Bits Setting



Note: The output signal is delay 2 lines timing from the VSYNC to the LCD

Figure 4. 17 BP/FP

Operation Mode	Number of Interlace Scan Field	BP	FP	BP + FP
System Interface	FLD1-0 = 01	$\geq 2$ lines	$\geq 2$ lines	$\leq 16$ lines
	FLD1-0 = 11	3 lines	5 lines	-
RGB Interface	-	$\geq 2$ lines	$\geq 2$ lines	$\leq 16$ lines
VSYNC Interface	-	$\geq 2$ lines	$\geq 2$ lines	16 lines

Table 4. 12 BP3-0, FP3-0 Setting Dependent on Operation Mode

#### 4.8.3 Display Control Register 3 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

Figure 4. 18 Display Control Register 3 (R09h)

**PTG1-0:** Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

Table 4. 13 PTG Bits Setting

**ISC3-0:** Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f <sub>FLM</sub> = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	43 ms
0	0	1	0	5 frames	71 ms
0	0	1	1	7 frames	100 ms
0	1	0	0	9 frames	129 ms
0	1	0	1	11 frames	157 ms
0	1	1	0	13 frames	186 ms
0	1	1	1	15 frames	214 ms
1	0	0	0	17 frames	243 ms
1	0	0	1	19 frames	271 ms
1	0	1	0	21 frames	300 ms
1	0	1	1	23 frames	329 ms
1	1	0	0	25 frames	357 ms
1	1	0	1	27 frames	386 ms
1	1	1	0	29 frames	414 ms
1	1	1	1	31 frames	443 ms

Table 4. 14 ISC Bit2 Setting

#### 4.9 Frame Cycle Control Register (R0Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GD1	GD0	SDT1	SDT0	CE1	CE0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 4. 19 Frame Cycle Control Register (R0Bh)

**RTN3-0:** Set the 1-line period in a clock unit.

Clock cycles=1/internal operation clock frequency

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Line
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
:	:	:	:	:
1	1	0	1	29
1	1	1	0	30
1	1	1	1	31

Table 4. 15 RTN Bits and Clock Cycles

**DIV1-0:** The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Table 4. 16 DIV Bits and Clock Frequency

#### Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL}+\text{BP}+\text{FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency

RTN bit: Clocks per line

DIV bit: Division ratio

NL: The number of lines

FP: Number of lines for front porch

BP: Number of lines for back porch

BP+FP  $\leq$  16

**CE1-0:** CE period can be set with CE1-0.

CE1	CE 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock cycle	8 clock cycles
1	0	2 clock cycles	16 clock cycles
1	1	3 clock cycles	24 clock cycles

Table 4. 17 CE Bits for Equalized Period

**SDT1-0:** Set delay amount from falling edge of the gate output signal for the source outputs.

SDT1	SDT0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	1 clock cycle	8 clock cycles
0	1	2 clock cycles	16 clock cycles
1	0	3 clock cycles	24 clock cycles
1	1	4 clock cycles	32 clock cycles

Table 4. 18 SDT Bits for Source Output Delay

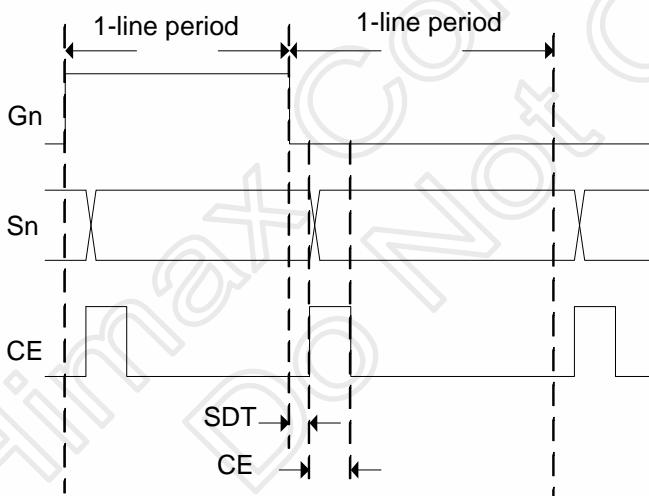


Figure 4. 20 Equalized Period and Source Output Delay

**GD1-0:** Set amount of non-overlap for the gate output.

GD1	GD0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (source clock: DOTCLK)
0	0	0 clock cycle	0 clock cycle
0	1	4 clock cycle s	32 clock cycle s
1	0	6 clock cycle s	48 clock cycle s
1	1	8 clock cycle s	64 clock cycle s

Table 4. 19 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulses

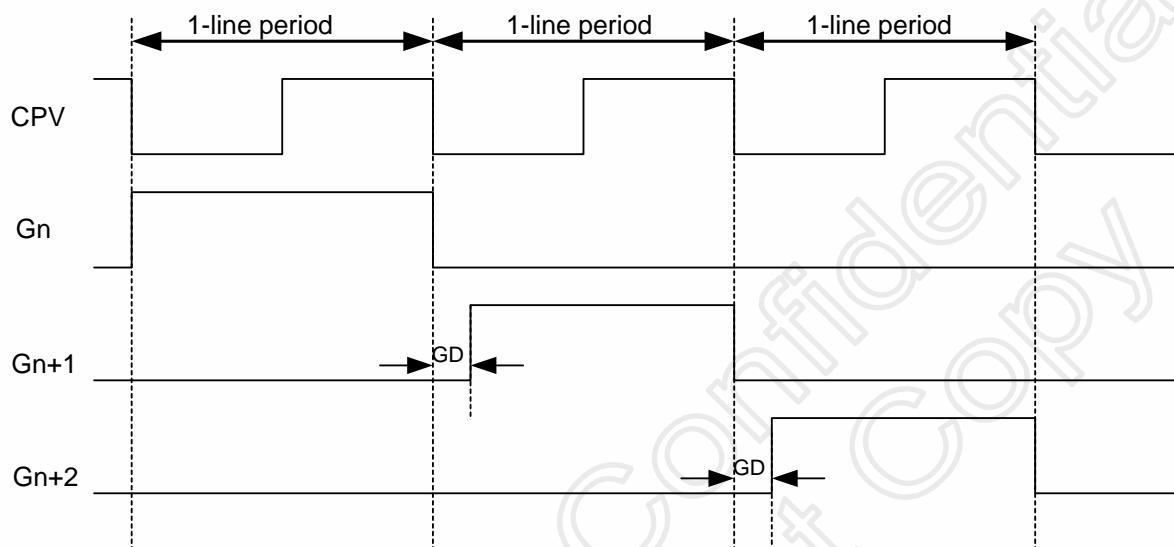


Figure 4. 21 Non-overlap Time between Two Adjacent Gate Output Pulses

Interface mode	Clock Source
System interface mode	R-C oscillator
RGB interface mode	DOTCLK
VSYNC interface mode	R-C oscillator

Table 4. 20 Clock Source for Interface Mode

#### 4.10 External Display Interface Control Register (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0	

Figure 4. 22 External Display Interface Control Register (R0Ch)

**RIM1-0:** Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode (1 transfer/pixel)
0	1	16-bit bus RGB interface Mode (1 transfer/pixel)
1	0	6-bit bus RGB interface Mode (3 transfers/pixel)
1	1	Ignore

**Table 4. 21 RIM Bits for Transfer Mode of RGB interface**

**DM1-0:** Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

**Table 4. 22 DM Bits for Operation Mode of LCD display**

**RM:** Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	-System interface -VSYNC interface
1	RGB interface

Note: the register is set only through the system interface.

Note: A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

**Table 4. 23 RM Bit for Access Interface of GRAM**

## 4.11 Power Control Register Set

### 4.11.1 Power Control Register 1 (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	SAP2	SAP1	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB

**Figure 4. 23 Power Control Register 1 (R10h)**

**STB:** When STB = "1", the HX8309-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. Anyway, have not any external clock are supplied. During the standby mode, only the following process can be executed.

- a. Exit the Standby mode (STB = "0")
- b. Start the oscillation

Within the standby mode, the GRAM data and register content may be lost. For preventing this, they have to set again after the standby mode is exited.

**SLP:** When SLP = 1, the HX8309-A enters the sleep mode, where the internal display operations are suspended except for the R-C oscillator, thus the current consumption can be reduced. Within the sleep mode, the GRAM data and register content cannot be accessed although they are retained.

**DK:** ON/OFF the operation of step-up circuit 1. When power on, the VLCDC no output until VGHC is set up completely. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

Table 4. 24 DK Bit for Operation of Step-up Circuit 1

**AP2-0:** Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff. Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP2-0 = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	Ignore
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

Table 4. 25 AP Bits and Amount of Current in Operational Amplifier

**BT2-0:** Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x Vci1	-1 x Vci1	6 x Vci1	-5 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B, C22 A/B
0	0	1	2 x Vci1	-1 x Vci1	6 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	0	2 x Vci1	-1 x Vci1	6 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	1	2 x Vci1	-1 x Vci1	5 x Vci1	-5 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	0	2 x Vci1	-1 x Vci1	5 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	1	2 x Vci1	-1 x Vci1	5 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	0	2 x Vci1	-1 x Vci1	4 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	2 x Vci1	-1 x Vci1	4 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B

Note: The factors of step-up for VGH are derived from Vci1 when VLCD and Vci2 are shorted. The conditions of VLCD  $\leq$  5.5V, VCL  $\leq$  -3.3V, VGH  $\leq$  16.5V, and VGL  $\leq$  -16.5V must be satisfied.

Table 4. 26 BT Bits and VLCD and VGH Outputs

**SAP2-0:** Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP2-0 = 000, the current consumption can be reduced by stopping the operational amplifier.

SAP2			SAP1			SAP0			Fixed Current of Operational Amplifier								
0	0	0	Stop														
0	0	1	Ignore														
0	1	0	0.62														
0	1	1	0.71														
1	0	0	1														
1	0	1	1.25														
1	1	0	1.43														
1	1	1	Ignore														

Table 4. 27 SAP Bits and Amount of Current in Operational Amplifier

#### 4.11.2 Power Control Register 2 (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0	

Figure 4. 24 Power Control Register 2 (R11h)

**VC2-0:** Set the reference voltage of VGAM1OUT and Vci1 by adjusting the rate of Vci.

VC2	VC1	VC0	Internal reference voltage (REGP) of VGM1OUT and Vci1
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	Ignore
1	1	1	Ignore

Table 4. 28 VC Settings and Internal Reference Voltage

**DC02–00:** Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1
0	0	0	fosc / 8
0	0	1	fosc / 16
0	1	0	fosc / 32
0	1	1	fosc / 64
1	0	0	fosc / 128
1	0	1	Ignore
1	1	0	Ignore
1	1	1	Ignore

Table 4. 29 Operation Frequency of Step-up Circuit 1

**DC12–10:** Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2
0	0	0	fosc / 16
0	0	1	fosc / 32
0	1	0	fosc / 64
0	1	1	fosc / 128
1	0	0	fosc / 256
1	0	1	Ignore
1	1	0	Ignore
1	1	1	Ignore

Note : Ensure that the operation frequency of step-up circuit 1  $\geq$  step-up circuit 2

Table 4. 30 Operation Frequency of Step-up Circuit 2

#### 4.11.3 Power Control Register 3 (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

Figure 4. 25 Power Control Register 3 (R12h)

**VRH3-0:** Set the magnification of amplification for VGAM1OUT voltage. (VCOM, reference voltage for grayscale voltage) It allows magnify the amplification of REGP from 1.33 to 1.9 times.

VRH3	VRH2	VRH1	VRH0	VGAM1OUT
0	0	0	0	REGP x 1.33
0	0	0	1	REGP x 1.45
0	0	1	0	REGP x 1.55
0	0	1	1	REGP x 1.65
0	1	0	0	REGP x 1.75
0	1	0	1	REGP x 1.80
0	1	1	0	REGP x 1.85
0	1	1	1	Stop
1	0	0	0	REGP x 1.90
1	0	0	1	Ignore
1	0	1	0	Ignore
1	0	1	1	Ignore
1	1	0	0	Ignore
1	1	0	1	Ignore
1	1	1	0	Ignore
1	1	1	1	Ignore

Table 4. 31 VRH Bits and VGAM1OUT Voltage

**PON:** ON/OFF the operation of step-up circuit 3. PON = 0 is to stop and PON = 1 to start operation.

#### 4.11.4 Power Control Register 4 (R13h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 4. 26 Power Control Register 4 (R13h)

**VCM4-0:** Set the VcomH voltage (voltage of higher side when Vcom is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VGAM1OUT voltage. When VCM4-0 = "11111", stop the internal volume adjustment and adjust the VcomH with external resistance from VcomR.

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	VGAM1OUT x 0.40
0	0	0	0	1	VGAM1OUT x 0.42
0	0	0	1	0	VGAM1OUT x 0.44
:	:	:	:	:	:
0	1	1	1	0	VGAM1OUT x 0.68
0	1	1	1	1	Stop the internal volume. VcomH can be adjusted from VcomR with a external VR (variable resister),
1	0	0	0	0	VGAM1OUT x 0.70
1	0	0	0	1	VGAM1OUT x 0.72
1	0	0	1	0	VGAM1OUT x 0.74
:	:	:	:	:	:
1	1	1	0	0	VGAM1OUT x 0.94
1	1	1	0	1	VGAM1OUT x 0.96
1	1	1	1	0	VGAM1OUT x 0.98
1	1	1	1	1	Stop the internal volume. VcomH can be adjusted from VcomR with a external VR (variable resister),

Note: Adjust VGAM1OUT and VCM4-0 so that the VcomH voltage is lower than VGAM1OUT.

**Table 4. 32 VCM4-0 Bits and VcomH Voltage**

**VDV4-0:** Sets the amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. It is possible to setup from 0.6 to 1.23 times of VGAM1OUT. When VCOMG = 0, the setup is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VGAM1OUT x 0.60
0	0	0	0	1	VGAM1OUT x 0.63
0	0	0	1	0	VGAM1OUT x 0.66
:	:	:	:	:	:
0	1	1	0	0	VGAM1OUT x 0.96
0	1	1	0	1	VGAM1OUT x 0.99
0	1	1	1	0	VGAM1OUT x 1.02
0	1	1	1	1	Inhibition
1	0	0	0	0	VGAM1OUT x 1.05
1	0	0	0	1	VGAM1OUT x 1.08
1	0	0	1	0	VGAM1OUT x 1.11
1	0	0	1	1	VGAM1OUT x 1.14
1	0	1	0	0	VGAM1OUT x 1.17
1	0	1	0	1	VGAM1OUT x 1.20
1	0	1	1	0	VGAM1OUT x 1.23
1	0	1	1	1	Inhibition
1	1	-	-	-	

Notes: Adjust VGAM1OUT and VDV4-0 so that the Vcom and Vgoff amplitudes are lower than 6.0V.

**Table 4. 33 VDV4-0 Bits and Vcom Amplitude**

**VCOMG:** When VCOMG = 1, VcomL voltage can output to negative voltage (1.0V ~ -Vci +0.5V). When VCOMG = 0, VcomL voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, when VCOMG = 0, setting of the VDV4-0 is invalid. In this case, adjustment of Vcom/Vgoff A/C amplitude must be adjusted with VcomH using VCM4-0.

#### 4.12 RAM Address Register (R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 4. 27 RAM Address Register (R21h)

**AD15–0:** Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

AD15-AD0	GRAM Setting
“0000” h – “00AF” h	Bitmap data for G1
“0100” h – “01AF” h	Bitmap data for G2
“0200” h – “02AF” h	Bitmap data for G3
:	:
“D900” h – “D9AF” h	Bitmap data for G218
“DA00” h – “DAAF” h	Bitmap data for G219
“DB00” h – “DBAF” h	Bitmap data for G220

Table 4. 34 GRAM Address Mapping

#### 4.13 Write Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
RGB-I/F mode:		PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
		WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 4. 28 Write Data Register (R22h)

**WD17– 0:** Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

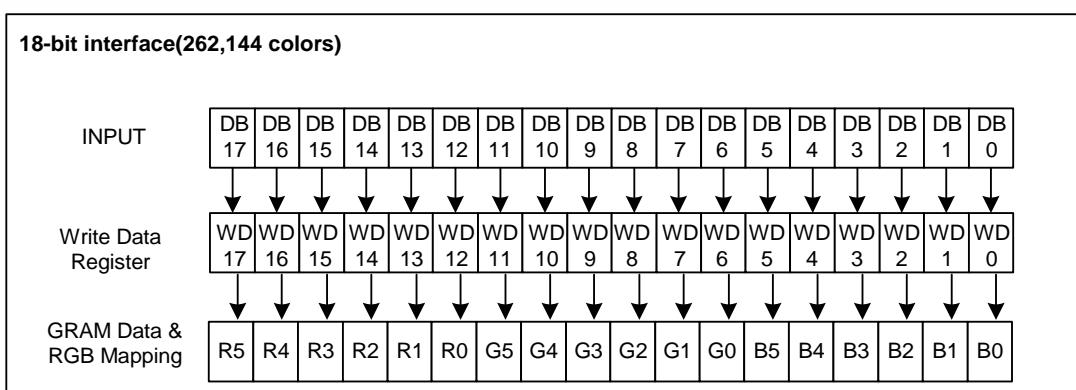


Figure 4. 29 Input Data Written to GRAM through Write Data Register in 18-bit Interface Mode

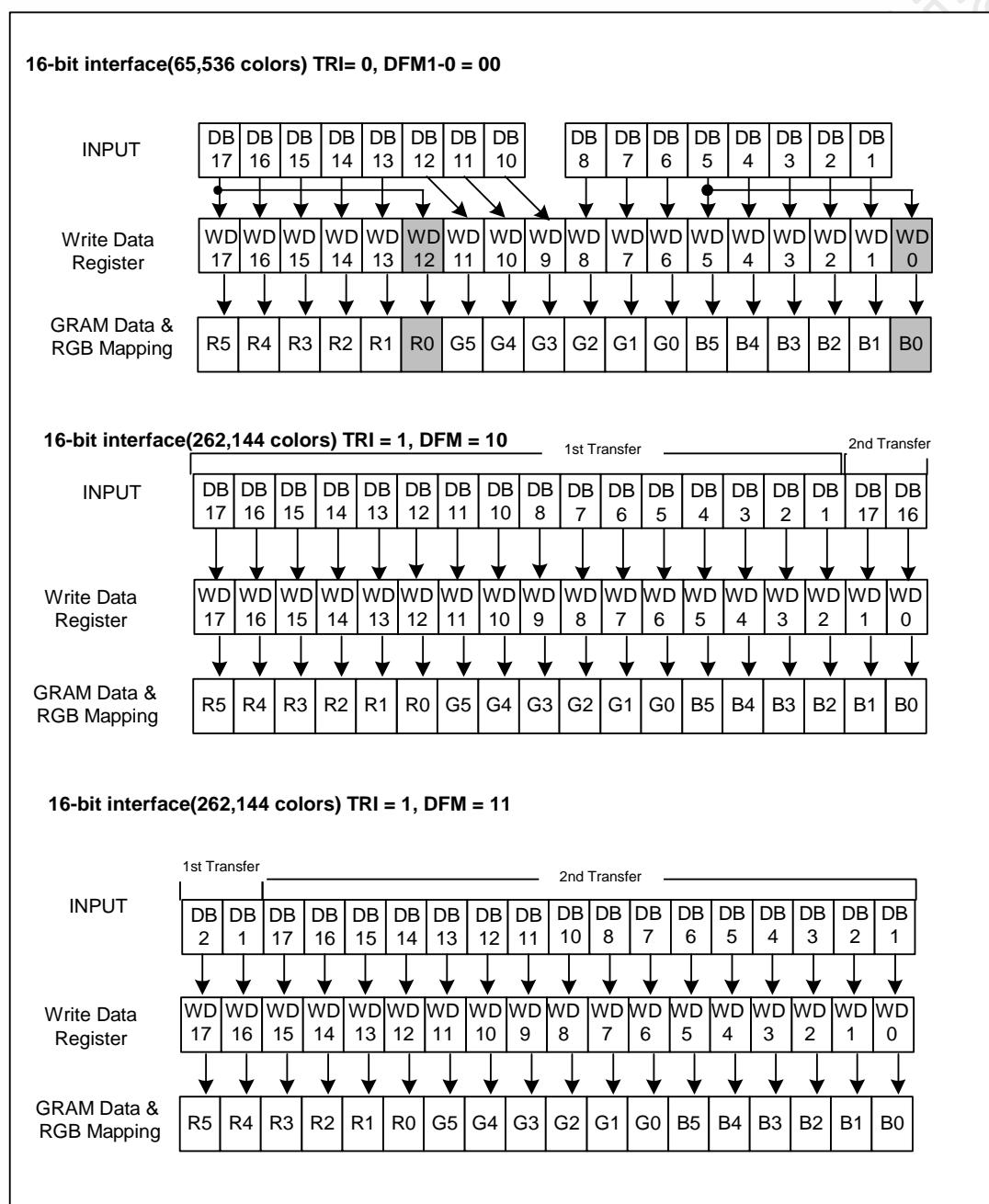


Figure 4. 30 Input Data Written to GRAM through Data Register in 16-bit Interface Mode

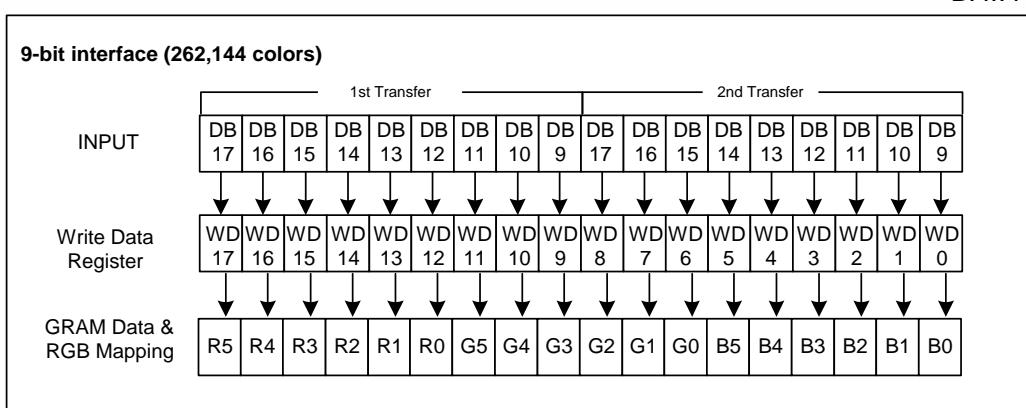


Figure 4. 31 Input Data Written to GRAM through Data Register in 9-bit Interface Mode

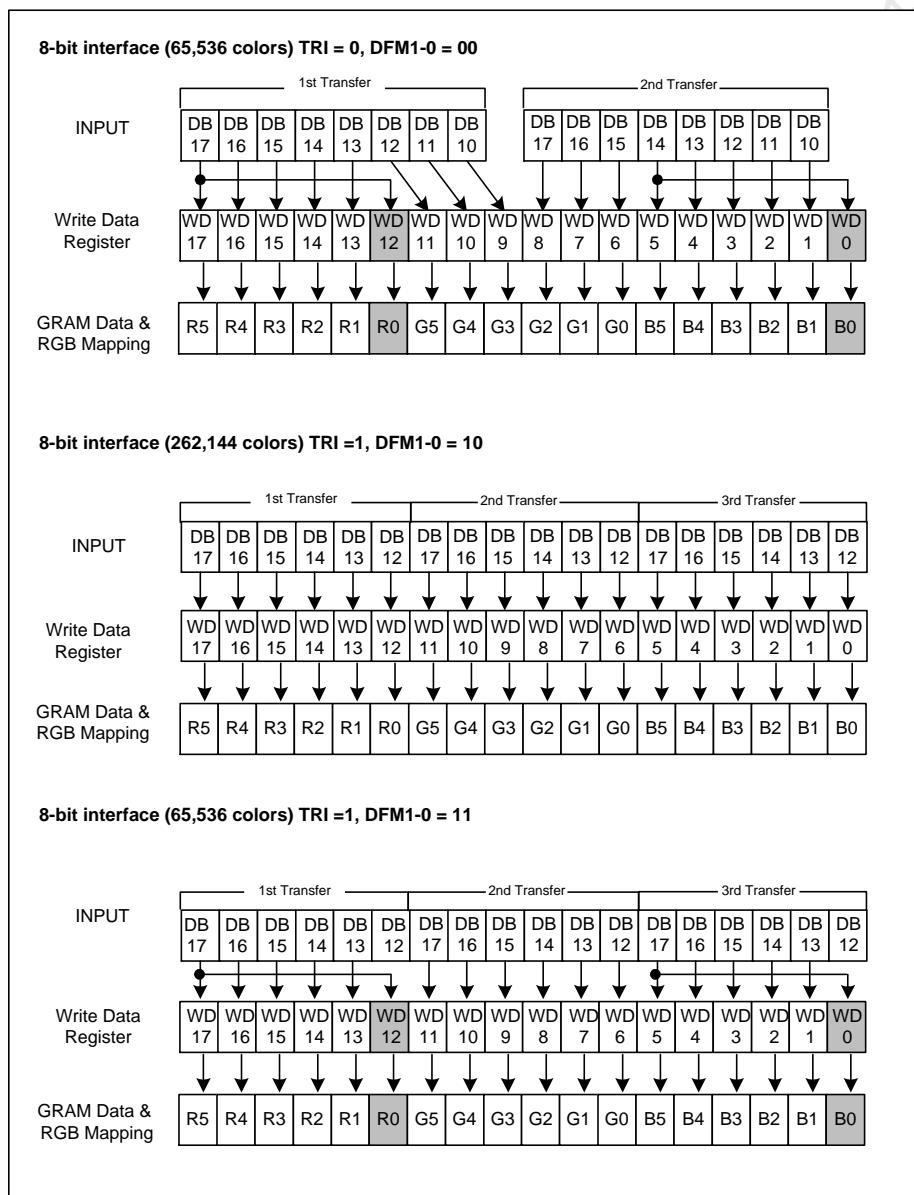
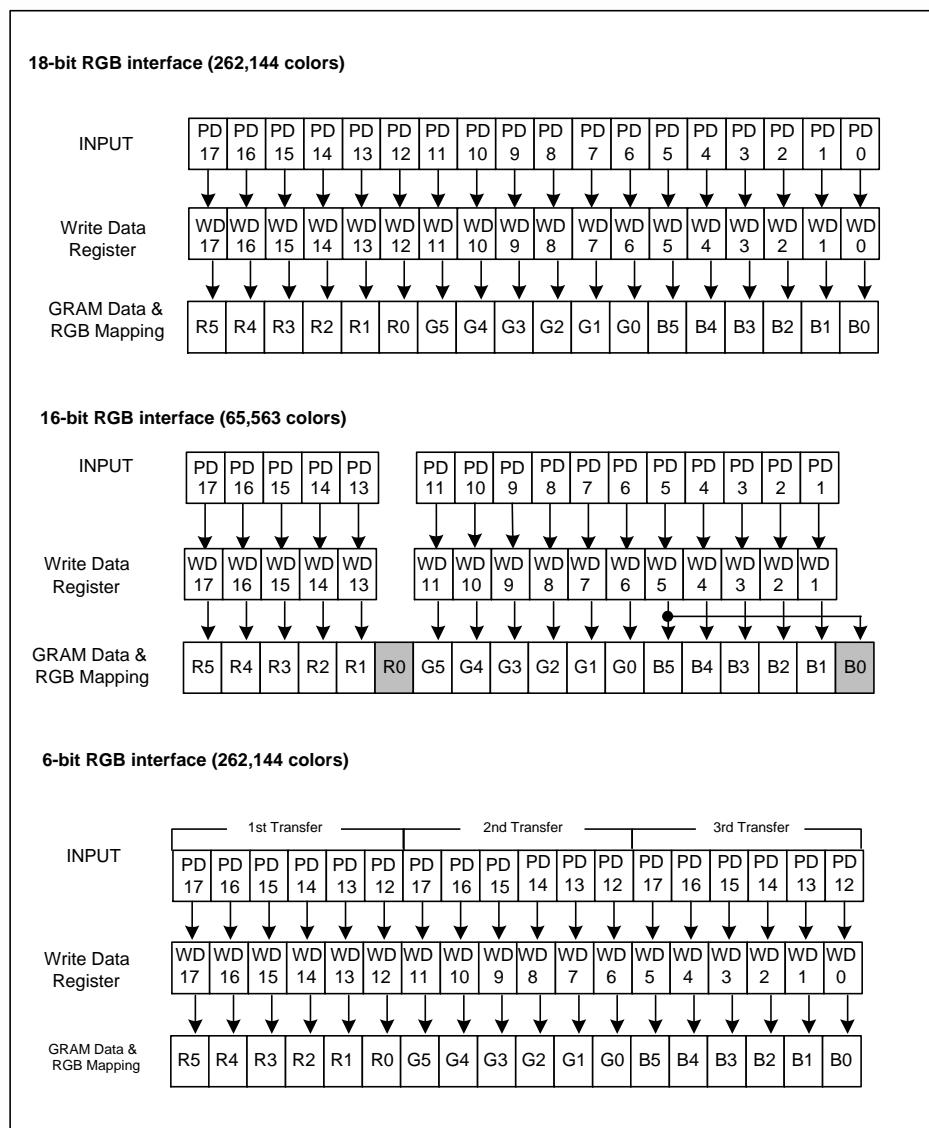


Figure 4. 32 Input Data Written to GRAM through Write Data Register in 8-bit Interface Mode



**Figure 4. 33 Input Data Written to GRAM through Write Data Register in 18-/16-/6-bit RGB Interface Mode**

GRAM data settings RGB	Grayscale	
	Positive	Negative
000000	VINP0	VINN7
000001	43/48*VINP1 + 5/48*VINP0	5/48*VINN7 + 43/48*VINN5
000010	6/48*VINP2 + 42/48*VINP1	42/48*VINN6 + 6/48*VINN5
000011	18/48*VINP2 + 30/48*VINP1	30/48*VINN6 + 18/48*VINN5
000100	25/48*VINP2 + 23/48*VINP1	23/48*VINN6 + 25/48*VINN5
000101	32/48*VINP2 + 16/48*VINP1	16/48*VINN6 + 32/48*VINN5
000110	36/48*VINP2 + 12/48*VINP1	12/48*VINN6 + 36/48*VINN5
000111	40/48*VINP2 + 8/48*VINP1	8/48*VINN6 + 40/48*VINN5
001000	44/48*VINP2 + 4/48*VINP1	4/48*VINN6 + 44/48*VINN5
001001	VINP2	VINN5
001010	4/48*VINP3 + 44/48*VINP2	44/48*VINN5 + 4/48*VINN4
001011	8/48*VINP3 + 40/48*VINP2	40/48*VINN5 + 8/48*VINN4
001100	12/48*VINP3 + 36/48*VINP2	36/48*VINN5 + 12/48*VINN4
001101	16/48*VINP2 + 32/48*VINP2	32/48*VINN5 + 16/48*VINN4
001110	20/48*VINP2 + 28/48*VINP2	28/48*VINN5 + 20/48*VINN4
001111	24/48*VINP2 + 24/48*VINP2	24/48*VINN5 + 24/48*VINN4
010000	28/48*VINP2 + 20/48*VINP2	20/48*VINN5 + 28/48*VINN4
010001	32/48*VINP2 + 16/48*VINP2	16/48*VINN5 + 32/48*VINN4
010010	36/48*VINP2 + 12/48*VINP2	12/48*VINN5 + 36/48*VINN4
010011	40/48*VINP2 + 8/48*VINP2	8/48*VINN5 + 40/48*VINN4
010100	44/48*VINP2 + 4/48*VINP2	4/48*VINN5 + 44/48*VINN4
010101	VINP3	VINN4
010110	3/48*VINP4 + 45/48*VINP3	45/48*VINN4 + 3/48*VINN3
010111	6/48*VINP4 + 42/48*VINP3	42/48*VINN4 + 6/48*VINN3
011000	8/48*VINP4 + 40/48*VINP3	40/48*VINN4 + 8/48*VINN3
011001	10/48*VINP4 + 38/48*VINP3	38/48*VINN4 + 10/48*VINN3
011010	12/48*VINP4 + 36/48*VINP3	36/48*VINN4 + 12/48*VINN3
011011	14/48*VINP4 + 34/48*VINP3	34/48*VINN4 + 14/48*VINN3
011100	16/48*VINP4 + 32/48*VINP3	32/48*VINN4 + 16/48*VINN3
011101	18/48*VINP4 + 30/48*VINP3	30/48*VINN4 + 18/48*VINN3
011110	20/48*VINP4 + 28/48*VINP3	28/48*VINN4 + 20/48*VINN3
011111	22/48*VINP4 + 26/48*VINP3	26/48*VINN4 + 22/48*VINN3
100000	24/48*VINP4 + 24/48*VINP3	24/48*VINN4 + 24/48*VINN3
100001	26/48*VINP4 + 22/48*VINP3	22/48*VINN4 + 26/48*VINN3
100010	28/48*VINP4 + 20/48*VINP3	20/48*VINN4 + 28/48*VINN3
100011	30/48*VINP4 + 18/48*VINP3	18/48*VINN4 + 30/48*VINN3
100100	32/48*VINP4 + 16/48*VINP3	16/48*VINN4 + 32/48*VINN3
100101	34/48*VINP4 + 14/48*VINP3	14/48*VINN4 + 34/48*VINN3
100110	36/48*VINP4 + 12/48*VINP3	12/48*VINN4 + 36/48*VINN3
100111	38/48*VINP4 + 10/48*VINP3	10/48*VINN4 + 38/48*VINN3
101000	40/48*VINP4 + 8/48*VINP3	8/48*VINN4 + 40/48*VINN3
101001	42/48*VINP4 + 6/48*VINP3	6/48*VINN4 + 42/48*VINN3
101010	45/48*VINP4 + 3/48*VINP3	3/48*VINN4 + 45/48*VINN3
101011	VINP4	VINN3
101100	4/48*VINP5 + 44/48*VINP4	44/48*VINN3 + 4/48*VINN2
101101	8/48*VINP5 + 40/48*VINP4	40/48*VINN3 + 8/48*VINN2
101110	12/48*VINP5 + 36/48*VINP4	36/48*VINN3 + 12/48*VINN2
101111	16/48*VINP5 + 32/48*VINP4	32/48*VINN3 + 16/48*VINN2
110000	20/48*VINP5 + 28/48*VINP4	28/48*VINN3 + 20/48*VINN2
110001	24/48*VINP5 + 24/48*VINP4	24/48*VINN3 + 24/48*VINN2
110010	28/48*VINP5 + 20/48*VINP4	20/48*VINN3 + 28/48*VINN2
110011	32/48*VINP5 + 16/48*VINP4	16/48*VINN3 + 32/48*VINN2
110100	36/48*VINP5 + 12/48*VINP4	12/48*VINN3 + 36/48*VINN2
110101	40/48*VINP5 + 8/48*VINP4	8/48*VINN3 + 40/48*VINN2
110110	44/48*VINP5 + 4/48*VINP4	4/48*VINN3 + 44/48*VINN2
110111	VINP5	VINN2
111000	4/48*VINP6 + 44/48*VINP5	44/48*VINN2 + 4/48*VINN1
111001	8/48*VINP6 + 40/48*VINP5	40/48*VINN2 + 8/48*VINN1
111010	12/48*VINP6 + 36/48*VINP5	36/48*VINN2 + 12/48*VINN1
111011	16/48*VINP6 + 32/48*VINP5	32/48*VINN2 + 16/48*VINN1
111100	23/48*VINP6 + 25/48*VINP5	25/48*VINN2 + 23/48*VINN1
111101	30/48*VINP6 + 18/48*VINP5	18/48*VINN2 + 30/48*VINN1
111110	15/48*VINP7 + 33/48*VINP6	43/48*VINN1 + 5/48*VINN0
111111	VINP7	VINN0

Table 4. 35 GRAM Data and Grayscale Level

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-P.113-  
November 2005

#### 4.14 Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 4. 34 Read Data Register (R22h)

**RD17–0:** Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

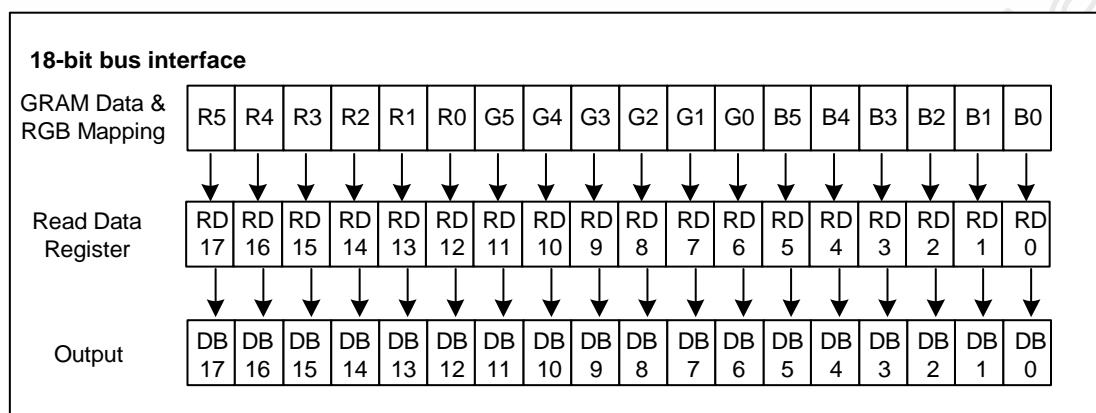
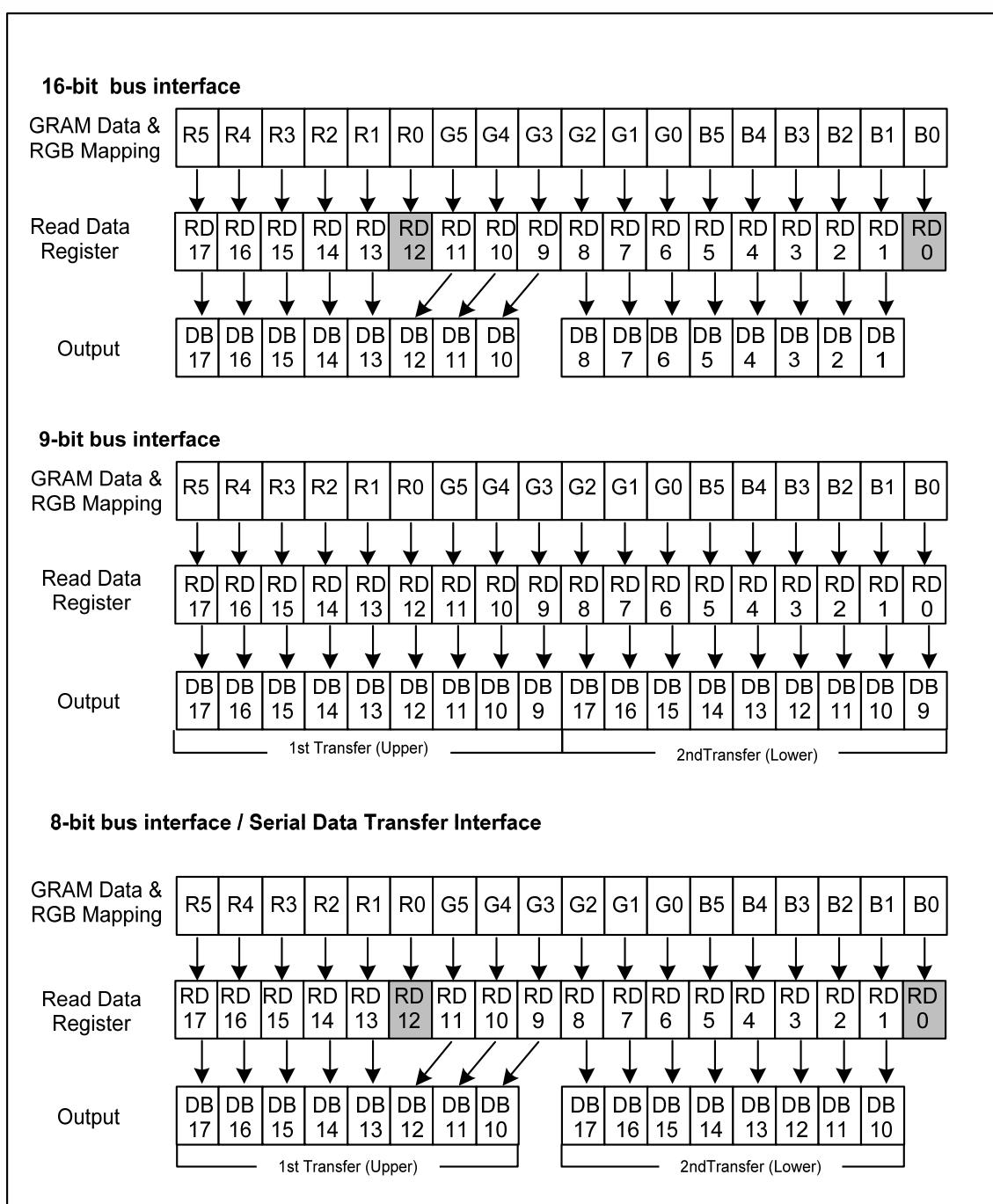


Figure 4. 35 Output Data Read from GRAM through Read Data Register in 18-bit Interface



**Figure 4. 36 Output Data Read from GRAM through Read Data Register in 16- /9- /8-bit Interface Mode**

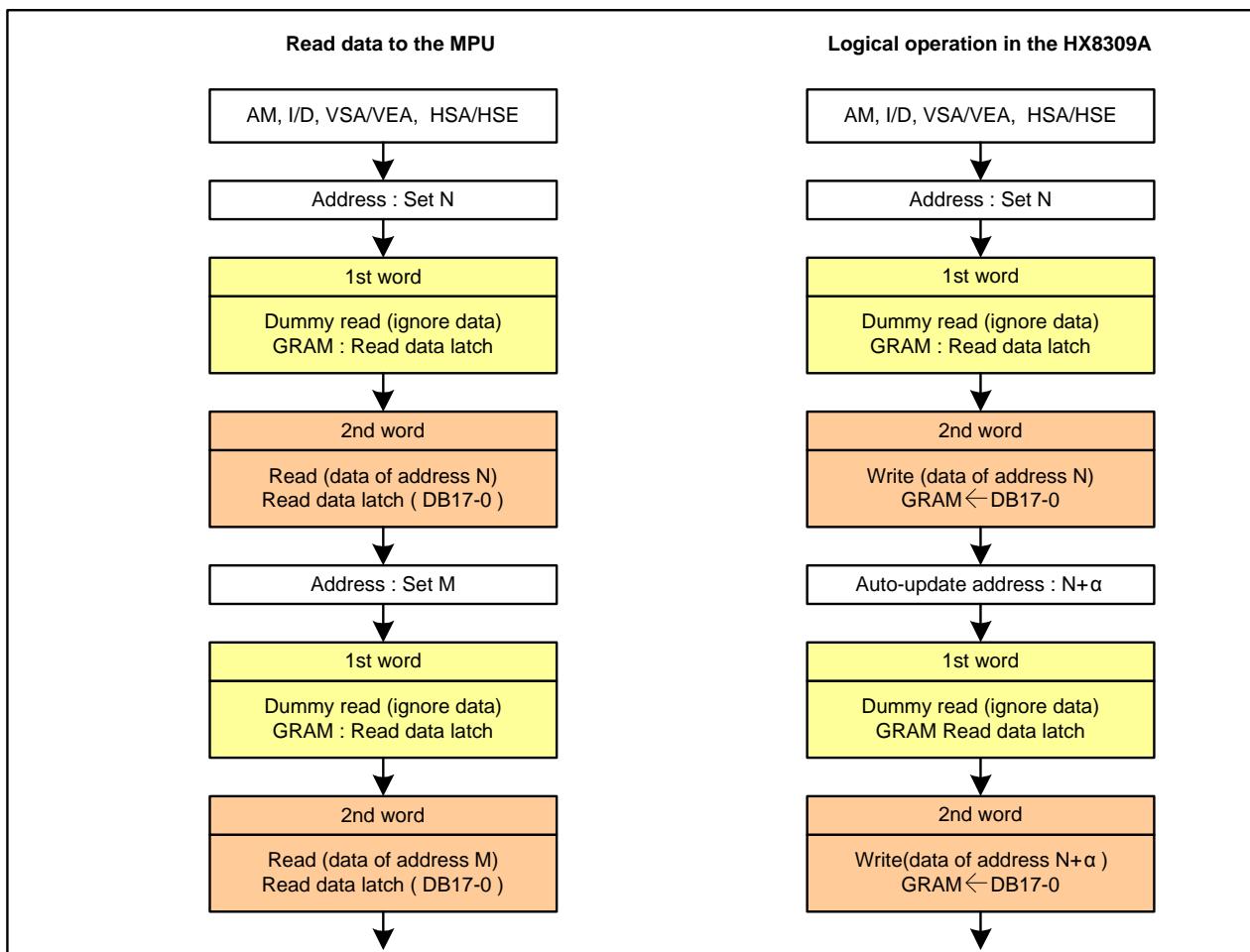


Figure 4.37 Flow Chart of GRAM Read Data

## 4.15 Write Data Mask Register Set

### 4.15.1 Write Data Mask Register 1 (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0

Figure 4.38 Write Data Mask Register 1 (R23h)

### 4.15.2 Write Data Mask Register 2 (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12

Figure 4.39 Write Data Mask Register 1 (R24h)

**WM17–0:** In writing to the GRAM, these bits mask writing in a bit unit. When WM17 = 1, this bit mask the write data of RB17 and does not write to the GRAM. Similarly, the WM16~WM0 bit masks the write data of RB16~RB0 in a bit unit. For details, see the Graphics Operation Function section.

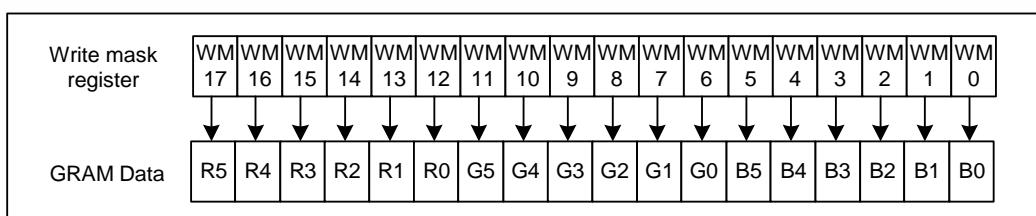


Figure 4. 40 GRAM Write Data Mask

#### 4.16 Gamma Control Register Set

	R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R30	<b>W</b>	<b>1</b>	0	0	0	0	0	MP1 (2)	MP1 (1)	MP1 (0)	0	0	0	0	0	MPO (2)	MPO (1)	MPO (0)
R31	<b>W</b>	<b>1</b>	0	0	0	0	0	MP3 (2)	MP3 (1)	MP3 (0)	0	0	0	0	0	MP2 (2)	MP2 (1)	MP2 (0)
R32	<b>W</b>	<b>1</b>	0	0	0	0	0	MP5 (2)	MP3 (1)	MP5 (0)	0	0	0	0	0	MP4 (2)	MP4 (1)	MP4 (0)
R33	<b>W</b>	<b>1</b>	0	0	0	0	0	CP1 (2)	CP1 (1)	CP1 (0)	0	0	0	0	0	CP0 (2)	CP0 (1)	CP0 (0)
R34	<b>W</b>	<b>1</b>	0	0	0	0	0	MN1 (2)	MN1 (1)	MN1 (0)	0	0	0	0	0	MN0 (2)	MN0 (1)	MN0 (0)
R35	<b>W</b>	<b>1</b>	0	0	0	0	0	MN3 (2)	MN3 (1)	MN3 (0)	0	0	0	0	0	MN2 (2)	MN2 (1)	MN2 (0)
R36	<b>W</b>	<b>1</b>	0	0	0	0	0	MN5 (2)	MN5 (1)	MN5 (0)	0	0	0	0	0	MN4 (2)	MN4 (1)	MN4 (0)
R37	<b>W</b>	<b>1</b>	0	0	0	0	0	CN1 (2)	CN1 (1)	CN1 (0)	0	0	0	0	0	CN0 (2)	CN0 (1)	CN0 (0)
R38	<b>W</b>	<b>1</b>	0	0	0	OP1 (4)	OP1 (3)	OP1 (2)	OP1 (1)	OP1 (0)	0	0	0	0	0	OP0 (3)	OP0 (2)	OP0 (1)
R39	<b>W</b>	<b>1</b>	0	0	0	ON1 (4)	ON1 (3)	ON1 (2)	ON1 (1)	ON1 (0)	0	0	0	0	0	ON0 (3)	ON0 (2)	ON0 (1)
																	ON0 (0)	

Figure 4. 41 Gamma Control Register 1~10 (R30h~R39h)

MP5-0 [2:0]: Gamma adjustment register for positive polarity output

CP1-0 [2:0]: Gamma gradient adjustment register for positive polarity output

MN5-0 [2:0]: Gamma adjustment register for negative polarity output

CN1-0 [2:0]: Gamma gradient adjustment register for negative polarity output

OP0 [3:0]/OP1 [4:0]: amplification adjustment resistor for positive polarity output

ON0 [3:0]/ON1 [4:0]: amplification average adjustment resistor for negative polarity output

For details, refer to Gamma Adjustment Function section.

#### 4.17 Gate Scan Position Register (R40h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 4. 42 Gate Scan Position Register (R40h)

**SCN4-0:** Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172
0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107
1	0	1	1	0	G177	G44	G130	G91
1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

Table 4. 36 SCN bits and Scanning Start Position for Gate Driver

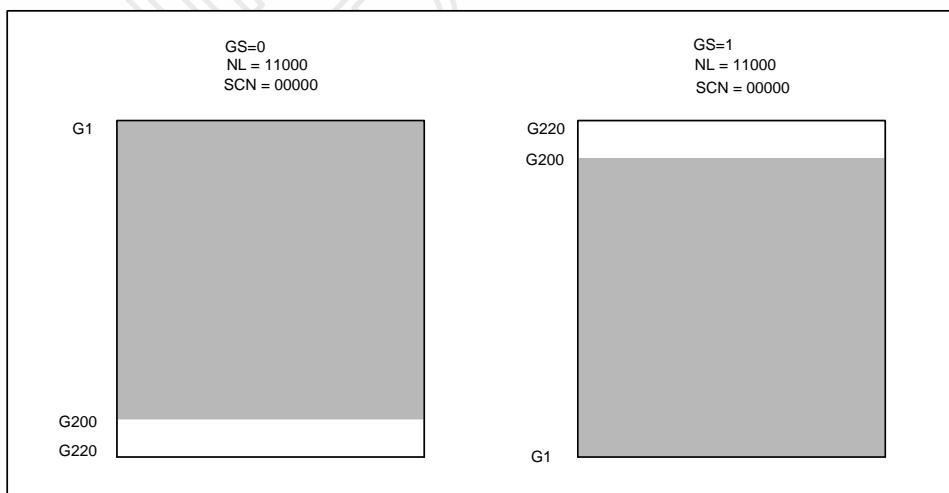


Figure 4. 43 SCN Bits and Scanning Start Position for Gate Driver

Note: Don't set NL, SCN over the end position of gate line (G220)

Note: Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 220.

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-P.118-

November 2005

#### 4.18 Vertical Scroll Control Register (R41h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	

Figure 4. 44 Vertical Scroll Control Register (R41h)

**VL7–0:** Specify the amount of scrolling line from 0 to 220 in the display to enable smooth vertical scrolling. If GRAM address mapping would exceed “DBxx”H, GRAM address mapping would restart from “00xx”H after the data in “DBxx”H of GRAM being displayed. The display-start line (VL7–0) is valid only when VLE1 = 1 or VLE2 = 1. The display-start line is fixed to zero when VLE2-1 = 00. (VLE1 is the 1st display window vertical-scroll enable bit, and VLE2 is the 2nd display window vertical-scroll enable bit.)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Length
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
:	:	:	:	:		:	:	:
1	1	0	1	1	0	0	1	217 lines
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

Table 4. 37 VL Bits and Scrolling Length

#### 4.19 First Display Window Driving Position Register (R42h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

Figure 4. 45 First Screen Driving Position Register (R42h)

**SS17-0:** Specify the driving start position for the first display window in a line unit.  
The LCD driving starts from the 'setting value + 1' scan line of gate driver.

**SE17-0:** Specify the driving end position for the first display window in a line unit. The LCD driving is performed to the 'setting value + 1' gate driver. See the Partial-Screen Display Function section for details.

#### 4.20 Second Display Window Driving Position Register (R43h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 4. 46 Second Screen Driving Position Register (R43h)

**SS27-0:** Specify the driving start position for the second display window in a line unit.  
The LCD driving starts from the 'setting value + 1' scan line of gate driver.  
The second display window is driven when SPT = 1.

**SE27-0:** Specify the driving end position for the second display window in a line unit.  
The LCD driving is performed to the 'setting value + 1' gate driver.

Note: Ensure that  $SS17-10 \leq SE17-10 < SS27-20 \leq SE27-20 \leq DBh$ . For details, see the Partial Screen Display Function section.

#### 4.21 Horizontal RAM Address Position Register (R44h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HAE2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

Figure 4. 47 Horizontal RAM Address Position Register (R44h)

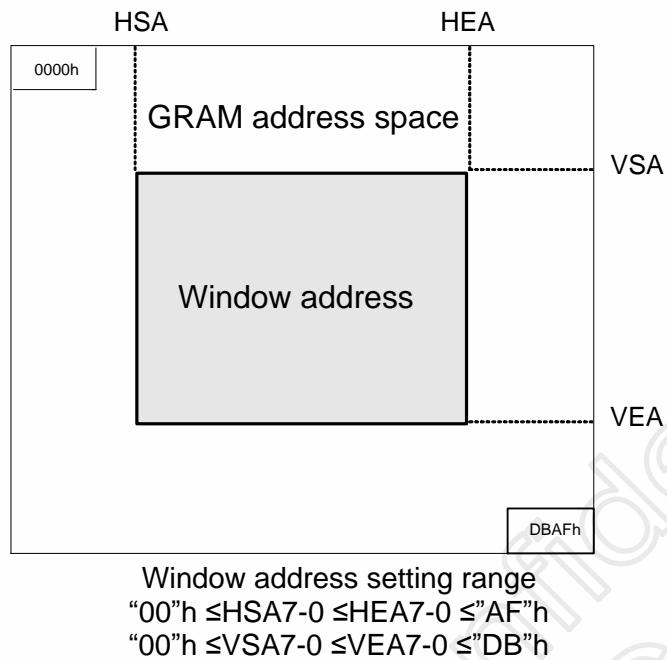
#### 4.22 Vertical RAM Address Position Register (R45h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 4. 48 Vertical RAM Address Position Register (R45h)

**HSA7-0/HEA7-0:** Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA7-0. Ensure that "00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "AF"h

**VSA7-0/VEA7-0:** Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA7-0 to the address specified by VEA7-0. Ensure that “00”h ≤VSA7-0 ≤VEA7-0 ≤“DB”h



**Figure 4. 49 Window Address Setting Range**

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high-speed mode so dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

## 4.23 Initialization

### Output Pin Initialization

1. Driver output pins (Source outputs): Output VSSD level
2. Driver output pins (Gate outputs): Output VGH level
3. Oscillator output pin (OSC2): Output oscillation signal

### Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4-0 = 11101, SS = 0, GS = 0)
3. LCD driving AC control ( FLD1-0 = 01, B/C = 0, EOR = 0, NW5-0 = 00000)
4. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2-0 = 00: Replace mode)
5. Compare register (CP17-0: 00000h)
6. Display control 1 (PT1-0 = 00, VLE2-1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL = 0: 262144-color mode, REV = 0, D1-0 = 00: Display off)
7. Frame cycle control (GD1-0 = 00, SDT1-0 = 00, CE1-0 = 00: No equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clocks in 1-line period)
8. External display interface control 1 (RIM1-0 = 00: 18-bit RGB interface, DM1-0 = 00: internal clock operation, RM = 0: System interface)
9. Power control 1 (BT2-0 = 000, DC2-0 = 000, AP2-0 = 000: LCD power off, DK = 1: step-up circuit 1 off, SLP = 0, STB = 0: Standby mode off)
10. Power control 2 (VC2-0 = 000)
11. Power control 3 (PON=0, VRH3-0 = 0000)
12. Power control 4 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
13. RAM address set (AD15-0 = 0000h)
14. RAM write data mask (WM17-0 = 000000000000000000000000: No mask)
15. Gamma control  
(MP02-00 = 000, MP12-10 = 000, MP22-20 = 000, MP32-30 = 000, MP42-40 = 000, MP52-50 = 000, CP02-00 = 000, CP12-10 = 000)  
(MN02-00 = 000, MN12-10 = 000, MN22-20 = 000, MN32-30 = 000, MN42-40 = 000, MN52-50 = 000, CN02-00 = 000, CN12-10 = 000)  
(OP03-00 = 0000, OP14-10 = 00000, ON03-00 = 0000, ON14-10 = 0000)
16. Gate scan starting position (SCN4-0 = 00000)
17. Vertical scroll (VL7-0 = 00000000)
18. 1st screen division (SE17-10 = 11011011, SS17-10 = 00000000)
19. 2nd screen division (SE27-20 = 11011011, SS27-20 = 00000000)
20. Horizontal RAM address position (HEA7-0 = 10101111, HSA7-0 = 00000000)
21. Vertical RAM address position (VEA7-0 = 11011011, VSA7-0 = 00000000)

#### 4.24 Reset Function

The HX8309-A is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from the MPU can be accepted. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

#### GRAM Data Initialization:

It must be initialized by software while display is off (D1-0=00).

## 5. Power Generation

### 5.1 Specification

The specification of power supply circuit and pins connection are shown as following table:

Pins connection	Recommended voltage	Capacity
VGAM1OUT, VciOUT, VLC, VcomH, VcomL, C11A/B, C12A/B	6V	1 µF (B characteristics)
VLCDC, C21A/B, C22A/B	10V	1 µF
TVCOMHI, TVCOMLI, TVMAG	16V	0.1uF
VGHC, VGLC	25V	1 µF

**Table 5. 1 Adoptability of Capacitor**

Pins connection	Feature
VSSD – VGL (Vci – VGH) (Vci – VLCD)	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

**Table 5. 2 Adoptability of Schottkey diode**

Reusable	Pins to connect
> 200 kΩ	VcomR

**Table 5. 3 Adoptability of Variable resistor**

## 5.2 Power supply Circuit

The power supply circuit of HX8309-A presides over generating supply voltages to drive a LCD panel.

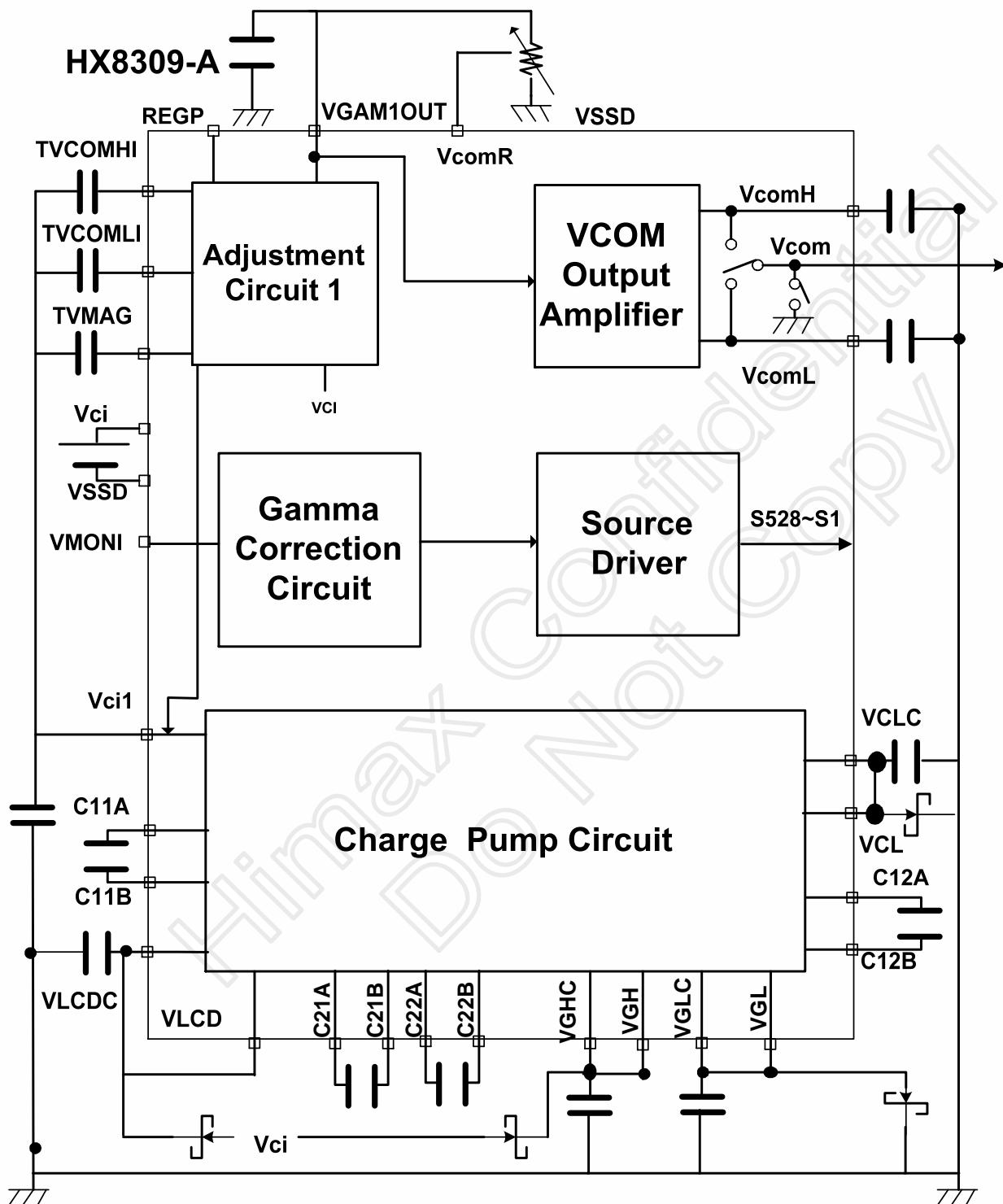
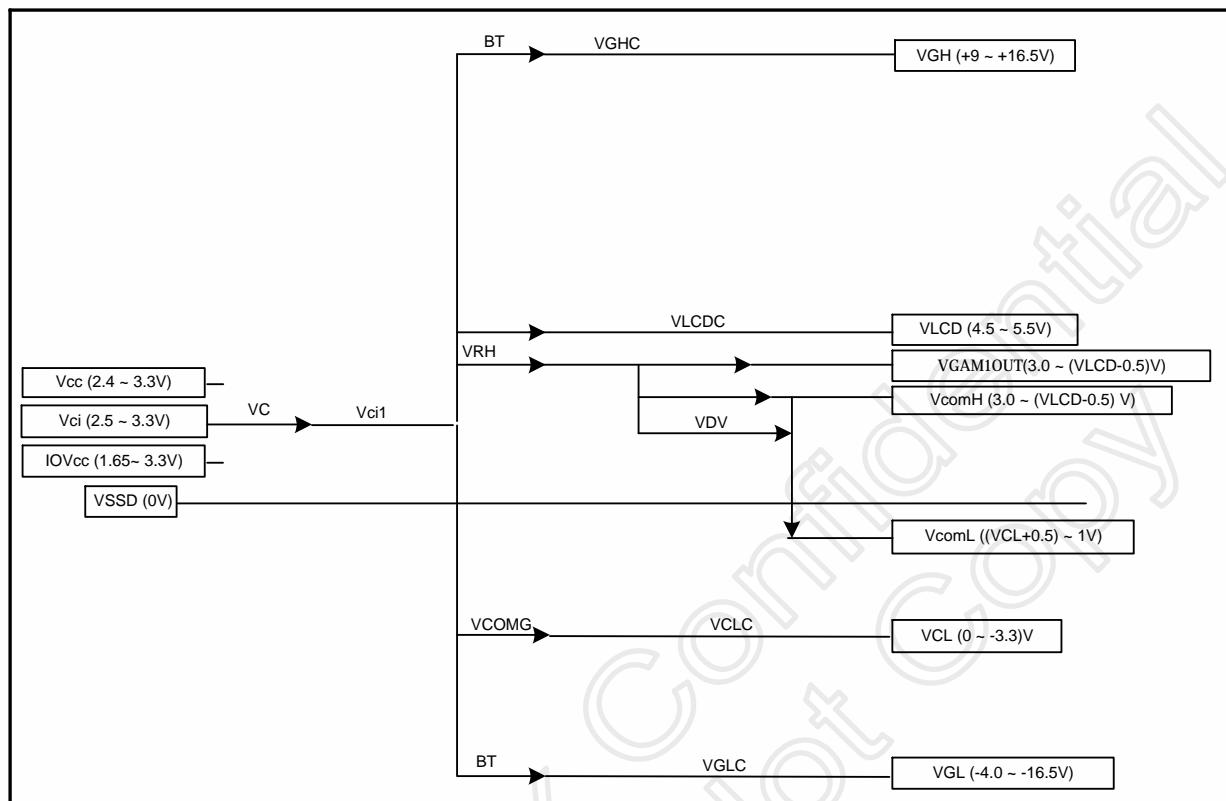


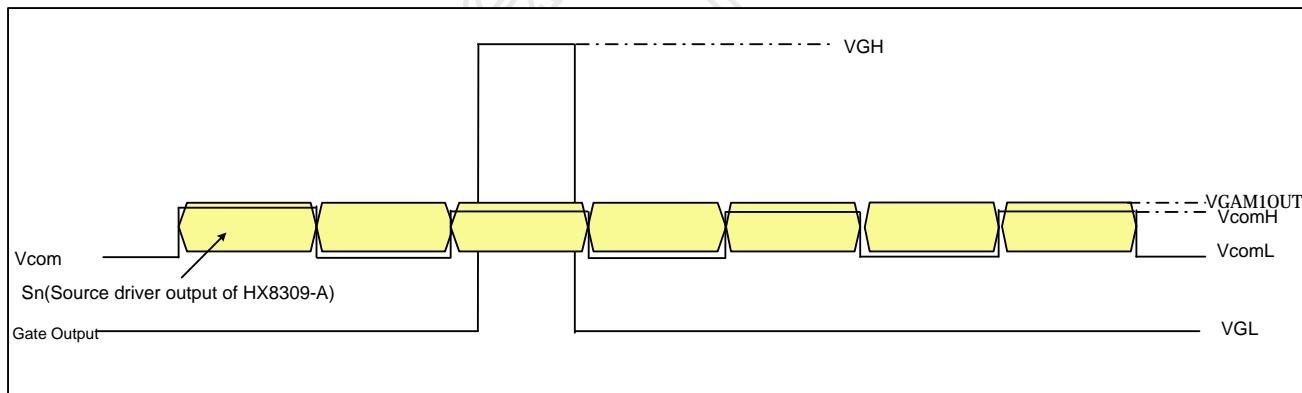
Figure 5. 1 Block Diagram of Power Supply Circuit

### 5.3 Voltage Setting

The voltage setting pattern diagram of the HX8309-A illustrates as following figure. The outputs of VLCD, VGH, VGL, and VCL are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption. When the Vcom voltage alternating cycle is high, the large current will be consumed.



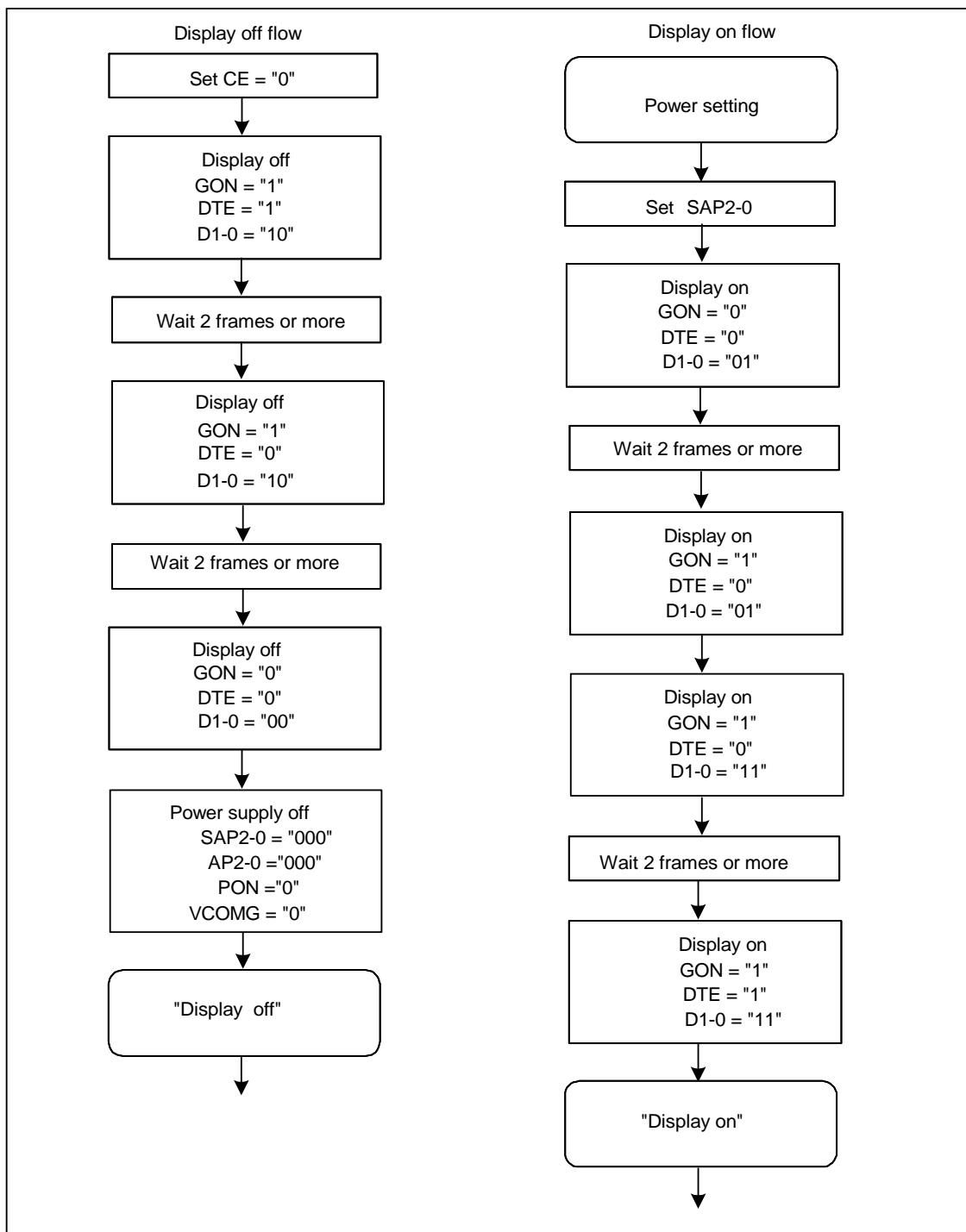
**Figure 5. 2 Voltage Setting Diagram**



**Figure 5. 3 Applied Voltage of TFT Display**

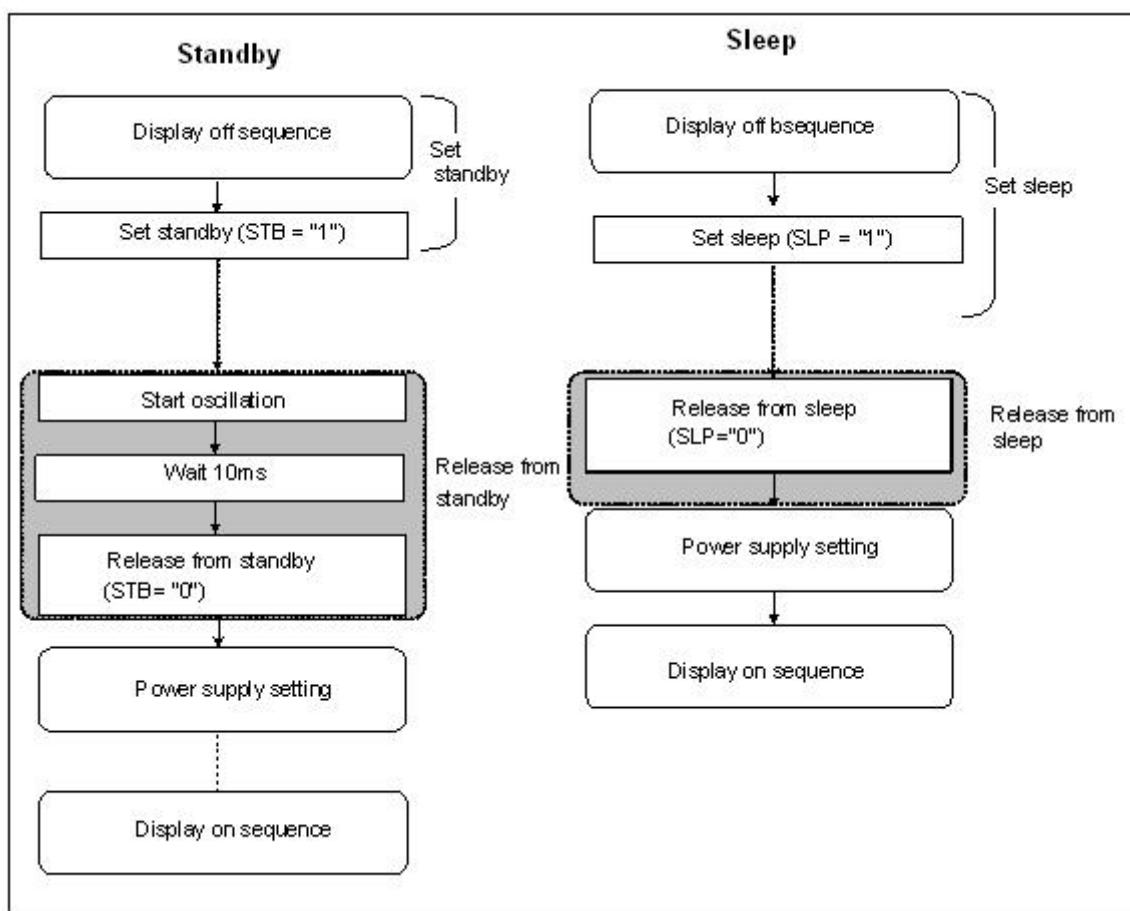
## 5.4 Register Setting

The following are the sequences of register setting flow that applied to the HX8309-A driving the TFT display.



**Figure 5.4 Register Setting Sequence**

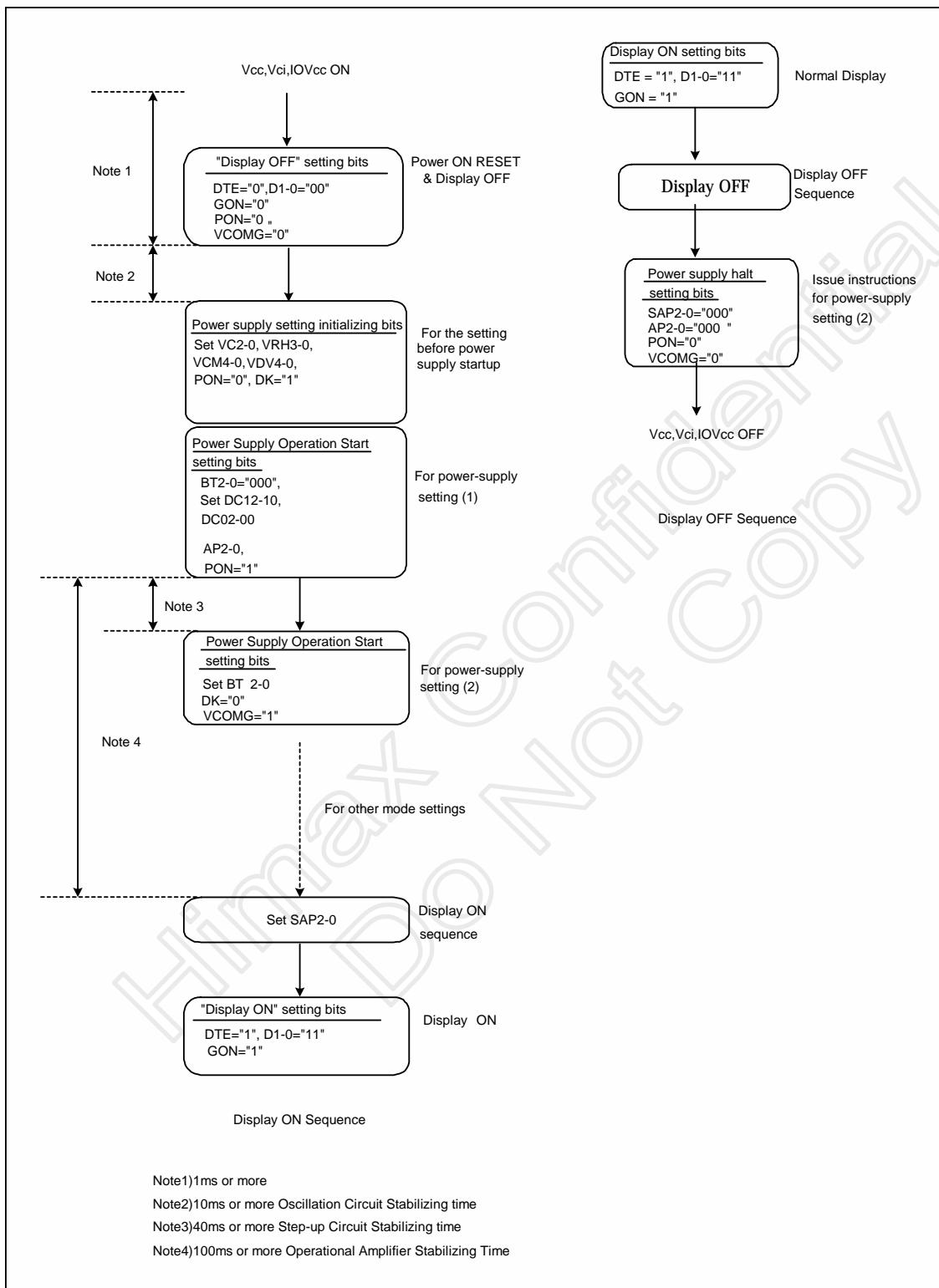
Standby mode and Sleep Mode setting flow:



**Figure 5. 5 Standby Mode and Sleep Mode Setting Sequence**

## 5.5 Power Supply Setting

The power supply setting sequence of the HX8309-A is follow as blew.



**Figure 5. 6 Power Supply Setting Flow**

## 6. Electrical Characteristic

### 6.1 Absolute Maximum Ratings

The absolute maximum ratings are listed on Table 6.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage (1)	Vcc, IOVcc	V	-0.3 to +4.6	1,2
Power Supply Voltage (2)	Vci ~ VSSA	V	-0.3 to +4.6	1,2
Power Supply Voltage (3)	VLCD ~ VSSA	V	-0.3 to +6.0	3
Power Supply Voltage (4)	VSSA ~ VCL	V	-0.3 to +4.6	4
Power Supply Voltage (5)	VLCD ~ VCL	V	-0.3 to +9	5
Power Supply Voltage (6)	VGH ~ VSSA	V	-0.3 to +18.5	6
Power Supply Voltage (7)	VSSA ~ VGL	V	-0.3 to +18.5	7
Input Voltage	Vi	V	-0.3 to Vcc+0.3	-
Operating Temperature	Topr	°C	-40 to +85	8,9
Storage Temperature	Tstg	°C	-55 to +110	8,9

**Table 6. 1 Absolute Maximum Rating**

Note:

1. Vcc, VSSD must be maintained.
2. To make sure IOVcc  $\geq$  VSSD.
3. To make sure Vci  $\geq$  VSSA.
4. To make sure VLCD  $\geq$  VSSA.
5. To make sure VLCD  $\geq$  VCL.
6. To make sure VGH  $\geq$  VSSA.
7. To make sure VSSA  $\geq$  VGL
8. For die and wafer products, specified up to +85°C.
9. This temperature specifications apply to the TCP package.

## 6.2 AC Characteristic

### Clock Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	$f_{cp}$	KHz	T.B.D	335	T.B.D	$V_{cc} = 2.4 \sim 3.3V$
External clock duty ratio	Duty	%	45	50	55	$V_{cc} = 2.4 \sim 3.3V$
External clock rise time	$t_{rcp}$	$\mu s$	-	-	0.2	$V_{cc} = 2.4 \sim 3.3V$
External clock fall time	$t_{fcp}$	$\mu s$	-	-	0.2	$V_{cc} = 2.4 \sim 3.3V$
R-C oscillation clock	$f_{osc}$	KHz	275	335	395	$R_f = 130K \Omega, V_{cc} = 2.8V$

Table 6. 2 Clock Characteristics ( $V_{cc} = 2.4 \sim 3.3V$ )

### 80-system(18/16 Bits) Bus Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Bus cycle time</b>	<b>Write</b>	$t_{CYCW}$	ns	350	-	Figure6.1
	<b>Read</b>	$t_{CYCR}$	ns	500	-	Figure6.1
<b>Write low-level pulse width</b>	$PW_{LW}$	ns	40	-	-	Figure6.1
<b>Read low-level pulse width</b>	$PW_{LR}$	ns	250	-	-	Figure6.1
<b>Write high-level pulse width</b>	$PW_{HW}$	ns	70	-	-	Figure6.1
<b>Read high-level pulse width</b>	$PW_{HR}$	ns	200	-	-	Figure6.1
<b>Write / Read rise / fall time</b>	$t_{WRr}, t_{WRF}$	ns	-	-	25	Figure6.1
<b>Setup time</b>	<b>Write ( RS to NCS, E_NWR )</b>	$t_{AS}$	ns	5	-	Figure6.1
				5	-	Figure6.1
<b>Address hold time</b>	$t_{AH}$	ns	5	-	-	Figure6.1
<b>Write data setup time</b>	$t_{DSW}$	ns	15	-	-	Figure6.1
<b>Write data hold time</b>	$t_H$	ns	15	-	-	Figure6.1
<b>Read data delay time</b>	$t_{DDR}$	ns	-	-	200	Figure6.1
<b>Read data hold time</b>	$t_{DHR}$	ns	5	-	-	Figure6.1

Table 6. 3 Normal Write Mode ( $HWM = 0$ ) / ( $IOV_{cc} = 1.65 \sim 2.4V$ ) / ( $V_{cc}=2.4\sim 3.3V$ )

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Bus cycle time</b>	<b>Write</b>	$t_{CYCW}$	ns	300	-	Figure6.1
	<b>Read</b>	$t_{CYCR}$	ns	500	-	Figure6.1
<b>Write low-level pulse width</b>	$PW_{LW}$	ns	40	-	-	Figure6.1
<b>Read low-level pulse width</b>	$PW_{LR}$	ns	250	-	-	Figure6.1
<b>Write high-level pulse width</b>	$PW_{HW}$	ns	30	-	-	Figure6.1
<b>Read high-level pulse width</b>	$PW_{HR}$	ns	200	-	-	Figure6.1
<b>Write / Read rise / fall time</b>	$t_{WRr}, t_{WRF}$	ns	-	-	25	Figure6.1
<b>Setup time</b>	<b>Write ( RS to NCS, E_NWR )</b>	$t_{AS}$	ns	5	-	Figure6.1
				5	-	Figure6.1
<b>Address hold time</b>	$t_{AH}$	ns	5	-	-	Figure6.1
<b>Write data setup time</b>	$t_{DSW}$	ns	15	-	-	Figure6.1
<b>Write data hold time</b>	$t_H$	ns	15	-	-	Figure6.1
<b>Read data delay time</b>	$t_{DDR}$	ns	-	-	80	Figure6.1
<b>Read data hold time</b>	$t_{DHR}$	ns	5	-	-	Figure6.1

Table 6. 4 Normal Write Mode ( $HWM = 0$ ) / ( $IOV_{cc} = 2.4 \sim 3.3V$ ) / ( $V_{cc}=2.4\sim 3.3V$ )

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Bus cycle time</b>	<b>Write</b>	t <sub>CYCW</sub>	ns	100	-	-	Figure6.1
	<b>Read</b>	t <sub>CYCR</sub>	ns	500	-	-	Figure6.1
	<b>Write low-level pulse width</b>	PW <sub>LW</sub>	ns	40	-	-	Figure6.1
	<b>Read low-level pulse width</b>	PW <sub>LR</sub>	ns	250	-	-	Figure6.1
	<b>Write high-level pulse width</b>	PW <sub>HW</sub>	ns	30	-	-	Figure6.1
	<b>Read high-level pulse width</b>	PW <sub>HR</sub>	ns	200	-	-	Figure6.1
	<b>Write / Read rise / fall time</b>	t <sub>WRr</sub> , t <sub>WRF</sub>	ns	-	-	25	Figure6.1
<b>Setup time</b>	<b>Write ( RS to NCS, E_NWR )</b>	t <sub>AS</sub>	ns	5	-	-	Figure6.1
	<b>Read ( RS to NCS, RW_NRD )</b>			5	-	-	Figure6.1
	<b>Address hold time</b>	t <sub>AH</sub>	ns	5	-	-	Figure6.1
	<b>Write data set up time</b>	t <sub>DSW</sub>	ns	15	-	-	Figure6.1
	<b>Write data hold time</b>	t <sub>H</sub>	ns	20	-	-	Figure6.1
	<b>Read data delay time</b>	t <sub>DDR</sub>	ns	-	-	200	Figure6.1
	<b>Read data hold time</b>	t <sub>DHR</sub>	ns	5	-	-	Figure6.1

Table 6. 5 High-Speed Write Mode (HWM = 1) / (IOVcc = 1.65 ~ 2.4V) / (Vcc=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Bus cycle time</b>	<b>Write</b>	t <sub>CYCW</sub>	ns	100	-	-	Figure6.1
	<b>Read</b>	t <sub>CYCR</sub>	ns	500	-	-	Figure6.1
	<b>Write low-level pulse width</b>	PW <sub>LW</sub>	ns	40	-	-	Figure6.1
	<b>Read low-level pulse width</b>	PW <sub>LR</sub>	ns	250	-	-	Figure6.1
	<b>Write high-level pulse width</b>	PW <sub>HW</sub>	ns	30	-	-	Figure6.1
	<b>Read high-level pulse width</b>	PW <sub>HR</sub>	ns	200	-	-	Figure6.1
	<b>Write / Read rise / fall time</b>	t <sub>WRr</sub> , t <sub>WRF</sub>	ns	-	-	25	Figure6.1
<b>Setup time</b>	<b>Write ( RS to NCS, E_NWR )</b>	t <sub>AS</sub>	ns	5	-	-	Figure6.1
	<b>Read ( RS to NCS, RW_NRD )</b>			5	-	-	Figure6.1
	<b>Address hold time</b>	t <sub>AH</sub>	ns	5	-	-	Figure6.1
	<b>Write data set up time</b>	t <sub>DSW</sub>	ns	15	-	-	Figure6.1
	<b>Write data hold time</b>	t <sub>H</sub>	ns	20	-	-	Figure6.1
	<b>Read data delay time</b>	t <sub>DDR</sub>	ns	-	-	200	Figure6.1
	<b>Read data hold time</b>	t <sub>DHR</sub>	ns	5	-	-	Figure6.1

Table 6. 6 High-Speed Write Mode (HWM = 1) / (IOVcc = 2.4 ~ 3.3V) / (Vcc=2.4~3.3V)

## 80-system(9/8 Bits) Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t <sub>CYCW</sub>	ns	350	-	-	Figure6.1
	Read	t <sub>CYCR</sub>	ns	500	-	-	Figure6.1
	Write low-level pulse width	PW <sub>LW</sub>	ns	40	-	-	Figure6.1
	Read low-level pulse width	PW <sub>LR</sub>	ns	250	-	-	Figure6.1
	Write high-level pulse width	PW <sub>HW</sub>	ns	30	-	-	Figure6.1
	Read high-level pulse width	PW <sub>HR</sub>	ns	200	-	-	Figure6.1
	Write / Read rise / fall time	t <sub>WRr</sub> , t <sub>WRF</sub>	ns	-	-	25	Figure6.1
Setup time	Write ( RS to NCS, E_NWR )	t <sub>AS</sub>	ns	5	-	-	Figure6.1
	Read ( RS to NCS , RW_NRD )			5	-	-	Figure6.1
	Address hold time	t <sub>AH</sub>	ns	5	-	-	Figure6.1
	Write data set up time	t <sub>DSW</sub>	ns	15	-	-	Figure6.1
	Write data hold time	t <sub>H</sub>	ns	20	-	-	Figure6.1
	Read data delay time	t <sub>DDR</sub>	ns	-	-	120	Figure6.1
	Read data hold time	t <sub>DHR</sub>	ns	5	-	-	Figure6.1

Table 6. 7 Normal Write Mode (HWM = 0) / (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t <sub>CYCW</sub>	ns	300	-	-	Figure6.1
	Read	t <sub>CYCR</sub>	ns	500	-	-	Figure6.1
	Write low-level pulse width	PW <sub>LW</sub>	ns	40	-	-	Figure6.1
	Read low-level pulse width	PW <sub>LR</sub>	ns	250	-	-	Figure6.1
	Write high-level pulse width	PW <sub>HW</sub>	ns	30	-	-	Figure6.1
	Read high-level pulse width	PW <sub>HR</sub>	ns	200	-	-	Figure6.1
	Write / Read rise / fall time	t <sub>WRr</sub> , t <sub>WRF</sub>	ns	-	-	25	Figure6.1
Setup time	Write ( RS to NCS, E_NWR )	t <sub>AS</sub>	ns	5	-	-	Figure6.1
	Read ( RS to NCS , RW_NRD )			5	-	-	Figure6.1
	Address hold time	t <sub>AH</sub>	ns	5	-	-	Figure6.1
	Write data set up time	t <sub>DSW</sub>	ns	15	-	-	Figure6.1
	Write data hold time	t <sub>H</sub>	ns	20	-	-	Figure6.1
	Read data delay time	t <sub>DDR</sub>	ns	-	-	120	Figure6.1
	Read data hold time	t <sub>DHR</sub>	ns	5	-	-	Figure6.1

Table 6. 8 Normal Write Mode (HWM = 0) / (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

## Serial Data Transfer Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Serial clock cycle time</b>	<b>Write ( received )</b>	t <sub>SCYC</sub>	μs	100	-	>1ms
	<b>Read ( transmitted )</b>	t <sub>SCYC</sub>	μs	350	-	>1ms
<b>Serial clock high – level pulse width</b>	<b>Write ( received )</b>	t <sub>SCH</sub>	ns	40	-	-
	<b>Read ( transmitted )</b>	t <sub>SCH</sub>	ns	150	-	-
<b>Serial clock low – level pulse width</b>	<b>Write ( received )</b>	t <sub>SCL</sub>	ns	40	-	-
	<b>Read ( transmitted )</b>	t <sub>SCL</sub>	ns	150	-	-
<b>Serial clock rise / fall time</b>	t <sub>scr</sub> , t <sub>scf</sub>	ns	-	-	-	Figure6.2
<b>Chip select set up time</b>	t <sub>CSU</sub>	ns	20	-	-	Figure6.2
<b>Chip select hold time</b>	t <sub>CH</sub>	ns	60	-	-	Figure6.2
<b>Serial input data set up time</b>	t <sub>SISU</sub>	ns	30	-	-	Figure6.2
<b>Serial input data hold time</b>	t <sub>SIH</sub>	ns	30	-	-	Figure6.2
<b>Serial output data set up time</b>	t <sub>SOD</sub>	ns	-	-	120	Figure6.2
<b>Serial output data hold time</b>	t <sub>SOH</sub>	ns	5	-	-	Figure6.2

Table 6. 9 (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
<b>Serial clock cycle time</b>	<b>Write ( received )</b>	t <sub>SCYC</sub>	μs	100	-	>1ms
	<b>Read ( transmitted )</b>	t <sub>SCYC</sub>	μs	350	-	>1ms
<b>Serial clock high – level pulse width</b>	<b>Write ( received )</b>	t <sub>SCH</sub>	ns	40	-	-
	<b>Read ( transmitted )</b>	t <sub>SCH</sub>	ns	150	-	-
<b>Serial clock low – level pulse width</b>	<b>Write ( received )</b>	t <sub>SCL</sub>	ns	40	-	-
	<b>Read ( transmitted )</b>	t <sub>SCL</sub>	ns	150	-	-
<b>Serial clock rise / fall time</b>	t <sub>scr</sub> , t <sub>scf</sub>	ns	-	-	-	Figure6.2
<b>Chip select set up time</b>	t <sub>CSU</sub>	ns	20	-	-	Figure6.2
<b>Chip select hold time</b>	t <sub>CH</sub>	ns	60	-	-	Figure6.2
<b>Serial input data set up time</b>	t <sub>SISU</sub>	ns	20	-	-	Figure6.2
<b>Serial input data hold time</b>	t <sub>SIH</sub>	ns	20	-	-	Figure6.2
<b>Serial output data set up time</b>	t <sub>SOD</sub>	ns	-	-	120	Figure6.2
<b>Serial output data hold time</b>	t <sub>SOH</sub>	ns	5	-	-	Figure6.2

Table 6. 10 (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

## RGB Interface Timing Characteristics

### 18/16-bit Interface

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	tSYNCS	ns	0	-	-	Figure6.3
ENABLE set up time	tENS	ns	10	-	-	Figure6.3
ENABLE hold time	tENH	ns	20	-	-	Figure6.3
DOTCK "low" level pulse width	PWDL	ns	40	-	-	Figure6.3
DOTCK "high" level pulse width	PWDH	ns	40	-	-	Figure6.3
DOTCK cycle time	tCYCD	ns	100	-	-	Figure6.3
DATA set up time	tPDS	ns	20	-	-	Figure6.3
DATA hold time	tPDH	ns	20	-	-	Figure6.3
DOTCLK , VSYNC , HSYNC rising and falling time	trgb <sub>r</sub> , trgb <sub>f</sub>	ns	-	-	25	Figure6.3

Table 6. 11 18-/16-bit Bus RGB Interface Mode and High-Speed Write Mode ( HWM = 1 ) /  
(IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	tSYNCS	ns	0	-	-	Figure6.3
ENABLE set up time	tENS	ns	10	-	-	Figure6.3
ENABLE hold time	tENH	ns	20	-	-	Figure6.3
DOTCK "low" level pulse width	PWDL	ns	40	-	-	Figure6.3
DOTCK "high" level pulse width	PWDH	ns	40	-	-	Figure6.3
DOTCK cycle time	tCYCD	ns	100	-	-	Figure6.3
DATA set up time	tPDS	ns	20	-	-	Figure6.3
DATA hold time	tPDH	ns	20	-	-	Figure6.3
DOTCLK , VSYNC , HSYNC rising and falling time	trgb <sub>r</sub> , trgb <sub>f</sub>	ns	-	-	25	Figure6.3

Table 6. 12 18-/16-bit Bus RGB Interface Mode and High-Speed Write Mode ( HWM = 1 ) /  
(IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

## 6-bit RGB Interface

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	tSYNCS	ns	0	-	-	Figure6.3
ENABLE set up time	tENS	ns	10	-	-	Figure6.3
ENABLE hold time	tENH	ns	20	-	-	Figure6.3
DOTCK "low" level pulse width	PWDL	ns	40	-	-	Figure6.3
DOTCK "high" level pulse width	PWDH	ns	40	-	-	Figure6.3
DOTCK cycle time	tCYCD	ns	100	-	-	Figure6.3
DATA set up time	tPDS	ns	20	-	-	Figure6.3
DATA hold time	tPDH	ns	20	-	-	Figure6.3
DOTCLK , VSYNC , HSYNC rising and falling time	trgb <sub>r</sub> , trgb <sub>f</sub>	ns	-	-	25	Figure6.3

Table 6. 13 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1) / (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	tSYNCS	ns	0	-	-	Figure6.3
ENABLE set up time	tENS	ns	10	-	-	Figure6.3
ENABLE hold time	tENH	ns	20	-	-	Figure6.3
DOTCK "low" level pulse width	PWDL	ns	40	-	-	Figure6.3
DOTCK "high" level pulse width	PWDH	ns	40	-	-	Figure6.3
DOTCK cycle time	tCYCD	ns	100	-	-	Figure6.3
DATA set up time	tPDS	ns	20	-	-	Figure6.3
DATA hold time	tPDH	ns	20	-	-	Figure6.3
DOTCLK , VSYNC , HSYNC rising and falling time	trgb <sub>r</sub> , trgb <sub>f</sub>	ns	-	-	25	Figure6.3

Table 6. 14 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1) / (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

## LCD driver output Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Driver output delay timing	tDD	us	-	35	-	Figure6.4 Vci=IOVcc=Vcc=2.8V , Ta=25°C , fOSC = 330KHz, (220 Line) GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, DC0=000, DC1=010,B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=10000, VCOMG=1, CL=0, MP5-0[2:0]=M5N-0[2:0]=000, CP1-0[2:0]=CN1-0[2:0]=000, OP0[3:0]= ON0[3:0]=0000 OP1[4:0]= ON1[4:0]=00000

Table 6. 15 Driver output delay timing

## Reset Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Reset low level width	tRES	ms	1	-	-	Figure6.5
Reset rise time	t <sub>r</sub> RES	ns	-	-	10	Figure6.5

Table 6. 16 (IOVcc=1.65~3.3V) / (Vcc = 2.4 ~ 3.3V)

### 6.3 DC Characteristic

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
<b>Input high voltage</b>	$V_{IH}$	V	$IOV_{cc} = 1.65 \sim 3.3V$	$0.8 \times IOV_{cc}$	-	$IOV_{cc}$	-
<b>Input low voltage</b>	$V_{IL}$	V	$IOV_{cc} = 1.65 \sim 3.3V$	-0.3V	-	$0.2 \times IOV_{cc}$	-
<b>Output high voltage(1) ( DB0-17 Pins )</b>	$V_{OH1}$	V	$I_{OH} = -0.1 \text{ mA}$	$0.8 \times IOV_{cc}$	-	-	-
<b>Output low voltage ( DB0-17 Pins )</b>	$V_{OL1}$	V	$IOV_{cc} = 1.65 \sim 2.4V$ $I_{OL} = 0.1\text{mA}$	-	-	$0.2 \times IOV_{cc}$	-
<b>I/O leakage current</b>	$I_{Li}$	$\mu A$	$V_{in} = 0 \sim V_{cc}$	-1	-	1	-
<b>Current consumption during normal operation ( <math>V_{cc} - V_{SSD}</math> ) + ( <math>IOV_{cc} - V_{SSD}</math> )</b>	$I_{OP(V_{cc})}$	$\mu A$	$V_{ci}=IOV_{cc}=V_{cc}=2.8V$ , $T_a=25^{\circ}\text{C}$ , $f_{OSC} = 330\text{KHz}$ (220 Line) GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, DC0=000, DC1=010,B/C=0, BT=001, VC=001, VRH=0011, VCM=10011,VDV=10000, VCOMG=1, CL=0, No panel load	-	150	300	-
<b>Current consumption during normal operation ( <math>V_{ci} - V_{SSD}</math> )</b>	$I_{OP(V_{ci})}$	mA			1.4	1.8	
<b>Current consumption during standby mode ( <math>V_{cc} - V_{SSD}</math> ) + ( <math>IOV_{cc} - V_{SSD}</math> )</b>	$I_{ST(V_{cc})}$	$\mu A$	$V_{cc}=2.8V$ , $T_a=25^{\circ}\text{C}$	-	1	10	-
<b>Current consumption during standby mode ( <math>V_{ci} - V_{SSD}</math> )</b>	$I_{ST(V_{ci})}$	$\mu A$			0.5	1	
<b>Output voltage deviation</b>	-	mV	-	-	5	-	-
<b>Dispersion of the Average Output Voltage</b>	V	mV	-	-	-	35	-

Table 6. 17 DC Characteristic ( $V_{cc} = 2.4 \sim 3.3V$ ,  $IOV_{cc} = 1.65 \sim 3.3V$ ,  $T_a = -40 \sim 85^{\circ}\text{C}$ )

## 6.4 Timing Characteristic

### 80-system Bus Operation

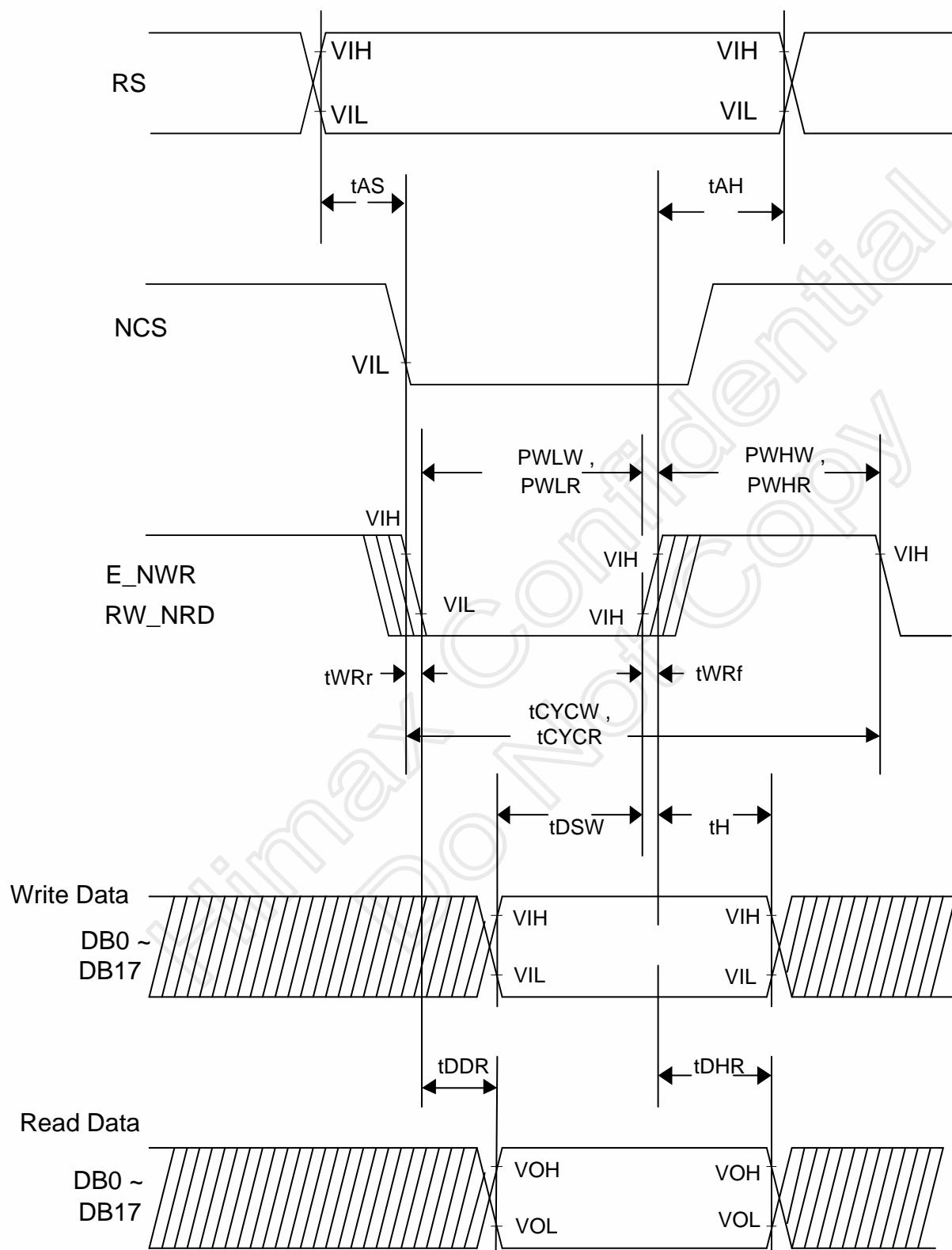


Figure 6. 1 80-system Bus Timing

### Clock Synchronized Serial Data Transfer Interface Operation

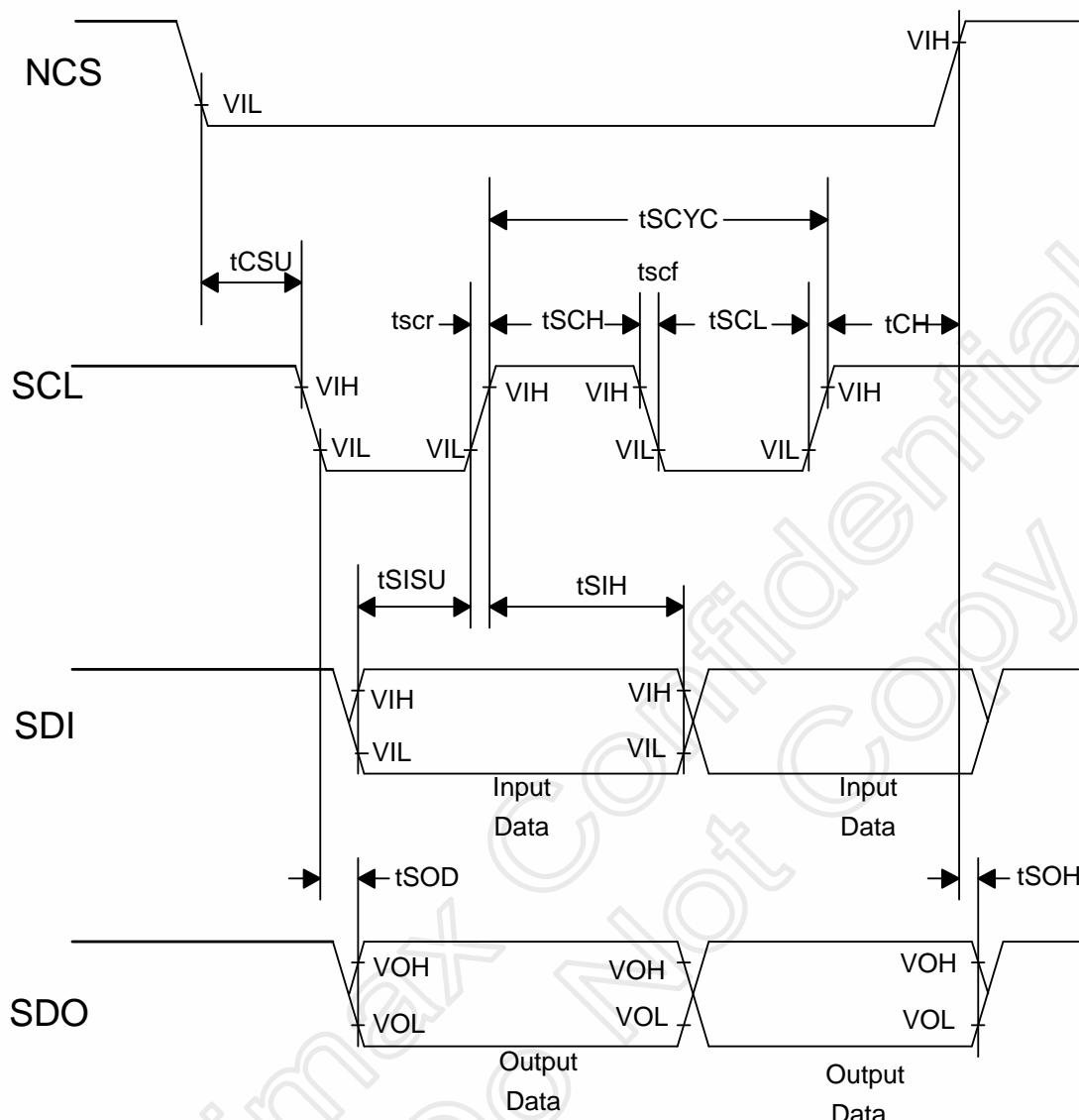


Figure 6. 2 Clock Synchronized Serial Data Transfer Interface Timing

## RGB Interface Operation

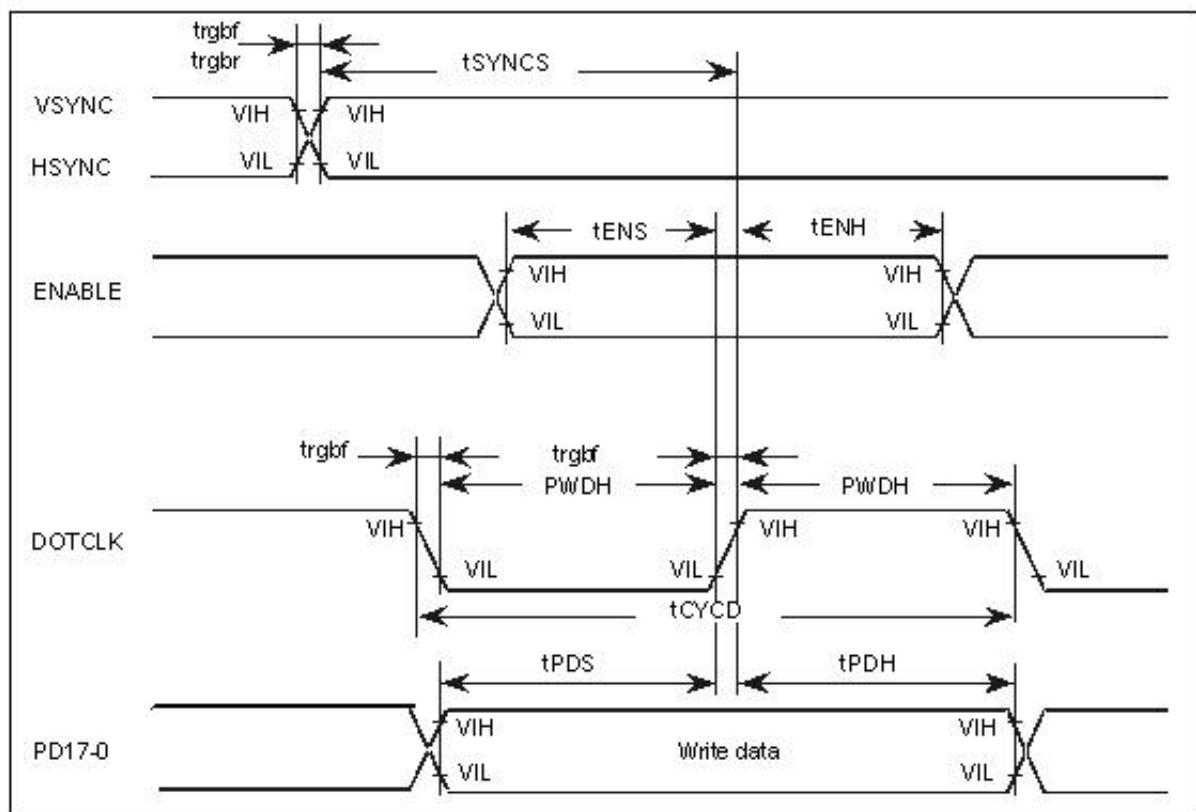
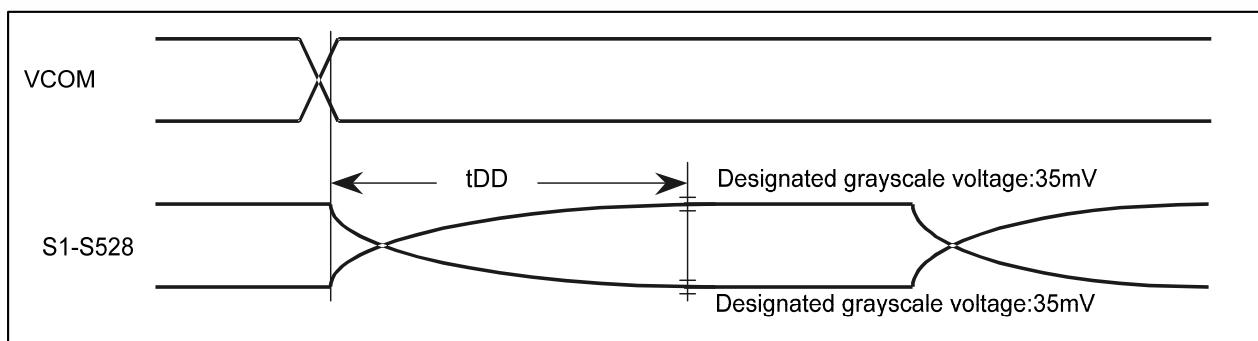
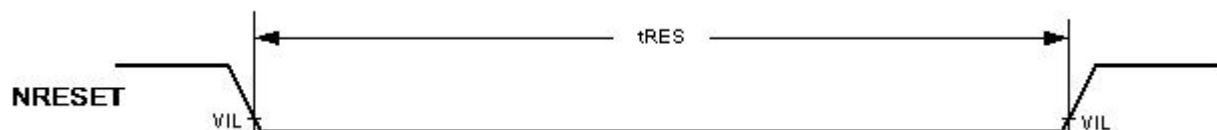


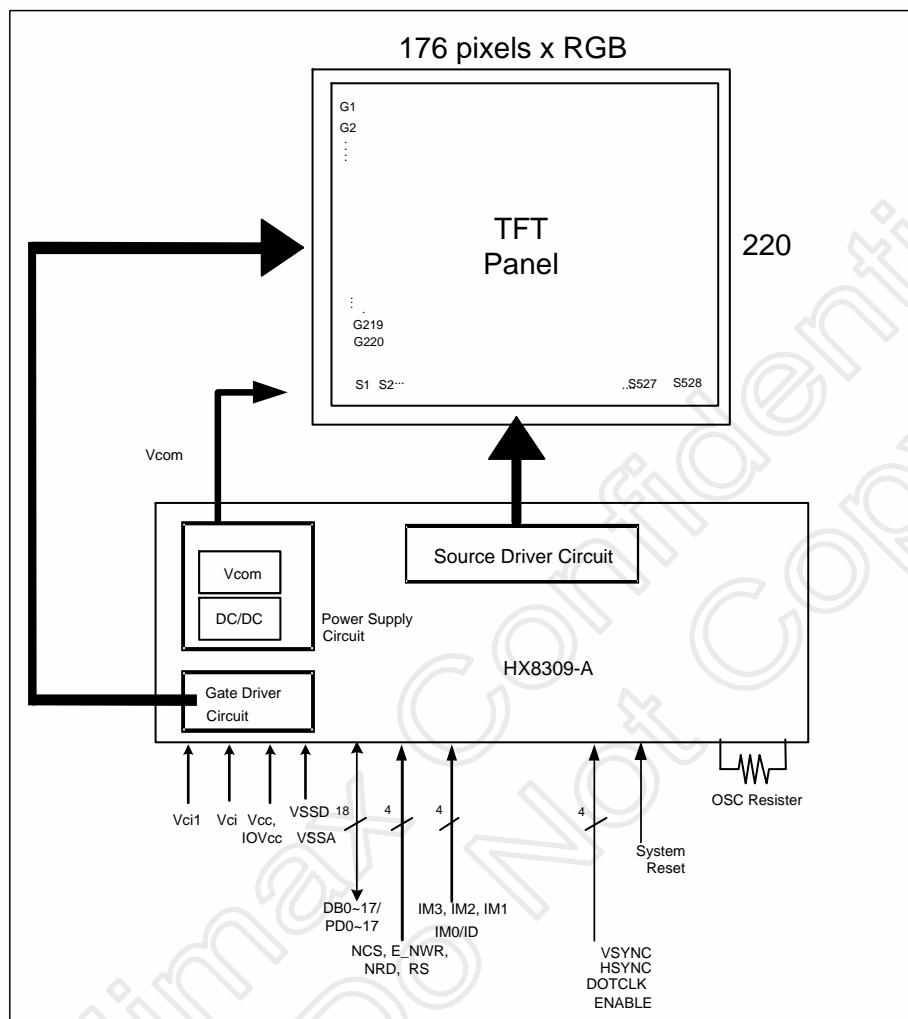
Figure 6. 3 RGB Interface Operation

**LCD Driving Output****Figure 6. 4 LCD Driving Output****Reset Operation****Figure 6. 5 Reset Timing**

## 7. System Configuration

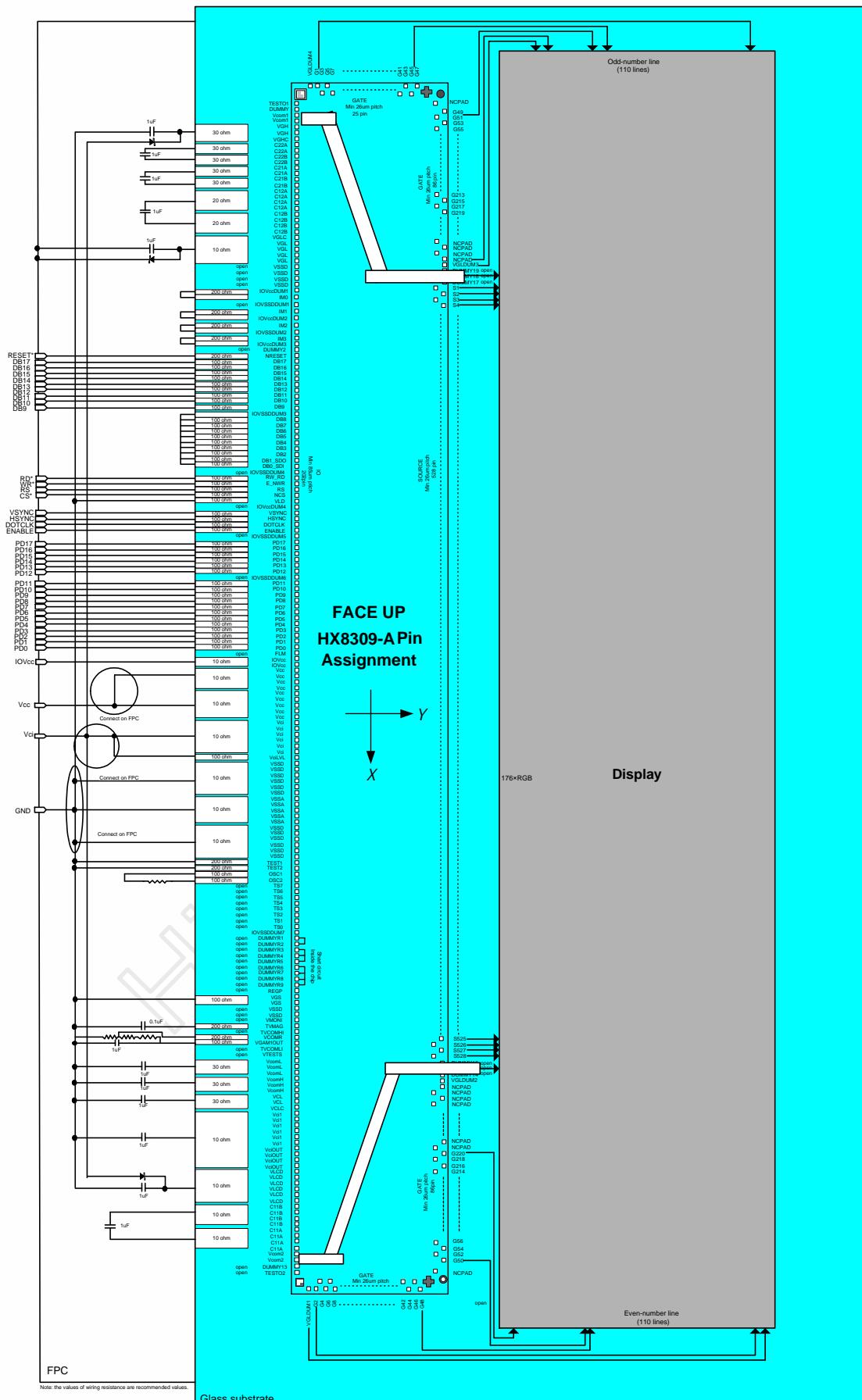
### 7.1 System Diagram

The system configuration diagram illustrates as following:



**Figure 7. 1 System Diagram of HX8309-A**

## 7.2 Layout Recommendation



## 8. Ordering information

Part NO.	Package
HX8309-A000 <u>PDxxx</u>	PD : mean COG xxx : mean chip thickness ( $\mu\text{m}$ ) , (default 400 $\mu\text{m}$ )

## 9. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2004/10/07	New setup
	2004/10/14	1. Modified the product name HX8309-A 2. Page 14: Modified the Bump size for typing error
	2005/02/03	1. Modified Table3.16 and Table3.18: Voltage Calculation Formula of Grayscale Voltage (Page76 and page 78) 2. Modified Table4.35: GRAM Data and Grayscale Level 3. Modified the Table 4.31: VRH Bits and VGAM1OUT Voltage 4. Modified the figure 5.1: Block Diagram of Power Supply Circuit (page 123) 5. Modified the Table 5.2: Adoptability of Schottkey diode (page 122) 6. Modify the description of SS bit of register 01 (page86) 7. Add the layout recommendation (page 142) 8. Modify the pin description of DB1_SDO. (page 12)
	2005/06/24	1. Add the Table 3.20: External Resistance Value and R-C Oscillation Frequency (Temporally Define) (page 85) 2. Add the Table 6. 17Clock Characteristics (Vcc = 2.4 ~ 3.3V) (page 133) 3. Add the VIH, VIL, VOH, VOL Characteristics specification (page 137) 4. Modify the description of TVCOMLI, TVCOMHI and TVMAG (page13) 5. Update the AC Characteristics Table 6.3 ~ Table 6.15 (Page132 ~ page137) 6. Add the Table 6.16 DC Characteristics(Vcc = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C)
	2005/07/21	1. Correct the figure of pin assignment (page 16) 2. Add the ordering information (page 146)
	2005/07/26	1. Modify the description of IOVCC (page 14)
	2005/08/29	1. Remove preliminary wording from the data sheet
	02	1. Modify the Figure 3.5 for typing error(page 47) 2. Modify the Figure 3.10 for typing error(page 51) 3. Modify the Figure 4.34 for typing error(page 113)