Electrical Rules Check Report

Class	Document	Message
		Successful Compile for VolCtrl_PCB.PrjPcb

Design Rules Verification Report

Filename : C:\Users\holzi\Dropbox\Projekte\BlackCat2_VolCtrl\BC2_VolCtrl_PCB\VolCtrl_PCB.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.5mm) (OnLayer('Keep-Out Layer')),(InPolygon)	0
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Clearance Constraint (Gap=0.3mm) (InPolygon),(All)	0
Clearance Constraint (Gap=0mm) (OnLayer('Keep-Out Layer')),(InComponent('L2') or	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.25mm) (Max=10mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.125mm) (All)	0
Hole Size Constraint (Min=0.2mm) (Max=5mm) (All)	0
Hole To Hole Clearance (Gap=0.3mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=80mm) (Prefered=12.7mm) (All)	0
Total	0

Difference Report For Project VolCtrl_PCB.PrjPcb

Different Descriptions Schematic Object	PCB Object
Bus-Transceiver [U4]	[U4]
Bus-Transceiver [U5]	[U5]
Electrolytic, 25V [C17]	[C17]
Low dropout regulator [U2]	[U2]
nmos [Q1]	[Q1]
nmos [Q2]	[Q2]
nmos [Q3]	[Q3]
nmos [Q4]	[Q4]
nmos [Q5]	[Q5]
nmos [Q6]	[Q6]
Testpoint [TP1]	[TP1]
Testpoint [TP2]	[TP2]
Testpoint [TP3]	[TP3]
Testpoint [TP4]	[TP4]
Different Component Parameters **Schematic Object**	**PCB Object**
[C17]	[C17]
[F1]	[F1]
[IC1]	[IC1]