R328-S3 Datasheet

Audio Application Processor

Revision 1.4

Apr.17, 2019

Revision History

Revision	Date	Description
1.4	Apr.17, 2019	1. Update ambient temperature description in section 5.2. 2. Add power-off requirements in section 5.12.2.
1.3	Mar.29, 2019	1. Add X32KFOUT output clock characteristics in section 5.9. 2. Update power on sequence in Figure 5-18.
1.2	Mar.15, 2019	Update package bottom view in Table 7-2.
1.1	Mar.04, 2019	Swap the ball position between MICIN3P and MICIN3N in Table 4-2 and Figure 7-1.
1.0	Feb.20, 2019	First release version

Declaration

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, the interface timing, thermal and package, and part reliability of the R328-S3 processor. For details about register descriptions of each module, see the ***Allwinner_R328-S3_User_Manual***.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

Allwinner's R328-S3 is a highly integrated dual-core SoC targeted for audio application markets. The R328-S3 integrates a dual-core ARM Cortex™-A7 operating up to 1.2GHz. An extensive set of audio interfaces such as audio codec, I2S/PCM,DMIC,one wire audio(OWA) are included for microphone voice wake-up/recognition/record/playback applications on connected audio products. In addition, voice activity detector(VAD) supports low power consumption wake-up function to reduce standby power consumption.

To reduce the BOM cost, a 1Gbit DDR3 die is embedded for the R328-S3. The R328-S3 comes with extensive connectivity and interfaces, such as USB, SDIO, SPI, UART, TWI, etc. Also the R328-S3 has ability to connect with other different peripherals like WIFI and BT via SDIO and UART.

Security functions are enabled and accelerated by hardware crypto engine, secure boot and secure efuse, etc. The small footprint with low-power consumption greatly reduces the PCB layout resource.

2. Features

2.1. CPU Architecture

- Dual-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions(LPAE)
- 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
- 256KB L2 cache shared

2.2. Memory Subsystem

2.2.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports system code download through USB OTG
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

2.2.2. SDRAM

- Embedded with 1Gbit DDR3
- Supports clock frequency up to 792MHz for DDR3

2.3. System Peripherals

2.3.1. VAD

- Supports 3 I2S interfaces, 1 DMIC PDM audio transfer interface
- Supported sample rate: 16 kHz, 48 kHz
- Supports voice detection module based on energy recognition
- Supports 4 working status: idle, wait, run, normal
- Supports voice activity: idle-> energy wake-up
- Supports 128KB SRAM used to store audio data
- Supports hardware interpolation for audio data channel numbers, including 5 modes: 2chs-4chs, 2chs-6chs, 2chs-8chs, 4chs-6chs, 4chs-8chs
- Supports secure protection for register configuration
- Supports secure protection of VAD_SRAM
- Supports VAD bypass function, after bypass, VAD_SRAM can be used as on-chip SRAM to work individual

2.3.2. Timer

- The timer module implements the timing and counting functions, which includes Timer0,Timer1 and Watchdog
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factor
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing

2.3.3. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

2.3.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 137 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization
- Uniprocessor and multiprocessor environments
- ARM architecture security extensions
- ARM architecture virtualization extensions
- Wakeup events in power-management environments

2.3.5. DMA

- Up to 10-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.3.6. CCU

- 6 PLLs
- One on-chip RC oscillator
- Supports one external 24MHz DCXO and one external 32.768kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.3.7. Thermal Sensor Controller

- Temperature accuracy : ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- One thermal sensor located in CPU

2.3.8. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control and CP15 control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc
- Including CPU debug control and status register

2.3.9. LDO Power

- Integrated 2 LDOs(LDOA, LDOB)
- LDOA: 1.8V power output, LDOB: 1.35V/1.5V/1.8V power output
- LDOA for IO and analog module, LDOB for SDRAM
- Input voltage is 2.4V~3.6V

2.3.10. Reset

- Integrated internal reset, which can select reset source by RST-BYP-N pin
- Internal reset R328-S3, also reset other IC

2.4. Audio Subsystem

2.4.1. Audio Codec

- One audio digital-to-analog(DAC) channel
  - Supports 16-bit and 24-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95±2dB SNR@A-weight, -80±3dB THD+N
- One audio output:
  - One differential LINEOUTP/N or single-ended LINEOUTL output
- Three audio analog-to-digital(ADC) channels
  - Supports 16-bit and 24-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95±2dB SNR@A-weight, -80±3dB THD+N
- Three audio inputs:
  - Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, MICIN3P/3N
- One low-noise analog microphone bias output
- Supports Dynamic Range Controller adjusting the DAC playback and ADC capture
- One 128x24-bits FIFO for DAC data transmit, one 128x24-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- DMA and Interrupt support

2.4.2. I2S/PCM

- Up to three I2S/PCM interfaces
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and Time Division Multiplexing(TDM) format

- TDM mode supports maximum 16 channels output and 16 channels input
- Supports full-duplex synchronous work mode
- Supports master/slave mode
- Supports clock up to 24.576 MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 kHz to 384 kHz(channels =2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds

2.4.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.4.4. OWA

- One OWA TX and one OWA RX
- IEC-60958 transmitter and receiver functionality
- Supports channel status capture on the receiver
- Supports channel status insertion for the transmitter
- Hardware parity checking on the receiver
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit,20-bit and 24-bit data formats

2.5. Security Engine

2.5.1. Crypto Engine(CE)

- Supports Symmetrical algorithm: AES,DES,TDES
  - Supports ECB,CBC,CTS,CTR,CFB,OFB mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB,CBC,CTR mode for DES/TDES
- Supports Hash algorithm: MD5,SHA,HMAC
  - Supports SHA1,SHA224,SHA256,SHA384,SHA512 for SHA
  - Supports HMAC-SHA1,HMAC-SHA256 for HMAC
  - MD5,SHA,HMAC are padded using hardware
- Supports Asymmetrical algorithm: RSA
  - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively
- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group(sg) are supported for both input and output data
- DMA has multiple channels, each corresponding to one suit of algorithm

2.5.2. Security ID

- Supports 1Kbit EFUSE for chip ID and security application

- EFUSE has secure zone and non-secure zone

2.5.3. Secure Memory Control(SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

2.5.4. Secure Peripherals Control(SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.6. External Peripherals

2.6.1. SMHC

- One SD/MMC host controller(SMHC) interface
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
  - 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.6.2. USB

- One USB 2.0 OTG, with integrated USB 2.0 analog PHY
- Compatible with USB2.0 Specification
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
- Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
- Up to 8 User-Configurable Endpoints(EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
- Supports (4KB+64Bytes) FIFO for EPs(including EP0)
- Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode

2.6.3. UART

- Up to 4 UART controllers(UART0,UART1,UART2,UART3)
- UART0: 2-wire; UART1, UART2, UART3: 4-wire
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.6.4. SPI

- Up to 2 SPI controllers(SPI0,SPI1)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to 32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

2.6.5. Two Wire Interface(TWI)

- Up to 2 TWI controllers(TWI0,TWI1)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

2.6.6. PWM

- 8 PWM channels(4 PWM pairs)
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~24MHz/100MHz
- Various duty-cycle: 0%~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

2.6.7. Low Rate ADC(LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: AVCC, power reference voltage: 0.75*AVCC, analog input and detected voltage range: 0~LEVELB(the maximum value is 1.286V)

2.6.8. General Purpose ADC(GPADC)

- Four GPADC input channels
- Successive approximation register(SAR) analog-to-digital converter(ADC) with 12-bit resolution
- 64 FIFO depth of data register

- Power reference voltage: AVCC, analog input voltage range: 0~AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

2.6.9. LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s

2.7. Package

- LFBGA144 balls, 0.65mm ball pitch, 0.35mm ball size, 9.15mm x 11.1mm body

3. Block Diagram

Figure 3-1 shows the system block diagram of the R328-S3.

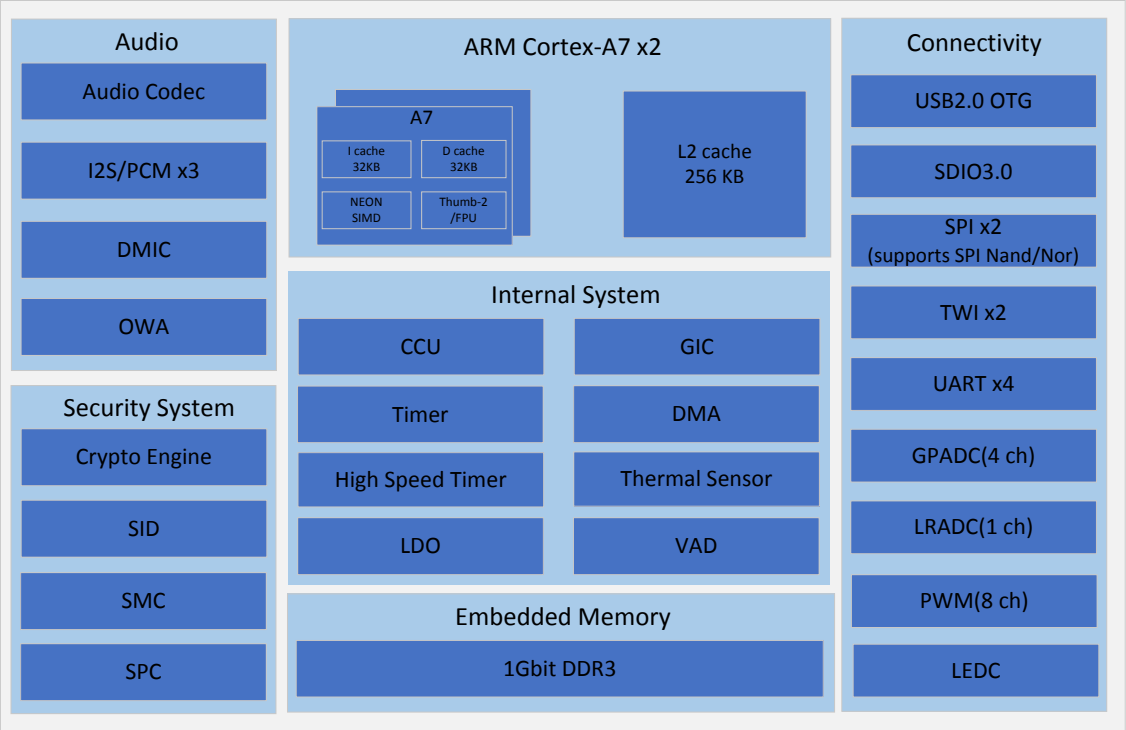


Figure 3-1. R328-S3 System Block Diagram

Figure 3-2 shows the intelligent speaker solution of the R328-S3.

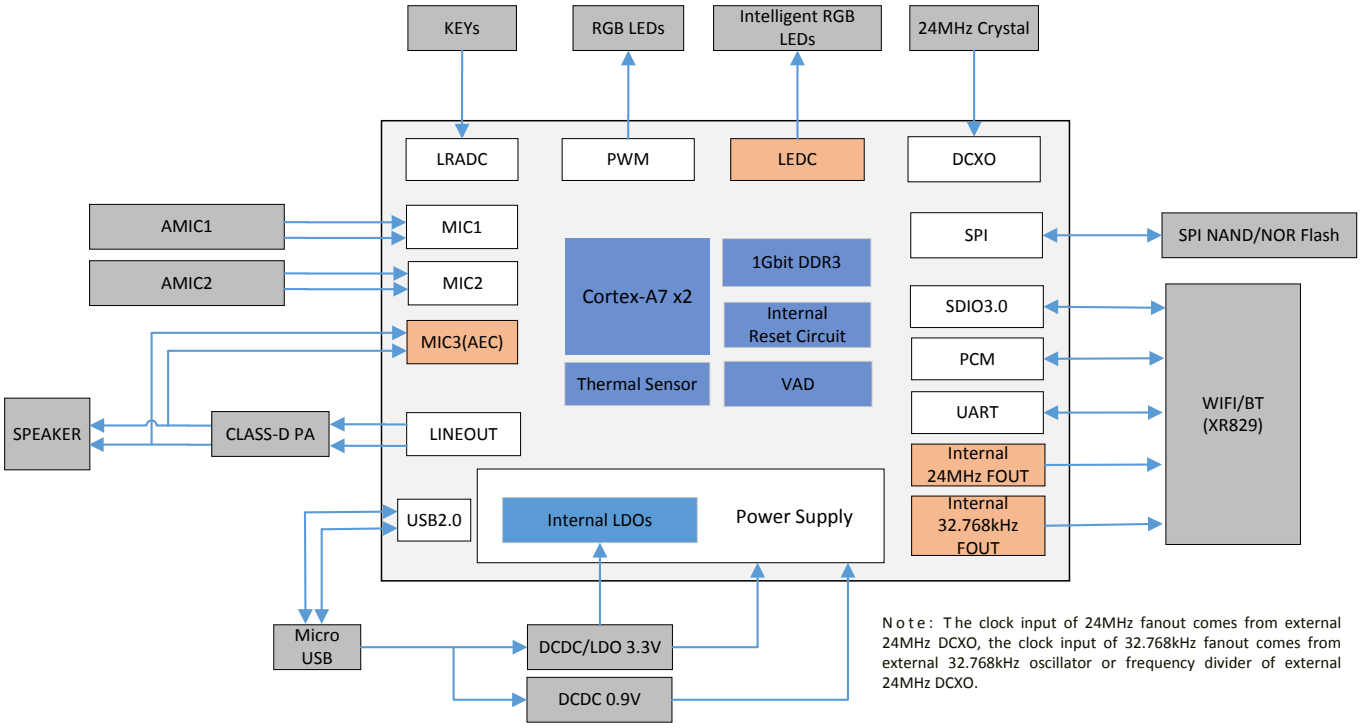


Figure 3-2. R328-S3 Intelligent Speaker Solution

4. Pin Description

4.1. Pin Quantity

Table 4-1 lists the pin quantity of the R328-S3.

Table 4-1. Pin Quantity

Pin Type	Quantity
I/O	87
Power	17
Ground	35
DDR Power	5
Total	144

4.2. Pin Characteristics

Table 4-2 lists the characteristics of the R328-S3 pins from the following seven aspects.
[1].Ball# : Package ball numbers associated with each signals.
[2].Pin Name : The name of the package pin.
[3].Type : Denotes the signal direction
I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
P (Power),
G (Ground)
[4].Ball Reset State : The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.
[5].Pull Up/Down : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.
[6].Default Buffer Strength : Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.
[7].Power Supply : The voltage supply for the terminal's IO buffers.

Table 4-2. Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
J9	DZQ	AI	NA	NA	NA	VCC-DRAM
J8	SZQ(2)	AI	NA	NA	NA	VCC-DRAM
E5	SVREF(3)	P	NA	NA	NA	VCC-DRAM
K1,K2,L1,L2	VCC-DRAM	P	NA	NA	NA	NA
GPIOB(7)						
N9	PB0	I/O	Z	PU/PD	4	VCC-IO
P8	PB1	I/O	Z	PU/PD	4	VCC-IO
M4	PB2	I/O	Z	PU/PD	4	VCC-IO
M3	PB3	I/O	Z	PU/PD	4	VCC-IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
P2	PB4	I/O	Z	PU/PD	4	VCC-IO
N1	PB5	I/O	Z	PU/PD	4	VCC-IO
P4	PB6	I/O	Z	PU/PD	4	VCC-IO
M5	PB7	I/O	Z	PU/PD	4	VCC-IO
N3	PB8	I/O	Z	PU/PD	4	VCC-IO
N4	PB9	I/O	Z	PU/PD	4	VCC-IO
M2	PB10	I/O	Z	PU/PD	4	VCC-IO
N2	PB11	I/O	Z	PU/PD	4	VCC-IO
P6	PB12	I/O	Z	PU/PD	4	VCC-IO
P5	PB13	I/O	Z	PU/PD	4	VCC-IO
GPIOC(7)						
J12	PC0(4)	I/O	Z	PU/PD	4	VCC-PC
J13	PC1	I/O	Z	PU/PD	4	VCC-PC
H13	PC2	I/O	Z	PU/PD	4	VCC-PC
G13	PC3(5)	I/O	PU	PU/PD	4	VCC-PC
D13	PC4	I/O	PU	PU/PD	4	VCC-PC
K11	PC15	I/O	Z	PU/PD	4	VCC-PC
G12	PC16(6)	I/O	Z	PU/PD	4	VCC-PC
E10	VCC-PC	P	NA	NA	NA	NA
GPIOE(7)						
N8	PE0	I/O	Z	PU/PD	4	VCC-PE
P9	PE1	I/O	Z	PU/PD	4	VCC-PE
P12	PE2	I/O	Z	PU/PD	4	VCC-PE
J14	PE3	I/O	Z	PU/PD	4	VCC-PE
P13	PE4	I/O	Z	PU/PD	4	VCC-PE
K14	PE5	I/O	Z	PU/PD	4	VCC-PE
N14	PE6	I/O	Z	PU/PD	4	VCC-PE
E12	VCC-PE	P	NA	NA	NA	NA
GPIOG(7)						
B2	PG0	I/O	Z	PU/PD	4	VCC-PG
D2	PG1	I/O	Z	PU/PD	4	VCC-PG
C2	PG2	I/O	Z	PU/PD	4	VCC-PG
C4	PG3	I/O	Z	PU/PD	4	VCC-PG
B3	PG4	I/O	Z	PU/PD	4	VCC-PG
B1	PG5	I/O	Z	PU/PD	4	VCC-PG
G1	PG6	I/O	Z	PU/PD	4	VCC-PG
H2	PG7	I/O	Z	PU/PD	4	VCC-PG
D3	PG8	I/O	Z	PU/PD	4	VCC-PG
F2	PG9	I/O	Z	PU/PD	4	VCC-PG
F3	PG10	I/O	Z	PU/PD	4	VCC-PG
G2	PG11	I/O	Z	PU/PD	4	VCC-PG
J2	PG12	I/O	Z	PU/PD	4	VCC-PG
E2	PG13	I/O	Z	PU/PD	4	VCC-PG

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
H1	PG14	I/O	Z	PU/PD	4	VCC-PG
C5	VCC-PG	P	NA	NA	NA	NA
GPIOH(7)						
N7	PH0	I/O	Z	PU/PD	4	VCC-IO
L14	PH1	I/O	Z	PU/PD	4	VCC-IO
M10	PH2	I/O	Z	PU/PD	4	VCC-IO
N12	PH3	I/O	Z	PU/PD	4	VCC-IO
M11	PH4	I/O	Z	PU/PD	4	VCC-IO
N11	PH5	I/O	Z	PU/PD	4	VCC-IO
N13	PH6	I/O	Z	PU/PD	4	VCC-IO
M13	PH7	I/O	Z	PU/PD	4	VCC-IO
M12	PH8	I/O	Z	PU/PD	4	VCC-IO
N10	PH9	I/O	Z	PU/PD	4	VCC-IO
System						
C7	RESET(8)	OD	Z	PU/PD	NA	VCC-PLL
D5	RST-BYP-N	I	PU	PU/PD	NA	VCC-PLL
E4	TEST(9)	I	PD	PU/PD	NA	VCC-PLL
GPADC						
C8	GPADC0	AI	NA	NA	NA	AVCC
B7	GPADC1	AI	NA	NA	NA	AVCC
B8	GPADC2	AI	NA	NA	NA	AVCC
A8	GPADC3	AI	NA	NA	NA	AVCC
LRADC						
D9	LRADC	AI	NA	NA	NA	AVCC
USB						
A2	USB0-DM(10)	A I/O	NA	NA	NA	VCC-IO
A1	USB0-DP(10)	A I/O	NA	NA	NA	VCC-IO
Audio Codec						
A13	MICIN1P(11)	AI	NA	NA	NA	AVCC
B13	MICIN1N(11)	AI	NA	NA	NA	AVCC
B12	MICIN2P(11)	AI	NA	NA	NA	AVCC
A12	MICIN2N(11)	AI	NA	NA	NA	AVCC
B14	MICIN3P(11)	AI	NA	NA	NA	AVCC
C14	MICIN3N(11)	AI	NA	NA	NA	AVCC
C9	MBIAS	AO	NA	NA	NA	VCC-IO
D12	VRA1(13)	AO	NA	NA	NA	AVCC
D11	VRA2(13)	AO	NA	NA	NA	AVCC
B9	VRP(13)	AO		NA	NA	AVCC
B10	AVCC(12) (13)	P	NA	NA	NA	NA
C12	LINEOUTN	AO	NA	NA	NA	AVCC
C13	LINEOUTP	AO	NA	NA	NA	AVCC
A10	AGND	G	NA	NA	NA	NA
C10	REXT	AO	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
RTC&PLL						
B5	X32KIN(14)	AI	NA	NA	NA	VCC-PLL
A4	X32KOUT(14)	AO	NA	NA	NA	VCC-PLL
B4	X32KFOUT(15)	OD	NA	NA	NA	VCC-PLL
D6	PLLTEST	OD	NA	NA	NA	VCC-PLL
D4	VCC-PLL	P	NA	NA	NA	NA
DCXO						
B6	DXIN	AI	NA	NA	NA	VCC-PLL
A6	DXOUT(16)	AO	NA	NA	NA	VCC-PLL
A5	DXLDO-OUT	AO	NA	NA	NA	VCC-PLL
E3	REFCLK-OUT	AO	NA	NA	NA	VCC-PLL
Power						
B11	LDO-IN	P	NA	NA	NA	NA
D10	LDOA-OUT	P	NA	NA	NA	NA
C11	LDOB-OUT	P	NA	NA	NA	NA
K7	VCC-EFUSE	P	NA	NA	NA	NA
K8	VDD-CPUFB	P	NA	NA	NA	NA
F12	VCC-IO	P	NA	NA	NA	NA
F9,G9,G10,H9	VDD-CPU	P	NA	NA	NA	NA
G6,G7,J7	VDD-SYS	P	NA	NA	NA	NA
Ground						
A14,C6,D8,E6, E7,E8,E9,F5,F6, F7,G4,G5,H3, H6,J1,J3,J4,K4, K10,L3,L4,L5,L6 ,L7,D7,G8,K3, M6,M7,M8,N5, N6,P1,P14	GND	G	NA	NA	NA	NA

(1).NA: no application.

(2).SZQ is an analog input signal that connects to an external 240Ω -1% grounded resistor which is used to calibrate the DDR PHY impedance.

(3).SVREF is a reference voltage input used to set the electric level of IO input buffers. The reference electric level is (VCC-DRAM/2).

(4).SPI-CLK is used to output clock to SPI flash. Suggest that connect to a 33Ω resistor in series to offer impedance matching and reduce high-frequency radiation.

(5).SPI-CS is low active and has an internal pull-up.

(6).SPI-HOLD is low active. For some SPI flash devices, their SPI-HOLD and Reset signals are multiplexed, in order to compatibility, SPI-HOLD needs an external pull-up resistor.

(7).If all IOs of a GPIO port are unused, we suggest that the GPIO port has normal power supply, all IOs shall be floated or connected to GND, and the corresponding register of all IOs can be set to Disable.

(8).RESET needs ESD protection and is suggested to connect to a external pull-up resistor.

(9).TEST is CP test signal that shall be floated.

(10).The differential characteristics impedance of each pair of differential signals (USB0-DP, USB0-DM) must be within (90Ω±20%).

(11).MICIN[3:1]P/[3:1]N is analog differential input signals that shall be far away from interference signals.

(12).AVCC is as the reference voltage of the internal analog circuit, so ACC shall be ensured ±2% voltage accuracy.

(13).The external capacitors of AVCC, VRP, VRA1, VRA2 shall be placed near the R328-S3 chip, and in order to reduce loop area, the negative terminals of these capacitors shall be placed near AGND.

(14).A 10MΩ resister is connected in parallel between X32KOUT and X32KIN, the resistor can create negative feedback in an inverter to ensure amplifier in linear amplifier region.
(15).32KFOUT can output 32.768kHz clock by software configuration to provide external Bluetooth to use. The 32KFOUT is open-drain output that connects to a pull-up resistor and then connects to working voltage.
(16).DXOUT connects to a 0Ω resistor in series by default, changing the resistor value can adjust clock buffer strength to restrain EMI.

For details about schematic diagram and PCB design recommendations, see the ***Allwinner R328-S3 Hardware Design Guide***.

4.3. GPIO Multiplex Function

The following table provides a description of the R328-S3 GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

Table 4-3. GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PB0	GPIOB	I/O	UART2-TX	PWM0	JTAG-MS	LEDC-DO	PB-EINT0
PB1		I/O	UART2-RX	PWM1	JTAG-CK		PB-EINT1
PB2		I/O	UART2-RTS	PWM2	JTAG-DO	I2S0-LRCK	PB-EINT2
PB3		I/O	UART2-CTS	PWM3	JTAG-DI	I2S0-BCLK	PB-EINT3
PB4		I/O		PWM4	I2S0-DOUT0	I2S0-DIN1	PB-EINT4
PB5		I/O		PWM5	I2S0-DOUT1	I2S0-DIN0	PB-EINT5
PB6		I/O		PWM6	I2S0-DOUT2	I2S0-DIN3	PB-EINT6
PB7		I/O		PWM7	I2S0-DOUT3	I2S0-DIN2	PB-EINT7
PB8		I/O	I2S1-LRCK	DMIC-DATA3	TWI1-SCK	UART0-TX	PB-EINT8
PB9		I/O	I2S1-BCLK	DMIC-DATA2	TWI1-SDA	UART0-RX	PB-EINT9
PB10		I/O	I2S1-DOUT0	DMIC-DATA1	I2S1-DIN1	UART2-RTS	PB-EINT10
PB11		I/O	I2S1-DOUT1	DMIC-DATA0	I2S1-DIN0	UART2-CTS	PB-EINT11
PB12		I/O	I2S1-MCLK	DMIC-CLK			PB-EINT12
PB13		I/O				I2S0-MCLK	PB-EINT13
PC0	GPIOC	I/O			SPI0-CLK		
PC1		I/O					
PC2		I/O			SPI0-MOSI		
PC3		I/O			SPI0-CS0		
PC4		I/O			SPI0-MISO		
PC15		I/O			SPI0-WP		
PC16		I/O			SPI0-HOLD		
PE0	GPIOE	I/O	I2S1-MCLK		UART2-RTS		PE-EINT0
PE1		I/O	OWA-OUT		OWA-IN		PE-EINT1
PE2		I/O	LEDC-DO				PE-EINT2
PE3		I/O	I2S1-LRCK		UART2-TX		PE-EINT3
PE4		I/O	I2S1-BCLK		UART2-RX		PE-EINT4
PE5		I/O	I2S1-DOUT0	I2S1-DIN1	PLL-LOCK-DBG		PE-EINT5
PE6		I/O	I2S1-DOUT1	I2S1-DIN0	UART2-CTS		PE-EINT6
PG0	GPIOG	I/O	SDC1-CLK				PG-EINT0
PG1		I/O	SDC1-CMD				PG-EINT1
PG2		I/O	SDC1-D0				PG-EINT2
PG3		I/O	SDC1-D1				PG-EINT3
PG4		I/O	SDC1-D2				PG-EINT4
PG5		I/O	SDC1-D3				PG-EINT5

PG6		I/O	UART1-TX				PG-EINT6
PG7		I/O	UART1-RX				PG-EINT7
PG8		I/O	UART1-RTS				PG-EINT8
PG9		I/O	UART1-CTS				PG-EINT9
PG10		I/O		I2S2-MCLK			PG-EINT10
PG11		I/O		I2S2-LRCK		BIST-RESULT0	PG-EINT11
PG12		I/O		I2S2-BCLK		BIST-RESULT1	PG-EINT12
PG13		I/O		I2S2-DOUT0	I2S2-DIN1		PG-EINT13
PG14		I/O		I2S2-DOUT1	I2S2-DIN0		PG-EINT14
PH0	GPIOH	I/O	TWI0-SCK	UART0-TX	SPI1-MOSI		PH-EINT0
PH1		I/O	TWI0-SDA	UART0-RX	SPI1-CLK		PH-EINT1
PH2		I/O	TWI1-SCK	LEDC-DO	SPI1-CS		PH-EINT2
PH3		I/O	TWI1-SDA	OWA-OUT	SPI1-MISO		PH-EINT3
PH4		I/O	UART3-TX	SPI1-CS			PH-EINT4
PH5		I/O	UART3-RX	SPI1-CLK			PH-EINT5
PH6		I/O	UART3-RTS	SPI1-MOSI			PH-EINT6
PH7		I/O	UART3-CTS	SPI1-MISO			PH-EINT7
PH8		I/O	LEDC-DO	OWA-IN			PH-EINT8
PH9		I/O			CPU-CUR-W		PH-EINT9

4.4. Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.
[1].Signal Name: The name of every signal.
[2].Description: The detailed function description of every signal.
[3].Type: Denotes the signal direction:
I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-4. Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
DZQ	DRAM ZQ Calibration for DDR3 Device	AI
SZQ	DRAM ZQ Calibration	AI
SVREF	DRAM Reference Voltage Input	P
VCC-DRAM	DRAM Power Supply	P
System Control		
TEST	Test Signal	I
RESET	Reset Signal(low active)	I/O
RST-BYP-N	Reset Source Select 0: use external reset Floating: use internal reset	I
Clock		
X32KIN	Clock Input of 32.768kHz Crystal	AI

Signal Name[1]	Description[2]	Type[3]
X32KOUT	Clock Output of 32.768kHz Crystal	AO
X32KFOUT	32.768kHz Clock Fanout Provides low frequency clock for external devices	OD
PLLTEST	PLL Test	OD
VCC-PLL	PLL Power Supply	P
DCXO		
DXLDO-OUT	Internal Supply Regulator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
USB		
USB0-DM	USB Data Signal DM	A I/O
USB0-DP	USB Data Signal DP	A I/O
GPADC		
GPADC0	General Purpose ADC Input Channel 0	AI
GPADC1	General Purpose ADC Input Channel 1	AI
GPADC2	General Purpose ADC Input Channel 2	AI
GPADC3	General Purpose ADC Input Channel 3	AI
LRADC		
LRADC	Low Rate ADC Input Channel	AI
AUDIO CODEC		
LINEOUTP	Differential Mono Positive Output(or Left Single-end Output for Lineout)	AO
LINEOUTN	Differential Mono Negative Output	AO
MBIAS	Master Analog Microphone Bias Voltage Output	AO
MICIN1P	Microphone Positive Input 1	AI
MICIN1N	Microphone Negative Input 1	AI
MICIN2P	Microphone Positive Input 2	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN3P	Microphone Positive Input 3	AI
MICIN3N	Microphone Negative Input 3	AI
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
REXT	External Reference Pin	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
SMHC		
SDC1-CMD	Command Signal for SDIO WIFI	OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
I2S/PCM		
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Sample Rate Clock	I/O

Signal Name[1]	Description[2]	Type[3]
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Sample Rate Clock	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Sample Rate Clock	I/O
I2S2-DOUT[1:0]	I2S2/PCM2 Serial Data Output Channel [1:0]	O
I2S2-DIN[1:0]	I2S2/PCM2 Serial Data Input Channel [1:0]	I
DMIC		
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA[3:0]	Digital Microphone Data Input	I
OWA		
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O
LEDC		
LEDC-DO	Intelligent Control LED Signal Output	O
Interrupt		
PB-EINT[13:0]	GPIO B Interrupt	I
PE-EINT[6:0]	GPIO E Interrupt	I
PG-EINT[14:0]	GPIO G Interrupt	I
PH-EINT[9:0]	GPIO H Interrupt	I
PWM		
PWM[7:0]	Pulse Width Modulation Output Channel [7:0]	I/O
SPI		
SPI0-CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active	I/O
SPI0-HOLD	SPI0 Hold Signal	I/O
SPI1-CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
UART		
UART0-TX	UART0 Data Transmit	O
UART0-RX	UART0 Data Receive	I
UART1-TX	UART1 Data Transmit	O
UART1-RX	UART1 Data Receive	I
UART1-CTS	UART1 Data Clear to Send	I

Signal Name[1]	Description[2]	Type[3]
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmit	O
UART2-RX	UART2 Data Receive	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmit	O
UART3-RX	UART3 Data Receive	I
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
TWI		
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
JTAG		
JTAG-MS	JTAG Mode Select	I
JTAG-CK	JTAG Clock Signal	I
JTAG-DO	JTAG Data Output	O
JTAG-DI	JTAG Data Input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
AVCC	Power Supply for Analog Part		-0.3	2.16	V
VCC-PC	Digital GPIO C Power		-0.3	3.96	V
VCC-PE	Digital GPIO E Power		-0.3	3.96	V
VCC-PG	Digital GPIO G Power		-0.3	3.96	V
VCC-IO	Power Supply for 3.3V Digital Part		-0.3	3.96	V
VCC-PLL	Power Supply for System PLL		-0.3	2.16	V
VCC-EFUSE	Power Supply for EFUSE Program Mode		-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM		-0.3	1.8	V
VDD-CPU	Power Supply for CPU		-0.3	1.1	V
VDD-SYS	Power Supply for System		-0.3	1.1	V
LDO-IN	Internal LDOA/B Input Voltage		-0.3	3.96	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO		-0.3	2.16	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM		-0.3	2.16	V
T_{STG}	Storage Temperature		-40	150	°C
Tj	Working Junction Temperature		-40	125	°C
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM)(1)	-2000	2000	V
		Charged Device Model(CDM)(2)	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(3)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(4)		Pass		

(1). Test method: JEDEC JS-001-2014. JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JEDEC JS-002-2014. JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D(Class I) and passed with I/O pin injection current as defined in JEDEC.

(4). Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I) and passed voltage injection as defined in JEDEC.

5.2. Recommended Operating Conditions

All R328-S3 modules are used under the operating conditions contained in Table 5-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature(when VCC-DRAM uses external power)	-20	-	85	°C
	Ambient Operating Temperature(when VCC-DRAM uses internal LDO)	-20	-	70	°C
Tj	Working Junction Temperature Range	-20	-	110(1)	°C
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VCC-PC	Digital GPIO C Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Digital GPIO E Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PG	Digital GPIO G Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-IO	Power Supply for 3.3V Digital Part	2.97	3.3	3.63	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-EFUSE	Power Supply for EFUSE Program Mode	1.8	1.89	1.98	V
VCC-DRAM	Power Supply for DRAM IO and DDR3	1.425	1.5	1.575	V
VDD-CPU	Power Supply for CPU	0.81	0.9	1.1	V
VDD-SYS	Power Supply for System	0.81	0.9	1.1	V
LDO-IN	Internal LDOA/B Input Voltage	2.4	3.3	3.6	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO	1.746	1.8	1.854	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	1.31 1.455 1.746	1.35(2) 1.5 1.8	1.39 1.545 1.854	V

(1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.
(2). The default voltage of LDOB-OUT is 1.35V.

5.3. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

5.4. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of the R328-S3.

Table 5-3. DC Electrical Characteristics (VCC-IO/VCC-PC/VCC-PE/VCC-PG)

Symbol	Parameter	Min	Typ	Max	Unit

V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	50 10	100 20(1)	150 30	kΩ
R_{PD}	Input Pull-down Resistance	50 10	100 20(1)	150 30	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO – 0.3	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

(1). The typical pull-up/down resistance of PC3 is 20kΩ, other GPIO pull-up/down resistances are 100kΩ.

5.5. SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

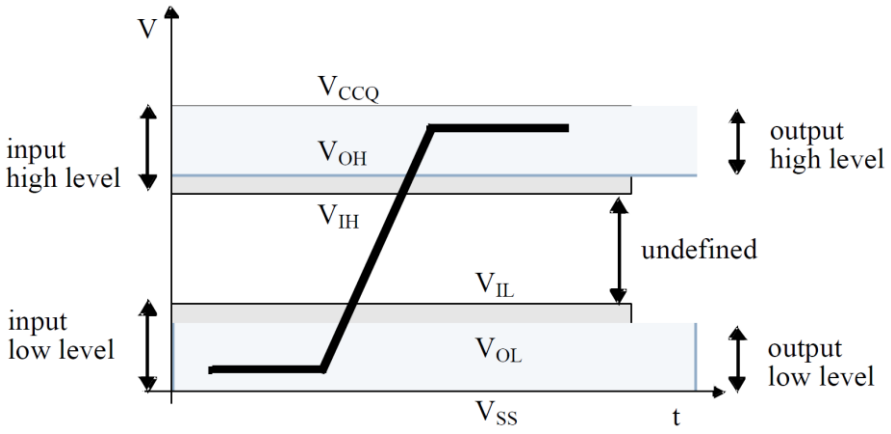


Table 5-4 shows 3.3V SDIO electrical parameters.

Table 5-4. 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8V SDIO electrical parameters.

Table 5-5. 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V

V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6. GPADC Electrical Characteristics

GPADC contains 4-ch analog-to-digital(ADC) converter. The ADC is a type of successive approximation register(SAR) converter. Table 5-6 lists GPADC electrical characteristics.

Table 5-6. GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.7. LRADC Electrical Characteristics

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 2kHz conversion rate. Table 5-7 lists LRADC electrical characteristics.

Table 5-7. LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.286V. For details, see the register description of LRADC in ***Allwinner_R328-S3_User_Manual.***				

5.8. Audio Codec Electrical Characteristics

TBD

5.9. Clock Electrical Characteristics

5.9.1. Input Clock Requirements

The R328-S3 has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal.
The 24MHz oscillator provides a 24MHz reference clock which is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through DXIN. Table 5-8 lists the recommended values of 24MHz crystal.

Table 5-8. 24MHz DCXO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit

$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24	-	MHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-20	-	+20	ppm
C_L	Equivalent Load Capacitance	12	18	22	pF
C_{SHUNT}	Shunt Capacitance	-	3	-	pF

The 32.768kHz oscillator provides a 32.768kHz reference clock which is used for RTC and low frequency operation. It supplies the wake-up domain for operation in low-power mode. The clock is provided through X32KIN. Table 5-9 lists the recommended values of 32.768kHz crystal.

Table 5-9. 32.768kHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	32.768	-	kHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-20	-	+20	ppm
C_L	Equivalent Load Capacitance	12	18	22	pF
C_{SHUNT}	Shunt Capacitance	-	1.1	-	pF

5.9.2. Output Clock Characteristics

The X32KFOUT signal can output 32.768kHz clock. Table 5-10 lists the output clock characteristics.

Table 5-10. X32KFOUT Output Clock Characteristics

Parameter	Specification	Unit
Input Source	24MHz crystal or 32.768kHz crystal	-
Nominal Output Frequency	32.768	kHz
Frequency Accuracy	±30	ppm
Duty Cycle	50	%
Output Signal Amplitude	Open-drain	-
Signal Type	Square-wave	-

NOTE

The output frequency accuracy is related to the accuracy of external crystal.

5.10. Internal Reset Electrical Characteristics

Table 5-11. Internal Reset Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max
Reset voltage threshold	Ta= -20°C to 85°C	-	0.4V	-
Reset active timeout period	Ta= -20°C to 85°C	-	150ms	170ms
Reset open-drain output voltage	Ta= -20°C to 85°C,pull up 3.3V	-0.3V	-	0.3*VCC
The rising rate of VDD-SYS	V_{low}=0.1V, V_{high}=0.8V, Ta=-20°C to 85°C	-	-	1ms

5.11. External Peripheral Electrical Characteristics

5.11.1. SMHC AC Electrical Characteristics

(1) SDR Mode

It is used for DS, HS, SDR12, SDR25, SDR50, SDR104(<100MHz).

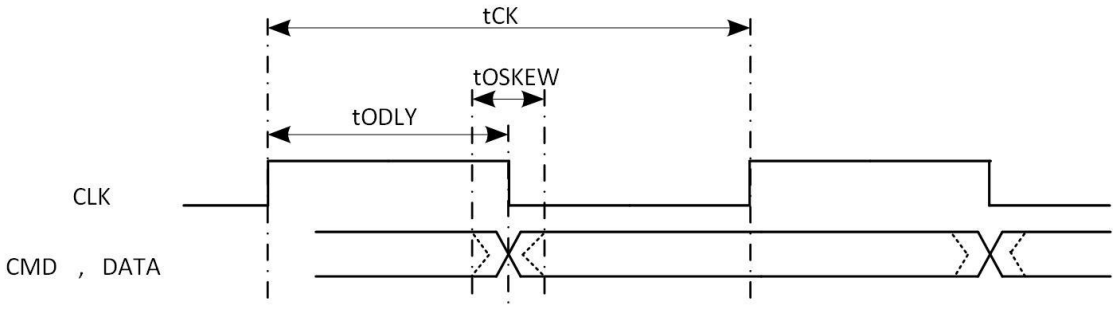


Figure 5-2. SMHC1 SDR Mode Output Timing Diagram

Table 5-12. SMHC1 SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	0.25	0.5	0.75	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

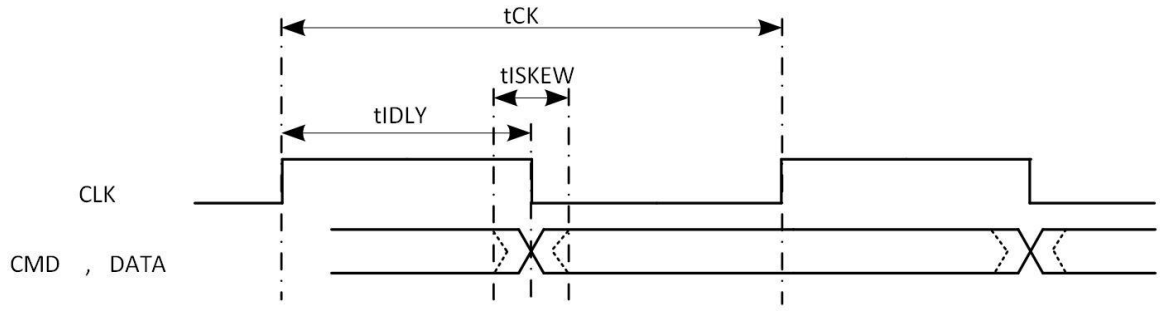


Figure 5-3. SMHC1 SDR Mode Input Timing Diagram

Table 5-13. SMHC1 SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	21.6	ns
Data input skew time in SDR mode	tISKEW	-	-	1.7	ns
The GPIO's driver strength level is 2 for test.					

(2) DDR50 Mode

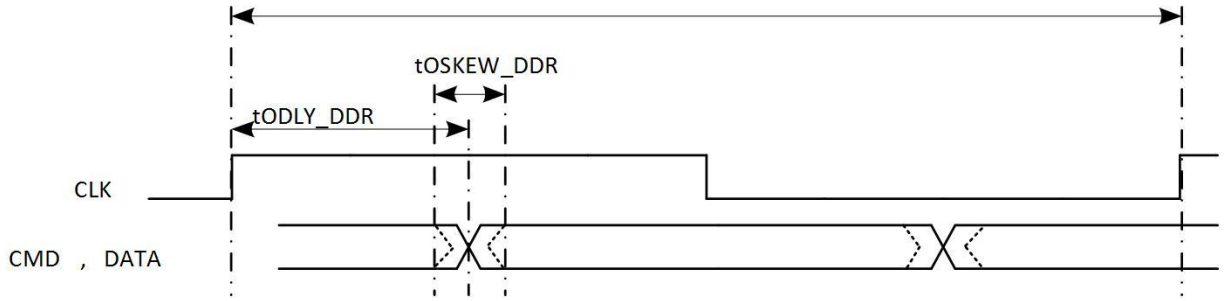


Figure 5-4. SMHC1 DDR50 Mode Output Timing Diagram

Table 5-14. SMHC1 DDR50 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	0.12	0.25	0.37	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

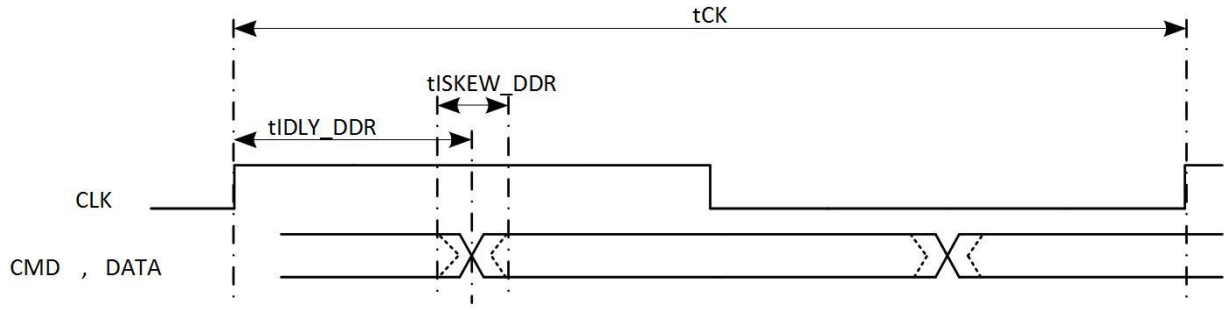


Figure 5-5. SMHC1 DDR50 Mode Input Timing Diagram

Table 5-15. SMHC1 DDR50 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	6.6	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.5	ns
The GPIO's driver strength level is 2 for test.					

(3) SDR104 Mode(>100MHz)

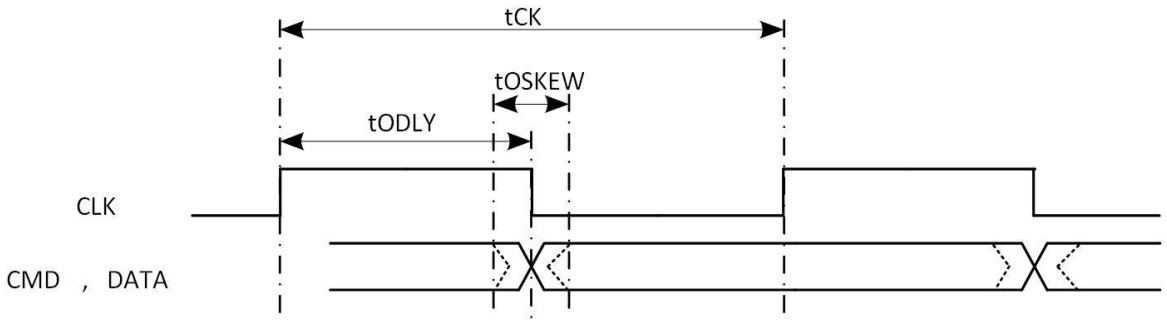


Figure 5-6. SMHC1 SDR104 Mode Output Timing Diagram

Table 5-16. SMHC1 SDR104 Mode Output Timing Constants

Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

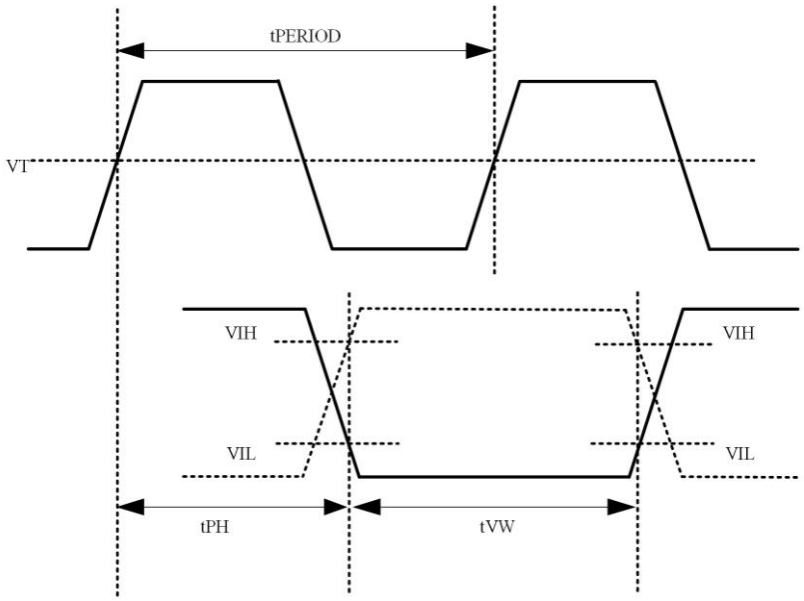


Figure 5-7. SMHC1 SDR104 Mode Input Timing Diagram

Table 5-17. SMHC1 SDR104 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. (2).The GPIO's driver strength level is 3 for test. (3).Temperature variation: -20°C.						

(4).Temperature variation: 90°C.

5.11.2. SPI AC Electrical Characteristics

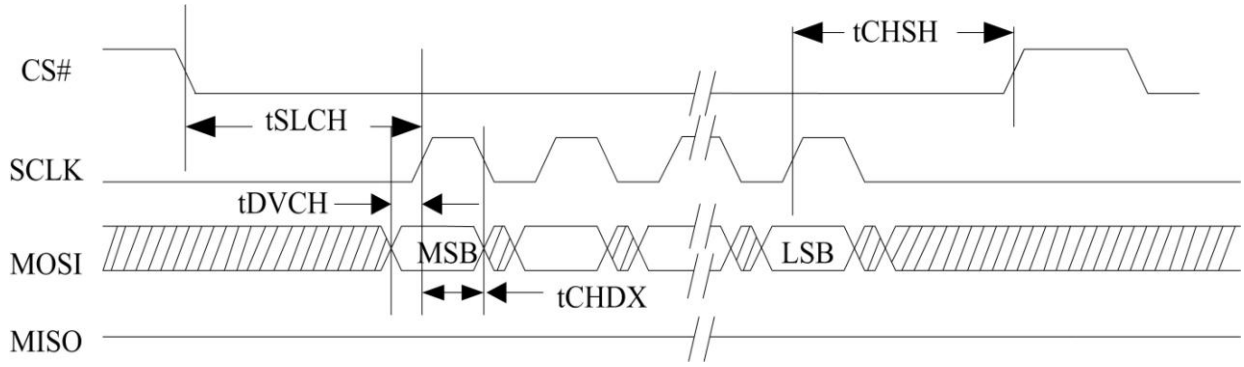


Figure 5-8. SPI MOSI Timing

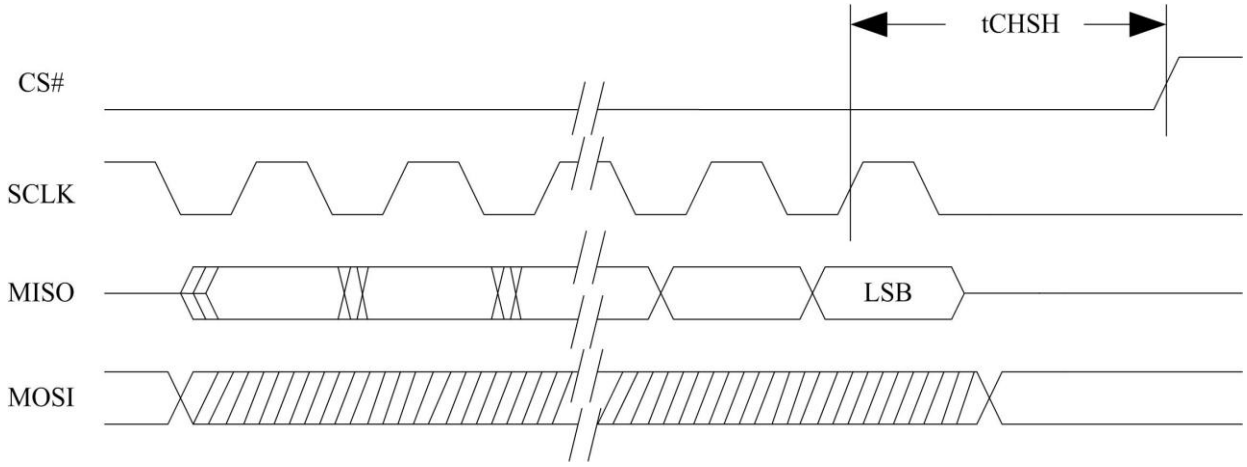


Figure 5-9. SPI MISO Timing

Table 5-18. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T(1)	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
NOTE (1):T is the cycle of clock.					

5.11.3. UART AC Electrical Characteristics

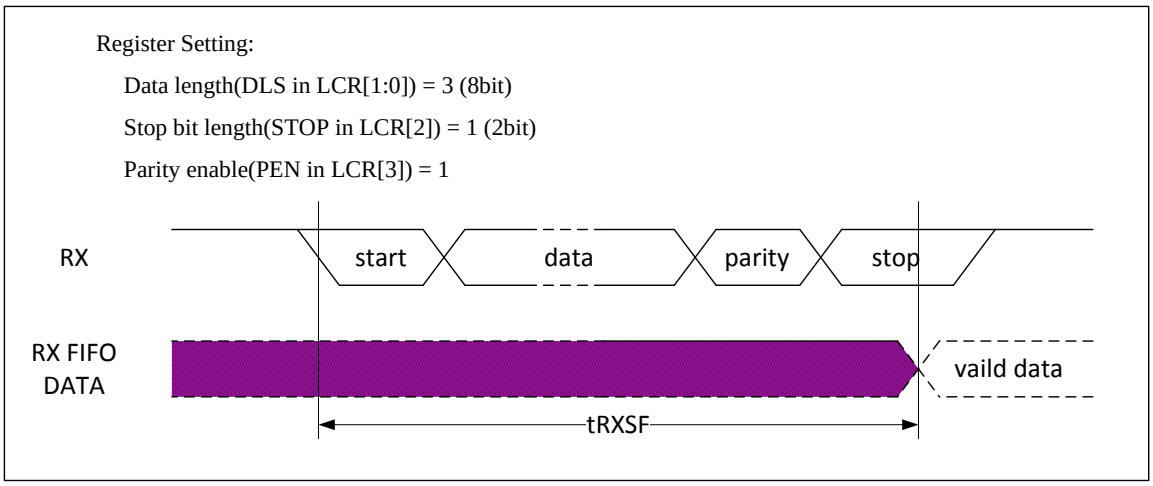


Figure 5-10. UART RX Timing

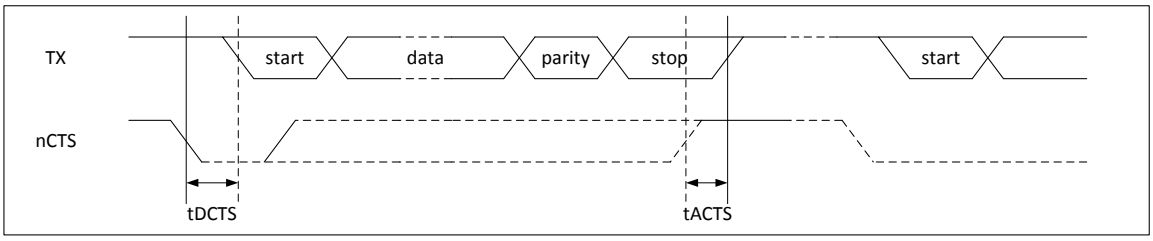


Figure 5-11. UART nCTS Timing

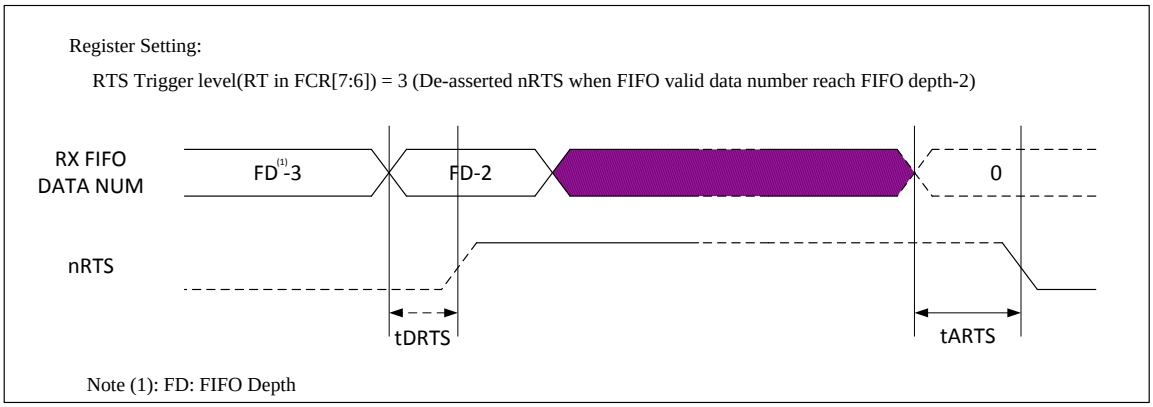


Figure 5-12. UART nRTS Timing

Table 5-19. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
NOTE (1): BRP(Baud-Rate Period).					

5.11.4. TWI AC Electrical Characteristics

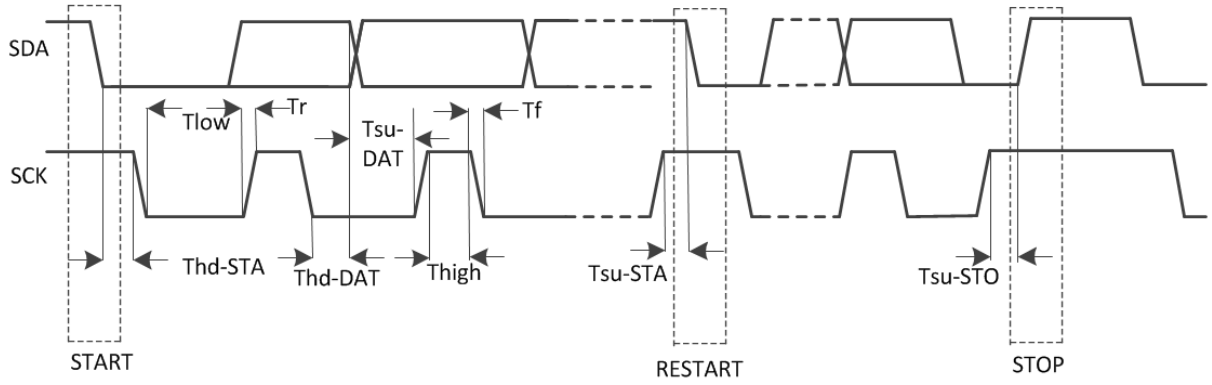


Figure 5-13. TWI Timing

Table 5-20. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.11.5. I2S/PCM AC Electrical Characteristics

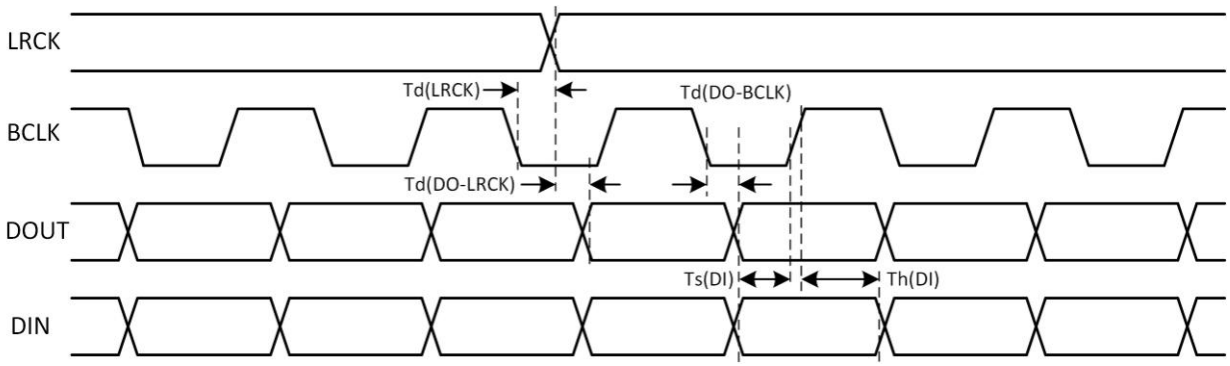


Figure 5-14. I2S/PCM Timing in Master Mode

Table 5-21. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

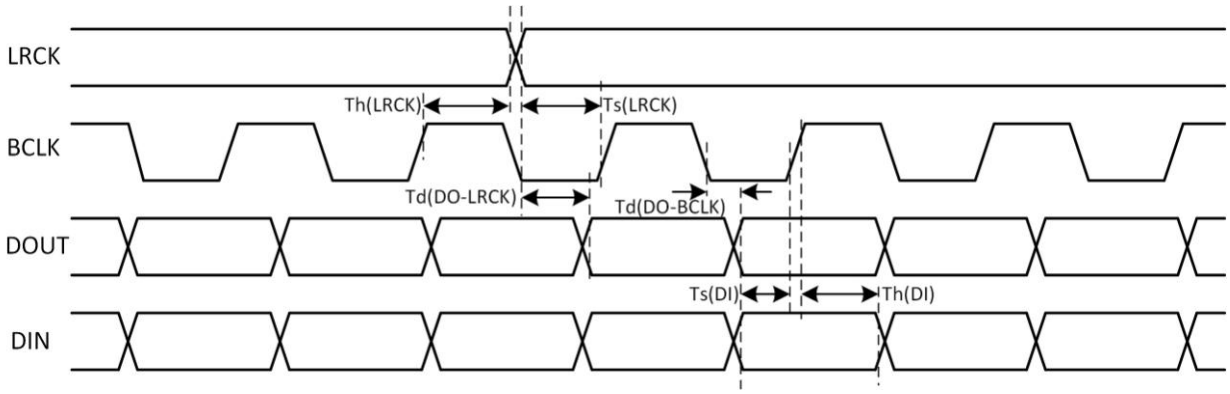


Figure 5-15. I2S/PCM Timing in Slave Mode

Table 5-22. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.11.6. DMIC AC Electrical Characteristics

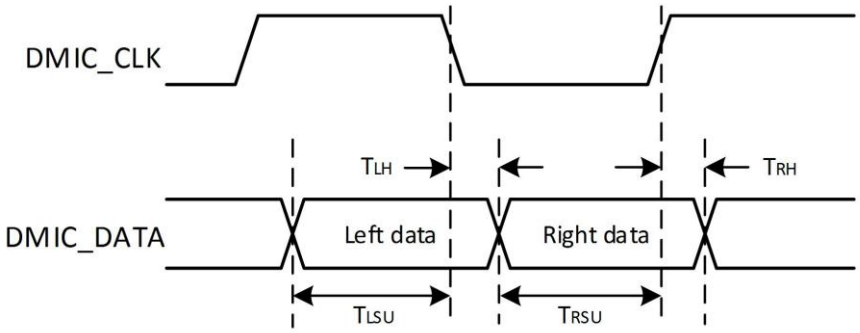


Figure 5-16. DMIC Timing

Table 5-23. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Left) setup time to falling edge of DMIC_CLK	TLSU	15	-	-	ns
DMIC_DATA(Left) hold time from falling edge of DMIC_CLK	TLH	0	-	-	ns
DMIC_DATA(Right) setup time to rising edge of DMIC_CLK	TRSU	15	-	-	ns
DMIC_DATA(Right) hold time from rising edge of DMIC_CLK	TRH	0	-	-	ns

5.11.7. OWA AC Electrical Characteristics

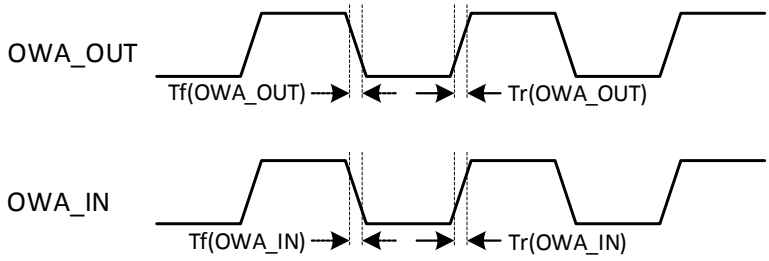


Figure 5-17. OWA Timing

Table 5-24. OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN rise time	Tr(OWA_IN)	-	-	4	ns
OWA_IN fall time	Tf(OWA_IN)	-	-	4	ns

5.12. Power-On and Power-Off Sequence

5.12.1. Power-On Sequence

Figure 5-18 shows an example of the power on sequence for the R328-S3 device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- VCC-IO must be ramped before VDD-SYS with a minimum delay of 800us.
- In order to prevent unintentional programming, VDD-SYS must be ramped before VCC-EFUSE with a minimum delay of 1ms.
- VCC-EFUSE needs be stable before eFuse programming.
- 24MHz clock needs to start oscillating and be stable.
- VCC-DRAM needs be stable before SDRAM driver initialization.
- When using external reset, during the entire power on sequence, the external RESET pin must be held on low until 24MHz clock and all other power rails(except VCC-DRAM and VCC-EFUSE) are stable.
- When using internal reset, the internal RESET also starts to ramp when VCC-IO ramps, and starts to power down when VDD-SYS ramps, and holds on low for a while, then the internal RESET starts to ramp after 24MHz clock and all other power rails(except VCC-DRAM and VCC-EFUSE) are stable with a minimum delay of 20ms.

NOTE

External RESET and internal RESET are not used simultaneously.

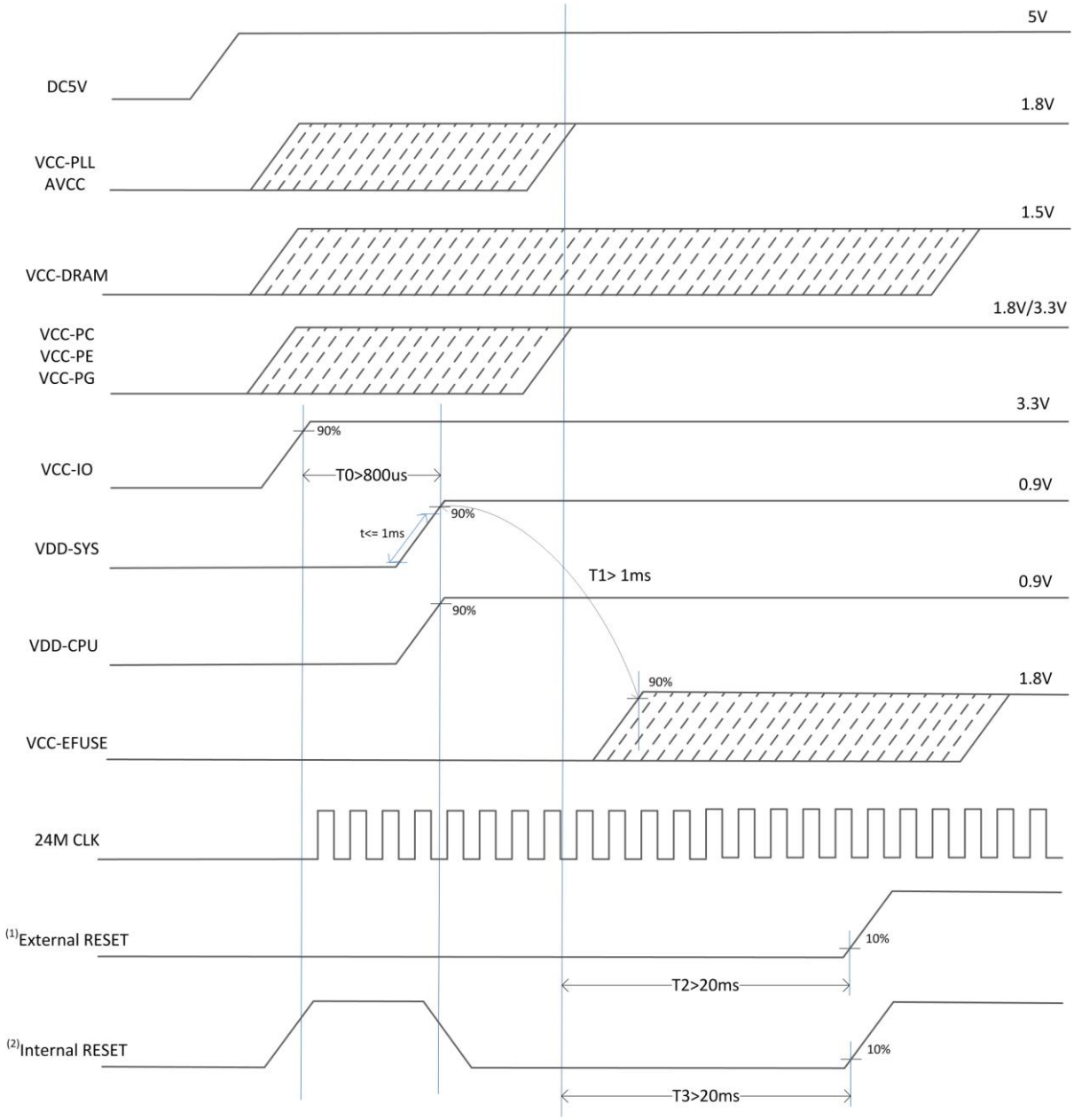


Figure 5-18. Power On Timing

CAUTION

When using internal reset, the ramp-up slew rate time of VDD-SYS from 0.1V to 0.8V cannot exceed 1ms, otherwise the reset is unsuccessful.

The internal LDO power sequence is as follows. The default voltage of LDOB is 1.35V, then it jumps to 1.5V.

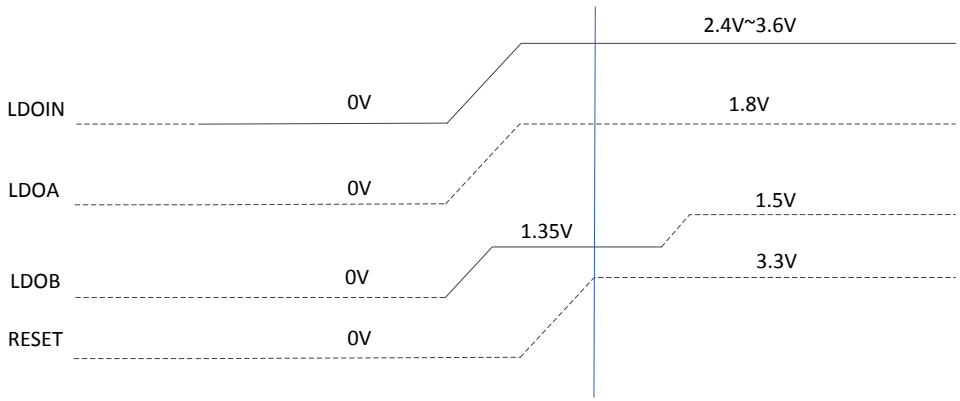


Figure 5-19. Internal LDO Sequence

5.12.2. Power-Off Sequence

The power-off requirements are as follows.

- In order to prevent unintentional programming, VCC-EFUSE must be prior to VDD-SYS power off with a minimum delay of 1ms.
- After VCC-PLL goes low, 24MHz clock starts to stop oscillating.
- No special restrictions for other power rails.

6. Package Thermal Characteristics

Table 6-1 shows thermal resistance parameters of the R328-S3. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board, natural convection, no air flow.

Table 6-1. R328-S3 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	28.9	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	14.7	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	9.2	-	°C/W

7. Pin Assignment

7.1. Pin Map

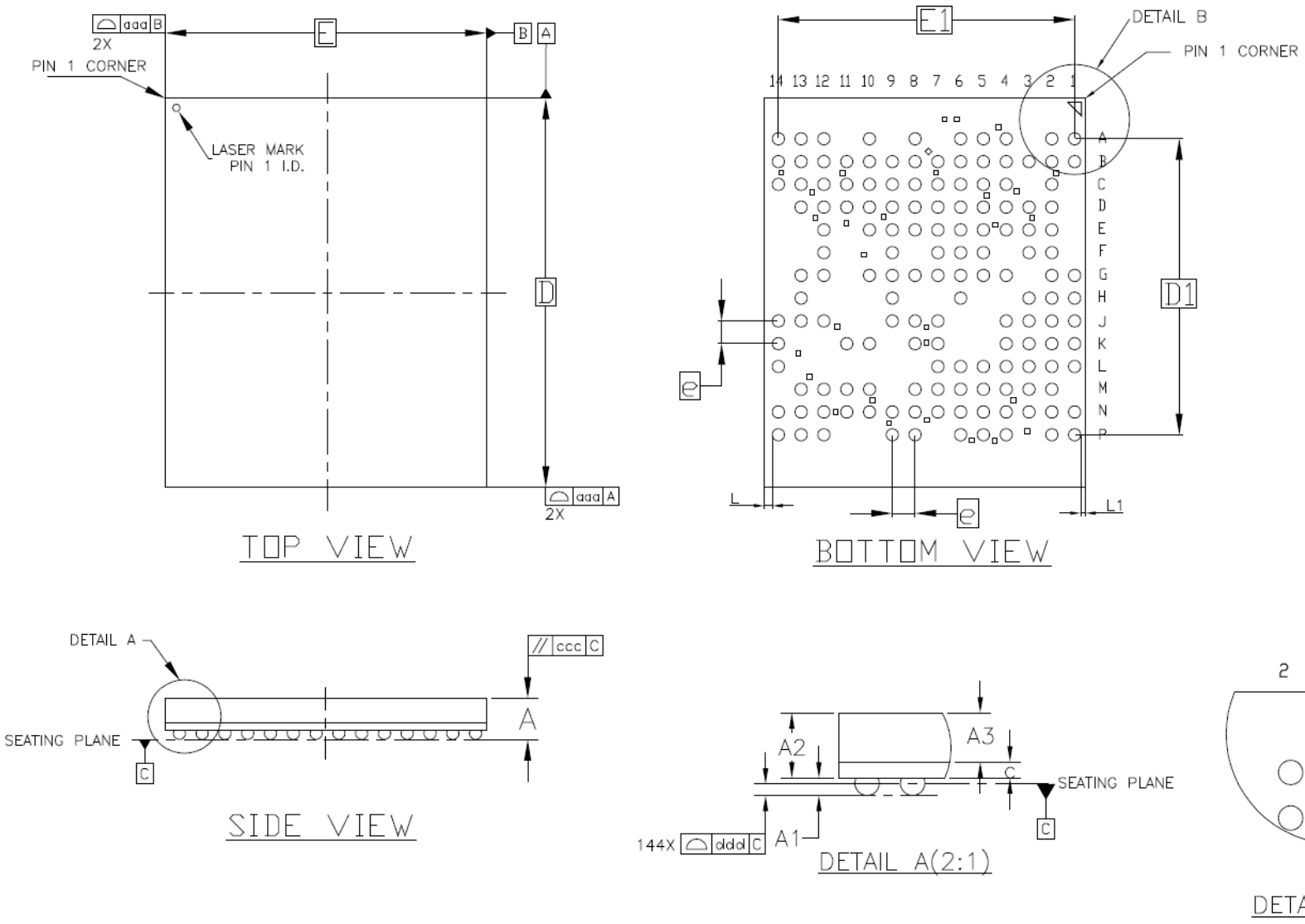
For R328-S3, LFBGA 144 balls, 9.15mm x 11.1mm, 0.65mm pitch package is offered. The pin maps are illustrated in Figure 7-1 and Figure 7-2 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	USB0-DP	USB0-DM		X32KOUT	DXLDO-OUT	DXOUT		GPADC3		AGND		MICIN2N	MICIN1P	GND
B	PG5	PG0	PG4	X32KFOUT	X32KIN	DXIN	GPADC1	GPADC2	VRP	AVCC	LDO-IN	MICIN2P	MICIN1N	MICIN3P
C		PG2		PG3	VCC-PG	GND	RESET	GPADC0	MBIAS	REXT	LDOB-OUT	LINEOUTN	LINEOUTP	MICIN3N
D		PG1	PG8	VCC-PLL	RST-BYP-N	PLLTEST	GND	GND	LRADC	LDOA-OUT	VRA2	VRA1	PC4	
E		PG13	REFCLK-OUT	TEST	SVREF	GND	GND	GND	GND	VCC-PC		VCC-PE		
F		PG9	PG10		GND	GND	GND		VDD-CPU			VCC-IO		
G	PG6	PG11		GND	GND	VDD-SYS	VDD-SYS	GND	VDD-CPU	VDD-CPU		PC16	PC3	
H	PG14	PG7	GND			GND			VDD-CPU				PC2	
J	GND	PG12	GND	GND			VDD-SYS	SZQ	DZQ			PC0	PC1	PE3
K	VCC-DRAM	VCC-DRAM	GND	GND			VCC-EFUSE	VDD-CPUFB		GND	PC15			PE5
L	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND							PH1
M		PB10	PB3	PB2	PB7	GND	GND	GND		PH2	PH4	PH8	PH7	
N	PB5	PB11	PB8	PB9	GND	GND	PH0	PE0	PB0	PH9	PH5	PH3	PH6	PE6
P	GND	PB4		PB6	PB13	PB12		PB1	PE1			PE2	PE4	GND

Figure 7-1. R328-S3 Pin Map

7.2. Package Dimension

Figure 7-2 shows the top, bottom, and side views of R328-S3 package dimension.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.10	1.18	1.26
A1	0.20	0.25	0.30
A2	0.88	0.93	0.98
A3	0.70 BASIC		
c	0.19	0.23	0.27
E	9.05	9.15	9.25
E1	8.45 BASIC		
D	11.00	11.10	11.20
D1	8.45 BASIC		
e	0.65 BASIC		
b	0.30	0.35	0.40
L	0.225 REF		
L1	0.125 REF		
aaa	0.15		
ccc	0.15		
ddd	0.12		
eee	0.15		
fff	0.08		

Figure 7-2. R328-S3 Package Dimension

8. Carrier, Storage and Baking Information

8.1. Carrier

8.1.1. Matrix Tray Information

Table 8-1 shows the R328-S3 matrix tray carrier information.

Table 8-1. Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	168 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

HIC : 

Desiccant : 

RoHS symbol: 

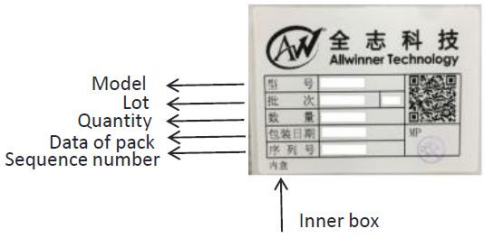
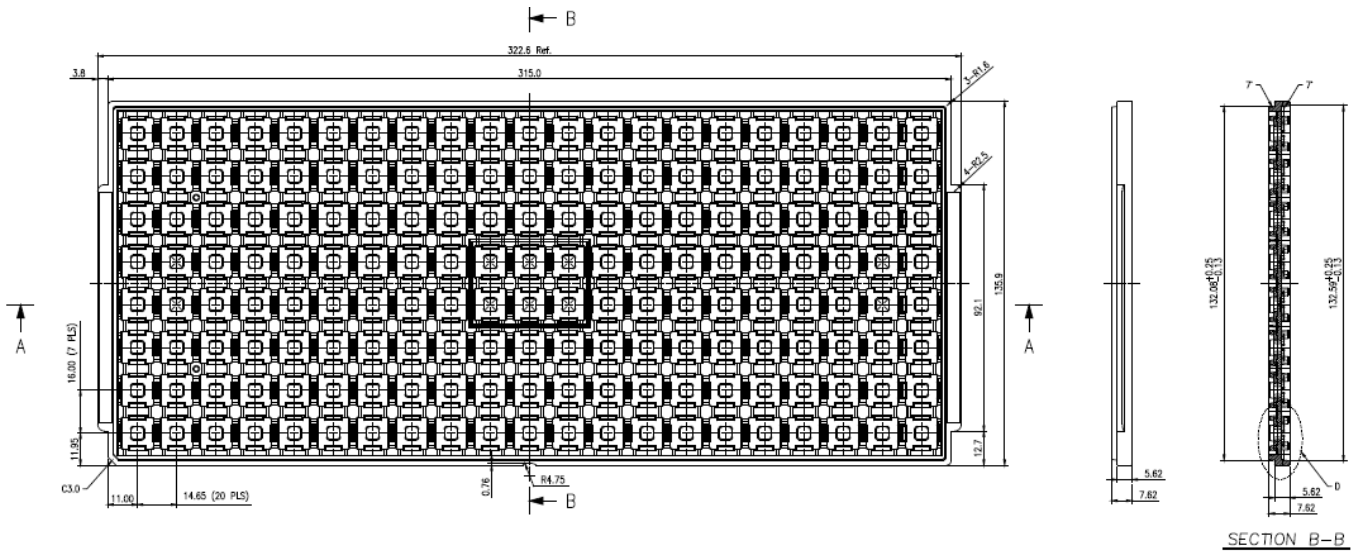
Product label: 

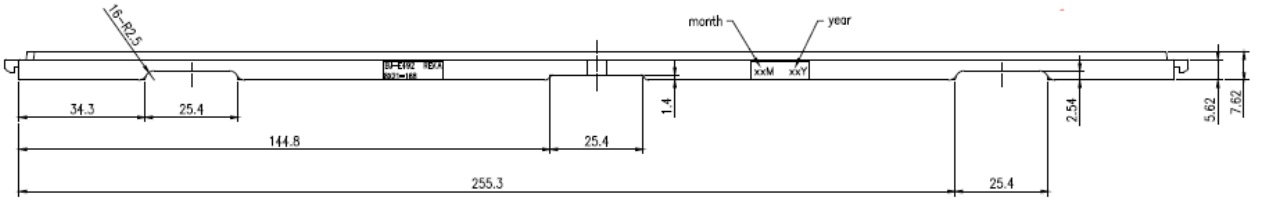
Table 8-2 shows the R328-S3 packing quantity.

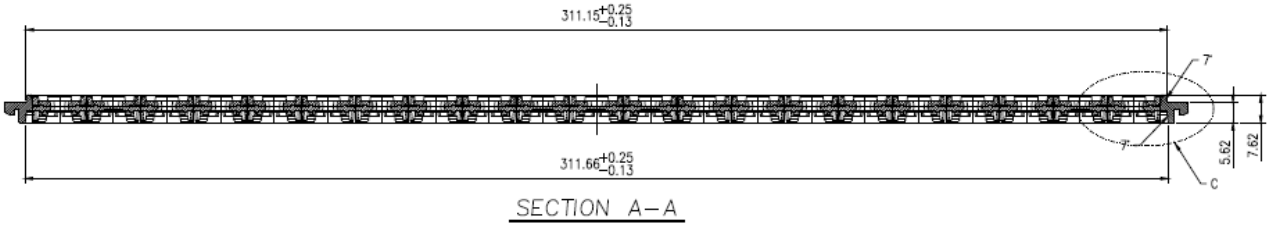
Table 8-2. Packing Quantity Information

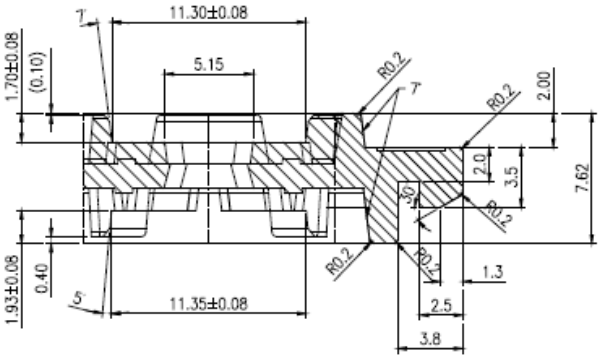
Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
R328-S3	9.15 x 11.1	168	10	1680	6	10080

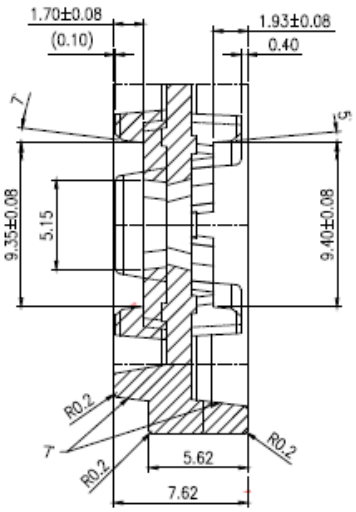
Figure 8-1 shows tray dimension drawing of the R328-S3.











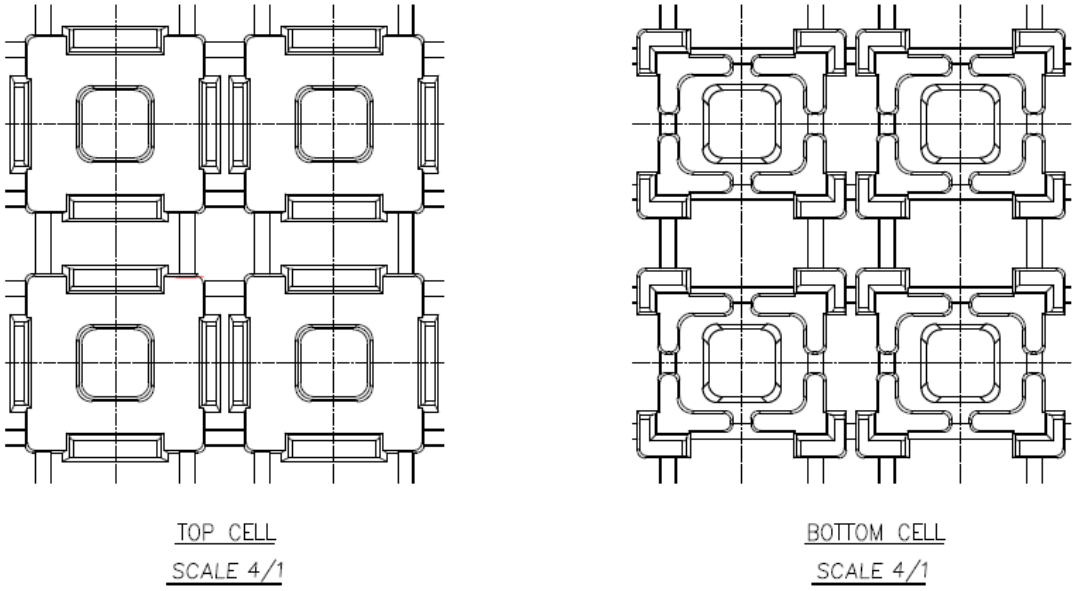


Figure 8-1. Tray Dimension Drawing

8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1. Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 8-3.

Table 8-3. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The R328-S3 device samples are classified as MSL3.

8.2.2. Bagged Storage Conditions

The shelf life of the R328-S3 device samples are defined in Table 8-4.

Table 8-4. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the R328-S3 are as follows.

Table 8-5. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3. Baking

It is not necessary to bake the R328-S3 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the R328-S3 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary bake the R328-S3 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the sample baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The appropriate reflow conditions are defined in Figure 9-1 and Table 9-1.

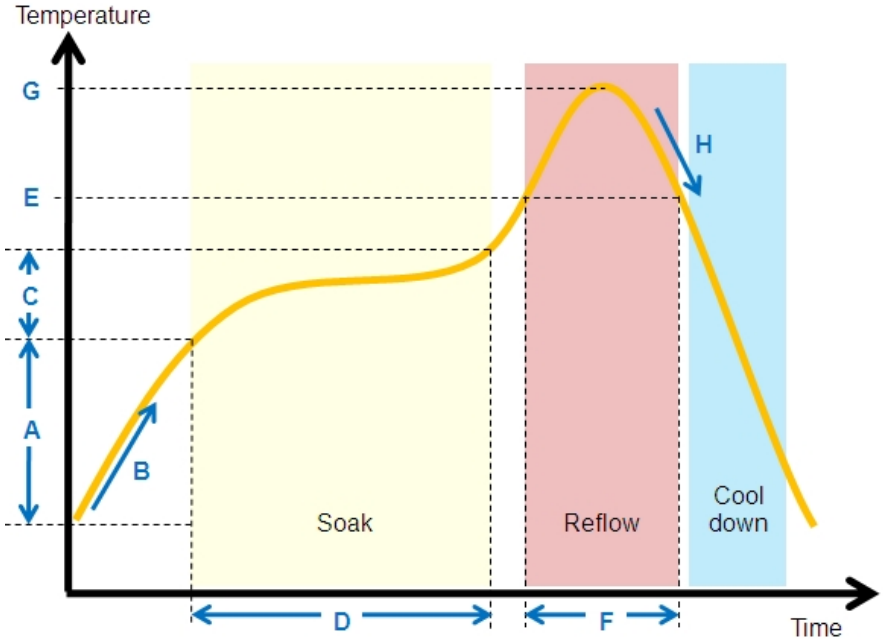


Figure 9-1. Lead-free Reflow Profile

Table 9-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

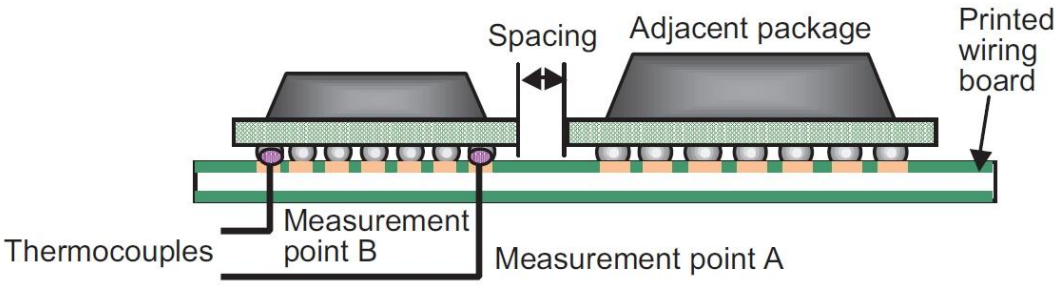


Figure 9-2. Measuring the Reflow Soldering Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10. FT and IQC Test

10.1. FT Test

FT test includes two parts, module verification and linux system testing. For module verification, it verifies the logic function of each module; for linux system testing, it mainly tests CPU, DDR, memory test and linpack, etc. The linux system testing can cover areas where module verification does not cover, with the goal of increasing coverage as much as possible.

10.2. IQC Test

IQC test system is used for sampling inspection before delivery, it is the final test for chip shipment before delivery to the customer. IQC test system includes QA test and QC test.

10.2.1. QA Test

QA test is a testing for each function module of chip by writing the linux system firmware similar to terminal client into SPI nor flash, which can judge whether chip can reach production standard by system total running results, single module testing fluency.

10.2.2. QC Test

QC test is used to test each module code booting from SPI nor flash, and run schedule by using PC control code, then read the return value of each module testing. If the return value is PASS, then continue to perform the next module testing; or else stop testing and remind the testing module FAIL.

11. Part Reliability

Package reliability:

Test Item	Standard	Condition	Sample Size	Result
Moisture sensitive level (MSL)	J-STD 020D	MSL 3, refer to PRC Total samples from three different lots	77	Pass
Preconditioning (PRC)	JESD22-A113F	Bake(125°C, 24 hrs), Soak(60°C/60%RH, 40 hrs), Reflow(260°C), 3 times Operating before TCT/uHAST Total samples from three different lots	144	Pass
Temperature cycle test (TCT)	JESD22-A104C, JESD74	Temperature: -65°C to 150°C Soak time at minimum/maximum temperature: 15 min 500 cycles Total samples from three different lots	77	Pass
Unbiased highly accelerated stress test (uHAST)	JESD22-A118	130°C/85%RH 96 hrs Total samples from three different lots	77	Pass
High temperature storage life(HTSL)	JESD22-A103	150°C, 500 hrs Total samples from three different lots	77	Pass

Silicon reliability:

Test Item	Standard	Condition	Sample Size	Result
ESD-HBM	JS-001-2014	Class-2 :2000V - < 4000V Total samples from one lot	3	Pass
ESD-CDM	JS-002-2014	Class-C1 : 250V - < 500V Total samples from one lot	6	Pass
Latch-up	JESD78D	Inom±200mA, 1.5 x VddMax Total samples from one lot	9	Pass
High temperature operating life(HTOL)	JESD22-A108	Tj=125(-0/+5)°C, 1000hrs Total samples from three different lots	25	Pass

12. Part Marking

Figure 12-1 shows the R328-S3 marking.

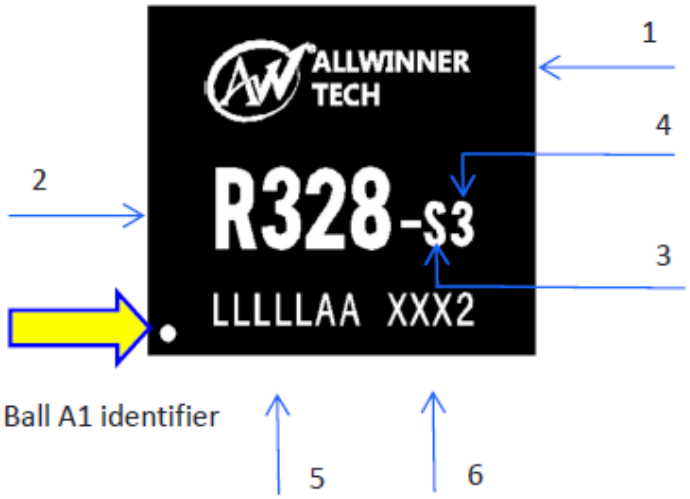


Figure 12-1. R328-S3 Marking

Table 12-1 describes the R328-S3 marking definitions.

Table 12-1. R328-S3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R328	Product name	Fixed
3	S	BGA package	Fixed
4	3	SIP 1Gbit DDR3	Fixed
5	LLLLLAA	Lot number	Dynamic
6	XXX2	Data code	Dynamic

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