

During my Computer Architecture class, I embarked on what I consider one of the most interesting hardware projects that I have worked on to date. The project was the design of an Out-of-Order CPU. In collaboration with two other students, we crafted an RV32I processor integrating out-of-order execution, leveraging Tomasulo's algorithm. Utilizing SystemVerilog we engineered the project from conception to implementation. To validate its functionality, I developed RISC-V assembly programs tailored to test the entire design, complemented by the development of testbenches for unit testing separate modules and simulated them using ModelSim. In an attempt optimize the performance of the CPU, integrated a tournament branch predictor. This project was very rewarding especially because it deviated from the class's original 5-stage pipeline CPU project. Due to the lack of documentation from the class about out-of-order execution and branch prediction, we undertook extensive independent research and gained a lot of new skills. The successful completion of this project underscores my readiness for the challenges that might present while working on the CORE-V Wally project. I am excited about the opportunity to contribute my skills and knowledge to the mentorship program. And I am also eager to embark on a journey of continuous learning and growth while working alongside the mentors. I have also attached a pdf of the OoO CPU Datapath to this repository symbolizing both my achievement and my commitment to excellence.