

Data Sheet

EMW3162

Embedded Wi-Fi module

2.2 Date: 2013-08-11 Data Sheet

Overview

EMW3162 is a low-power embedded Wi-Fi module integrates a wireless LAN MAC/baseband /radio, and a Cortex-M3 microcontroller STM32F205 that runs a unique "self-hosted" Wi-Fi networking library and software application stack. EMW3162 has 1M bytes flash, 128k RAM and rich peripherals for your embedded Wi-Fi applications.

EMW3162 is also an mxchipWNetTM compatible platform, users can build their own embedded Wi-Fi applications based on mxchipWNetTM library which manage all of the Wi-Fi MAC and TCP/IP stack processing. We also provide several mxchipWNetTM firmware to meet typical applications: wireless UART, wireless audio, wireless sensor etc.

When using mxchipWNet™ -DTU firmware, you can establish Wi-Fi networking for any device with a micro-controller and a UART interface. Quick development cycles enables fast time to market.

EMW3162 and EMW3280 are pin compatible.

Applications

- Building Automation / Access Control
- Smart home appliances
- Medical/Health Care
- Industrial Automation Systems
- Point Of Sale system (POS)
- Auto electronics

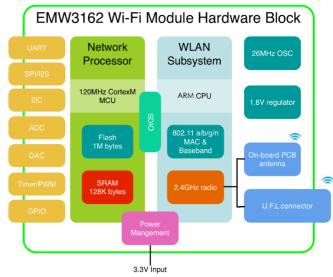


Product list

Module	-		Antenna
EMW3162	-	Р	On-board PCB antenna
	-	Е	IPEX connector

Firmware/Library	Function
mxchipWNet TM -	Predefined firmware:
DTU	UART/Wi-Fi conversion
mxchip <mark>W</mark> Net™	Software library used to
Library	develop custom firmware
mxchip <mark>W</mark> Net™	Software library based on
Library Plus	RTOS
WICED™ Firmware	WICED™ source codes
development kit	with TCP/IP, Wi-Fi MAC
development kit	RTOS and GCC tool chain

Hardware block



MXCHIP Co., Ltd

Contents

1	INTRODUCTION1	3.8.	1 Basic RF characteristics 1	.1
-	11111000011011	3.8.		
1.1	Features 1	3.8.	3	
		3.8.	4 IEEE802.11n 20MHz bandwidth mode1	.3
		3.9	Mechanical Dimensions 1	5
2	INTERFACE3	3.9.	1 EMW3162 Mechanical Dimensions1	.5
2.1	Led3			
2.2	Pinouts3	4	ANTENNA INFORMATION 1	7
2.3	Pin Arrangement4	4.1	Minimizing radio interference 1	7
		4.2	U.F.L RF Connector1	8
3	ELECTRICAL PARAMETERS6			
3.1	Absolute maximum ratings:6	5	OTHERS1	9
3.1.1	Voltage & Current6	5.1	Recommended Reflow Profile1	a
3.2	Operating conditions6			
3.2.1	Voltage & Current6	5.2	MSL/Storage Condition1	9
3.3	Digital I/O port characteristics9			
3.3.1	Output voltage levels9	6	SALES INFORMATION20	Λ
3.3.2		,	SALLS IN ORWALION2	J
3.3.3	nRESET pin characteristics10			
3.4	Other MCU electrical parameters10			
3.5	Temperature and Humidity10	7	TECHNICAL SUPPORT 2	0
3.6	ESD11			
3.7	Static latch-up11			
3.8	RF characteristics11			

1 Introduction

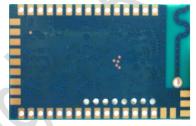
EMW3162 is a low-power embedded Wi-Fi module integrates a wireless LAN MAC/baseband /radio, and a Cortex-M3 microcontroller STM32F205 that runs a unique "self-hosted" Wi-Fi networking library and software application stack. EMW3162 has 1M bytes flash, 128k RAM and rich peripherals for your embedded Wi-Fi applications.

EMW3162 is also an **mxchipWNetTM** compatible platform, users can build their own embedded Wi-Fi applications based on **mxchipWNetTM** library which manage all of the Wi-Fi MAC and TCP/IP stack processing. We also provide several **mxchipWNetTM** firmware to meet typical applications: wireless UART, wireless audio, wireless sensor etc.

When using **mxchipWNetTM**-DTU firmware, you can establish Wi-Fi networking for any device with a micro-controller and a serial interface. Quick development cycles enables fast time to market.

EMW3162 and EMW3280 are pin compatible.





1.1 Features

- ★ Single operation voltage : 3.3V
- **★** Power consumption:
 - Only ~7mA while module is connected to access point and no data is transmitting, Only ~24mA while sending data under 20kbps,
 - Only 8µA under standby mode.
- ★ STM32F2 MCU frequency: 120MHz , flash size: 1M bytes , RAM size: 128k bytes.
- ★ On-chip functionality Single-chip: MAC/BB/RF
- ★ Peripherals :
 - 32 x GPIOs
 - 2 x UARTs , includes hardware flow control
 - 1 x SPI/I2S
 - 8 x ADC input channels , 2 DAC output channel
 - 1 x USB OTG, 2 x CAN
 - 1 x I2C
 - PWM/Timer input/output available on every GPIO pin
 - SWD debug interface

- ★ Wi-Fi connectivity
 - 802.11b, 802.11g, 802.11n (single stream) on channel 1-14@2.4GHz
 - WEP, WPA/WPA2 PSK/Enterprise
 - Transmit power: 18.5dBm@11b , 15.5dBm@11g , 14.5dBm@11n
 - MIN Receiver Sensitivity: -96 dBm
 - Max Data rate: 11Mbps@11b , 54Mbps@11g , 72Mbps@11n HT20
 - Wi-Fi modes : Station, Soft AP and Wi-Fi direct
 - Advanced 1x1 802.11n features

Full/Half Guard Interval

Frame Aggregation

Space Time Block Coding (STBC)

Low Density Parity Check (LDPC) Encoding

- Hardware Encryption: WEP, WPA/WPA2
- WPS 2.0, EasyLink
- Multiple power save modes
- On-board chip antenna, IPEX connector for external antenna
- CE , FCC compliant
- ★ Operating Temperature: -40°C to 85°C
- ★ MSL level 3

2 Interface

2.1 **Led**



Table 2.1 LED functions

Name	Color	GPIO
D1	Green	PB0
D2	Red	PB1

2.2 **Pinouts**

EMW3162 has two groups of pins (1X15 +1X15). The lead pitch is 2mm.

Pinout is shown in the Figure 2.1. Table 2.2 lists the pin functions.



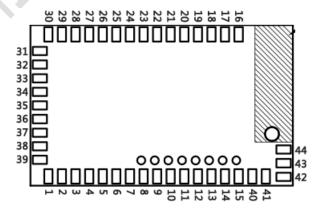


Figure 2.1 EMW 3162: appearance and pinout

2.3 **Pin Arrangement**

Figure 2.2 EMW3162 pin arrangement

1 PB6 I/O FT PB6 I2C1_SCL/ USART1_TX / TIM4_CH1 / CAN2_TX 2 PB7 I/O FT PB7 I2C1_SDA / USART1_RX / TIM4_CH2 3 PA13 I/O FT SWDIO 4 PC7 I/O FT PC7 I2S3_MCK / TIM8_CH2 / TIM3_CH2 / USART6_RX 5 PA3 I/O FT PA3 TIM5_CH4 / TIM9_CH2 / TIM3_CH2 / SPI1_NSS / PI3_NSS / TIM2_CH4 / ADC123_TIM2_CH4 / ADC123_TIM2_CH2 / TIM3_CH2 / SPI1_NSS / SPI3_NSS / DAC1_O 6 PA4 I/O FT PA4 SPI1_NSS / SPI3_NSS / DAC1_O 7 PB3 I/O FT JTDO/ TRACESWO / I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK / SPI3_SCK / SPI3_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_TIM10_CH1 / TIM3_CH1 / TIM8_CH2N/ 12 PC2 I/O FT PB14 TIM1_C					Main function	<u> </u>	Other
1	Pins	Name	Туре	IO level	(after reset)	Alternate functions	functions
TIM4_CH1 / CAN2_TX	4	DD 6	7.10		DD.C	I2C1_SCL/ USART1_TX /	
2 PB7 I/O FT PB7 TIM4_CH2 3 PA13 I/O FT SWDIO 4 PC7 I/O FT PC7 I2S3_MCK / TIM8_CH2 / TIM3_CH2 / TIM3_CH2 / TIM3_CH2 / TIM3_CH4 / TIM9_CH2 / TIM3_CH4 / TIM9_CH2 / TIM2_CH4 / ADC123_TIM2_CH4 / ADC123_TIM2_CH2 / TIM2_CH4 / TIM2_CH4 / TIM4_CH4 / TI		PB6	1/0	FI	PB6	TIM4_CH1 / CAN2_TX	
TIM4_CH2	2	557	7.10		227	I2C1_SDA / USART1_RX/	
4 PC7 I/O FT PC7 I2S3_MCK / TIM8_CH2/ TIM3_CH2 / USART6_RX 5 PA3 I/O FT PA3 TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / ADC123_ ADC123_ 6 PA4 I/O TT PA4 SPI1_NSS / SPI3_NSS / I2S3_WS ADC12_IN DAC1_O 7 PB3 I/O FT JTDO/ TRACESWO JTDO/ TRACESWO/ I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK/ 8 PB4 I/O FT NJTRST NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ TIM8_CH1 / TIM3_CH1 / USART6_TX	2	PB/	1/0	FI	PB/	TIM4_CH2	
4 PC7 I/O FT PC7 TIM3_CH2 / USART6_RX 5 PA3 I/O FT PA3 TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / ADC123_TIM2_CH4 / ADC123_TIM2_CH2 / SPI1_NSS / SPI3_NSS / DAC1_O ADC12_IN DAC1_O 7 PB3 I/O FT JTDO/ TRACESWO / I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK / SPI3_SCK / NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 8 PB4 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 9 PB5 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM2_CH2 ADC123_TIM3_CH2 / ADC123_TIM3_CH2 / TIM3_CH1 / TIM3_CH1 / TIM8_CH2 / TIM8_CH2 / TIM3_CH1 / TIM8_CH2 /	3	PA13	I/O	FT	SWDIO		
5 PA3 I/O FT PA3 TIM3_CH2/USART6_RX TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / TIM2_CH4 / ADC123_MS 6 PA4 I/O TT PA4 SPI1_NSS / SPI3_NSS / TIM2_CH2 / SPI1_NSS / SPI3_NSS / DAC1_O ADC12_INDO/TRACESWO/TIM2_CH2 / SPI1_SCK / SPI3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK / SPI3_SCK / SPI3_SCK / SPI3_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MISO / SPI3_MOSI / CAN2_RX I2C1_SMBA / TIM3_CH2 / SPI1_MOSI / SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_IMADC13_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_IMADC123_I	4	PC7	I/O	FT	PC7	I2S3_MCK / TIM8_CH2/	
5 PA3 I/O FT PA3 TIM2_CH4 / ADC123_ 6 PA4 I/O TT PA4 SPI1_NSS / SPI3_NSS / I2S3_WS ADC12_IN DAC1_O 7 PB3 I/O FT JTDO/ TRACESWO JTDO/ TRACESWO/ I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK / NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 8 PB4 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 9 PB5 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 10 PB8 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM3_CH1 / TIM8_CH2N/ 13 PB14 I/O FT PB14 TIM8_CH1 / TIM3_CH1 / USART6_TX	'	1 07	1,0		1 67	TIM3_CH2 / USART6_RX	
TIM2_CH4 / SPI1_NSS / SPI3_NSS / ADC12_IN	5	PA3	I/O	FT	PA3	TIM5_CH4 / TIM9_CH2 /	ADC123_IN3
6 PA4 I/O TT PA4 I2S3_WS DAC1_O 7 PB3 I/O FT JTDO/ TRACESWO JTDO/ TRACESWO/ I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK/ 8 PB4 I/O FT NJTRST NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX		17.5	1,0		17.5	TIM2_CH4 /	7.0 0123_1113
Table Tabl	6	ΡΔ4	1/0	тт	ΡΔ Δ	SPI1_NSS / SPI3_NSS /	ADC12_IN4 /
7 PB3 I/O FT JIDO/ TRACESWO I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK/ 8 PB4 I/O FT NJTRST NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX		174	1,0		174	I2S3_WS	DAC1_OUT
7 PB3 I/O FT TRACESWO I2S3_SCK / TIM2_CH2 / SPI1_SCK / SPI3_SCK / SPI3_SCK / NJTRST / SPI3_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MISO / TIM3_CH1 / SPI1_MOSI / SPI3_MOSI / CAN2_RX 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_IMMOSI / ADC123_IMMOSI / IMM10_CH1 / IMM10_					ITDO/	JTDO/ TRACESWO/	
8 PB4 I/O FT NJTRST NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_IMMOSI / ADC123_IMMOSI / ADC123_IMMOSI / IAMMOSI / IA	7	PB3	I/O	FT		I2S3_SCK / TIM2_CH2 /	
8 PB4 I/O FT NJTRST TIM3_CH1 / SPI1_MISO/ 9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX					TIO (CESTVO		
TIM3_CH1 / SPI1_MISO/ I2C1_SMBA / TIM3_CH2 / SPI1_MOSI / SPI3_MOSI / CAN2_RX TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX TIM5_CH2 / TIM2_CH2 ADC123_ TIM5_CH2 / TIM2_CH2 ADC123_ TIM5_CH2 / TIM5_CH2 / TIM5_CH2 / TIM5_CH2 / TIM5_CH1 / TIM5_CH1 / TIM5_CH1 / USART6_TX	8	PB4	I/O	FT	NJTRST	NJTRST/ SPI3_MISO /	
9 PB5 I/O FT PB5 SPI1_MOSI/ SPI3_MOSI / CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_ 12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX			1,0		101101	TIM3_CH1 / SPI1_MISO/	
CAN2_RX 10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_ 12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX					01/	I2C1_SMBA / TIM3_CH2 /	
10 PB8 I/O FT PB8 TIM4_CH3 / TIM10_CH1 / I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_I 12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX	9	PB5	I/O	FT	PB5	SPI1_MOSI/ SPI3_MOSI /	
10 PB8 I/O FT PB8 I2C1_SCL / CAN1_RX 11 PA1 I/O FT PA1 TIM5_CH2 / TIM2_CH2 ADC123_1 12 PC2 I/O FT PC2 ADC123_1 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX						_	
I2C1_SCL / CAN1_RX 11	10	PB8	I/O	FT	PB8		
12 PC2 I/O FT PC2 ADC123_I 13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX			·			I2C1_SCL / CAN1_RX	
13 PB14 I/O FT PB14 TIM1_CH2N / TIM12_CH1 / TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM3_CH1 / USART6_TX	11	PA1	I/O	FT	PA1	TIM5_CH2 / TIM2_CH2	ADC123_IN1
13 PB14 I/O FT PB14 TIM8_CH2N/ 14 PC6 I/O FT PC6 TIM8_CH1 / TIM8_CH1 / USART6_TX	12	PC2	I/O	FT	PC2		ADC123_ IN12
TIM8_CH2N/ TIM8_CH2N/ TIM8_CH1 / TIM3_CH1 / USART6_TX	10	DD14	1/0	ГТ	DD1.4	TIM1_CH2N / TIM12_CH1 /	
14 PC6 I/O FT PC6 USART6_TX	13	PD14	1/0	ГІ	PD14	TIM8_CH2N/	
USART6_TX	14	DC6	1/0	ГТ	DC6	TIM8_CH1 / TIM3_CH1 /	
15 GND	14	PCO	1/0	FI	PC6	USART6_TX	
	15	GND					
TIM3_CH4 / TIM8_CH3N/						TIM3_CH4 / TIM8_CH3N/	
16 PB1 I/O PB1 TIM1_CH3N/ ADC12_I	16	PB1	I/O		PB1		ADC12_IN9
17 nRESET	17	nRESET					
18 PA15 I/O FT JTDI JTDI/ SPI3_NSS/ I2S3_WS/	10		1/0		ITDI	JTDI/ SPI3_NSS/ I2S3_WS/	
TIM2_CH1_ETR / SPI1_NSS	10	LWT2	1/0	F I	וחול	TIM2_CH1_ETR / SPI1_NSS	
19 PB11 I/O FT PB11 TIM2_CH4	19	PB11	I/O	FT	PB11	TIM2_CH4	
30 BA13 I/O FT BA13 USART1_RTS / CAN1_TX/	20	D410	7.00		DA40	USART1_RTS / CAN1_TX/	
20 PA12 I/O FT PA12 SJANTING STATE TIM1_ETR/ OTG_FS_DP	20	PA12	1/0	FT	PA12		

Pins	Name	Туре	IO level	Main function (after reset)	Alternate functions	Other functions
					USART1_CTS / CAN1_RX /	
21	PA11	I/O	FT	PA11	TIM1_CH4 / OTG_FS_DM	
22	PA9	I/O	FT	PA9	USART1_TX/ TIM1_CH2	OTG_FS_VBUS
23	PA10	I/O	FT	PA10	USART1_RX/ TIM1_CH3/ OTG_FS_ID	
24	VCC					
25	GND					
26	NC					
27	воото	I		BOOT0		
28	PA14	I/O		JTCK- SWCLK	JTCK-SWCLK	
29	PA0- WKUP	I/O		PA0-WKUP	TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR	ADC123_IN0/ WKUP
30	PB9	I/O		PB9	TIM4_CH4/ TIM11_CH1 / I2C1_SDA / CAN1_TX	
31	PA5	I/O	TT	PA5	SPI1_SCK / TIM2_CH1_ETR/ TIM8_CHIN	ADC12_IN5 /DAC2_OUT
32	PA6	I/O	FT	PA6	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / TIM3_CH1 / TIM1_BKIN	ADC12_IN6
33	PA8	I/O	FT	PA8	MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL	
34	PB15	I/O	FT	PB15	TIM1_CH3N / TIM8_CH3N / TIM12_CH2 /RTC_50Hz	
35	PC3	I/O	FT	PC3		ADC123_ IN13
36	PC4	I/O	FT	PC4		ADC12_IN14
37	NC					
38	NC					
39	GND					
40	GND					
41	GND					
42	GND					
43	GND					
44						

- 1. FT = 5 V tolerant; TT = 3.6 V tolerant.
- 2. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
- 3. I = input, O = output, S = supply.
- 4. STM32 peripherals are not listed if they cannot be presented on current pins

3 Electrical Parameters

3.1 **Absolute maximum ratings:**

3.1.1 Voltage & Current

Stresses above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit
V _{DD} -V _{SS}	Voltage	-0.3	4.0	V
V _{IN}	Input voltage on five volt tolerant pin	V _{SS} -0.3	5.5	V
V _{IN}	Input voltage on any other pin	V _{SS} -0.3	V _{DD} +0.3	V

Symbol	Ratings	Max	Unit
I _{VDD}	Total current into VDD power lines (source)	320	mA
I _{VSS}	Total current out of VSS ground lines (sink)	320	
T	Output current sunk by any I/O and control pin	25	
I_{IO}	Output current source by any I/O and control pin	-25	

3.2 **Operating conditions**

3.2.1 Voltage & Current

Symbol	Note	Conditions	Specification			
	Note	Conditions	Min.	Typical	Max.	Unit
V _{DD}	Voltage		2.4	3.3	3.5	V

WLAN Subsystem

Symbol	Note	Conditions	Typical	Unit
${ m I}_{\sf RF}$	OFF ¹		2	μΑ
${ m I}_{\sf RF}$	SLEEP ⁴		200	μΑ
${ m I}_{\sf RF}$	Rx(Listen) ²		52	mA
${ m I}_{\sf RF}$	Rx(Active) ³		59	mA
${ m I}_{\sf RF}$	Power Save ^{5 6}		1.9	mA
${ m I}_{\sf RF}$	Tx CCK ⁷ 10	11 Mbps at 18.5 dBm	320	mA
${ m I}_{\sf RF}$	Tx OFDM ⁸ 10	54 Mbps at 15.5 dBm	270	mA
I_{RF}	Tx OFDM ⁹ 10	65 Mbps at 14.5 dBm	260	mA

Note 1: Power is off.

Note 2: Carrier Sense (CCA) when no carrier present

Note 3: Carrier Sense (CS) detect/Packet Rx

Note 4: Intra-beacon Sleep

Note 5: Beacon Interval = 102.4ms, DTIM = 1, Beacon duration = 1 ms @1 Mbps.

Integrated Sleep + wakeup + Beacon Rx current over 1 DTIM interval.

Note 6: In WLAN power-saving mode, the following blocks are powered down: Crystal oscillator, Baseband PLL, AFE, RF PLL, Radio

Note 7: CCK power at chip port. Duty cycle is 100%. Includes PA contribution.

Note 8: OFDM power at chip port. Duty cycle is 100%. Includes PA contribution.

Note 9: OFDM power at chip port is 16 dBm, duty cycle is 100%, includes PA contribution.

Note 10: Absolute junction temperature limits maintained through active thermal monitoring and dynamic Tx duty cycle limiting.

Microcontroller Subsystem

Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM

Councils of	Candisiana	£	Running Mode	Sleep Mode	11!4
Symbol	Conditions	f _{HCLK}	T _A =25°C	T _A =25°C 38 30 20 11 8 6 3.6 2.4 1.9 8 7 5 3.5 2.5 2.1 1.7	Unit
		120MHz	49	38	
		90MHz	38	30	
		60MHz	26	20	
	External clock all	30MHz	14	11	
	External clock, all	25MHz	11	8	
	peripherals enabled	16MHz	8	6	
		8MHz	5	3.6	
		4MHz	3	2.4	
T .		2MHz	2	1.9	m A
I _{MCU}		120MHz	21	8	mA
		90MHz	17	7	
		60MHz	12	5	
	F	30MHz	7	3.5	
	External clock, all	25MHz	5	2.5	
	peripherals disabled	16MHz	4	2.1	
		8MHz	2.5	1.7	
		4MHz	2	1.5	
		2MHz	1.6	1.4	

Typical and maximum current consumptions in Stop mode

Symbol	Doromotor	Conditions	Тур	Max	Unit
Symbol	Parameter	Conditions	T _A =25°C	T _A =25°C	Onit
1	Supply current in Stop mode with	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.55	1.2	
_	main regulator in Run mode	Flash in Deep power down mode, low- speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.5	1.2	
I _{MCU}	Supply current in Stop mode with	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.35	1.1	mA
	main regulator in Low Power mode	Flash in Deep power down mode, low- speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.3	1.1	

Typical and maximum current consumptions in Standby mode

Symbol	Danamatan	Conditions	Тур	Unit
Symbol	Parameter	Conditions	T _A =25°C	Onit
	Complete accompany	Backup SRAM ON, low-speed oscillator and RTC ON	4.0	
_	Supply current	Backup SRAM OFF, low-speed oscillator and RTC ON	3.3	
I _{MCU} In Stan	in Standby	Backup SRAM ON, RTC OFF	3.0	μΑ
	mode	Backup SRAM OFF, RTC OFF	2.2	

Power consumption in typical operation modes³

Symbol	Davameter	meter Conditions		Min Average		Unit
	Parameter	Conditions	T _A =25°C	T _A =25°C	T _A =25°C	Unit
	_	No Wi-Fi data is transmitting ¹	2.8	7.2	73.5	mA
I	Total power consumption on EMW3162	Receive data in UDP mode, 20k bps¹	2.8	12	262	mA
I module		Send data in UDP mode, 20k bps ¹	3	24	280	mA
	module	RF off, MCU enter standby mode ²	4	6	8	μΑ
		Connecting to AP	52	74	320	mA

Note1: TA=25°C, MCU frequency=120MHz, with data processing running from Flash memory (ART accelerator enabled). Firmware process TCP/IP stack and IEEE 802.11 MAC every 250 milliseconds, enter stop mode when no task is pending.

RF subsystem is connected to an access point and run under power save mode in IEEE 802.11n@14.5 dBm Tx power. AP Beacon Interval = 102.4 ms, DTIM = 1.

Note2: Wi-Fi connection is disconnected.

Note3: These data may not be the same depend on different firmware functions.

3.3 **Digital I/O port characteristics**

3.3.1 Output voltage levels

Symbol	Note	Parameter	Conditions	Min.	Max.	Unit
V _{OL}		Output low level voltage	I_{IO} = +8 mA		0.4	V
V _{OH}	UART& IO	Output high level voltage	2.7 V < VDD < 3.6 V	V_{DD} -0.4		V
V _{OL}	output voltage	Output low level voltage	I_{IO} = +20 mA		1.3	V
V _{OH}		Output high level voltage	2.7 V < VDD < 3.6 V	V _{DD} -1.3		V

3.3.2 Output voltage levels

Symbol	Note	Parameter	Conditions	Min.	Max.	Unit
V_{IL}		Input low level voltage		-0.5	0.8	V
		Input high level voltage	TT: 1	2	VDD+0.5	V
V _{IH}	UART& IO input voltage	Input high level voltage (5V input tolerant)	TTL level	2	5.5	V
V _{IL}		Input low level voltage	CMOS level	-0.5	0.35VDD	V
V _{IH}		Input high level voltage	CiviO3 level	0.65VDD	VDD+0.5	V

3.3.3 nRESET pin characteristics

The nRESET pin input driver uses CMOS technology. EMW3162 contains RC (resistance-capacitance) reset circuit which ensures the module reset accurately when it powers up. If you need to reset manually, just connect the external control signals to the reset pins directly, but the control signal should be Open Drain Mode.

Symbol	Item	Conditions	Min.	Typical	Max.	Unit
V _{IL(NRST)}	nRESET input low level		-0.5		0.8	V
$V_{\text{IH(NRST)}}$	nRESET input high level		2		VDD+0.5	V
R_{PU}	Resistor for Pulling up	V _{IN} = VSS	7.5	8	8.3	kΩ
C_{PD}	Capacitor for charging and Resetting			100	1000	pF

3.4 Other MCU electrical parameters

Please refer to STM32F215RGT6 data sheet.

3.5 **Temperature and Humidity**

Symbol Ratings		Max	Unit
T _{STG}	Storage temperature	-55 to +125	$^{\circ}$
TA	Working temperature	-40 to +85	$^{\circ}$
Humidity	Non condensing, relative humidity	Max. 95%	

3.6 **ESD**

Absolute maximum ratings: The Electromagnetic Environment Electrostatic discharge

Symbol	Ratings	Conditions	Class	Max	Unit
V _{ESD} (HBM)	Electrostatic discharge voltage (human body model)	TA= +25 °C conforming to JESD22-A114	2	2000	V
V _{ESD} (CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to JESD22-C101	II	500	

3.7 **Static latch-up**

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Symbol	Parameter	Class	Class
LU	Static latch-up class	TA= +105 °C conforming to JESD78A	II level A

3.8 **RF characteristics**

3.8.1 Basic RF characteristics

Item	Specification
Operating Frequency	2.412~2.484GHz
Wi-Fi Standard	802.11b/g/n(single stream n)
Modulation Type	11b: DBPSK, DQPSK,CCK for DSSS 11g: BPSK, QPSK, 16QAM, 64QAM for OFDM 11n: MCS0~7,OFDM *
Data Rates	11b:1, 2, 5.5 and 11Mbps 11g:6, 9, 12, 18, 24, 36, 48 and 54 Mbps 11n: MCS0~7, up to 72Mbps
Antenna type	One U.F.L connector for external antenna PCB printed ANT (Reserve)

3.8.2 **IEEE802.11b** mode

Item	Specification
Modulation Type	DSSS / CCK
Frequency range	2400MHz~2484MHz
Channel	CH1 to CH14
Data rate	1, 2, 5.5, 11Mbps

TX Characteristics	Min.	Typical	Max.	Unit			
Transmitter Output Power							
11bTarget Power		18.5		dBm			
Spectrum Mask @ target power							
fc +/-11MHz to +/-22MHz			-30	dBr			
fc > +/-22MHz		NO	-50	dBr			
Frequency Error	-20		+ 20	ppm			
Constellation Error(peak EVM)@ target power							
1~11Mbps		-17	-10				

RX Characteristics	Min.	Typical	Max.	Unit		
Minimum Input Level Sensitivity						
1Mbps (FER≦8%)		-97	-83	dBm		
2Mbps (FER≦8%)		-93	-80	dBm		
5.5Mbps (FER≦8%)		-91	-79	dBm		
11Mbps (FER≦8%)		-89	-76	dBm		
Maximum Input Level (FER≦8%)	-10			dBm		

3.8.3 **IEEE802.11g** mode

Item	Specification
Modulation Type	OFDM
Frequency range	2400MHz~2484MHz
Channel	CH1 to CH14
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps

TX Characteristics	Min.	Typical	Max.	Unit
Transmitter Output Power				

11gTarget Power		15.5		dBm	
Spectrum Mask @ target power					
fc +/-11MHz			-20	dBr	
fc +/-20MHz			-28	dBr	
fc > +/-30MHz			-40	dBr	
Frequency Error	-20		+ 20	ppm	
Constellation Error(peak EVM)@ targe	et power				
6Mbps			-5	dB	
9Mbps			-8	dB	
12Mbps			-10	dB	
18Mbps			-13	dB	
24Mbps		(-16	dB	
36Mbps			-19	dB	
48Mbps			-22	dB	
54Mbps		-30	-25	dB	
Transmit spectrum mask					
@ 11MHz			-20	dBr	
@ 20MHz			-28	dBr	
@ 30MHz	4)		-40	dBr	

RX Characteristics	Min.	Typical	Max.	Unit	
Minimum Input Level Sensitivity					
6Mbps (FER≦10%)		-90	-82	dBm	
9Mbps (FER≤10%)		-88	-87	dBm	
12Mbps (FER≦10%)		-86	-79	dBm	
18Mbps (FER≤10%)		-85	-77	dBm	
24Mbps (FER≤10%)		-82	-74	dBm	
36Mbps (FER≤10%)		-79	-70	dBm	
48Mbps (FER≦10%)		-75	-66	dBm	
54Mbps (FER≤10%)		-72	-65	dBm	
Maximum Input Level (FER≤10%)	-20			dBm	

3.8.4 IEEE802.11n 20MHz bandwidth mode

Item	Specification
Modulation Type	MIMO-OFDM

Channel	CH1 to CH14
Data rate	MCS0/1/2/3/4/5/6/7

TX Characteristics	Min.	Typical	Max.	Unit
Transmitter Output Power				
11n HT20 Target Power		14.5		dBm
Spectrum Mask @ target power				
fc +/-11MHz			-20	dBr
fc +/-20MHz			-28	dBr
fc > +/-30MHz			-45	dBr
Frequency Error	-25	-1.2	+ 25	ppm
Constellation Error(peak EVM)@ targe	et power		0)	
MCS0			-5	dBm
MCS1		OK	-10	dBm
MCS2			-13	dBm
MCS3	7.C		-16	dBm
MCS4			-19	dBm
MCS5			-22	dBm
MCS6			-25	dBm
MCS7		-32	-28	dBm
Transmit spectrum mask				
@ 11MHz			-20	dBr
@ 20MHz			-28	dBr
@ 30MHz			-40	dBr

RX Characteristics	Min.	Typical	Max.	Unit	
Minimum Input Level Sensitivity					
MCS0 (FER≦10%)		-89	-82	dBm	
MCS1 (FER≦10%)		-86	-79	dBm	
MCS2 (FER≦10%)		-84	-77	dBm	
MCS3 (FER≦10%)		-82	-74	dBm	
MCS4 (FER≦10%)		-78	-70	dBm	
MCS5 (FER≦10%)		-74	-66	dBm	
MCS6 (FER≦10%)		-72	-65	dBm	
MCS7 (FER≤10%)		-69	-64	dBm	
Maximum Input Level (FER≤10%)	-20			dBm	

3.9 **Mechanical Dimensions**

3.9.1 EMW3162 Mechanical Dimensions

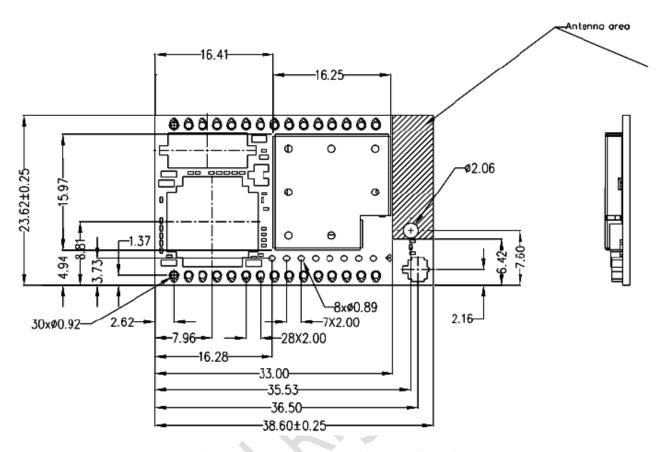


Figure 3.1 EMW3162 top view(Metric units)

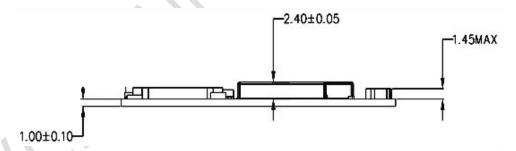


Figure 3.2 EMW3162 side view(Metric units)

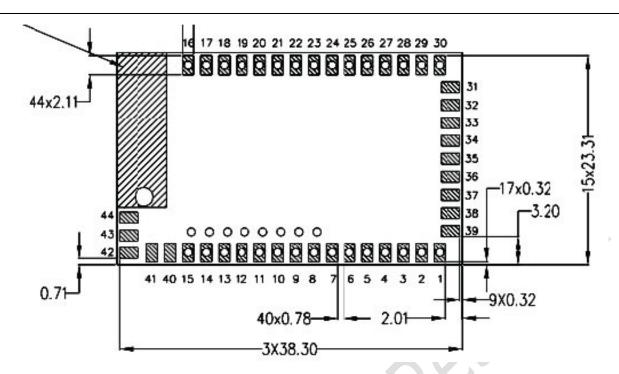


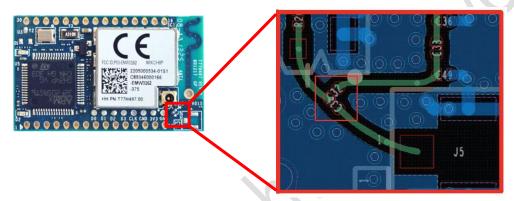
Figure 3.3 EMW3162 bottom view(Metric units)

4 Antenna information

There is co-layout design (C35&C32) for antenna connection. Please order your module carefully. Users can also modify the capacitor position but MXCHIP would not take any responsibility for this behavior.

EMW3280-E load the capacitor C35 (10pF/0201), it means can use U.F.L RF connector for external antenna. If want to use on-board PCB printed antenna, just need load the capacitor from C35 to C32 (EMW3280-P).

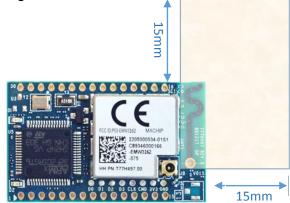
In order to get the maximum performance, strongly suggest customer use external antenna connected with U.F.L RF connector.



4.1 Minimizing radio interference

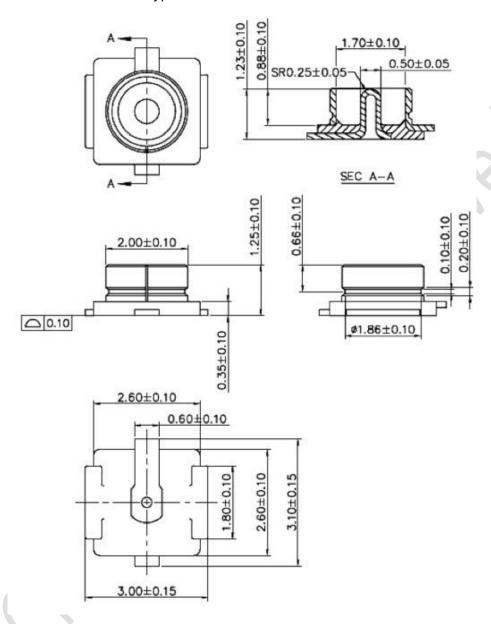
When integrating the Wi-Fi module with on board PCB printed antenna, make sure the area around the antenna end the module protrudes at least 15mm from the mother board PCB and any metal enclosure. If this is not possible use the on board U.FL connector to route to an external antenna.

The area (6.5mmx17.3mm) under the antenna end of the module should be keep clear of metallic components, connectors, vias, traces and other materials that can interfere with the radio signal.



4.2 **U.F.L RF Connector**

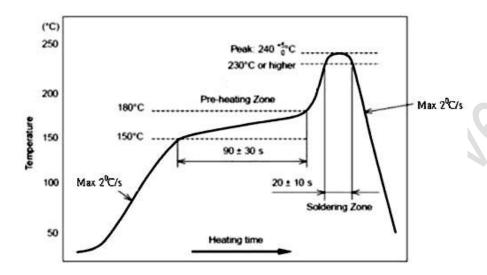
This module use U.F.L type RF connector for external antenna connection.



5 Others

5.1 Recommended Reflow Profile

Reflow times <= 2times (Max.)



Temperature profile for evaluation of solder heat resistance of a component (at solder joint)

5.2 **MSL/Storage Condition**



6 Sales Information

If you need to buy this product, please call MXCHIP during the working hours. (Monday \sim Friday A.M.9:00 \sim 12:00; P.M. 1:00 \sim 6:00)

Telephone: +86-21-52655026 / 52655025

Address: Room 811, Tongpu Building, No.1220 Tongpu Road, Shanghai

Post Code: 200333

Email: sales@mxchip.com

7 Technical Support

If you need to get the latest information on this product or our other product information, you can visit: http://www.mxchip.com/

If you need to get technical support, please call us during the working hours:

ST ARM technical support

+86 (021)52655026-822 Email: support@mxchip.com

Wireless network technical support

+86 (021)58655026-812 Email: support@mxchip.com

Development tools technical support

+86 (021) 52655026-822 Email: support@mxchip.com