Home Work 2

ECE3056

Fall 2014

This homework is to be turned in online on T-square. Handwritten (scanned) solutions are fine too.

You will be graded on your attempt to solve the problem, and not on correctness. If you attempt more than half of the questions and submit the solutions before the deadline, you will get the full 2 points regardless of your answers.

The solutions to the homework will be posted shortly after the submission deadline. The objective is that you will compare your solutions with ours and determine where you could have gone wrong.

Remember, even though this homework is only 2 points, if you do it with seriousness it will help you identify where you may be weak, and thus help you get more points on the Midterm (which is worth 20 points!).

The first few pages of the homework are taken from the midterm from my last offering of ECE3056.

Good Luck!

Department of Electrical and Computer Engineering

Georgia Institute of Technology

ECE3056A: Architecture, Concurrency, and Energy

Moinuddin K. Qureshi, Instructor

Exam 2, April 9, 2013

**Name :\_**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_



**GT Account:**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_



Problem 1 (20 points): \_\_\_\_\_\_\_



Problem 2 (20 points): \_\_\_\_\_\_\_



Problem 3 (20 points): \_\_\_\_\_\_\_



Problem 4 (20 points): \_\_\_\_\_\_\_



Problem 5 (20 points): \_\_\_\_\_\_\_



**Total (100 points)** : \_\_\_\_\_\_



This exam is given under the Georgia Tech Honor Code System. Anyone found to have submitted copied work instead of original work will be dealt with in full accordance with Institute policies.

Georgia Tech Honor Pledge: “**I have neither given nor received aid on this exam.”**

[**MUST sign**:] \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Note: Where needed, show all your intermediate results to receive full credit. Do all your work in this examination handout.

Use the back of the exam sheets if necessary.

Note: For your benefit, we have provided the ISA instructions, datapath, State machine, and control store table for LC-3b at the end of the exam sheet.

**GOOD LUCK!**

Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Problem 1 – “Potpourri” (20 points, there are four parts, each worth 5 points)

I. Write-back and Write-through are two policies for a cache.

Which policy require larger tag-store overhead? \_\_\_\_\_\_\_\_\_\_\_\_ Why (less than five words)?

The disadvantage of write-through policy is that it requires higher \_\_\_\_\_\_\_\_\_\_\_

II. Interrupts and exceptions are similar in that they both stop an executing process to execute a very different segment of code. However, two primary differences between interrupts and exceptions are as follows (in less than ten words each):

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

III. We have a 16KB L1 cache with linesize of 128 bytes. We wish to operate this cache without having TLB in the critical path of cache access while incurring very little hardware and software complexity. To do so, we must architect the cache to be (four words only) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

IV. We have a machine with 36-bit address space. We wish to use this machine with an OS that uses a pagesize of 4KB. If each Page Table Entry (PTE) is 4-bytes, the size of the page table will be \_\_\_\_\_\_\_\_

Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Problem 2 “Power of Vector Processors” (20 points) –

Consider the following code that averages four values, operating on arrays of 64 elements.

**for(i=0; i<64; i++){**

**A[i]=(B[i]+C[i]+D[i]+E[i])/4**

**}**

Assume that memory accesses take 11-cycle for an operation (Load or Store), ADD takes 2 cycles, and SHF operation takes 1 cycle.

I. Write the above code for a single-issue in-order scalar machine that contains auto-increment memory addressing mode and a single instruction (DECBNZ) that can do decrement of register value and conditional branch in one cycle.

How many dynamic instructions does this code execute: \_\_\_\_\_\_\_\_

How many cycles will this code take to execute:\_\_\_\_\_\_\_\_\_\_\_

**NOTE:** We did not cover Vector Processors yet. So, the portion on Vector Processors is removed from this question.

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Problem 3 “Architecting New Instruction” (20 points)

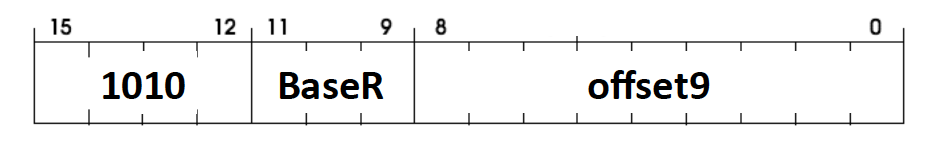
We want to add a new instruction ByteSwap (BSWAP) to the LC-3b ISA using the unused opcode “1010”. The specification of the BSWAP instruction is shown below:

**BSWAP**

**Assembler Formats**

BSWAP BaseR, offset9

**Encoding**

****

**Operation**

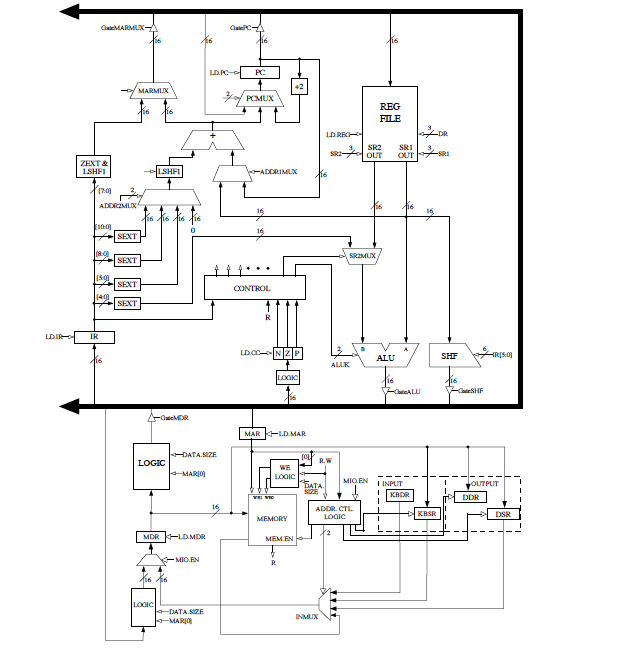
First Byte: MEM[BaseR + LSHF(SEXT(offset6), 1)]

Second Byte: MEM[BaseR + LSHF(SEXT(offset6), 1)+1]

Swap Contents of (First Byte, Second Byte)

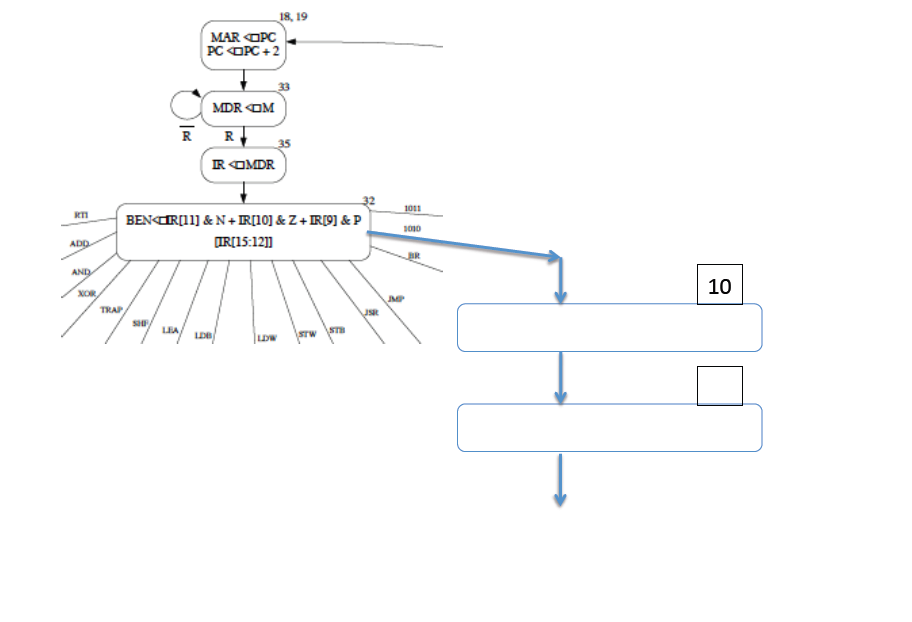
A word aligned memory location is accessed. The address of this location is computed with a Base Register and a 9-bit word offset. The two bytes of the word are swapped. This modified value is written to the memory word. Note, none of the register values or condition codes should be affected by the execution of this instruction (except for PC=PC+2, of course).   
  
  
I. Show the changes to the datapath of LC-3b as shown on the next page. While you are free to change the datapath any way you like, you should try to keep the changes to a minimum (simple solution is desirable).

Problem 3 Continued



Problem 3 Continued

II) Your job now is to develop the state assignments for the BSWAP instruction, and define what action needs to happen in each state. You must also specify the **control signals** that must be asserted in each newly added state (ignore the control signals that are not asserted). If your newly added structures to the datapath require any control signals, you must specify those signals as well. You can add as many states as you need. You must also specify the cond bits, J-bits, and state numbers (feel free to use any unused states, but your state assignments should work with the existing micro-sequencer). The last state must be connected back to state 18/19.



Problem 3 Continued

III) Assuming memory access takes 1 cycle, how many cycles would it take to execute the BSWAP instruction?

\_\_\_\_\_\_

IV) If we did not have the BSWAP instruction, how would you perform the BSWAP operation using existing instructions?

V) Assuming memory access takes 1 cycle, how many cycles would it take to execute the set of instructions in (IV)? \_\_\_\_\_\_\_\_

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Problem 4 “Caching Insights” (20 points)

An LC-3b computer system has a 256 byte physically addressed cache, with a linesize of 16 bytes.

The following loop is executed on this machine:

**sum=0;**

**for(i=0; i<256; i++){**

**sum += (Y[i]\*Z[i]);**

**}**

The starting address of the array are:

X: x4000

Y: x5180

Z: x6280   
  
Each element in the each array is stored as a 16-bit word. Assume that **sum** and **i** stored in registers.

I) Calculate the cache hit ratio for the loop if the cache is direct mapped. \_\_\_\_\_\_\_\_

II) What is the minimum associativity of the cache that will yield an improvement in hit rate, assuming that the cache capacity remains at 256B? Please be brief and specific

III) What is the improved hit rate with the new cache configuration? \_\_\_\_\_\_\_\_

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Problem 5 “DRAM Systems” (20 points)

We have a DRAM-based memory system of 64KB. This system has row-buffer size of 256 bytes, and 16-banks. The data-mapping policy is geared towards increasing the hit rate for applications with good spatial locality.

To open a row it takes 10 ns, to read/write from an open row it takes 8 ns, and to precharge (close) the row it takes 10ns. Assume that the row buffer of associated with each banks is initially empty.

Assume that the system has a cache linesize of 16 bytes. Shown below is a stream of eight cache misses that arrive at the memory system (note that the address that arrives at the memory system is the line-address and not the byte address).

**0xCAB, 0xCAD, 0xBAD, 0xDAB, 0xBBB, 0xCCC, 0x100, 0x10F**

You can assume that a request arrives at the memory system a long time after a previous request has been satisfied. The memory system supports both open-page and closed-page policies.

I) If we employ an open page policy, specify whether the row-buffer access outcome is a row buffer hit, row buffer miss, or row buffer conflict. Also specify the time required to service each access. Given your data mapping policy you should also specify the ID of the bank that a given request maps to.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Accesss | 0xCAB | 0xCAD | 0xBAD | 0XDAB | 0xBBB | 0xCCC | 0x100 | 0x10F |
| BankID |  |  |  |  |  |  |  |  |
| Rowbuf access  Outcome |  |  |  |  |  |  |  |  |
| Latency (ns) |  |  |  |  |  |  |  |  |

What is the total time to service the eight requests? \_\_\_\_\_

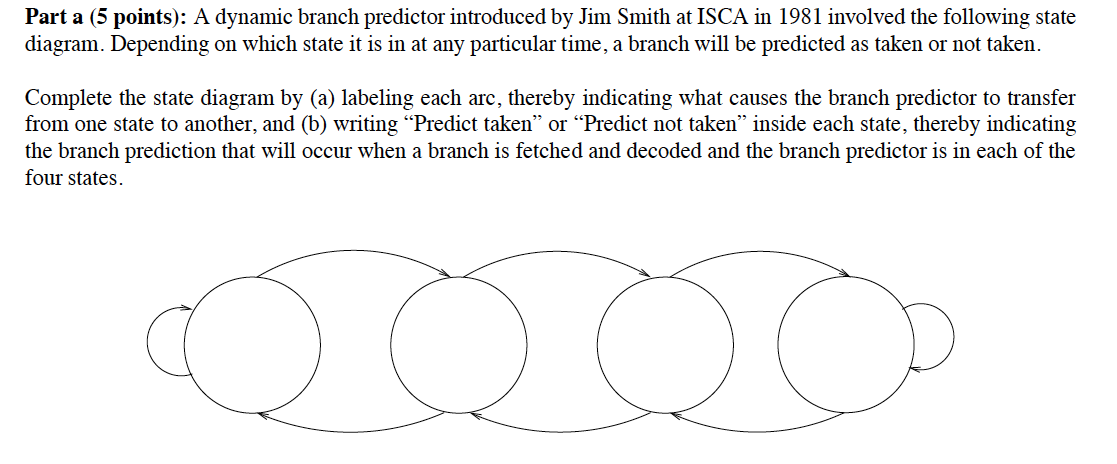
II) If we employ a closed-page policy, specify the time required to service each access. You may also specify the ID of the row-buffer for the given request, and the ID of the bank that request maps to.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Accesss | 0xCAB | 0xCAD | 0xBAD | 0xDAB | 0xBBB | 0xCCC | 0x100 | 0x10F |
| Latency (ns) |  |  |  |  |  |  |  |  |

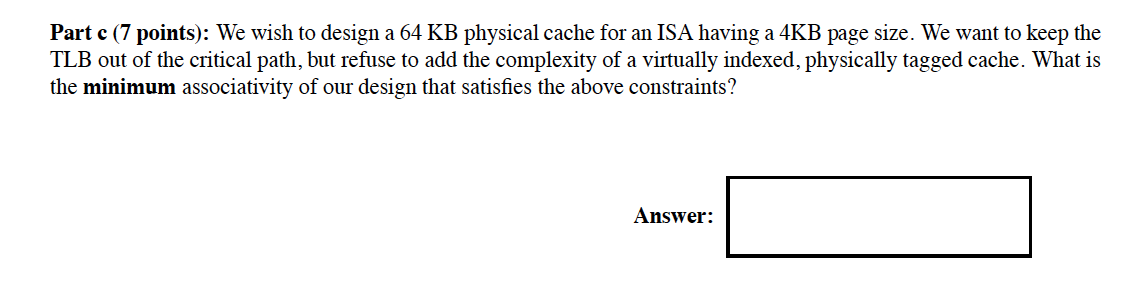
What is the total time to service the eight requests? \_\_\_\_\_

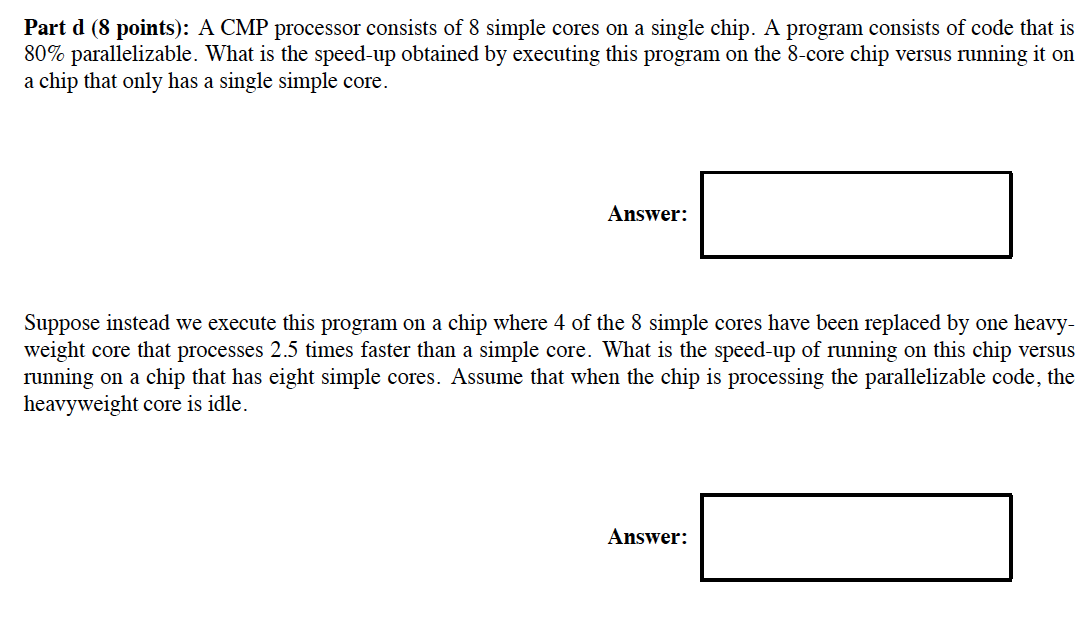
III) What policy would you recommend, open-page or closed-page? \_\_\_\_\_\_\_\_

Problem 6

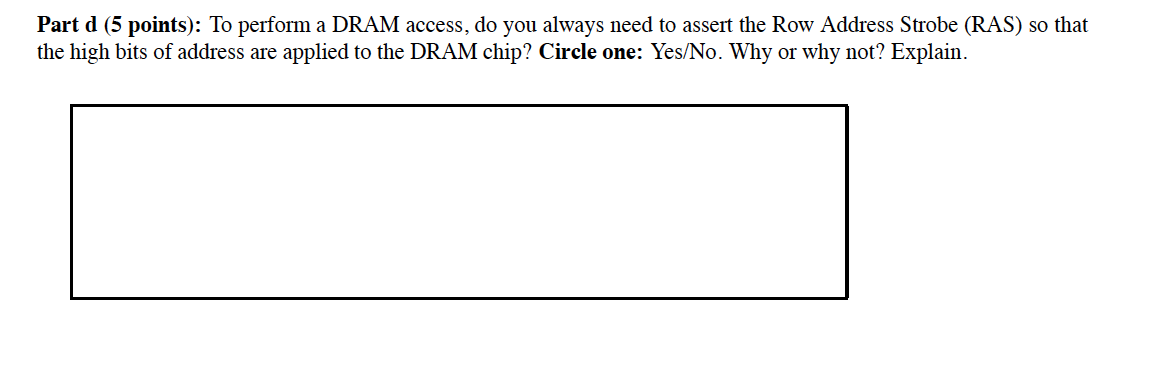


**Part B omitted**

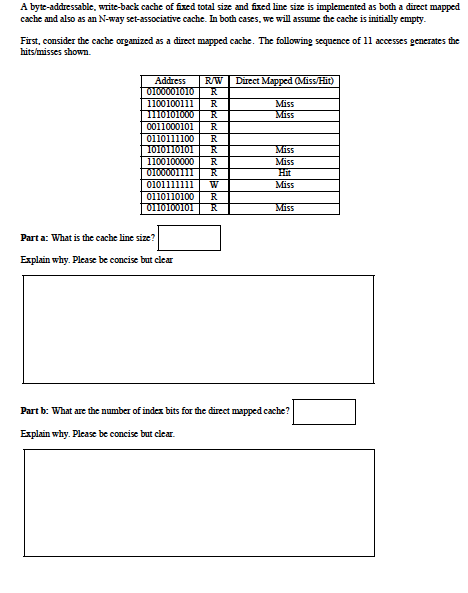


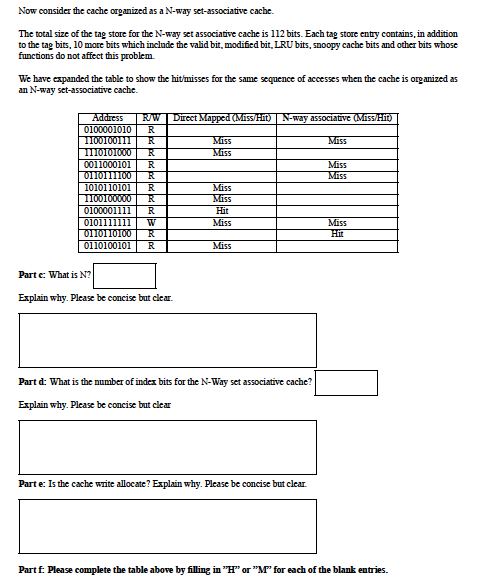


The below is part E (and not D)

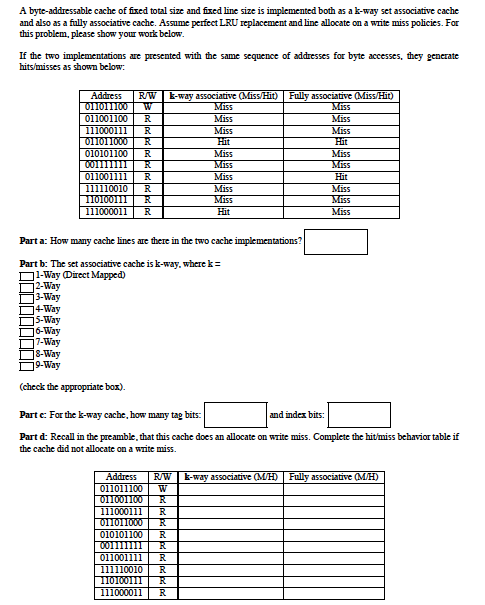


Q7:

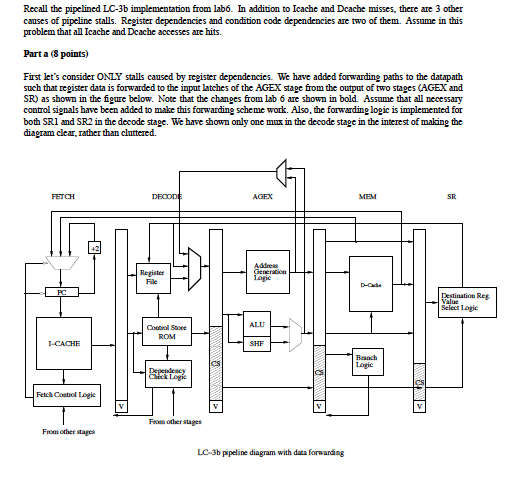




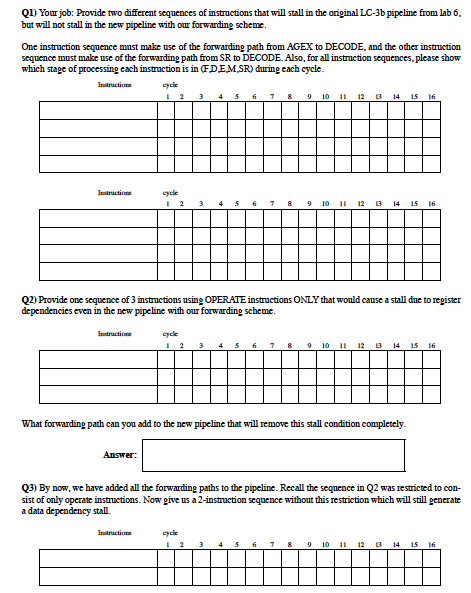
Q8:



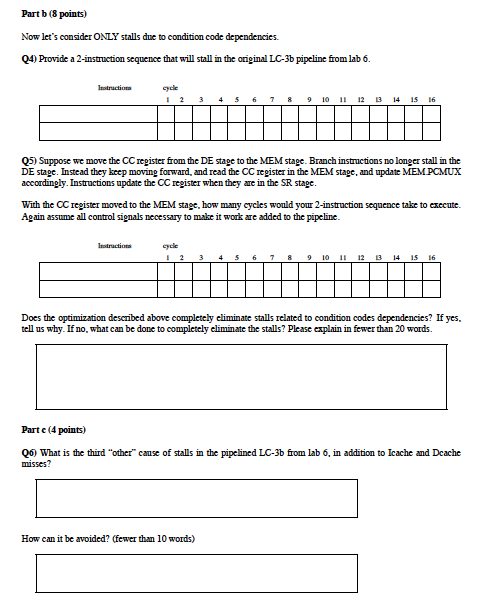
PROBLEM 9:



PROBLEM 9 Continued:



PROBLEM 9: Continued …



PROBLEM 10:

