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Micro Processors & Interfacing

16CS307

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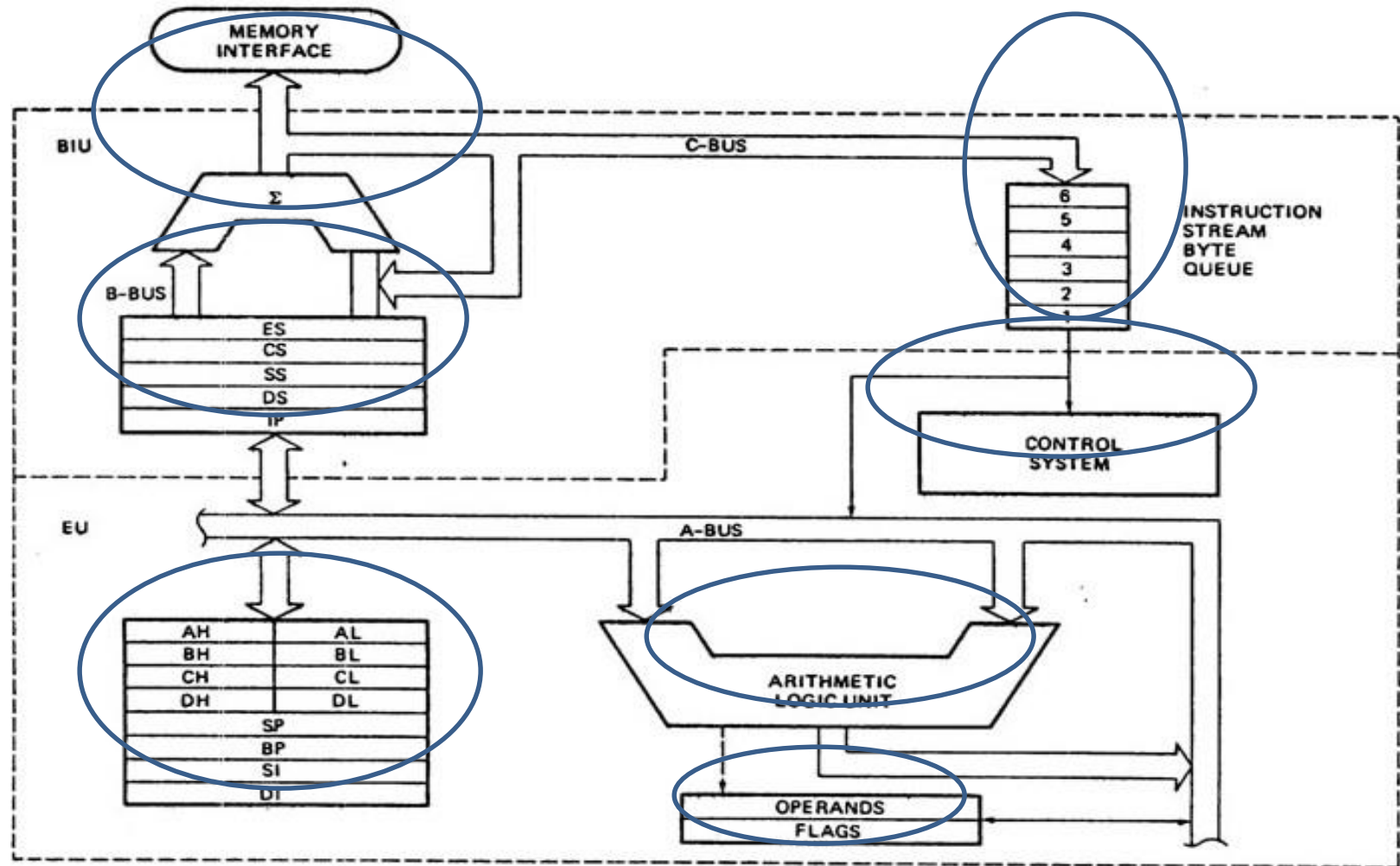


Architecture of 8086 Microprocessor

The 8086 CPU is divided into two independent functional units:

- Bus Interface Unit (BIU)
- Execution Unit (EU)

Ref: Hall



Architecture of 8086 Microprocessor

Functions of **Bus Interface Unit**

1. It sends address of the memory or I/O.
2. It fetches instruction from memory.
3. It reads data from port/memory.
4. It writes data into port/memory.
5. It supports instruction queuing.
6. It provides the address relocation facility.

Note:

- BIU contains the circuit for **physical address calculations**
and
- a pre-decoding instruction byte queue (6 Bytes long)

Architecture of 8086 Microprocessor

Instruction Queue

- To increase the execution speed,
- BIU fetches as many as six instruction bytes ahead to time from memory.
- All six bytes are then held in first in first out (**FIFO**) 6 byte register called instruction queue.
- Then all bytes have to be given to EU one by one.
- This pre fetching operation of BIU may be in parallel with execution operation of EU, which improves the speed execution of the instruction.

PIPELINING

Fetching the next instruction while the current instruction executes is called pipelining.

| | | | | | | |
|------|---------|--------|---------|--------|-------|--|
| 8085 | FETCH A | EXEC A | FETCH B | EXEC B | ----- | |
|------|---------|--------|---------|--------|-------|--|

| | | | | | | |
|------|---------|---------|---------|---------|-------|--|
| 8086 | FETCH A | FETCH B | FETCH C | FETCH D | ----- | |
| | | EXEC A | EXEC B | EXEC C | ----- | |

Instruction fetching and executing in 8085 and 8086.

It increases the speed of operation of microprocessor 8086

Architecture of 8086 Microprocessor

Execution Unit (EU)

The functions of execution unit are:

- To tell BIU where to fetch the instructions or data from.
- To decode the instructions.
- To execute the instructions.
- The EU contains the control circuitry to perform various internal operations.
- A decoder in EU decodes the instruction fetched memory to generate different internal or external control signals required to perform the operation.
- EU has 16-bit ALU, which can perform arithmetic and logical operations on 8-bit as well as 16-bit.

Architecture of 8086 Microprocessor

Execution Unit (EU)

EU has the following functional parts these are

- a). ALU
- b). Register Set.
- c). Operand & Flag Register.
- d). Control System.

Architecture of 8086 Microprocessor

ALU in Execution Unit (EU)

a). **ALU (Arithmetic and Logical Unit):-** It performs Arithmetic and Logical operations on 8 bits/16bits. The Bit Capacity of ALU is 16bits.

It can do the following **arithmetic** operations :

- | | | |
|--------------|-----------------|---------------------|
| i) Addition | ii) Subtraction | iii) Multiplication |
| iv) Division | v) Increment | vi) Decrement |

Arithmetic operations may be performed on four types of numbers

- | | |
|---------------------------------|-----------------------------------|
| Unsigned binary numbers | Signed binary numbers (Integers) |
| Unsigned packed decimal numbers | Unsigned unpacked decimal numbers |

The ALU can also perform **logical** operations such as

- | | | | | | |
|-----------------------|----------------------------------|---------|-----------|---------|-------------------|
| i) NOT | ii) AND | iii) OR | iv) EX-OR | v) TEST | vi) Logical Shift |
| vii) Arithmetic Shift | viii) Circular Shift (or) Rotate | | | | |

Architecture of 8086 Microprocessor

Control Unit & Registers in Execution Unit (EU)

b). Control System: - It is divided into 2 parts. They are

Decoding circuit----it decodes the instruction.

Timing circuit---- it generates control signals at appropriate times.

c). Register Set:- It is used to hold the 16-bit information.

The information is address, data or result of some operation.

d). Operand & Flag Register: -

Operand holds the result produced by ALU.

Flags are also called as PSW (program status word) of 8086.

Each single bit is called flag.