

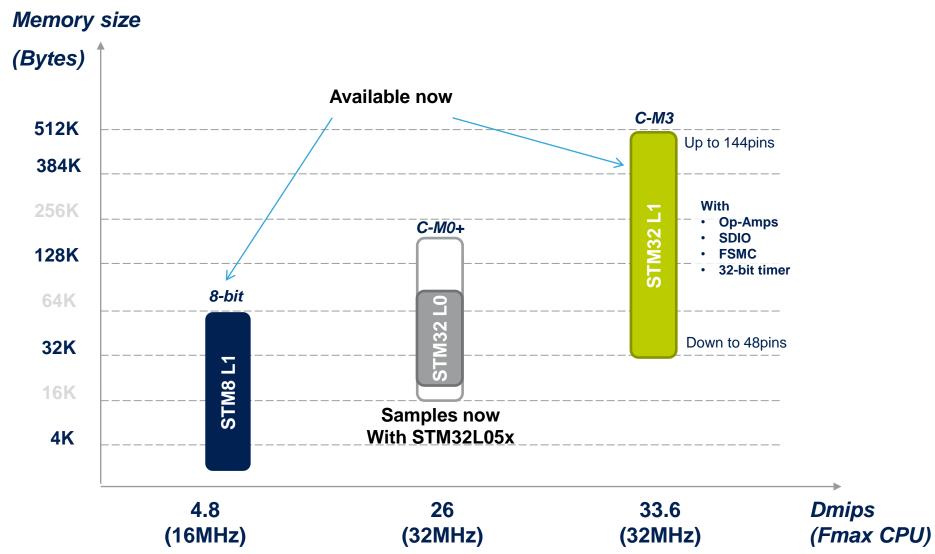
STM32 Ultra-low-power CortexTM-M0+







STMx Ultra-low-power Family







What's new on STM32L0 Platform

- Cortex[™]-M0+ on board with MPU
- Smaller package for STM32L family MCU (down to 20pins)
- Aggressive power consumption: -20% vs. STM32L1 (Active mode)
- Stop mode down 950nA with
 - Full RAM retention (400 nA)
 - RTC Running (400 nA)
 - Pulse Counter (150 nA)
 - Snooze wakeup on UART
- Larger temperature range functionality: -40°C up to +125°C¹
- New analog peripherals (12-bit ADC 1Msps @ 240 μA)
- USB 2.0 FS: Crystal less, BCD², LPM³





Innovative Peripherals (**)



Autonomous Peripherals

Low-power Pulse counter

- Independent 16-bit timer, available also in Stop mode
- Pulse counter with no clock running
- · Or clocked by LSE, LSI, HSI, APB.
- It is able to wakeup the system from Stop mode.
- Programmable digital glitch filter
- Encoder mode

UART

- Snooze wakeup
- Wake from Stop using UART with dedicated ID/Byte
- · Baud rate independent from APB clock

Low-Power UART

- Up to 9600 bauds running on LSE 32kHz
- Snooze wakeup
- · Wake from Stop using UART with dedicated ID/Byte

I2C

- with FM+ (programmable add, data bit length)
- frequency independent from APB clock

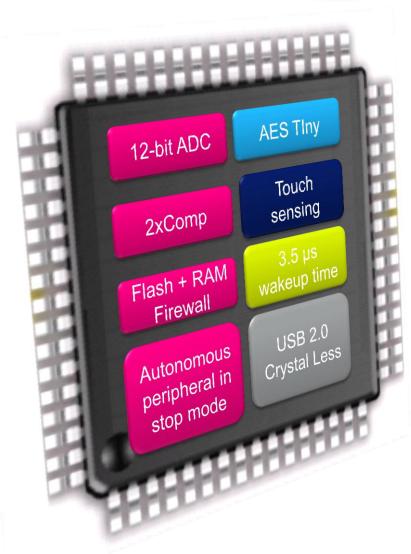
Analog

12 bit ADC: 1MSPS → 240 μA / 10kSPS → 24 μA

system

- Firewall
- Wakeup on MSI, HSI or HSI/4
- USB+CRS= crystal less







STM32 L0xx – Product lines

Common features architecture

Cortex-M0+
32 MHz speed with MPU

Multiple USART, SPI, I²C Low-power UART

Multiple 16-bit timers Low-power 16-bit timer

Built-in 16 MHz and 38 kHz RC oscillators

2x watchdogs

Reset circuitry POR/PDR

Brown Out Reset Program Voltage Detector

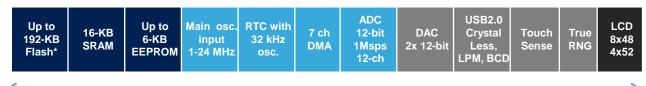
2x comparators

AES 128-bit

Dynamic Voltage Scaling

Firewall protection (Flash and RAM)

STM32L0x3 - USB & LCD line - 32-K to 192-Kbyte Flash



32 pins to 100pins

STM32L0x2 – USB line - 32 to 192-Kbyte Flash

Up to 128-KB Flash	16-KB SRAM	6-KB	Main osc. input 1-24 MHz	32 kHz	7 ch DMA	12-bit ADC 1Msps 12-ch		USB2.0 Crystal Less, LPM, BCD	Sense	True RNG
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32 pins to 100pins

STM32L0x1 – Access line - 16-K to 192-Kbyte Flash

Up to 128-KB Flash	16-KB SRAM	Up to 6-KB EEPROM	input	RTC with 32 kHz osc.	4 ch DMA	12-bit ADC 1Msps 12-ch

20 pins to 100pins





STM32L05* block diagram - 64-KB

Key features

- 2x12-bit DAC
- USB FS Charging class/ Clock recove
- 2 SPI, 1 I2S
- Touch-Sensing up to 24 keys
- LCD Display 8x28
- Flash + Ram Firewall
- 3x16 bit timers (1x4ch + 2x2ch)
- AES 128-bit

Improvement

- Full 1.8V to 3.6V functional @32MHz
- SAR 12-bit-ULP 1Msps (240µA-linear)
- · Com. periph.
 - 2xl²C (1 available in stop)
 - 2xUSART
 - 1xLPUART available in stop
- 16-bit LPTIM
- 175 µA/MHz product
- 0.8 µA: Stop mode + RTC + 8KB RAM
 - Wakeup time from stop
 - <5µs from Flash
 - <3.5µs from Ram

System

Power supply 1.8 V regulator POR/PDR/PVD/BOR

Xtal oscillators 32 kHz + 1 ~32 MHz

Internal RC oscillators 38 kHz + 16 MHz

PLL

Internal multispeed ULP RC oscillator 64 kHz to 4 MHz Clock control

RTC/AWU

SysTick timer

2x watchdogs (independent and window)

26/37/51 I/Os

Cyclic redundancy check (CRC)

Voltage scaling 3 modes

Display

LCD driver 8x28

ARM Cortex-M0+ CPU 32 MHz

Nested vector interrupt controller (NVIC) Memory protection unit (MPU)

SW debug

AHB-Lite+ bus matrix

APB-bus

Up to 7-channel DMA

Touch-sensing Up to 24 keys

Analog

2x ultra-low-power

Temperature sensor

1x 12-bit ADC SAR 16 channels / 1 µs

1x 12-bit DAC

Up to 64-Kbyte Flash memory

Up to 8-Kbyte SRAM Up to 2-Kbyte EEPROM

20-byte backup data

BOOT ROM

Connectivity

2x SPI, 2x I2C

2x USART LIN, smartcard, IrDA, modem control

1x ULP UART

1x USB 2.0 FS (Crystal-less)

Control

1x ultra-low-power 16-bit timer

3x 16-bit timer

Encryption

AES (128-bit)





STM32L07* block diagram - 192-KB

Key features

- 2x12-bit DAC
- USB FS Charging class/ Clock recovery
- 2 SPI, 1 I2S
- Touch-Sensing up to 24 keys
- LCD Display 8x48
- Flash + Ram Firewall
- 4x16 bit timers (2x4ch + 2x2ch)
- AES 128-bit

Improvement

- Full 1.8V to 3.6V functional @32MHz
- SAR 12-bit-ULP 1Msps (240µA-linear)
- · Com. periph.
 - 3xl²C, 1 available in stop
 - 4xUSART
 - 1xLPUART available in stop
- 16-bit LPTIM
- 175 µA/MHz product
- 0.8 µA: Stop mode + RTC + 20KB RAM
- Wakeup time from stop



- <5us from Flash
- <3.5us from Ram

System

Power supply 1.8 V regulator POR/PDR/PVD/BOR

Xtal oscillators 32 kHz + 1 ~32 MHz

Internal RC oscillators 38 kHz + 16 MHz

PLL

Internal multispeed ULP RC oscillator 64 kHz to 4 MHz

Clock control

RTC/AWU

SysTick timer

2x watchdogs (independent and window)

26/37/51 I/Os

Cyclic redundancy check (CRC)

Voltage scaling 3 modes

Display

LCD driver 8x48

ARM Cortex-M0+ CPU **32 MHz**

Nested vector interrupt controller (NVIC) Memory protection unit (MPU)

SW debug

AHB-Lite+ bus matrix

APB-bus - I/O port Bus

Up to 7-channel DMA

Touch-sensing Up to 24 keys

Analog

2x ultra-low-power

Temperature sensor

1x 12-bit ADC SAR 16 channels / 1 µs

1x 12-bit DAC

Up to 192-Kbyte Flash memory Up to 20-Kbyte SRAM

Up to 6-Kbyte EEPROM

20-byte backup data

BOOT ROM

Connectivity

2x SPI. 3x I2C

3x USART LIN, smartcard, IrDA, modem control

1x ULP UART

1x USB 2.0 FS (Crystal-less)

Control

1x ultra-low-power 16-bit timer

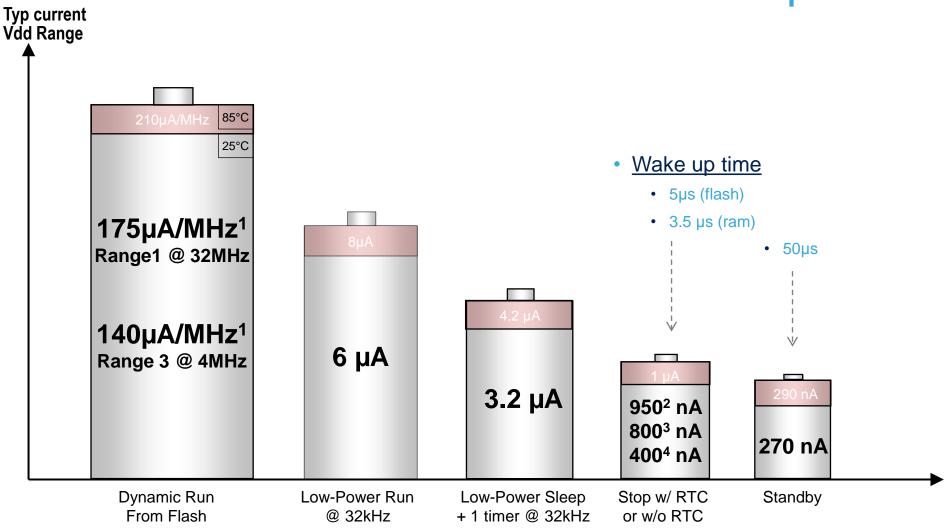
4x 16-bit timer

Encryption

AES (128-bit)



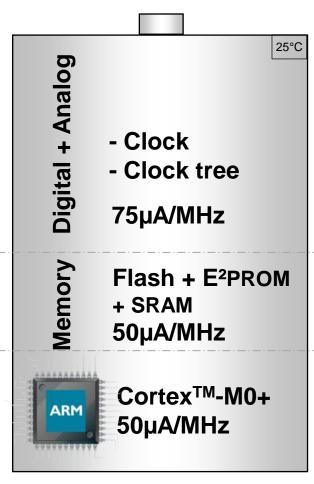
STM32 L05* - Power consumption





- Dhrystone power consumption value executed from Flash with VDD=3V
- 2. STOP mode consumption with : Full Ram retention + RTC + Low-power Pulse counter
- 3. STOP mode consumption with : Full Ram retention + RTC
- 4. STOP mode consumption with : Full Ram retention

STM32 L05* - Ultra-low-power platform



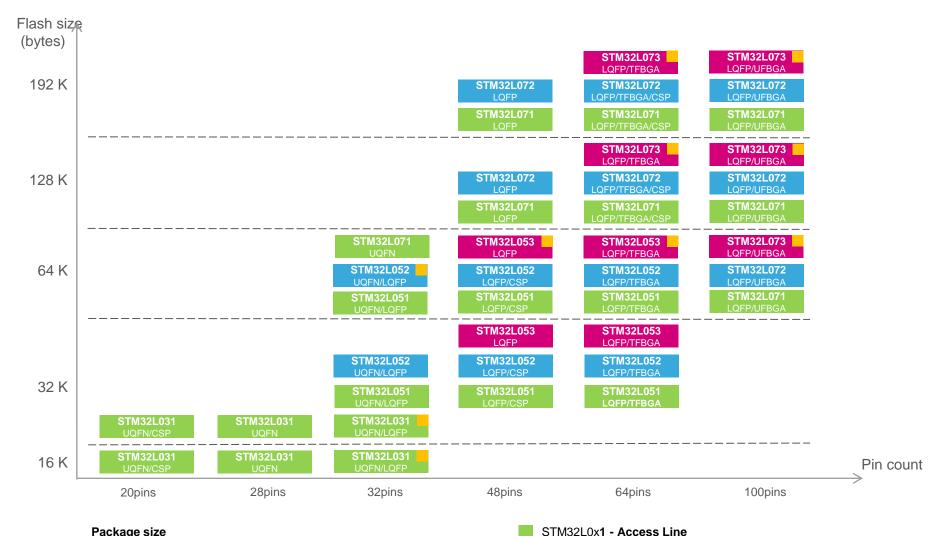
Dynamic Run From Flash VDD=3.6V – CPU speed 32MHz





STM32L0x – portfolio

CortexTM-M0+ @ 32MHz - 100+ P/N





UQFN: 20pins in 3x3mm / 28pins in 4x4mm / 32pins in 5x5mm LQFP: 32-to 48pins in 7x7mm / 64pins in 10x10mm / 100pins in 14x14mm

BGA: 64pins in 5x5mm / 100pins in 7x7mm



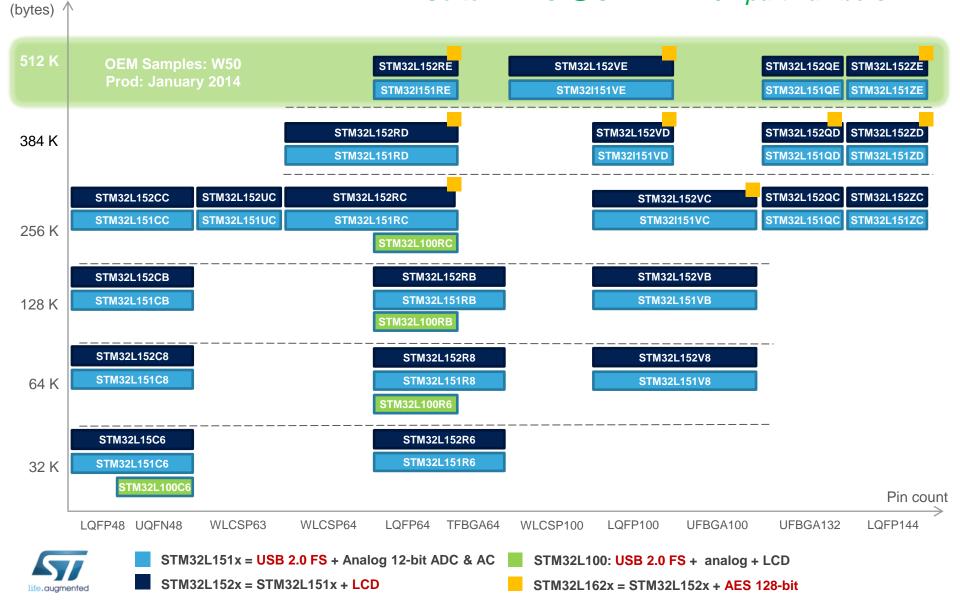




Flash size

STM32L1x – portfolio

CortexTM-M3 @ 32MHz - 70+ part numbers





www.st.com/stm32

