AN4445
Application note

STM32L0xx ultra-low power features overview

Introduction

The STM32L0x Series ARM Cortex™-M0+ based belongs to the STMicroelectronics ultra-low power continuum and complements the well known 8-bit STM8Lx Series and 32-bit ARM Cortex™-M3 based microcontrollers offering new peripherals package size.

Both microcontroller families are based on the ST's proprietary 110 nm ultra-low leakage process and have many analog and digital peripherals in common, which eases the transition from one architecture to the other and offers users the opportunity to capitalize on the knowledge acquired on one platform.

This application note describes the key low power features of the STM32L0xx family and explains their benefits for applications where energy consumption is a major concern.

Important note: This document is not intended to replace STM32L0xx datasheets. All values given in this document are for guidance only. Please refer to the related datasheet to get guaranteed values and up-to-date characterization data.

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1 STM32L0xx main features

Based on the solid foundations of the award-winning STM32F0x and STM32L1 families, the STM32L0xx embeds various innovations which minimize the consumption in different configurations, while maintaining most of the existing peripherals and a quasi pin-to-pin compatibility.

For a given manufacturing process and die area, the consumption of a microcontroller largely depends on two factors which can be controlled dynamically: voltage and frequency. In the STM32L0xx devices, an internal low drop regulator supplies most of the logic circuitry with a fixed voltage: this guarantees that consumption is kept minimal whatever the supply voltage, along the lifetime of portable battery-supplied products, down to 1.65 V.

If we consider the clock sources, several cascaded clock prescalers, gating techniques and peripheral-by-peripheral clock management allow only the necessary logic gates to be activated, and at the adequate frequency. These are now design practices commonly used for reducing the consumption in Run mode. For the STM32L0xx, additional efforts have been done in this direction with the implementation of voltage scaling to reach an even higher processing efficiency.

However, all ultra-low power requirements cannot be met by simply focusing on run time: for most applications, the challenge is to spend the minimum time and energy in this mode and find the adequate low power mode.

The improvements do not come only from the deep sleep modes optimized to eliminate every ten nA of leakage. The system has also been complemented with seven low power modes and a set of peripherals tuned for low power (such as the calendar real-time clock and glass LCD controller). These items are described in more detail hereafter.

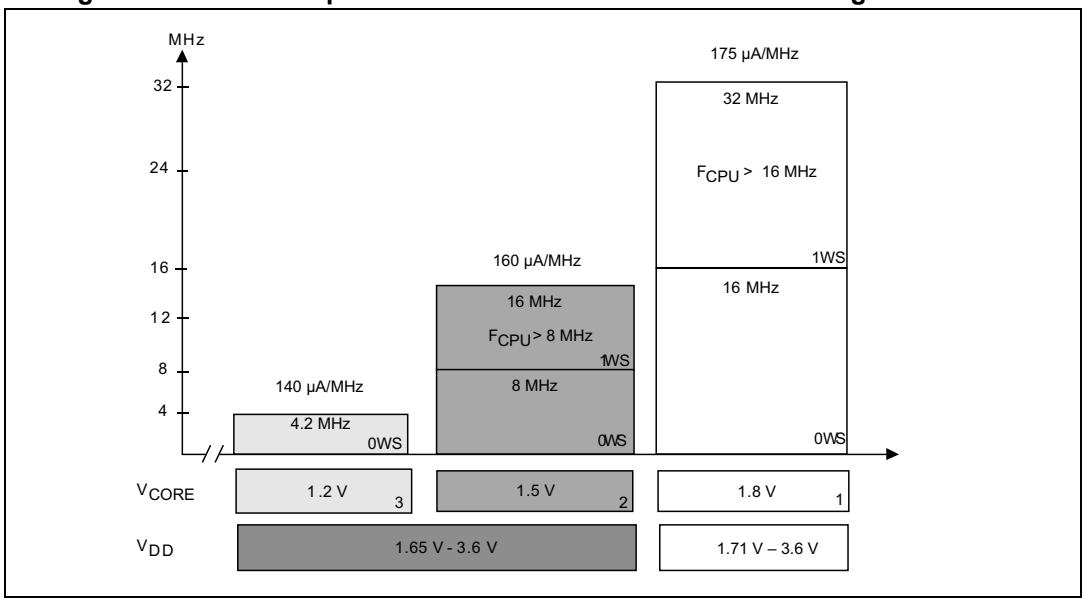
2 Energy-efficient processing

The STM32L0 is built around the Cortex-M0+, an industry standard 32-bit core, which has been designed, among other criteria, for low power applications.

The Cortex-M0+ offers a class-leading performance and code density. Although performance is not naturally linked with low current consumption, it is a key benefit for most of the low power applications which have to wake up periodically to execute software tasks. In this case, the Cortex-M0+ spends less time in Run mode due to its processing performance, thus maximizing the time in deep sleep mode. If we consider only the processing consumption, expressed in mA/DMIPS (DMIPS standing for Dhrystone MIPS measured using the public benchmark Rev 2.0), the performance of the Cortex M0+ is significantly better than that of the other architectures, in particular 16-bit microcontrollers.

The performance in DMIPS/MHz being given by the core and its memory interface, the processing consumption in mA/DMIPS can be maximized using voltage scaling. This method, also called undervolting, consists of adapting dynamically the supply voltage of the internal logic with the operating frequency. The STM32L0xx offers three dynamically selectable voltage ranges, as summarized in the following figure, from 1.8 V (range 1) down to 1.2 V (range 3), which offers a gain of more than 25% in terms of consumption.

Figure 1. STM32L0xx performance versus VDD and VCORE range



A typical example is portable healthcare equipment with USB device capability.

As long as it works in standalone mode, 4 MHz are sufficient to acquire and process the data from the analog front-end. In this case, the internal logic can be supplied with 1.2 V only.

However, executing a USB software stack when the system is connected to the USB interface of a PC requires more processing power: in this case, the device can be placed in "high-performance mode", where the internal voltage is 1.8 V. It can then execute code at 32 MHz while the USB peripheral is supplied by a 48-MHz clock. Voltage scaling is used to deal with the contradictory requirements of these two operating modes without having to compromise on the dynamic current consumption.

3 Numerous low power modes

At a higher architectural level, the power consumption of the STM32L0 can be modulated by entering one of seven low power modes. The power consumption can be reduced by progressively disabling the frequency-independent current sources (the clock sources, the non-volatile memory and the regulator) up to the point where most of the chip is powered down. The following table summarizes the features available for each mode and provides an indication of the current consumption.

Table 1. STM32L0xx low power mode overview

Low power mode	Consumption	CPU	Flash / EEPROM	RAM	DMA & Peripherals	Clock	LCD	RTC
Sleep	41 µA/MHz (Range 1) 36 µA / MHz (Range 2) 35 µA/MHz (Range 3)	No	ON	ON	Active	Any	Available	
Low power run	8.55 µA (Flash OFF, 32 kHz)	Yes	ON or OFF	ON	Active	MSI	Available	
Low power sleep	4.65 µA (peripherals OFF)	No	OFF	ON	Active	MSI	Available	
Stop with RTC	0.82 µA (1.8 V) 1.0 µA (3 V)	No	OFF	ON	Frozen	LSE, LSI	OFF	ON
Stop	415 nA	No	OFF	ON	Frozen	-	OFF	OFF
Standby with RTC	655 nA (3 V) 845 nA (1.8 V)	OFF	OFF	OFF	OFF	LSE	OFF	ON
Standby	290 nA	OFF	OFF	OFF	OFF	-	OFF	OFF

Two new modes have been implemented on the STM32L0xx in addition to the STM32F modes: the Low power run and Low power sleep modes. They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is processing continuously at low speed to minimize current variations. Several functional blocks can be used to reach a very low current:

- The voltage regulator is in low power (LP) mode to reduce its quiescent current
- Non-volatile memory can be switched off, processing being done on the 8-Kbyte RAM
- The master clock source comes from the MSI internal RC oscillator, which can be reduced down to 1.5 µA.

The maximum current that the regulator can deliver in LP mode only limits the operating frequency and the number of peripherals that can be activated.

4 A set of peripherals tailored for low power

Several peripherals require special attention, either because of their intrinsic high consumption or because they are always powered up.

The STM32L0xx embeds a 12-bit / 1.14 MSps ADC. This very fast but accurate converter can jeopardize the battery lifetime if left powered-up continuously, with a 300 µA typical consumption at maximum speed. As the ADC consumption is roughly proportional to the acquisition frequency, from consumption standpoint the application can choose between two solutions, either performing the acquisition at low speed to limit maximum current or doing it at maximum speed to switch in ultra-low power mode quickly.

When the acquisition is performed slowly, the ADC consumption itself can go down to few tens of µA drastically limiting the maximum current. This can be mandatory when the power source provides a limited current. The drawback, if the CPU has no other task to perform during that time, can be the increased time spent in run or sleep mode (or Low Power run or Low power sleep modes) versus the time spent in ultra-low power mode (stop or standby).

When the acquisition is made at high speed the ADC can go in low power mode thanks to auto-off mode very quickly and the micro controller can go into ultra-low power mode as soon as the acquisition is processed.

Seven peripherals have been developed to operate continuously even in Stop mode, where the system clock is stopped, with the main oscillator and memory powered down.

- A pair of ultra-low power comparators is available to monitor analog voltages with a current down to 3 µA. These comparators can wake up the MCU as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.
- An RTC peripheral provides a clock/calendar with two alarms, includes a periodic wake-up unit and several application specific functions (timestamp, tamper detection …). It can remain enabled in the lowest power mode (standby) where most of the chip is powered down, and wake up the full MCU circuitry in case of an alarm or tamper detection for instance. It also contains 80 bytes of backup registers to store contextual information when exiting from standby mode. This peripheral has been designed using asynchronous design techniques to minimize its consumption (below 1 µA).
- The glass LCD is one of the most common displays in low power applications, because of its inherently low current consumption, low price and customization easiness. The STM32L0xx includes a versatile LCD controller, which can drive displays with up to 8 common lines and 32 segments, with the capability of selecting individually the I/O ports assigned to the LCD for an optimal use of the chip alternate functions. It also controls an optional internal step-up converter to maintain the LCD contrast on a wide range of V_{DD} values with consumptions as low as 5 µA (LCD consumption not included).
- The Low power timer (LPTIM) is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to its diversity of clock sources, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as «Pulse Counter» which can be useful in some applications. Also the LPTIM capability to wake up the system from low power modes, makes it suitable to realize «Timeout functions» with extremely low power consumption. The LPTIM introduces a flexible clock scheme

that provides the needed functionalities and performance, while minimizing the power consumption.

- The low power universal asynchronous receiver transmitter (LPUART) is an UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 baud/s. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock. Even when the microcontroller is in deep stop mode , the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption).
- The I2C is able to wakeup the MCU from Stop mode (APB clock is off), when it is addressed. All addressing modes are supported. The HSI16 oscillator must be selected as the clock source for I2CCLK in order to allow wakeup from STOP. During Stop mode, the HSI16 is switched off. When a START is detected, the I2C interface switches the HSI16 on, and stretches SCL low until HSI16 is woken up. HSI16 is then used for the address reception. In case of an address match, the I2C stretches SCL low during MCU wakeup time. The stretch is released when ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI16 is switched off again and the MCU is not woken up.
- The USART is able to wakeup the MCU from Stop mode when USART clock is HSI16 or LSE. Several sources of wakeup from STOP mode can be selected:
  – Wakeup on adress match
  – Wakeup on Start bit detection
  – Wakeup on RXNE.

Table 2. Functionalities depending on working mode (from Run/active to standby)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	-	Y	-	-	-	-	-
Flash memory	Y	Y	Y	N	-	-	-	-
RAM	Y	Y	Y	Y	Y	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-
EEPROM	Y	-	Y	Y	Y	-	-	-
Brown-out rest (BOR)	Y	Y	Y	Y	Y	Y	Y	-
DMA	Y	Y	Y	Y	-	-	-	-
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	-
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	-

Table 2. Functionalities depending on working mode (from Run/active to standby) (continued)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	-
Power Down Rest (PDR)	Y	Y	Y	Y	Y	-	Y	-
High Speed Internal (HSI16)	Y	Y	-	-	-	-	-	-
High Speed External (HSE)	Y	Y	-	-	-	-	-	-
Low Speed Internal (LSI)	Y	Y	Y	Y	Y	-	-	-
Low Speed External (LSE)	Y	Y	Y	Y	Y	-	-	-
Multi-Speed Internal (MSI)	Y	Y	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	-	-	-	-
RTC	Y	Y	Y	Y	Y	Y	Y	-
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto WakeUp (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
USART	Y	Y	Y	Y	Y	Y	-	-
LPUART	Y	Y	Y	Y	Y	Y	-	-
SPI	Y	Y	Y	Y	-	-	-	-
I2C	Y	Y	Y	Y	-	Y	-	-
ADC	Y	Y	-	-	-	-	-	-
DAC	Y	Y	Y	Y	Y	-	-	-
Temperature sensor	Y	Y	Y	Y	Y	-	-	-
Comparators	Y	Y	Y	Y	Y	Y	-	-
16-bit and 32-bit Timers	Y	Y	Y	Y	-	-	-	-
LPTIMER	Y	Y	Y	Y	Y	Y	-	-
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing controller (TSC)	Y	Y	-	-	-	-	-	-
SysTick Timer	Y	Y	Y	Y	-	-	-	-

Table 2. Functionalities depending on working mode (from Run/active to standby) (continued)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
GPIOs	Y	Y	Y	Y	Y	Y	-	2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash)	Down to 37 µA/MHz (from Flash)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the five possible clock sources of the STM32L0.

Two external oscillators can be used for applications requiring high precision:

- The HSE clock (4-24 MHz high speed external clock), typically used to feed the PLL and to generate a CPU clock frequency of up to 32 MHz and a 48-MHz frequency for the USB controller
- The LSE (typically 32.768 kHz low speed external clock) normally used to provide a low power clock source to the real time clock but which can also be used as LCD clock.

Four internal oscillators can be selected for various tasks:

- The LSI clock (37 kHz low speed internal clock) is a low accuracy ultra-low power source that can feed the real time clock (with a limited accuracy), the LCD controller and the independent watchdog
- The HSI16 clock (16 MHz high speed internal clock) is a high speed voltage-compensated oscillator
- The HSI48 clock (48 MHz high speed internal clock) is a high speed voltage controlled oscillator that can be automatically trimmed thanks to LSE or USB's start of frame signal. It is used to achieve the USB crystal less feature
- The MSI clock (64 kHz to 4.2 MHz multi speed internal clock) is a medium accuracy oscillator with adjustable frequency and low current consumption. It is designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies.

The following table summarizes the characteristics and uses of the various oscillators.

Table 3. STM32L0xx clock source characteristics (preliminary data(1))

Clock source	Use	Frequency	Consumption (typical)	Accuracy	Factory trimming	User trimmable
HSE	Master clock (+ RTC & LCD)	1-24 MHz	0.5 to 0.7 mA	Crystal dependent, down to tens of ppm	Not applicable	
LSE	RTC and LCD	32.768 kHz (typical)	0.45 µA (1.8 V) 0.6 µA (3 V)	Crystal dependent, down to a few ppm		
HSI16	Master clock	16 MHz	100 µA	0.4% typical(2)	Yes	Yes
HSI48	USB, Random number generator	48 MHz	300 µA	Fits USB needs	±1.7%	±0.1%
MSI	Master clock	65.5 kHz 131 kHz 262 kHz 524 kHz 1.05 MHz 2.1 MHz 4.2 MHz	0.75 µA 1.0 µA 1.5 µA 2.5 µA 4.5 µA 8.0 µA 15 µA	0.5% typical(2)	Yes	Yes
LSI	RTC, LCD & ind. WDG	38 kHz	0.4 µA (3 V)	-30% to +50%(3)	No	No, but f_{LSI} can be measured

1. Based on preliminary characterization or design simulations. See product datasheet for detailed electrical characteristics

2. Accuracy reached after trimming. See product datasheet for low voltage and temperature drift details
3. -10% to +4% drift after initial measurement

The price of a crystal oscillator may not be neglected in cost sensitive applications. For this reason, the STM32L0xx offers several options to measure the internal oscillators.

Although HSI16 and MSI are factory trimmed, they can be further trimmed by 0.5% steps during run time to compensate for frequency deviations due to temperature and voltage changes. Similarly, manufacturing process deviations of the LSI can be evaluated and compensated using a higher accuracy clock reference, either internally (HSI16) or externally (LSE or HSE).

As an example, in an application where a 32.768 kHz crystal is used for the RTC, it is interesting to use the low power MSI oscillator which can provide a clock frequency of up to 4 MHz for the CPU with a typical consumption of 20 µA. Taking advantage of the high precision of the LSE crystals (typically a few tens of ppm), it is possible to determine the MSI frequency with the same resolution, and then to trim it on-the-fly.

6 Ultra-safe supply monitoring

The STM32L0xx includes a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) retrieved from the non-volatile memory to perform MCU initialization, even before the user's reset phase. This is also during this period that V_{DD} can be altered with glitches coming from the battery insertion or because of a weak power source.

The ultra-safe power-on reset circuitry guarantees that the reset is released only if the V_{DD} is above 1.8 V, whatever the slope of the V_{DD} ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts.

Once the power-up phase is completed, the user can choose to activate or not the brown-out reset (BOR) detector for a continuous battery monitoring, and select one of 5 thresholds. This is an option stored in the non-volatile memory to make this power supervision completely software independent. It is completed by a 7-level programmable voltage detector (PVD) that can be enabled by software to generate an early interrupt in case of a voltage drop.

The consumption of both the BOR and PVD modules is below 3 µA, when continuously powered, but it can remain significant in the deep sleep modes. If needed, the power supervision module can be programmed to have the BOR and the PVD disabled during the deep sleep phase and enabled again automatically on wake-up events. This minimizes the current consumption when the application is in idle mode (with usually a slightly higher and very stable supply due to an extremely light load). However, this does not jeopardize the safety when the execution starts again.

The STM32L0 is one of the few standard MCUs on the market with an operating range down to 1.65 V and only very few limitations (ADC and DAC need 1.8 V to achieve defined accuracy, USB needs VDD above 1.71 V to run and its transceiver needs VDD_USB above 3.0 V to be USB compliant.). A dedicated STM32L0xx device with permanently disabled BOR is available and can be used in applications with a voltage tolerance of 1.8 V $\pm$8%.

In this case, a "zero current" Power-on / Power-down reset (POR/PDR) module remains active and releases the reset after a hard-coded temporization. It is then up to the user to guarantee that the V_{DD} slope during the start-up is steep enough to reach at least 1.65 V when the reset vector is fetched.

7 Conclusion

The main features of the STM32L0xx devices are presented in this application note. They show the benefits offered by this microcontroller family to reduce the MCU's current consumption in embedded systems.

The STM32L0 family extends the ST's ultra-low power family already built with STM8L and STM32L1, offering a larger MCU choice to address the 8/16-bit applications. It complements the STM32 portfolio keeping compatibility with other STM32 devices.

With its Cortex-M0+ core and its energy-efficient architecture system, this microcontroller family supports low power modes without compromising the processing performance.

Its rich set of peripherals can cover a wide range of applications, while numerous low power modes give a full flexibility to adjust on-the-fly the consumption to any task.

This results in an extended operating lifetime for today's and tomorrow's always greener applications.

8 Revision history

Table 4. Document revision history

Date	Revision	Changes
28-Feb-2014	1	Initial release.