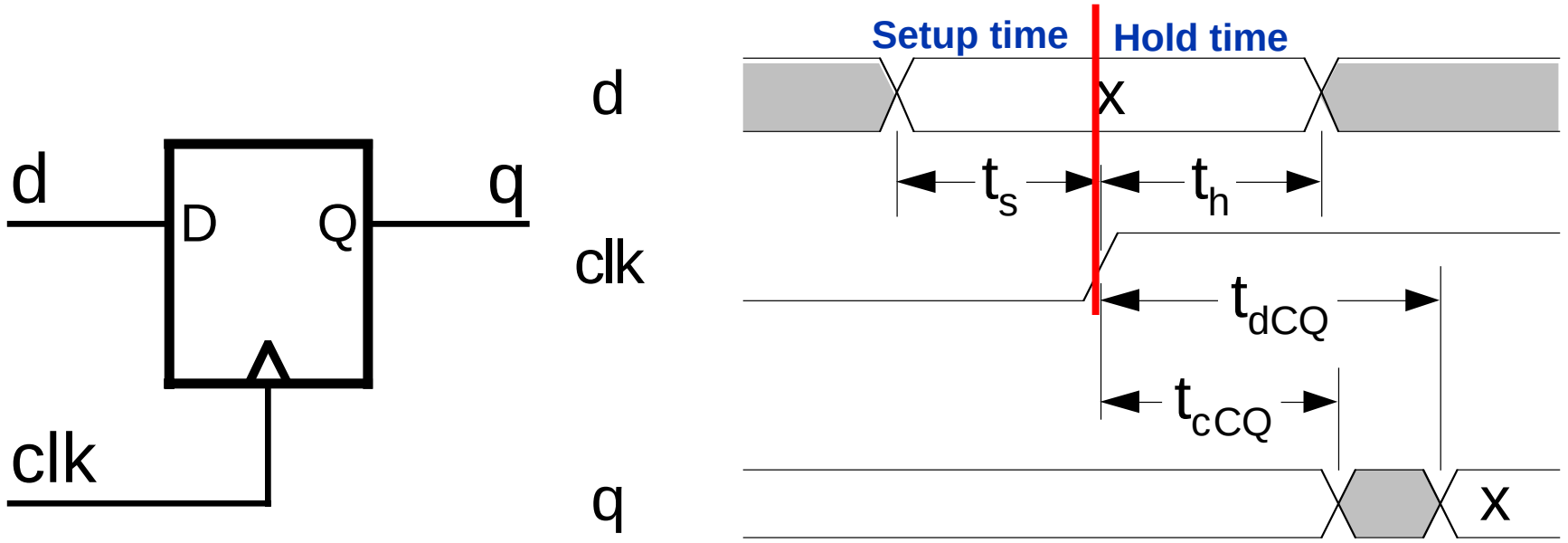
Lecture 3-2 Timing

Outlines

- Timing definition
- How to read a timing report

SOME DEFINTIONS

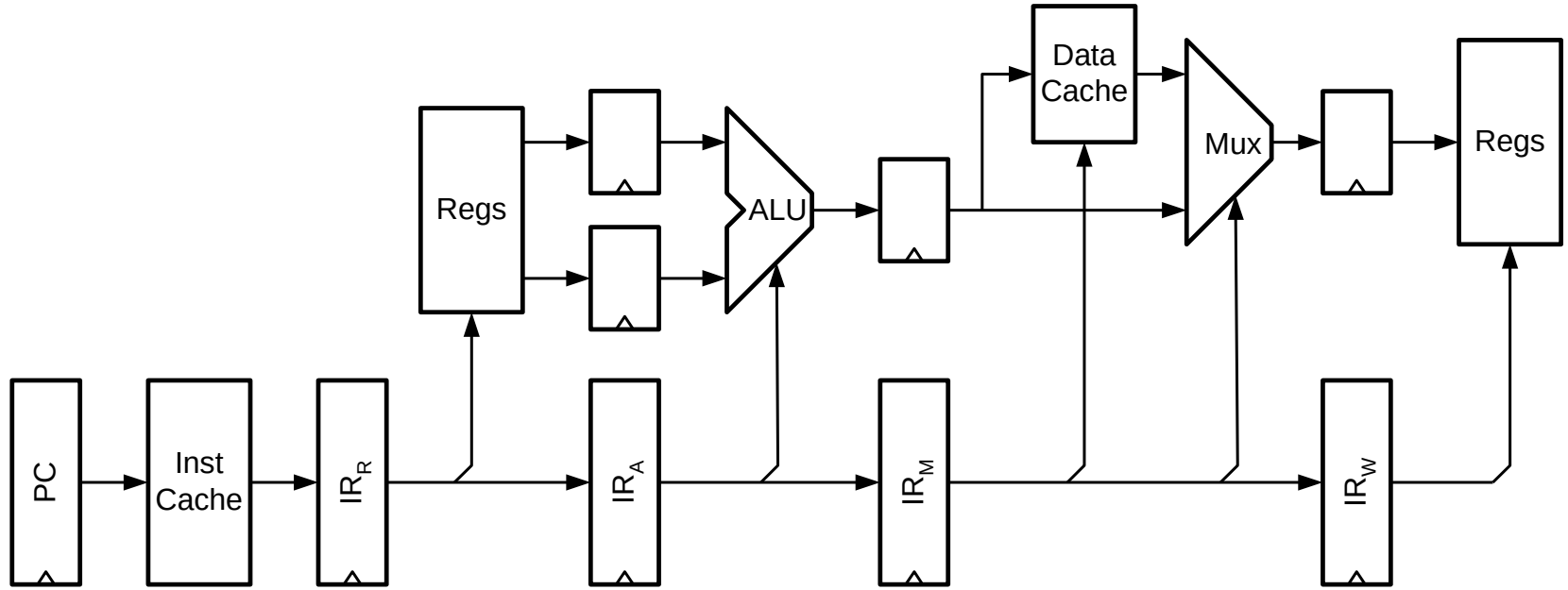
Edge-Triggered D Flip Flop

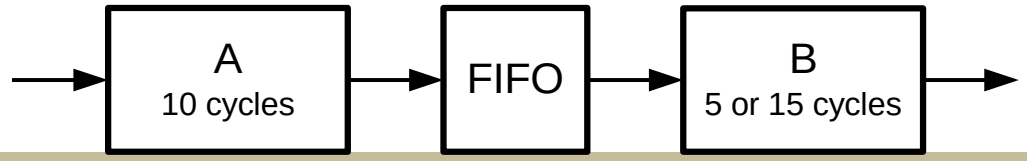


Setup time: inputs become stable before rising clock;
Hold time: inputs remain stable after rising clock;

How Fast My Design Can Run?

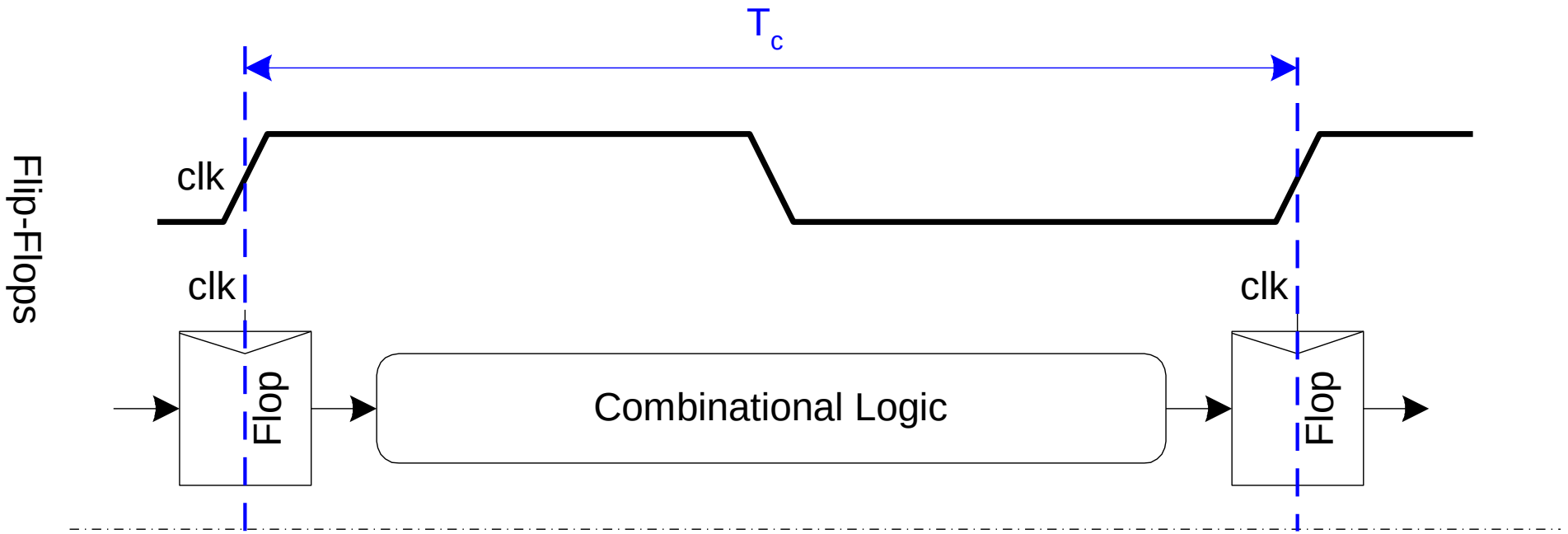
- Up to 100MHz? 200MHz?
- Slower at 10KHz, 20KHz? Any speed?



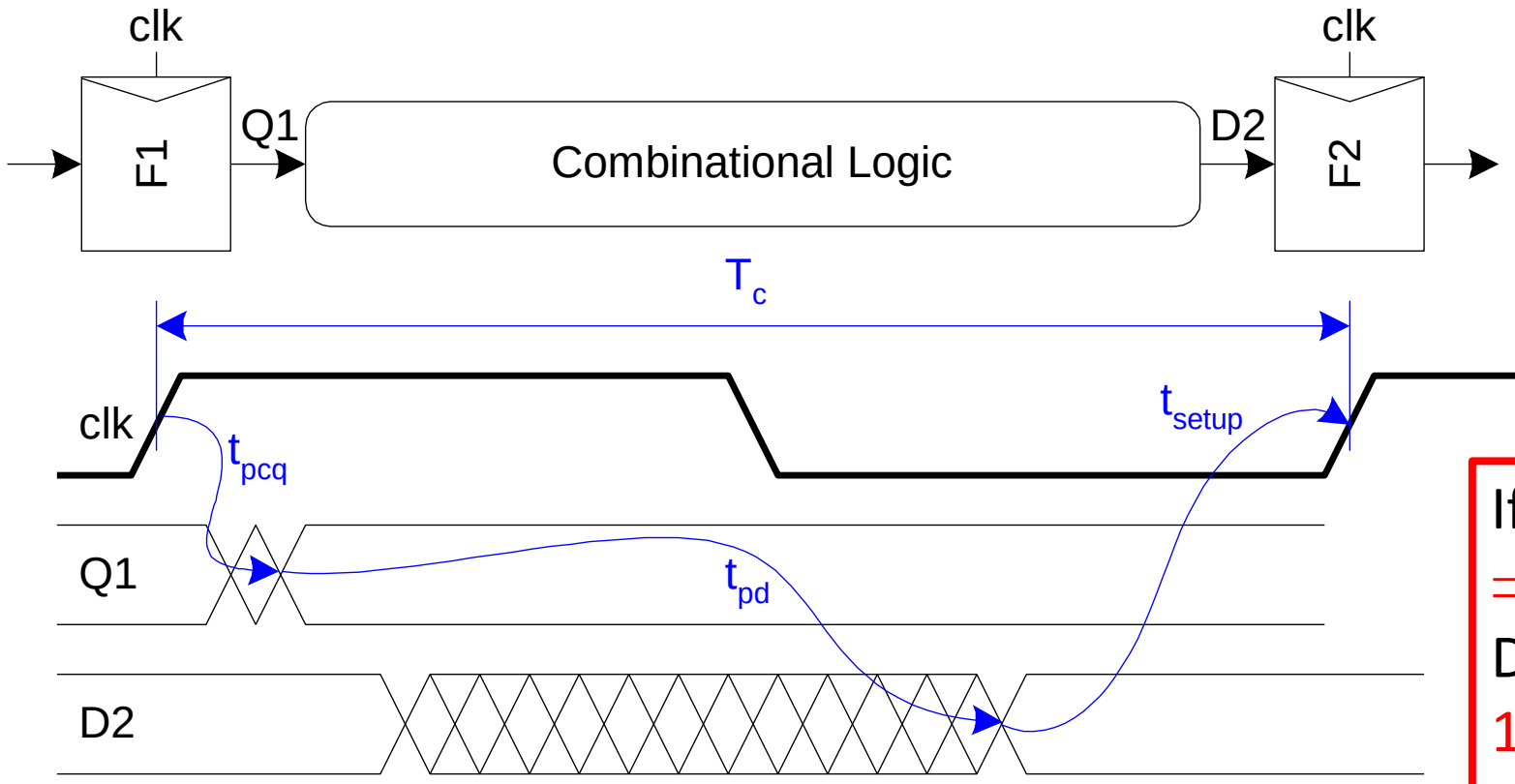


How Fast My Design Can Run?

- Fastest clock cycle time: T_c



Max Delay



$$T_c >= t_{pcq} + t_{pd} + t_{setup}$$

$$t_{pd} <= T_c - (t_{pcq} + t_{setup})$$

Register overhead

If delay of comb. Logic is too long)

⇒ Setup time violation

DFF will catch the wrong value

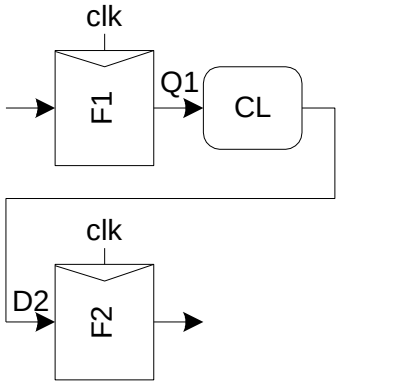
1. clock run slower

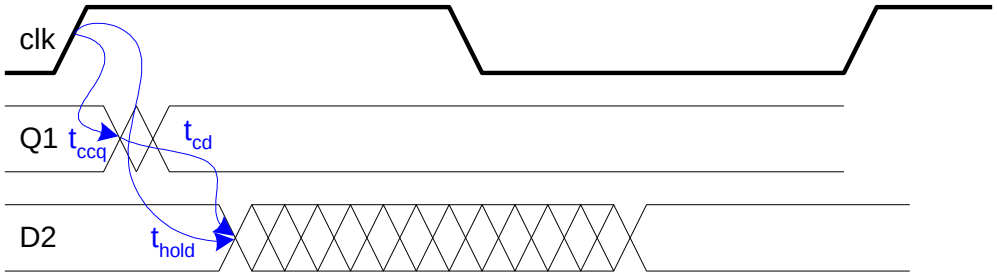
   T_c become larger

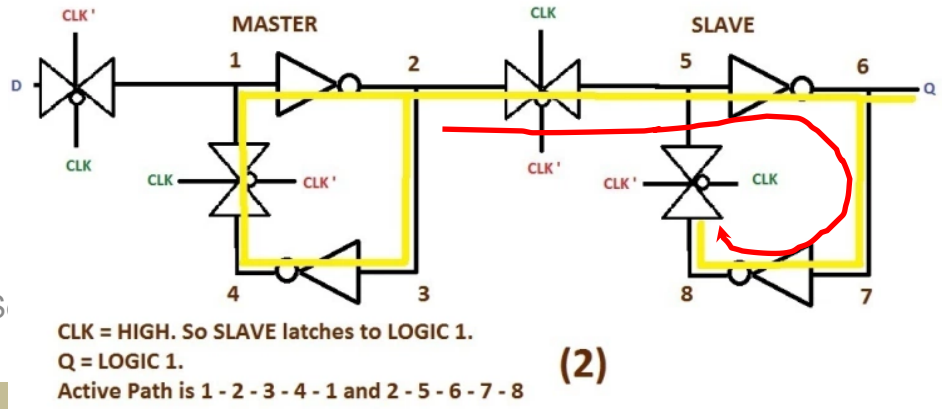
2. comb. Logic faster

   T_{pd} smaller by pipeline or algorithm change

Min-Delay: Flip-Flops







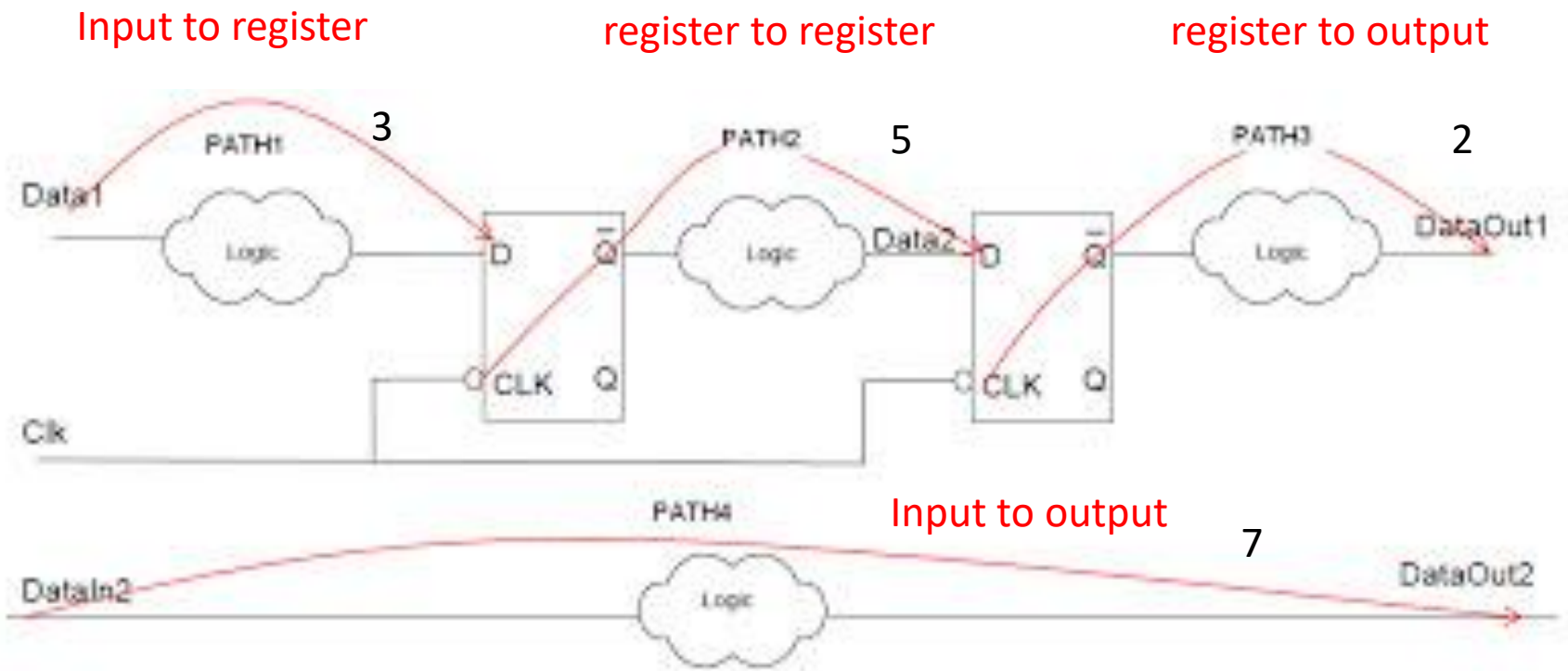
$$t_{cd} + t_{ccq} \geq t_{hold}$$

$$t_{cd} \geq t_{\text{hold}} - t_{ccq}$$

If not hold,
(comb. Logic delay is too short)
⇒ hold time violation
⇒ DFF will catch the wrong value
1. Decreasing clock rate does not work
2. Increase tcd (e.g. add delay, buffer)

Timing Paths

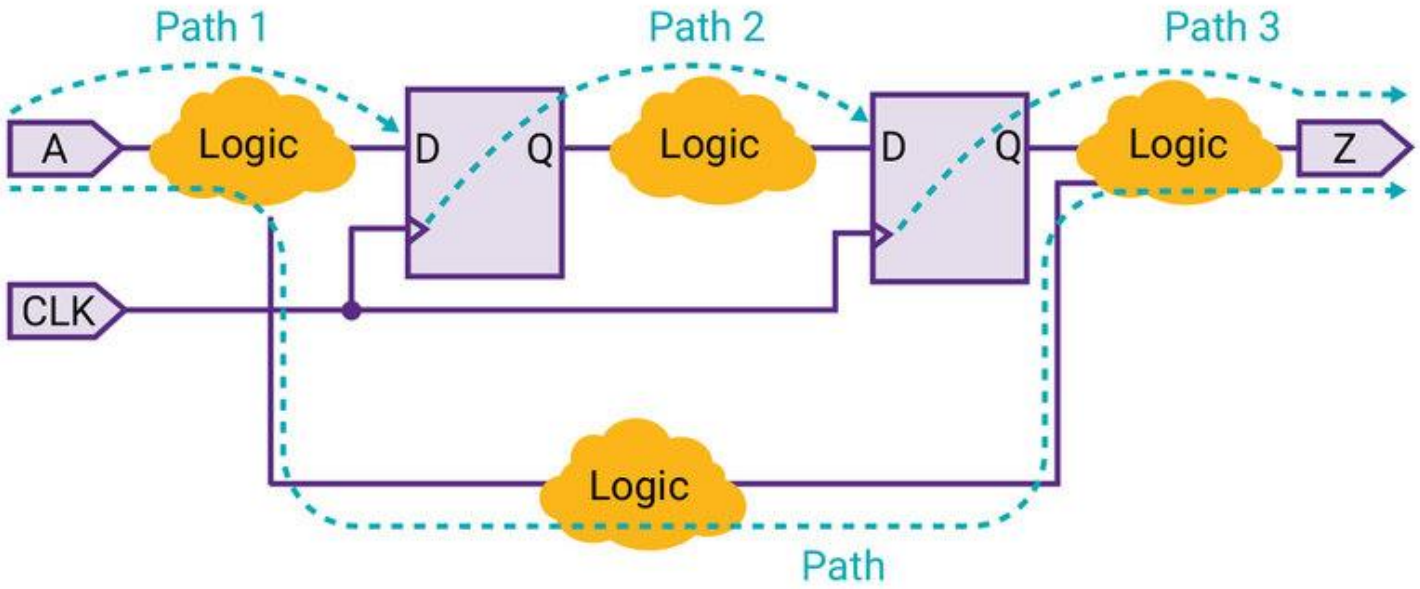
- Input to register, register to register, register to output
  - Start from or end to DFFs
- Input to output



http://www.vlsi-expert.com/2011/03/static-timing-analysis-sta-basic-timing.html

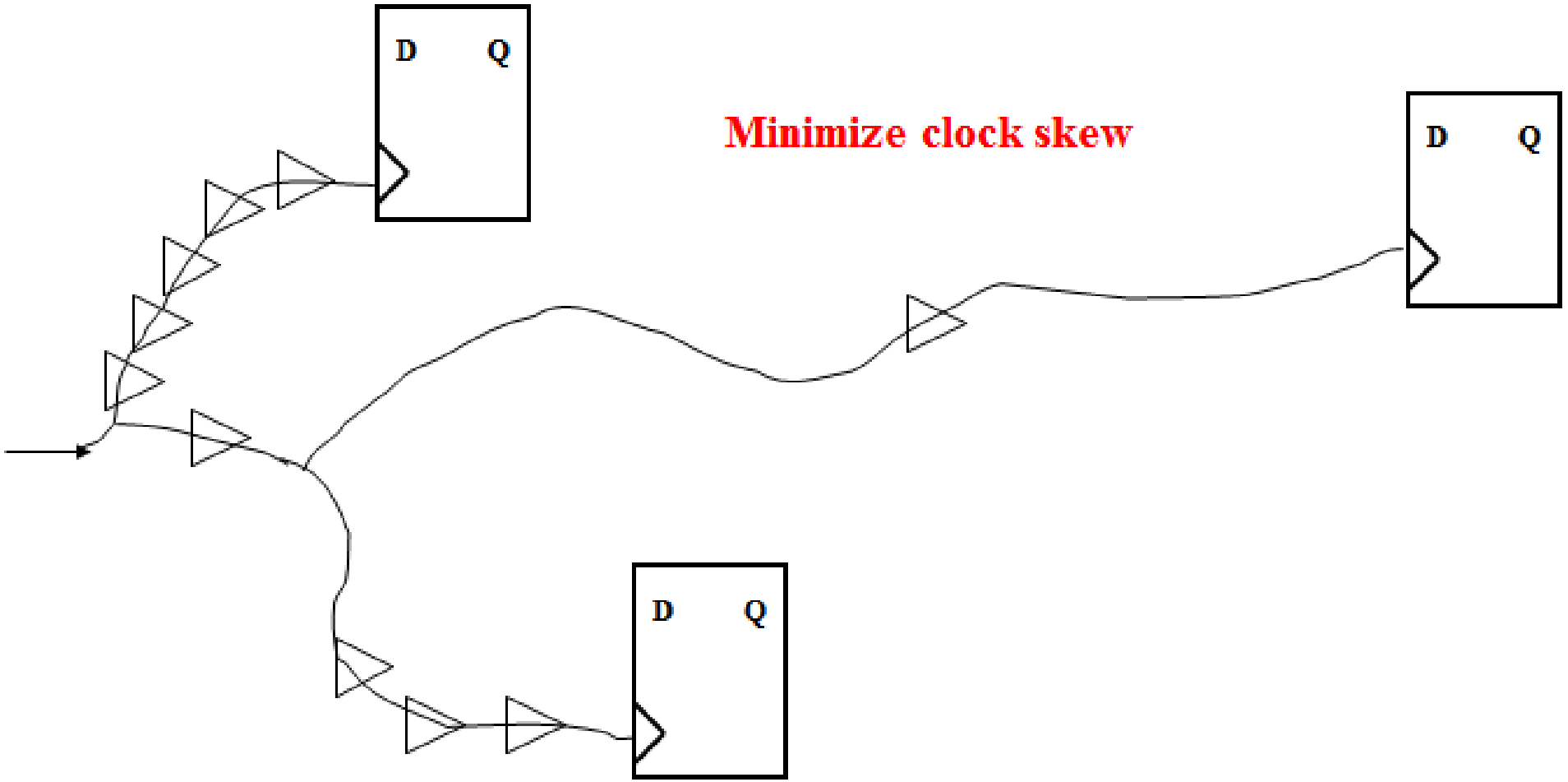
SYNOPSYS®

Timing paths



In the example, each logic cloud represents a combinational logic network. Each path starts at a data launch point, passes through some combinational logic, and ends at a data capture point.

Path	Startpoint	Endpoint
Path 1	Input port	Data input of a sequential element
Path 2	Clock pin of a sequential element	Data input of a sequential element
Path 3	Clock pin of a sequential element	Output port
Path 4	Input port	Output port


Minimize clock skew
D
Q
D
Q
D
Q

Example

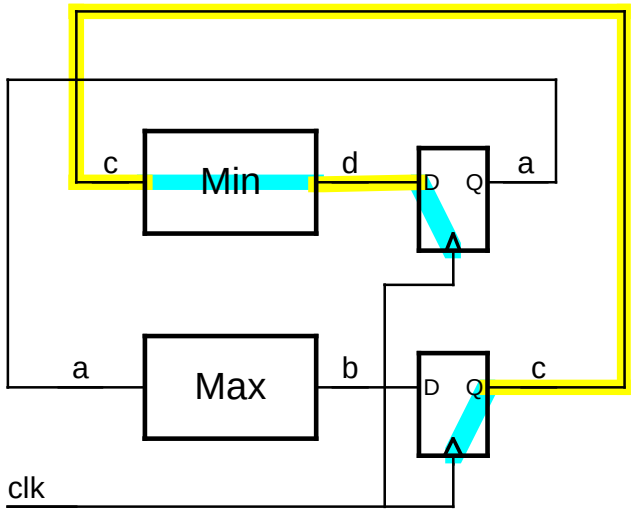
$t_{dCQ} = t_{cCQ} = t_s = 150ps$
$t_h = 250ps$
$t_{dMax} = 850ps$
$t_{cMin} = 100ps$

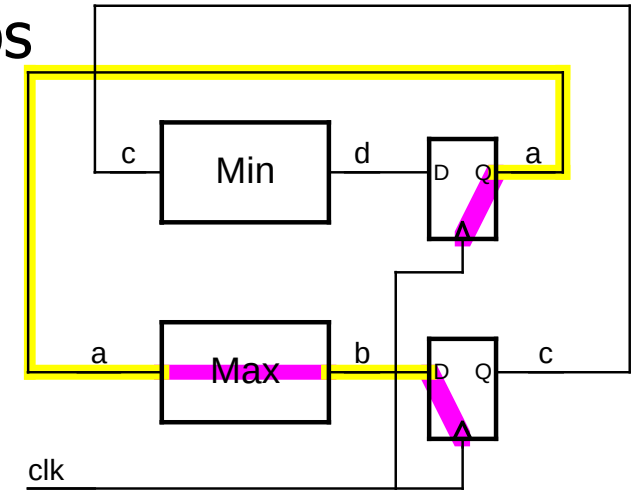
Is hold time constraint met?

$t_h \leq t_{cCQ} + t_{cMin}$ 250ps <= 100+ 150ps

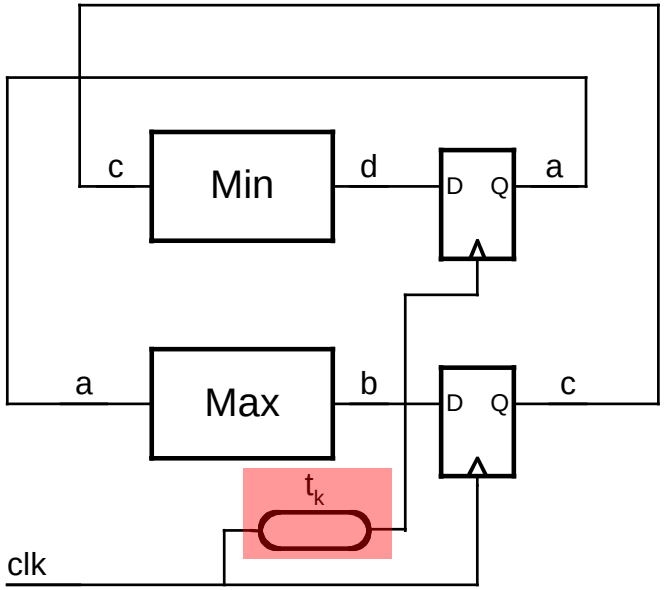
What is the minimum cycle time?

$t_{cy} \geq t_{dCQ} + t_{dMax} + t_s$ t_{cy} >= 1150ps





Add Clock Skew t_k

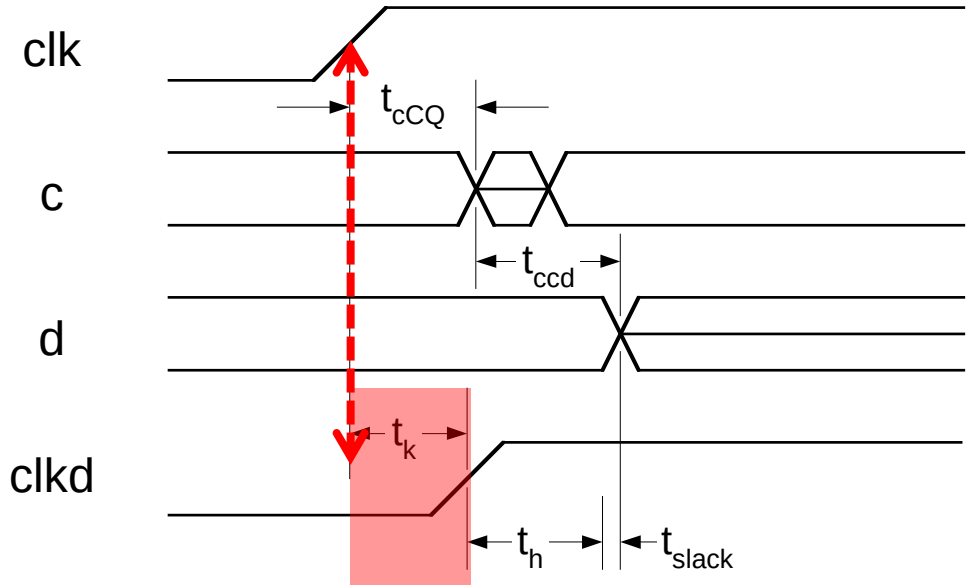


Clock skew: arrival time of clock signal difference

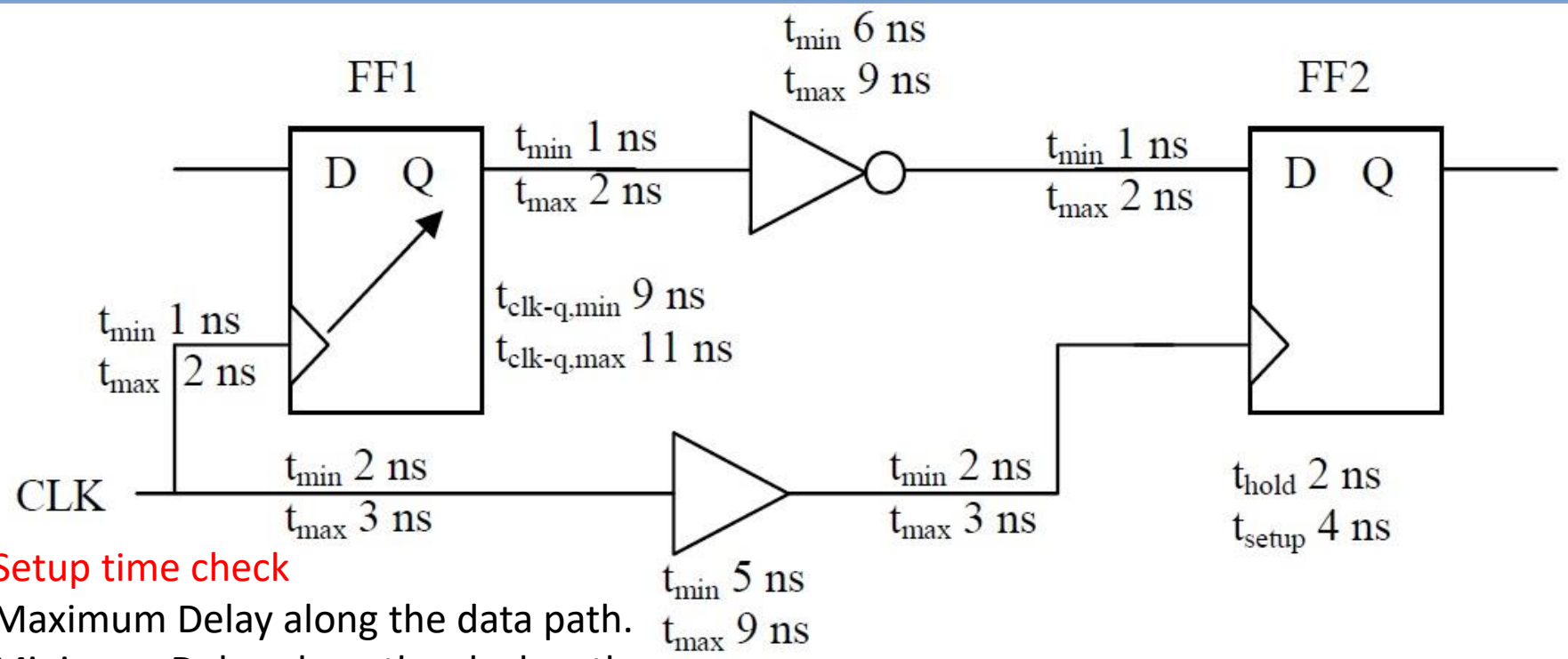
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$ Cycle get larger

$$t_h < t_{cCQ} + t_{cMin} - t_k$$ Hold time tigher

Skew always reduces slack (margin)



check timing path as in timing report



Setup time check

Maximum Delay along the data path.

Minimum Delay along the clock path.

Delay in Data path

= max(wire delay to the clock input of FF1) + max(Clk-to-Q delay of FF1) +max(cell delay of inverter) + max(2 wire delay- "Qof FF1-to-inverter"and "inverter-to-D of FF2")

=Td = 2+11+9+(2+2) = 26ns

Clock path Delay

= (Clock period) + min(wire delay from CLK to Buffer input) + min(cell delay of Buffer) + min(wire delay from Buffer output to FF2/CLK pin) -(Setup time of FF2)

=Tclk = 15+2+5+2-4=20ns

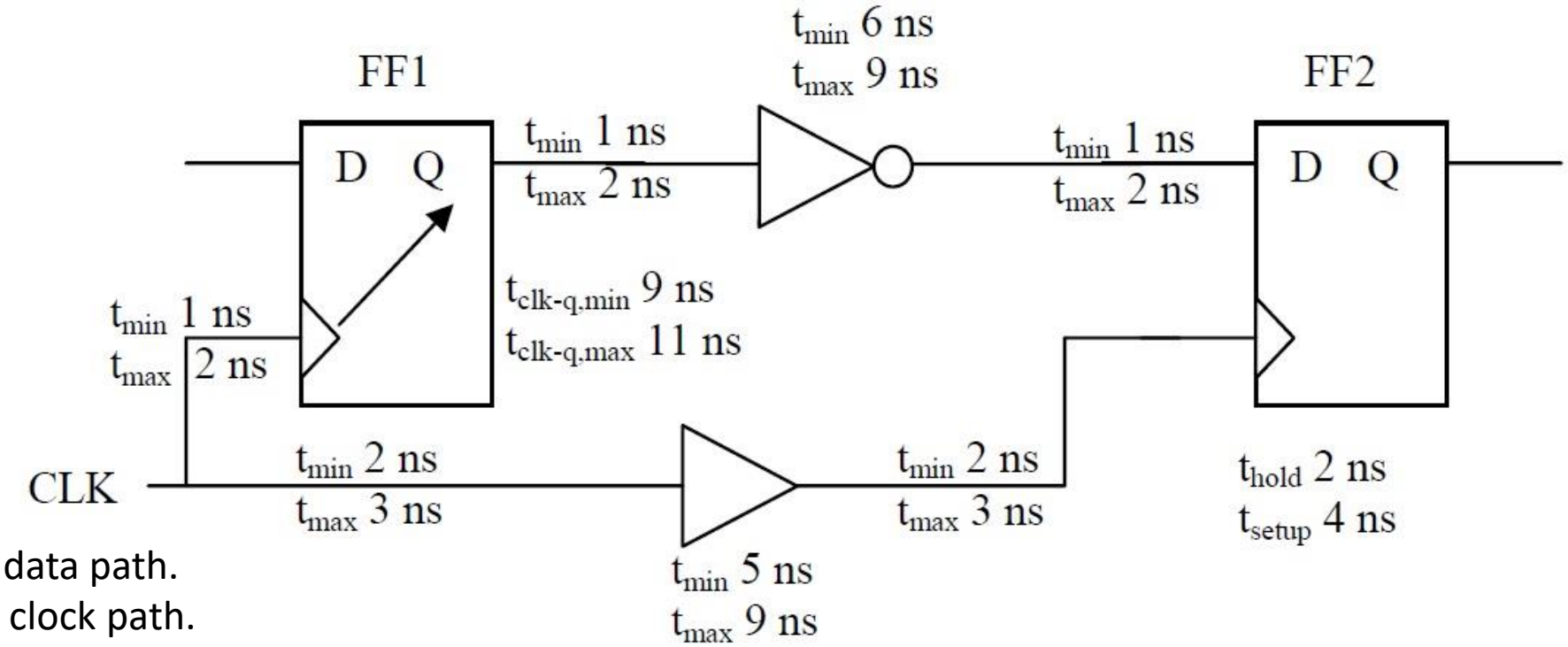
Setup Slack = Tclk - Td = 20ns - 26ns = -6ns.

Since Setup Slack is negative -> Setup violation.

If Clock period is 22ns then

Tclk = 22+2+5+2-4=31-4=27ns AND Td = 26ns

Setup Slack = Tclk - Td = 27-26=1ns (No Violation)



Hold Analysis

Minimum Delay along the data path.

Maximum Delay along the clock path.

Delay in Data path

= min(wire delay to the clock input of FF1) + min(Clk-to-Q delay of FF1) +min(cell delay of inverter) + min(2 wire delay- "Qof FF1-to-inverter" and"inverter-to-D of FF2")

=Td = 1+9+6+(1+1)=18ns

Clock path Delay

= max(wire delay from CLK to Buffer input) + max(cell delay of Buffer) + max(wire delay from Buffer output to FF2/CLK pin) + (hold time of FF2)

=Tclk = 3+9+3+2 = 17 ns

Hold Slack = Td - Tclk = 18ns -17ns = 1ns

Since Hold Slack is positive-> No hold Violation.

Note:

If the hold time had been 4 ns instead of 2 ns, then there would have been a hold violation.

Td=18ns and Tclk = 3+9+3+4=19ns

So Hold Slack=Td - Tclk = 18ns - 19ns = -1ns (Violation)

Summary

- Delays in digital systems
  - Propagation delay
  - Contamination delay
- Flip-flop timing constraints
  - Setup time (t_s)
  - Hold time (t_h)
- Cycle time determined by maximum delay

$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$

- Correct operation depends on minimum delay

$$t_h < t_{cCQ} + t_{cMin}$$

- Clock skew affects both

$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$

$$t_h < t_{cCQ} + t_{cMin} - t_k$$

HOW TO READ YOUR TIMING REPORT

How to Read and Interpret Timing Report

`report_timing`

Header

```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max
```

Data arrival

```
Point                                          Incr       Path
-----------------------------------------------------------------
clock Clk (rise edge)                          0.00       0.00
clock network delay (propagated)               1.10 *     1.10
FF1/CLK (fdef1a15)                             0.00       1.10 r
FF1/Q (fdef1a15)                               0.50 *     1.60 r
U2/Y  (buf1a27)                                0.11 *     1.71 r
U3/Y  (buf1a27)                                0.11 *     1.82 r
FF2/D (fdef1a15)                               0.05 *     1.87 r
data arrival time                                         1.87
```

Data required

```
clock Clk (rise edge)                          4.00       4.00
clock network delay (propagated)               1.00 *     5.00
FF2/CLK (fdef1a15)                                        5.00 r
library setup time                            -0.21 *     4.79
data required time                                        4.79
-----------------------------------------------------------------
```

Slack

```
data required time                                        4.79
data arrival time                                        -1.87
-----------------------------------------------------------------
slack (MET)                                               2.92
```

Constraint File (note. These numbers may not match the following slides)

```
//設定clock, I/O 限制
create_clock "clk" -name clk -period 2 -waveform {0 1.7}
set_clock_uncertainty 0.2 clk
set_fix_hold all_clocks()
set_input_delay 0.5 -clock clk {in}
set_output_delay -max 0.8 -clock clk {isprime}
//設定 loading
set_load -pin_load 5 {isprime}
```

//Note: these commands are for practical applications to include
// clock jitter, input/output loading capacitances

Global

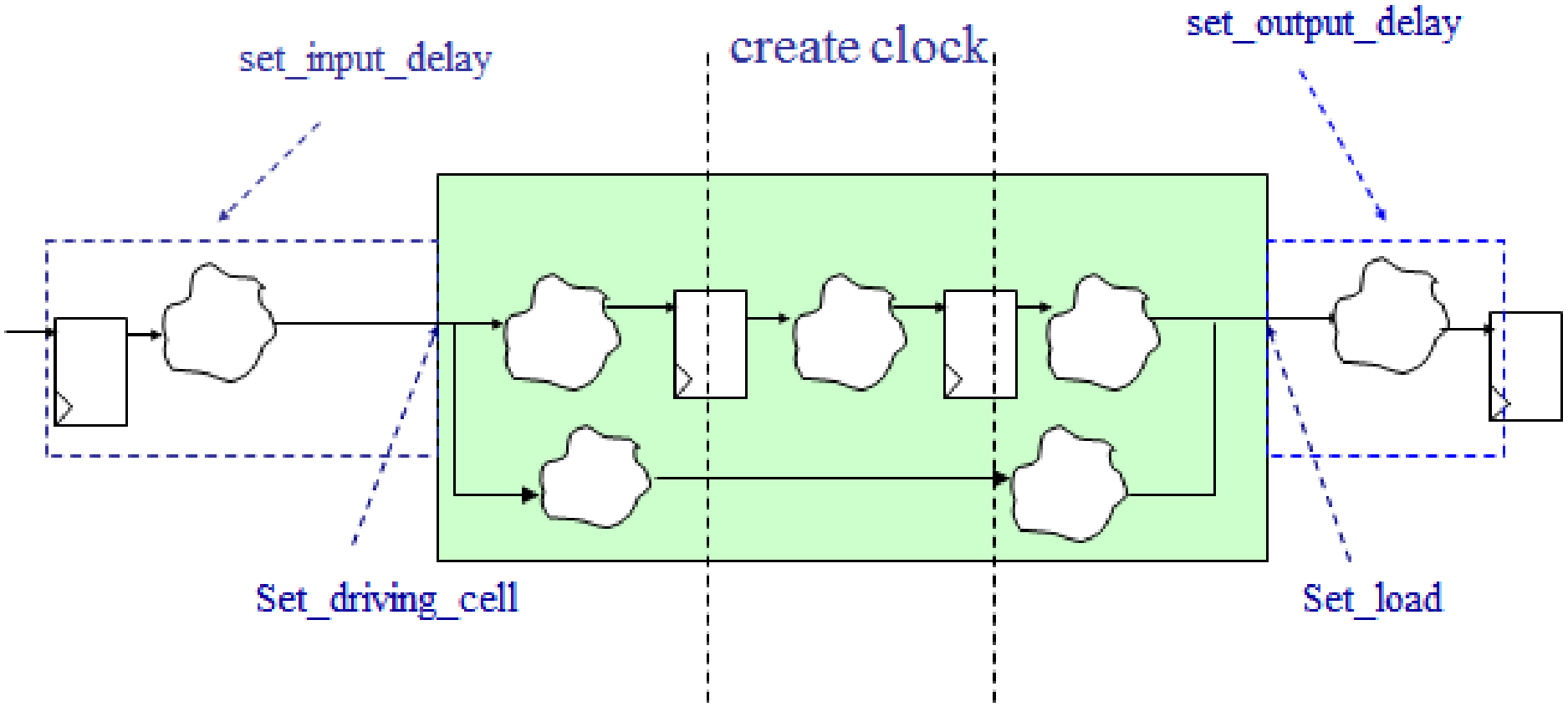
- Target_library
- Set_operating_conditions
- Set_wire_load
- Set_max_transition

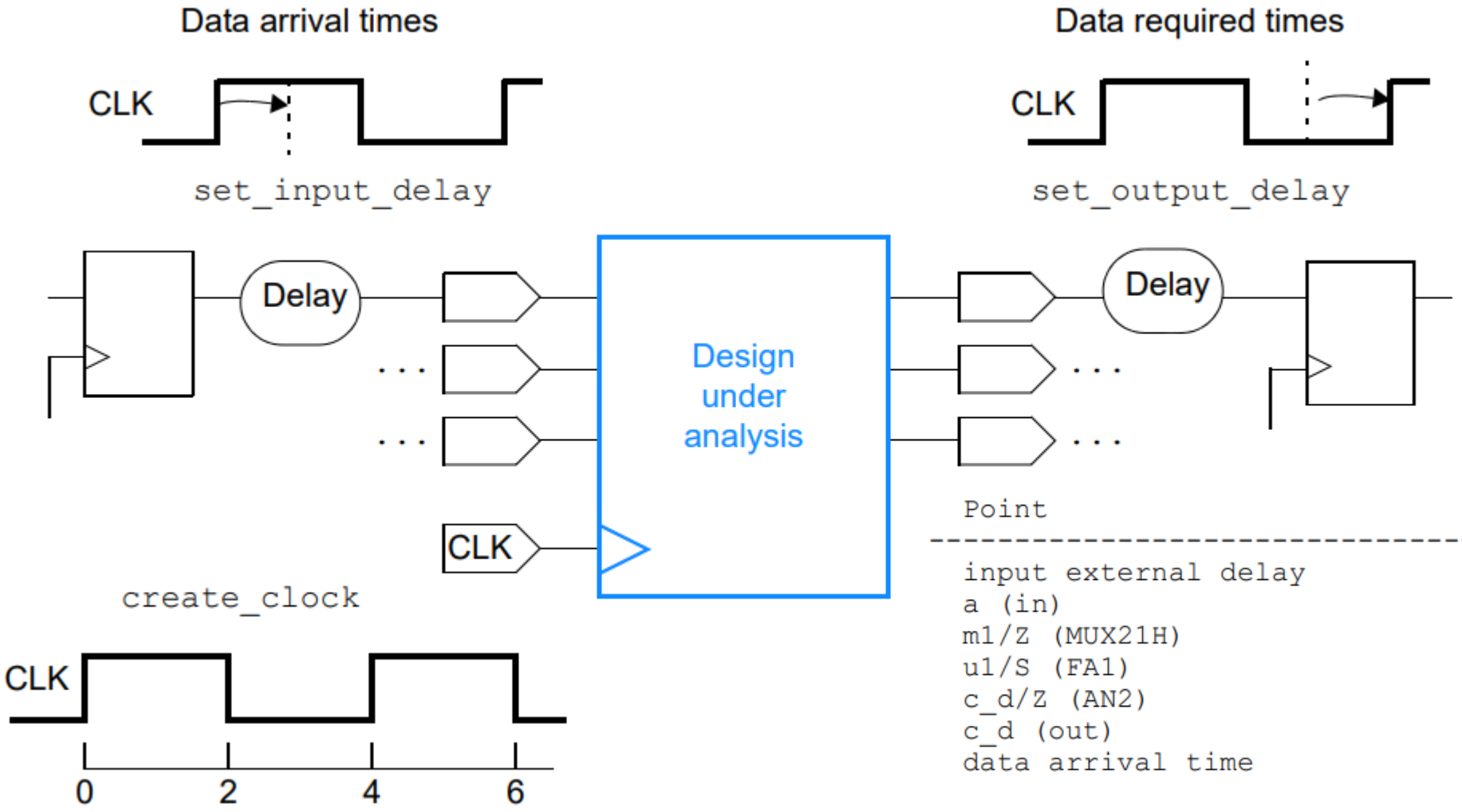
Clock

- Create_clock
- Set_dont_touch_network
- Set_ideal_net (for sdf)
- Set_clock_uncertainty

Timing Exception

- Set_false_path
- Set_multicycle_path



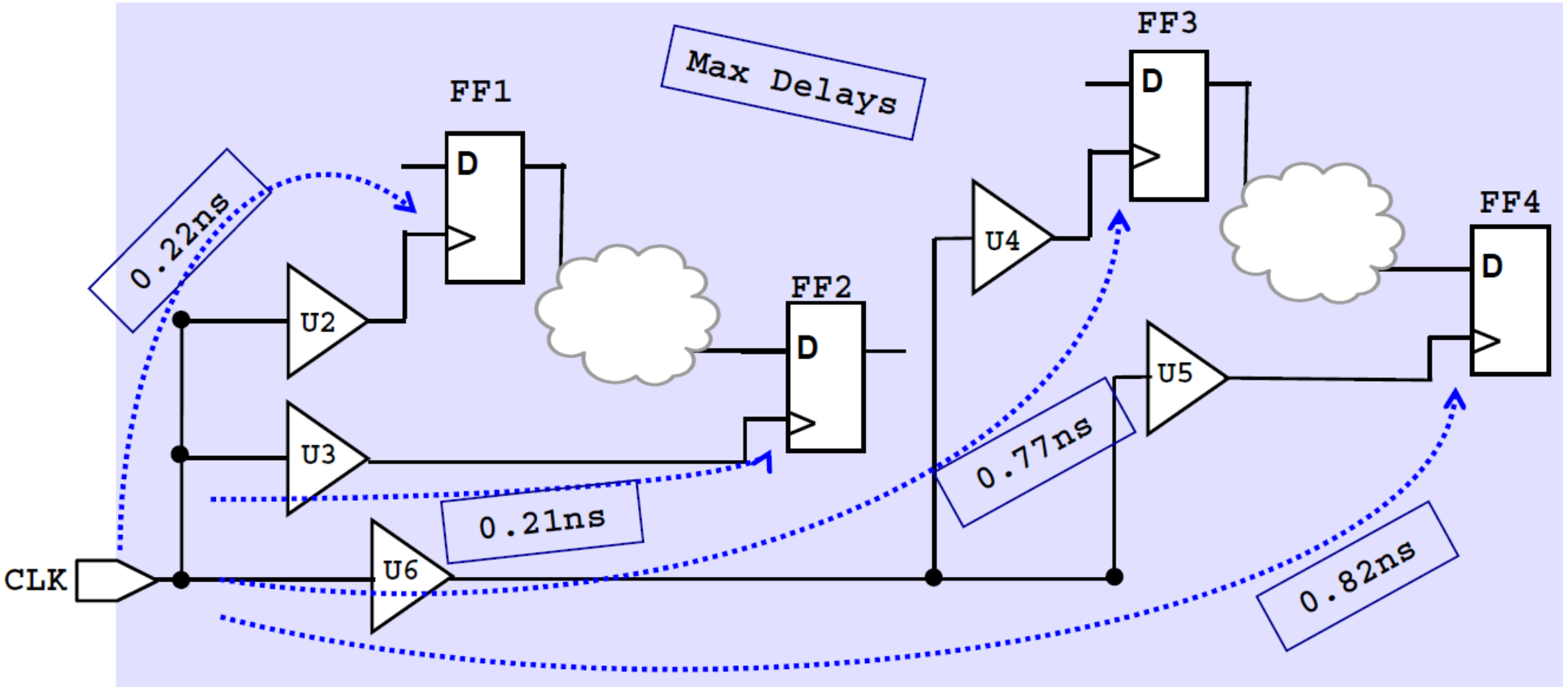


Point	Incr	Path
input external delay	10.00	10.00 r
a (in)	0.00	10.00 r
m1/Z (MUX21H)	1.00	11.00 r
u1/S (FA1)	1.00	12.00 r
c_d/Z (AN2)	1.00	13.00 r
c_d (out)	0.00	13.00 r
data arrival time		13.00
max_delay	15.00	15.00
output external delay	-10.00	5.00
data required time		5.00
data required time		5.00
data arrival time		-13.00
slack (VIOLATED)	-8.00	

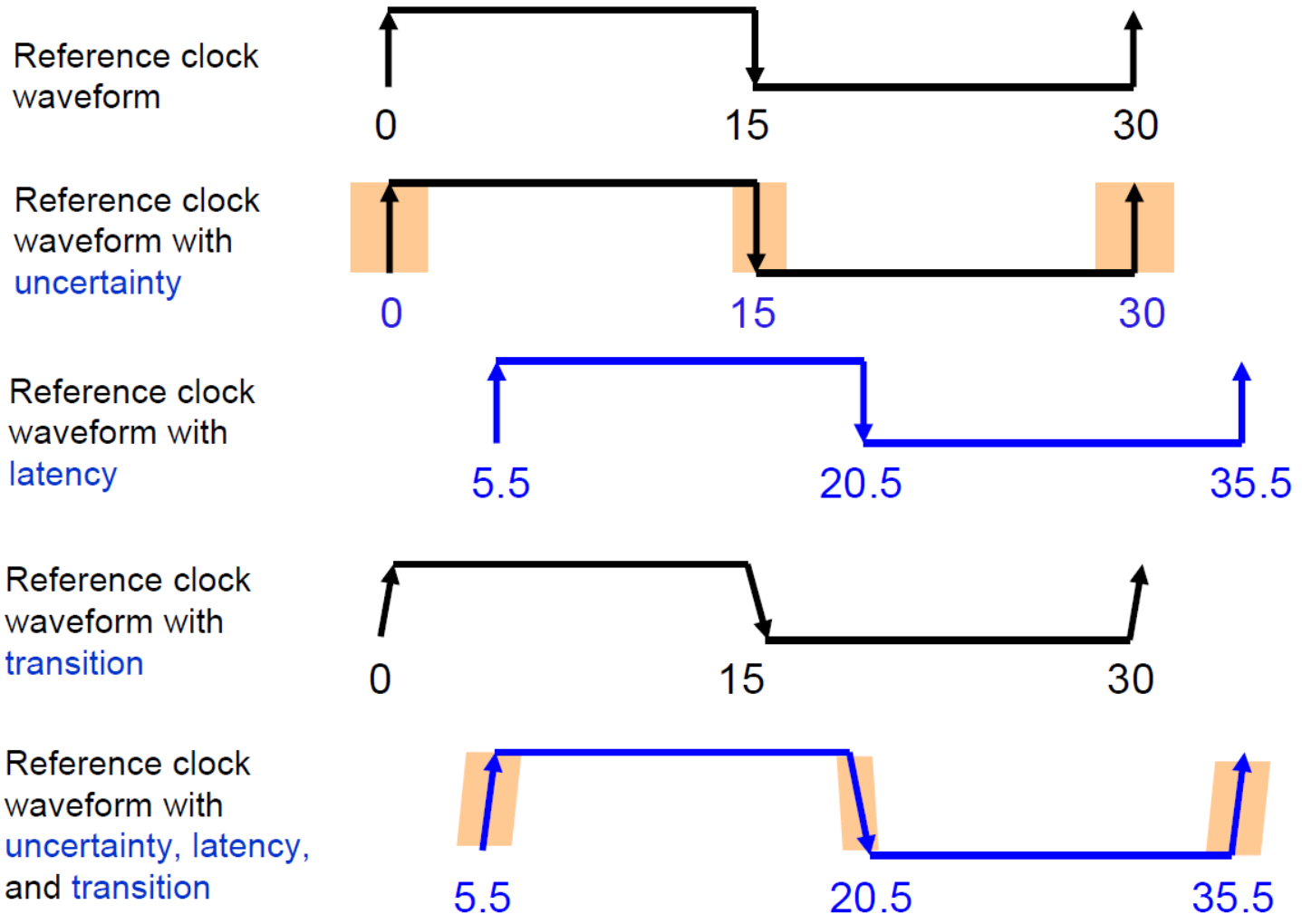
Clock Network and Clock Skew

```
report_clock_timing -type skew
```

For each clock, report *REAL* skew

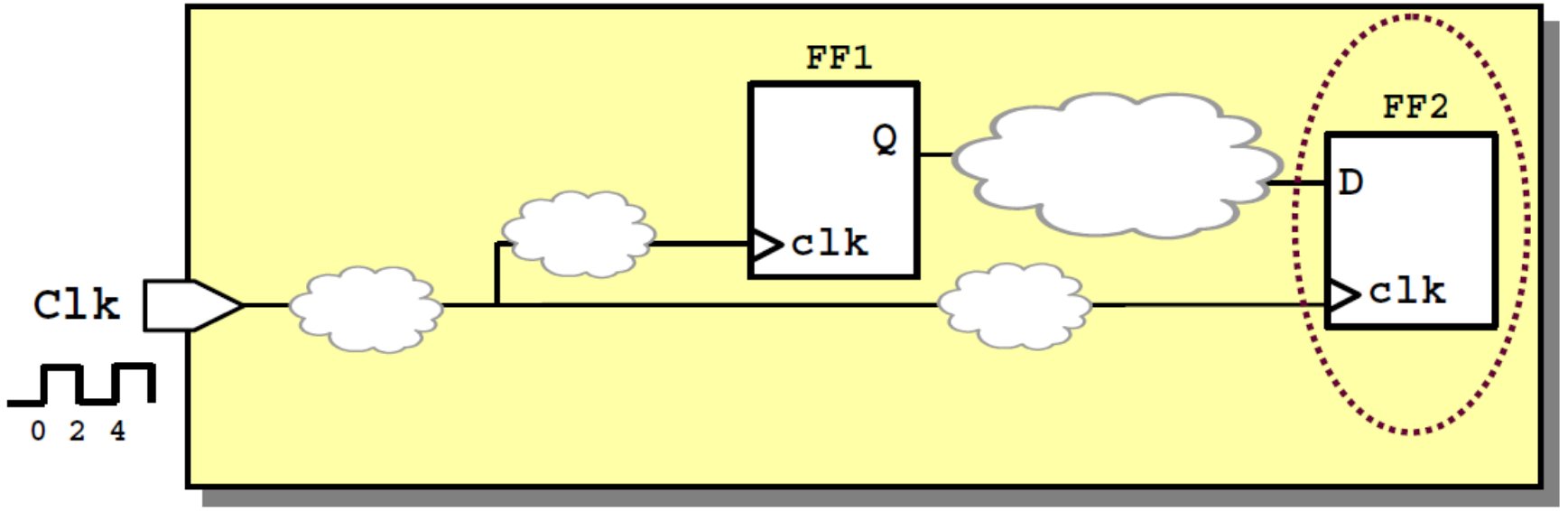


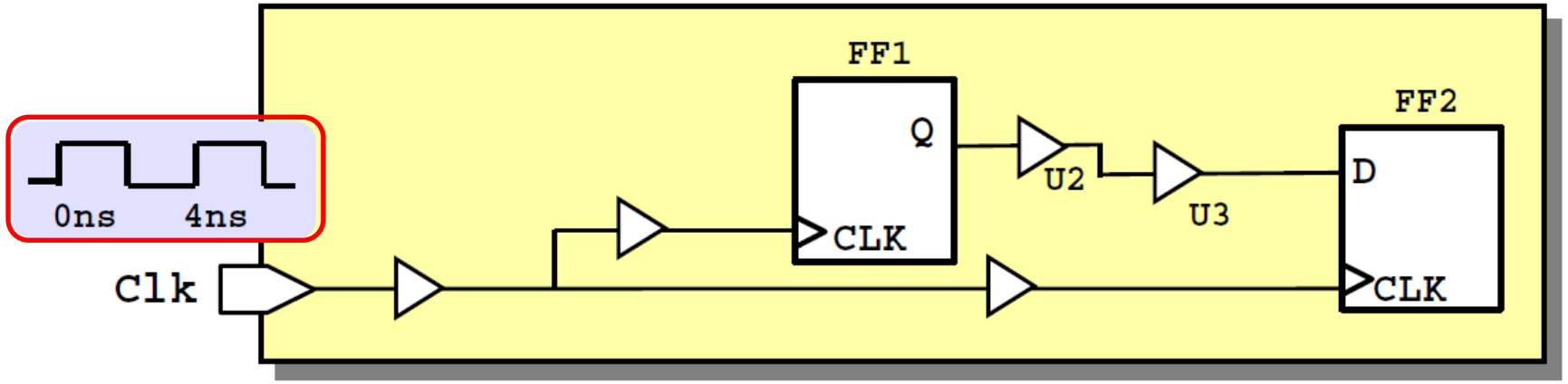
Specify Timing Assertions

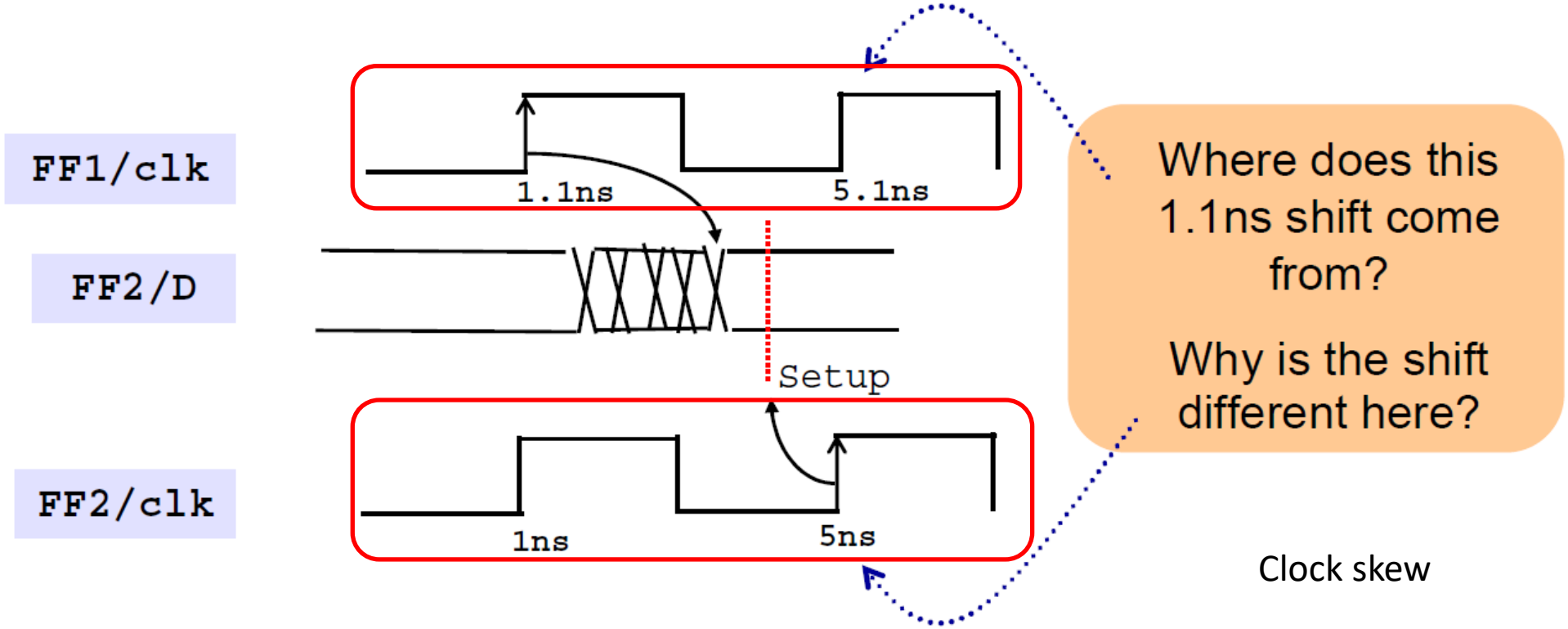


Timing Verification of Synchronous Designs

All “registers” must reliably capture data at the desired clock edges.

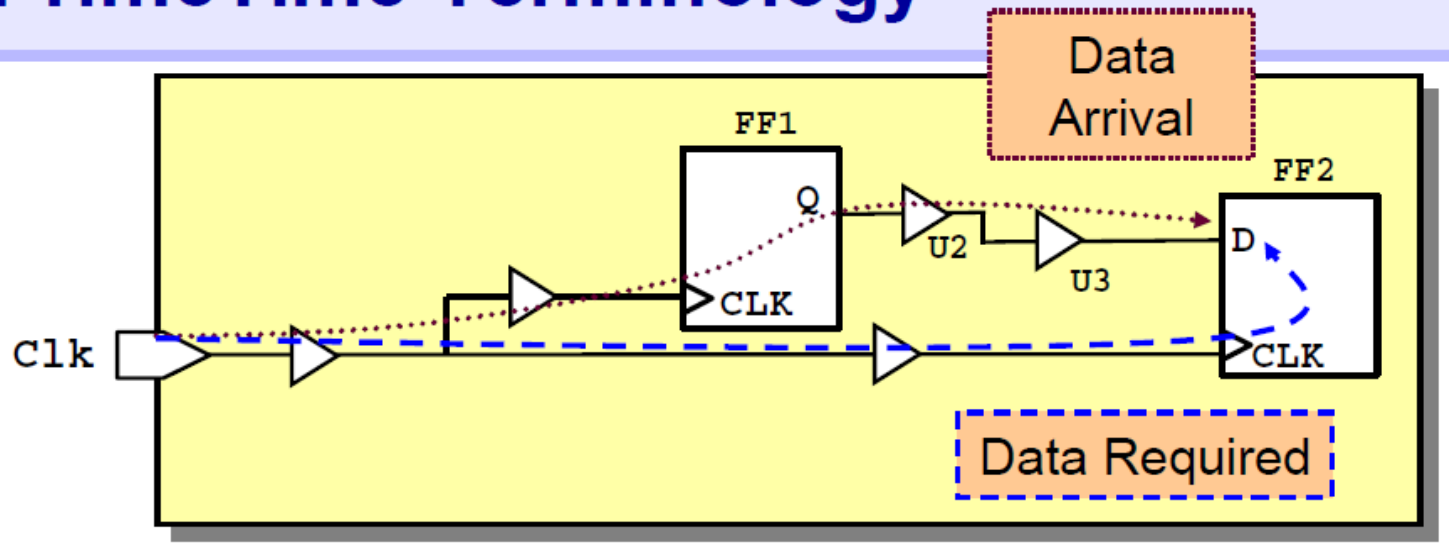


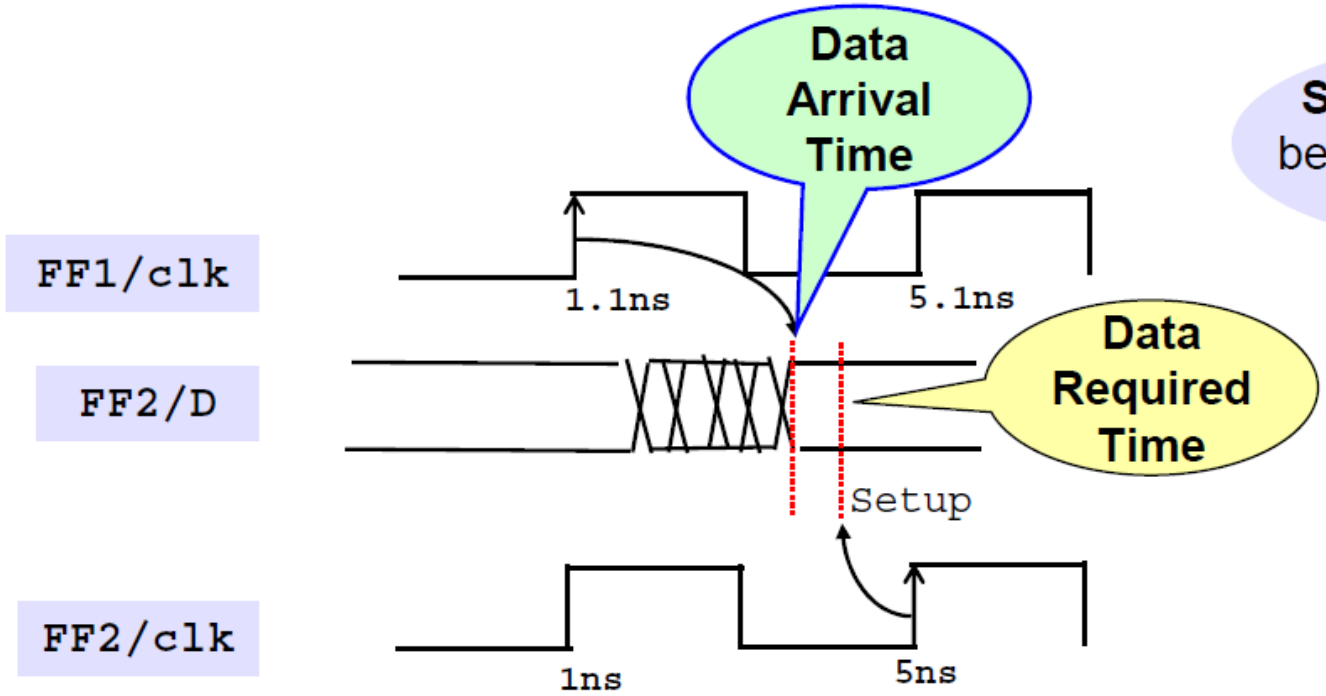

FF1
Q
CLK
FF2
D
CLK
U2
U3
0ns
4ns
Clk


FF1/clk
FF2/D
FF2/clk
1.1ns
5.1ns
Setup
1ns
5ns
Where does this 1.1ns shift come from?
Why is the shift different here?

Clock skew

PrimeTime Terminology





Slack is the difference between data arrival and data required.

Four Sections in a Timing Report

`report_timing`

Header

```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max
```

Data arrival

```
Point                                          Incr       Path
-----------------------------------------------------------------
clock Clk (rise edge)                          0.00       0.00
clock network delay (propagated)               1.10 *     1.10
FF1/CLK (fdef1a15)                             0.00       1.10 r
FF1/Q (fdef1a15)                               0.50 *     1.60 r
U2/Y  (buf1a27)                                0.11 *     1.71 r
U3/Y  (buf1a27)                                0.11 *     1.82 r
FF2/D (fdef1a15)                               0.05 *     1.87 r
data arrival time                                         1.87
```

Data required

```
clock Clk (rise edge)                          4.00       4.00
clock network delay (propagated)               1.00 *     5.00
FF2/CLK (fdef1a15)                                        5.00 r
library setup time                            -0.21 *     4.79
data required time                                        4.79
-----------------------------------------------------------------
```

Slack

```
data required time                                        4.79
data arrival time                                        -1.87
-----------------------------------------------------------------
slack (MET)                                               2.92
```

Data Arrival Section

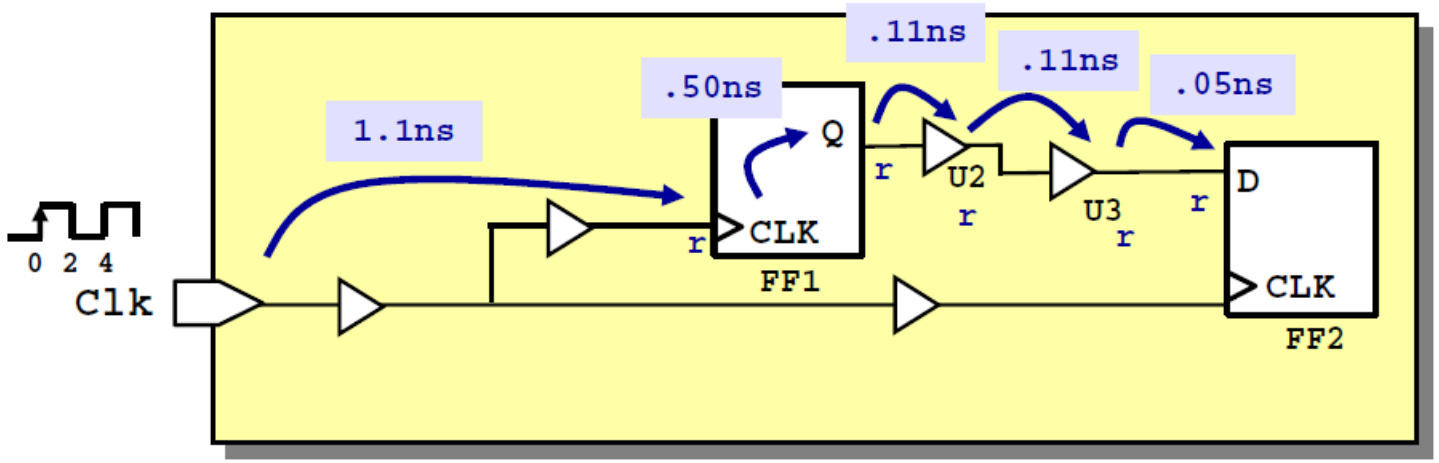
Calculated latency

SDF

Point	Incr	Path
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87

Data arrival

Library reference names

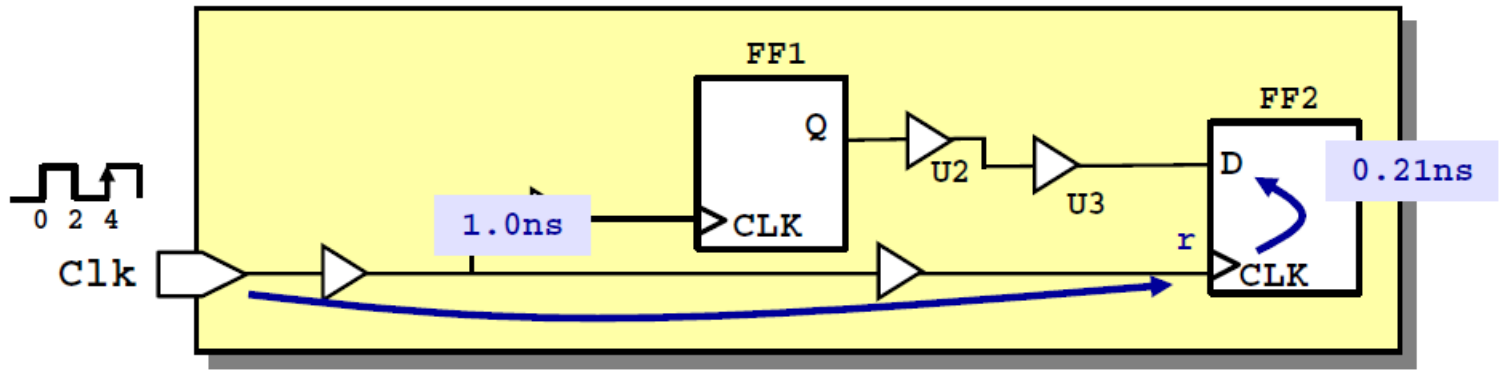


Data Required Section

Point	Incr	Path
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87
clock Clk (rise edge)	4.00	4.00
clock network delay (propagated)	1.00 *	5.00
FF2/CLK (fdef1a15)		5.00 r
library setup time	-0.21 *	4.79
data required time		4.79

Data required

SDF



Summary - Slack

`report_timing`

```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock Clk (rise edge)                    0.00       0.00
clock network delay (propagated)         1.10 *     1.10
FF1/CLK (fdef1a15)                       0.00       1.10 r
FF1/Q (fdef1a15)                         0.50 *     1.60 r
U2/Y  (buf1a27)                          0.11 *     1.71 r
U3/Y  (buf1a27)                          0.11 *     1.82 r
FF2/D (fdef1a15)                         0.05 *     1.87 r
data arrival time                                   1.87

clock Clk (rise edge)                    4.00       4.00
clock network delay (propagated)         1.00 *     5.00
FF2/CLK (fdef1a15)                                  5.00 r
library setup time                      -0.21 *     4.79
data required time                                  4.79
-----------------------------------------------------------
data required time                                  4.79
data arrival time                                  -1.87
-----------------------------------------------------------
slack (MET)                                         2.92
```

Slack