PMIC Project1_report

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1.Pre-layout simulation specifications

Parameters	SPEC.	Design	Unit
Input Voltage (V_{IN})	1.8	1.8	V
Output Voltage (V_{OUT})	1.2 (1.19~1.21)	1.202, 1.206, 1.206	V
Load Current (I_{LOAD})	10, 90, 180	10, 90, 180	mA
Inverter Chain	>5	9	stage
Output Capacitance	10	10	uF
Output Ripple	< 20 (10mA, 90mA, 180mA)	8.385 12.57, 12.19	mV
Power Conversion Efficiency (post-layout)	>92 (10mA, 90mA, 180mA)	94.96, 96.31, 93.52	%

2.post-layout simulation specifications

Parameters	SPEC.	Design	Unit
Input Voltage (V_{IN})	1.8	1.8	V
Output Voltage (V_{OUT})	1.2 (1.19~1.21)	1.201, 1.2, 1.195	V
Load Current (I_{LOAD})	10, 90, 180	10, 90, 180	mA
Inverter Chain	>5	9	stage
Output Capacitance	10	10	uF
Output Ripple	< 20 (10mA, 90mA, 180mA)	7.241, 6.518, 9.027	mV
Power Conversion Efficiency (post-layout)	>92 (10mA, 90mA, 180mA)	94.03, 95.13, 92.6	%

3.TABLE1

Estimated percentage of total losses from pre-layout simulation data (V_{IN}=1.8V, V_{out}=1.2V)

Source of Losses	I_{load} = 10mA (CCM)	I_{load} = 90 mA (CCM)	I_{load} = 180mA (CCM)
Inductor series resistance	26μ (4.08%)	2.106 m (50.58%)	8.424 m (55.97%)
nFET gate driver	145.3μ (22.78%)	134.7μ (3.23%)	124.1 (0.82%)
nFET channel resistance	68.04μ (10.67%)	270.5μ (6.5%)	961.2μ (6.39%)
pFET gate driver	268.6 μ (42.11%)	275.2 (6.61%)	275.5 (1.83%)
pFET channel resistance	127.8μ (20.03%)	1.386 m (33.29%)	5.286m (35.12%)
L_X node capacitance	77.06μ (12.08%)	79.86 μ (1.92%)	82.33μ (0.55%)
Others?	-74.9μ (-11.74%)	-88.16μ (-2.12%)	-103.13μ (-0.69%)
total loss	632.9μ (100%)	4.164 m (100%)	15.05 m (100%)

*Efficiency should be optimized at each condition.

*Conduction loss (%) should increase as output load increases.