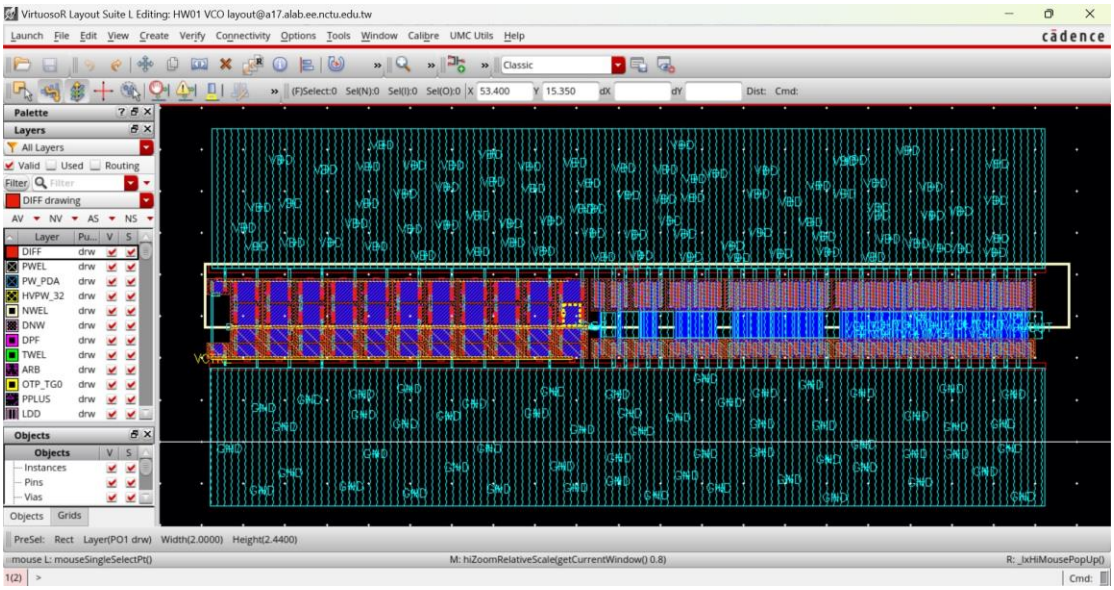
PMIC HW1_report

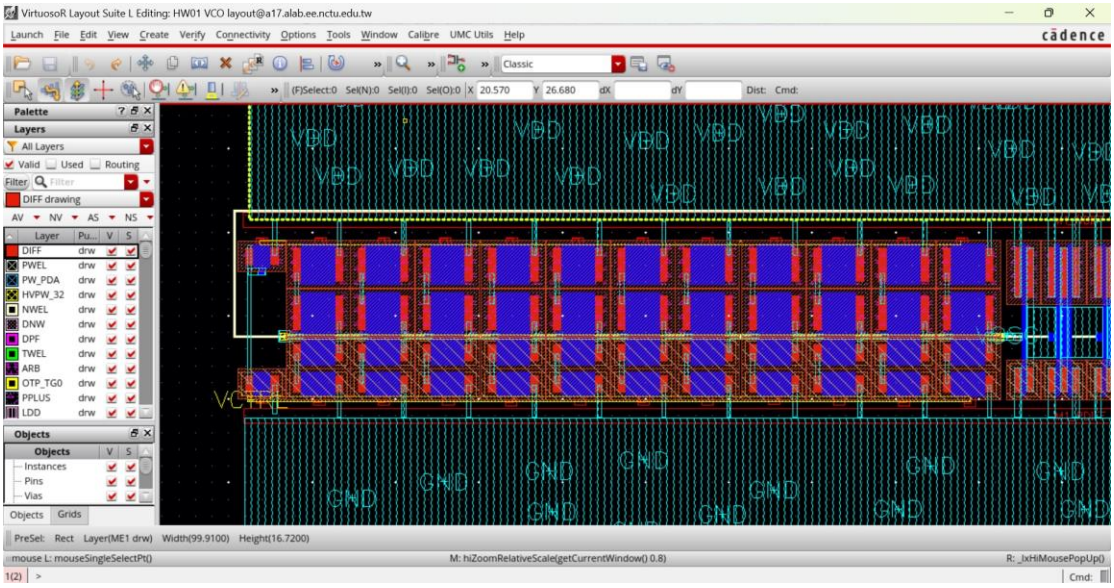
110511277 蔡東宏

1. Layout

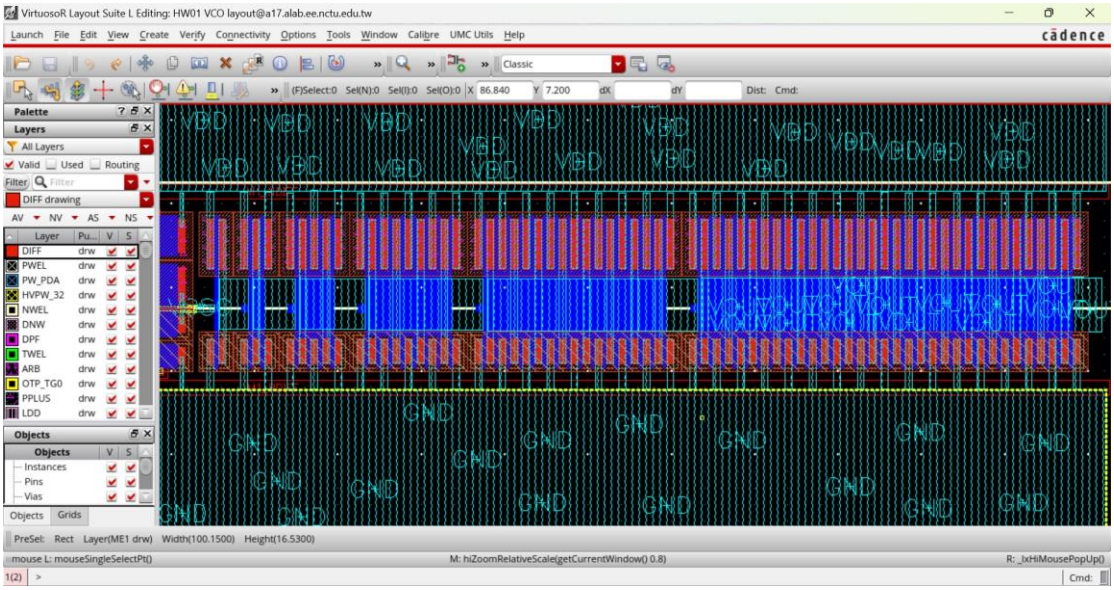
11 級 oscillator+6 級 buffer



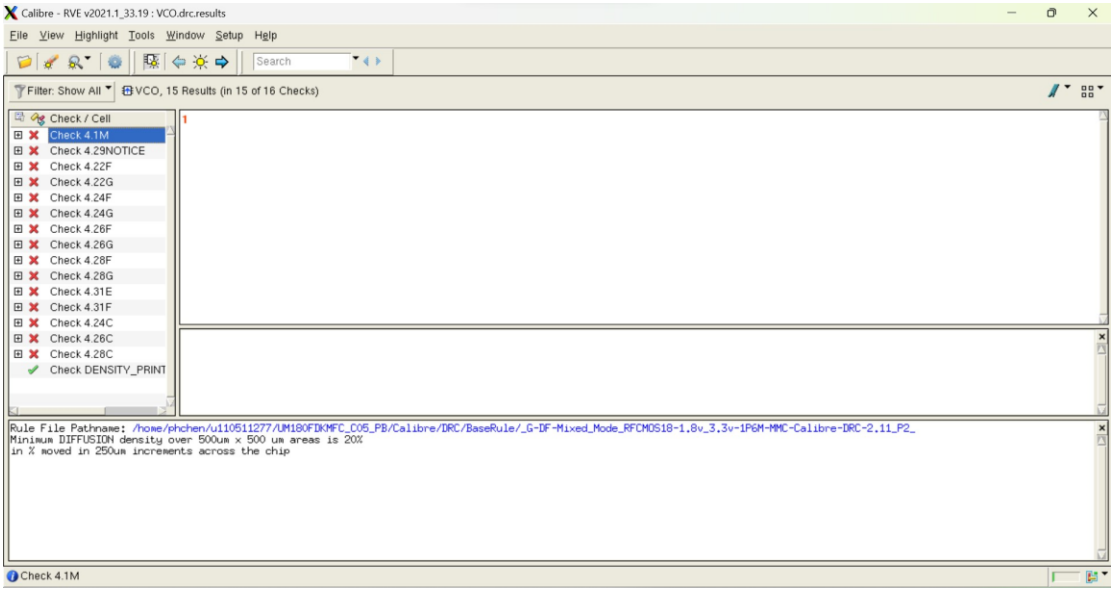
Oscillator:



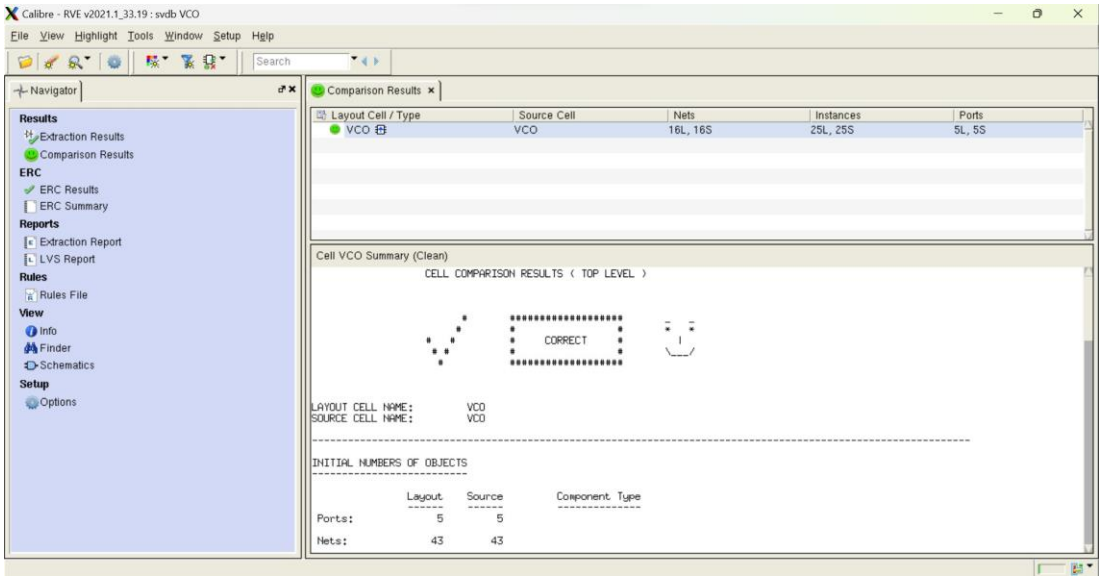
Buffer:


VirtuosoR Layout Suite L Editing: HW01 VCO layout@a17.alab.ee.nctu.edu.tw
Launch File Edit View Create Verify Connectivity Options Tools Window Calibre UMC Utils Help
cadence
Palette
Layers
All Layers
Valid Used Routing
DIFF drawing
Layer
DIFF
PWEL
PW_PDA
HVPW_32
NWEL
DNW
DPF
TWEL
ARB
OTP_TG0
PPLUS
LDD
Objects
Instances
Pins
Vias
Objects Grids
VDD
GND
PreSel: Rect Layer(ME1 drw) Width(100.1500) Height(16.5300)
mouse L: mouseSingleSelectPt()
M: hiZoomRelativeScale(getCurrentWindow() 0.8)
R: _lxHiMousePopUp()
Cmd:

2. DRC


Calibre - RVE v2021.1_33.19 : VCO.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
VCO, 15 Results (in 15 of 16 Checks)
Check / Cell
Check 4.1M
Check 4.29NOTICE
Check 4.22F
Check 4.22G
Check 4.24F
Check 4.24G
Check 4.26F
Check 4.26G
Check 4.28F
Check 4.28G
Check 4.31E
Check 4.31F
Check 4.24C
Check 4.26C
Check 4.28C
Check DENSITY_PRINT
Rule File Pathname: /home/phchen/u1105112277/UM180FDKMFC_C05_PB/Calibre/DRC/BaseRule/_G-DF-Mixed_Mode_RFCMOS18-1.8v_3.3v-1P6M-MMC-Calibre-DRC-2.11_P2_
Minimum DIFFUSION density over 500um x 500 um areas is 20%
in % moved in 250um increments across the chip
Check 4.1M

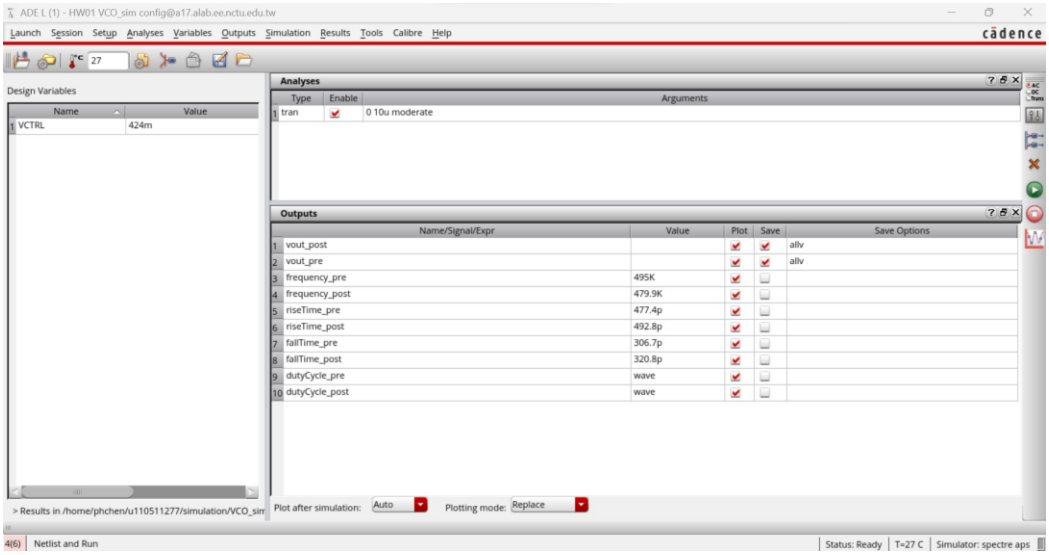
3. LVS



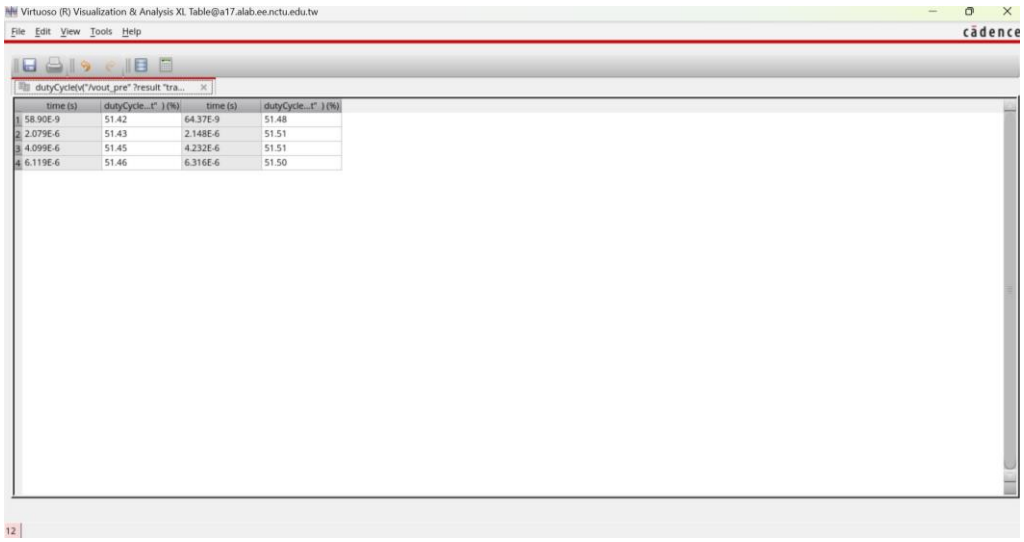
4. Result table

Parameter	Target	Pre-layout Simulation	Post-layout Simulation	Error Calculation
Supply Voltage (V_{DD})	1.8V	1.8 V	1.8 V	
Oscillation Range (f_{min}~f_{max})	0.5MHz @V_{CTRL}	495kHz @424mV	479.9kHz	3.05%
	2.5MHz @V_{CTRL}	2.523MHz @548mV	2.444MHz	3.13%
Rising Time (t_F)	<0.5ns @0.5MHz	477.4ps	492.5ps	3.16%
	<0.5ns @2.5MHz	475.2ps	496.2ps	4.42%
Falling Time (t_R)	<0.5ns @0.5MHz	306.7ps	320.8ps	4.6%
	<0.5ns @2.5MHz	307ps	321.7ps	4.79%
Duty-cycle	47%<D<53%	51.1%	51.4%	
Number of Stage (N)	Any	11級OSC +	6級 buffer	

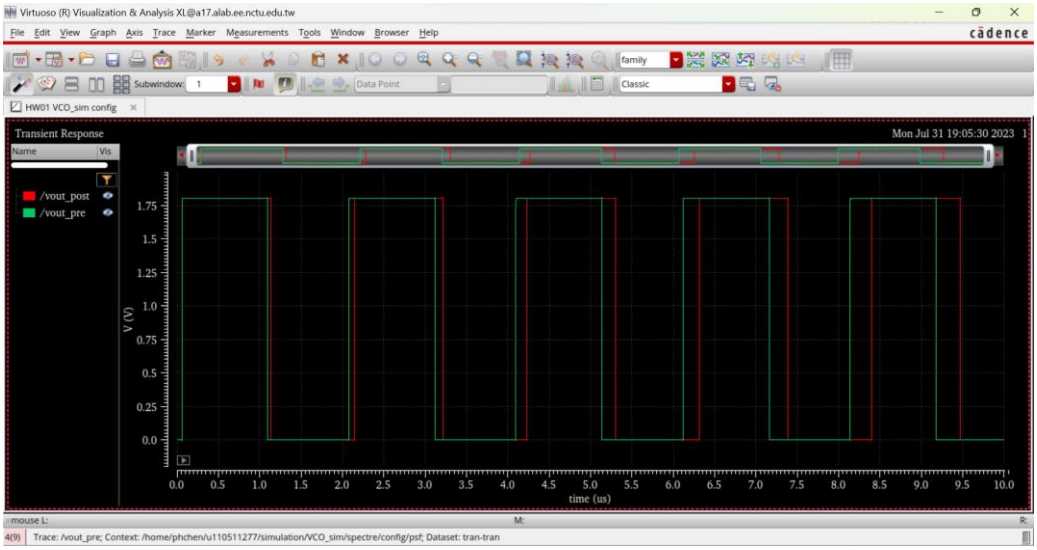
Outcome(fmin) vctrl=424mV



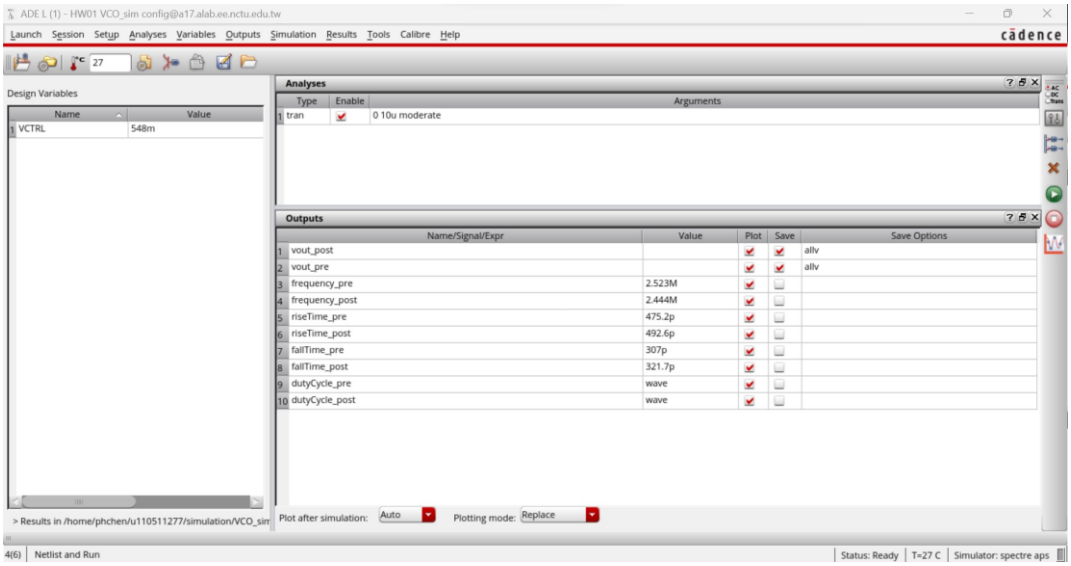
duty cycle(第一排為 pre-sim 第二排為 post-sim)



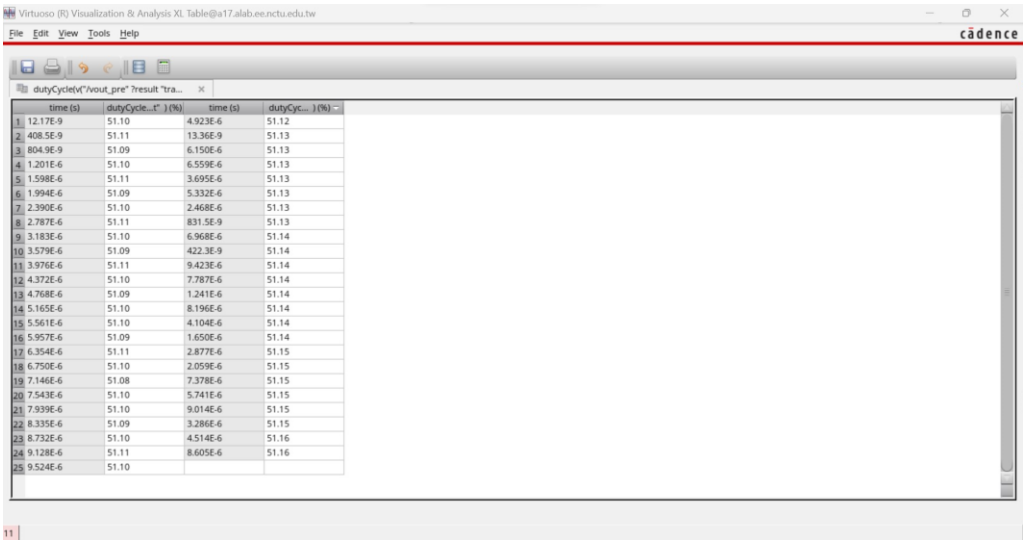
波型



Outcome(fmax) vctrl=548mV



duty cycle(第一排為 pre-sim 第二排為 post-sim)



波型