

# 電源管理晶片設計與實作

## *Buck Converter Design*

### Power MOS Layout

TA: 溫晨羽, 劉子寧

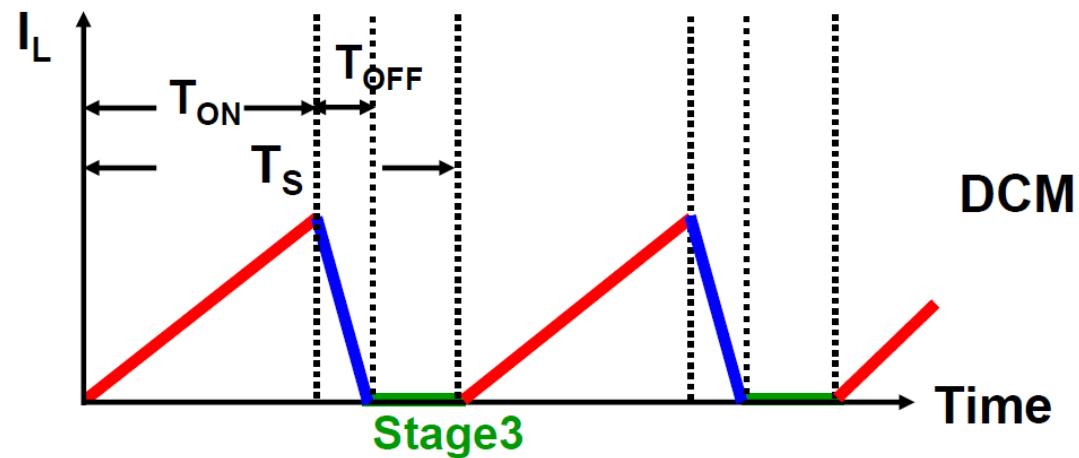
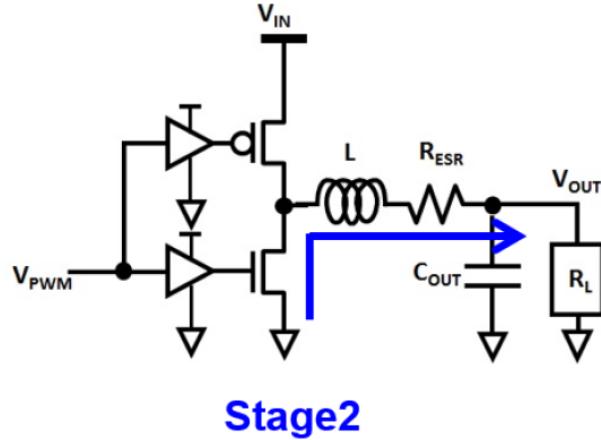
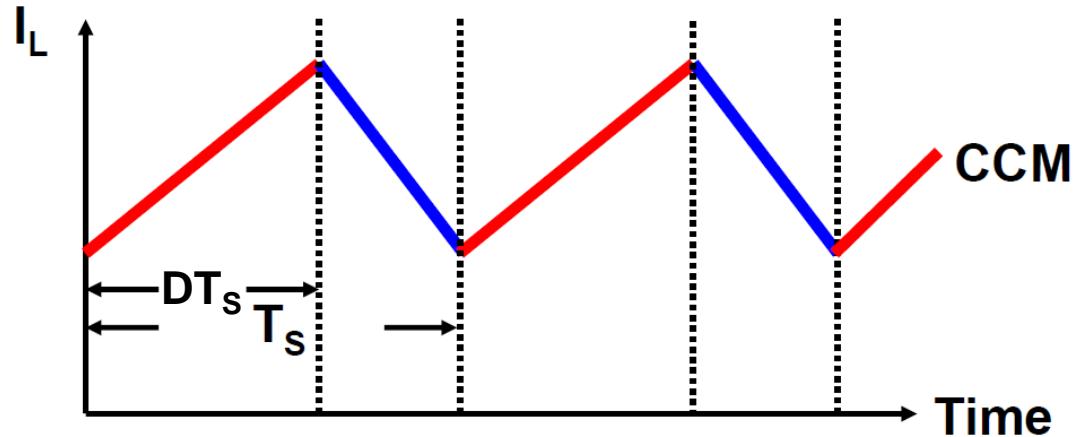
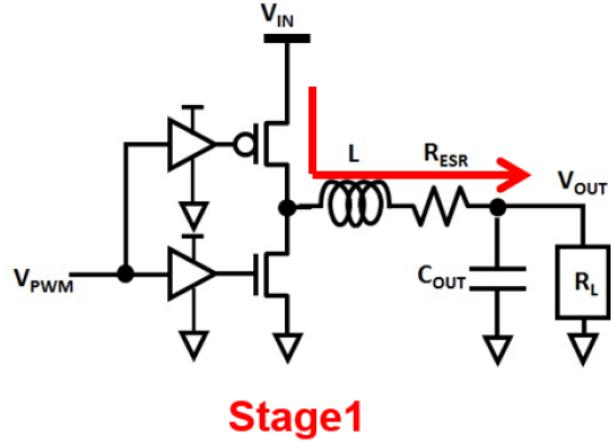
August 8th, 2023

*National Yang Ming Chiao Tung University*



# Buck Converter Introduction

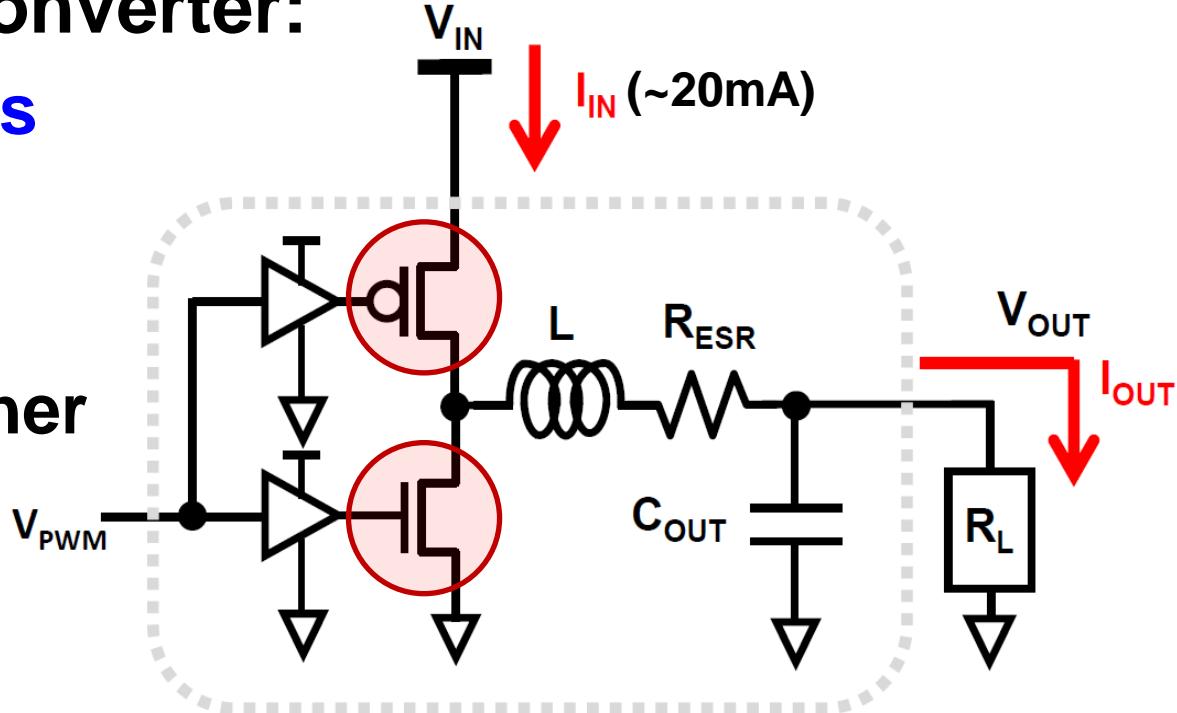
## ◆ Inductor current waveforms:



# Buck Converter Introduction

- ◆ Efficiency:  $P_{OUT} / P_{IN} = (I_{OUT} \times V_{OUT}) / (I_{IN} \times V_{IN})$
- ◆ Loss in power converter:

- Conduction loss
- Switching loss
- ESR loss
- Controller & other



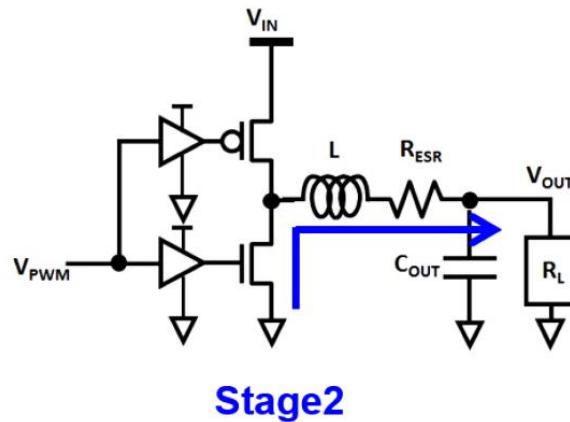
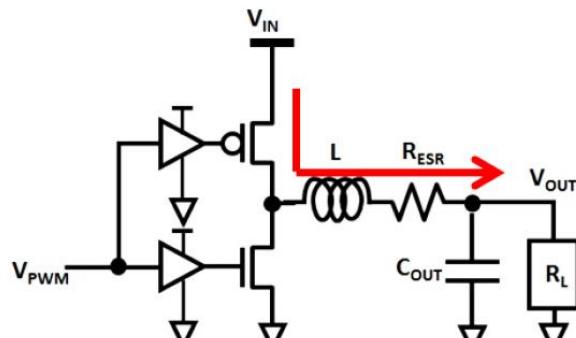
- ◆ Integrated power MOS is the important factor that affecting efficiency of DC-DC converters.



# Loss in Power Converter

## ◆ Conduction loss:

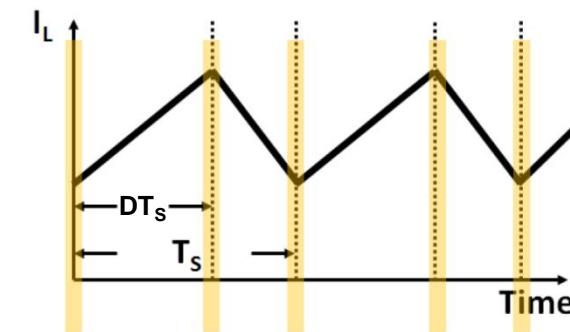
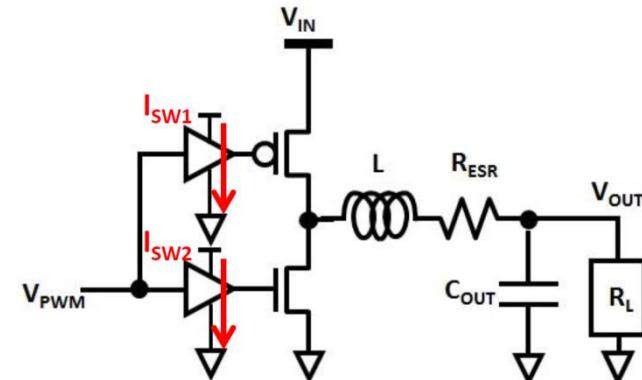
$$\triangleright I^2 \times R_{ds,ON} = I \times V_{ds}$$



## ◆ Switching loss:

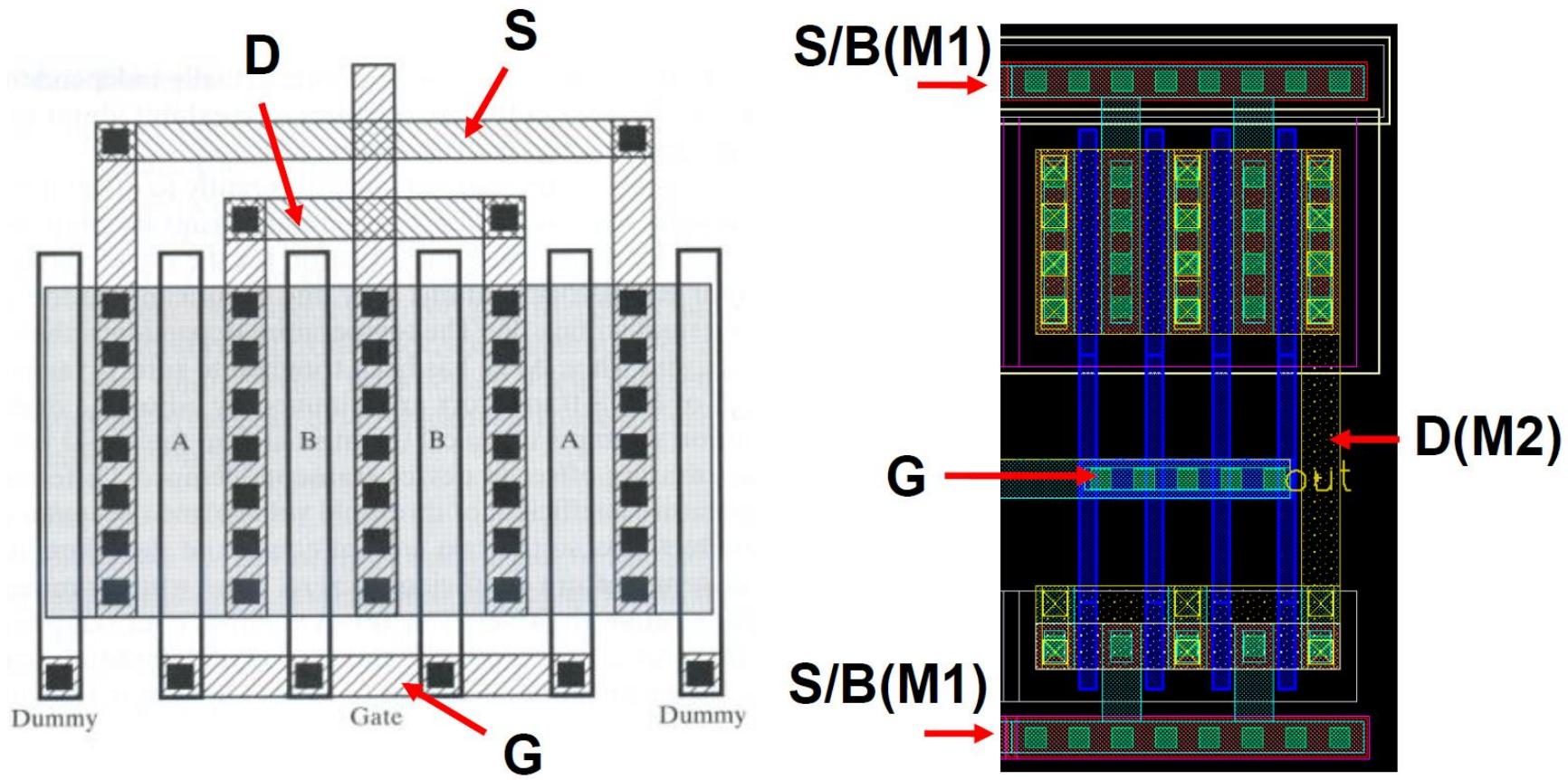
$$\triangleright 0.5 \times F_{SW} \times C_g \times V_{IN}^2$$

$$\triangleright (I_{sw1} + I_{sw2}) \times V_{IN}$$



# S/D Metallization of General MOS

## ◆ General interdigitated MOS



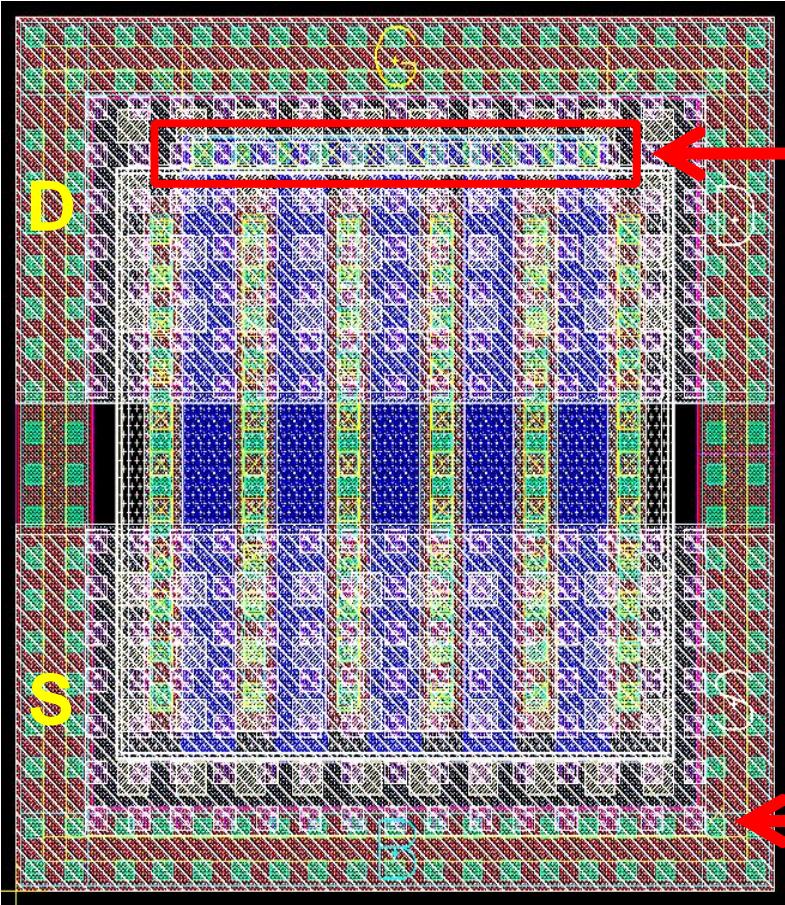
⌚ Width of S/D metal line can't afford large current.



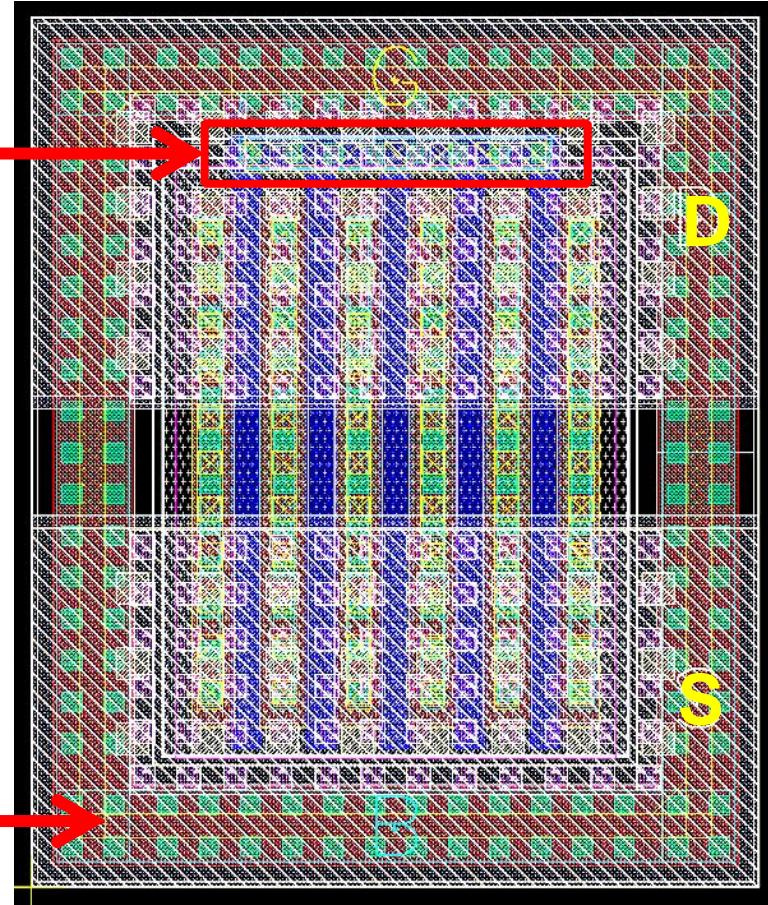
# Power MOS Layout Example

- ◆ Power MOS cell:  $W \cdot N_f = 6\mu \cdot 5$

NMOS



PMOS

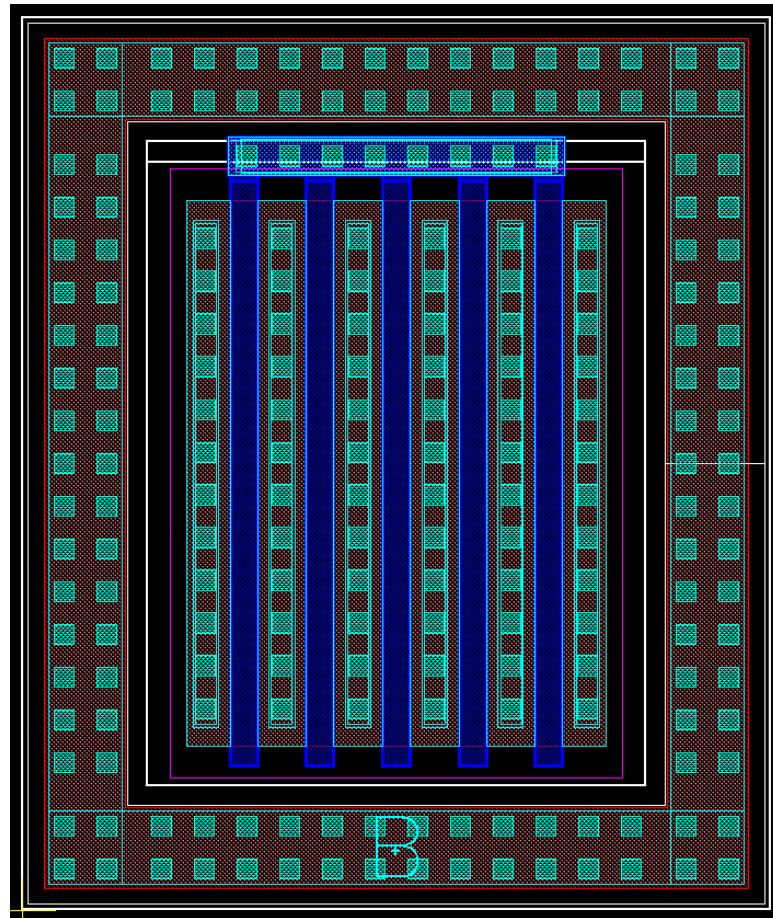


S/D  
(M3~M6)

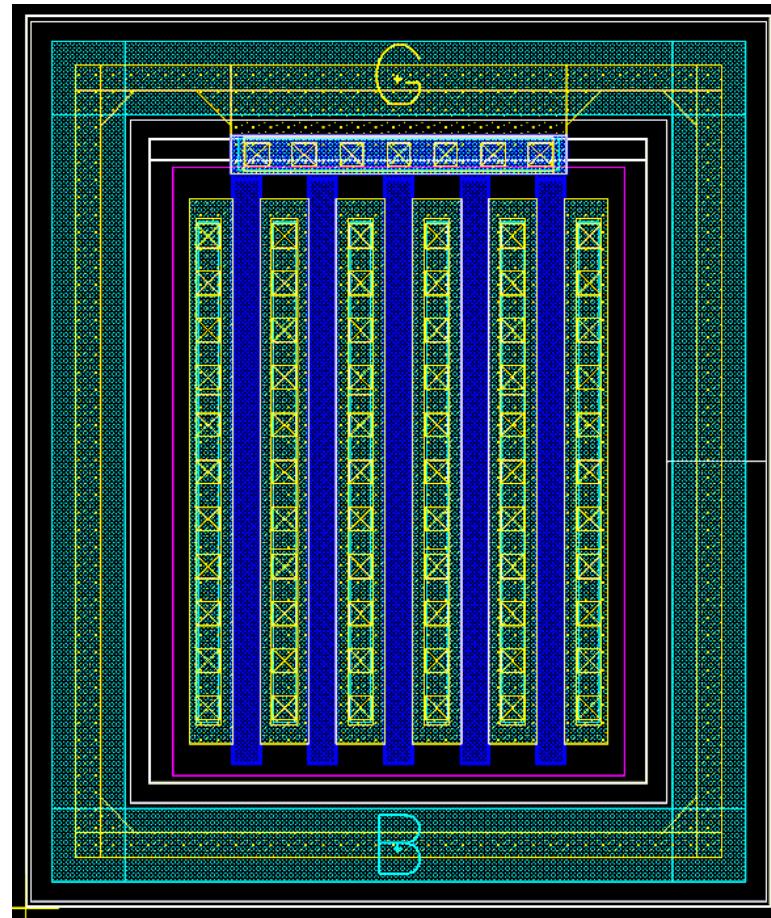
← Body(M1) →

# Power MOS Layout Example

## ◆ Power PMOS cell



PMOS + Metal1

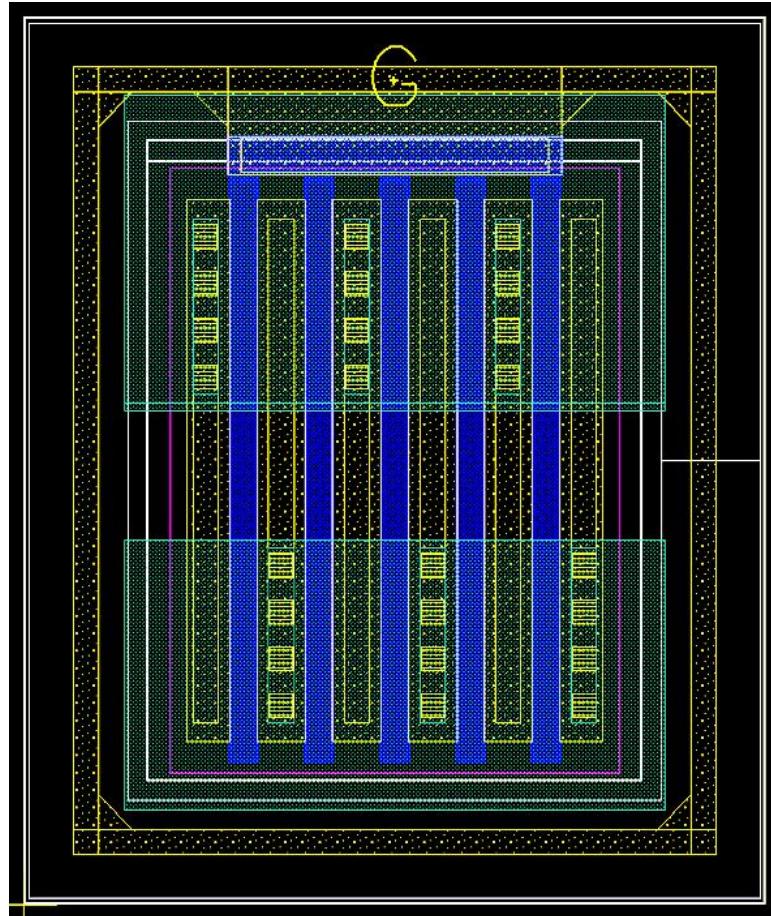


Metal1~2 + via1

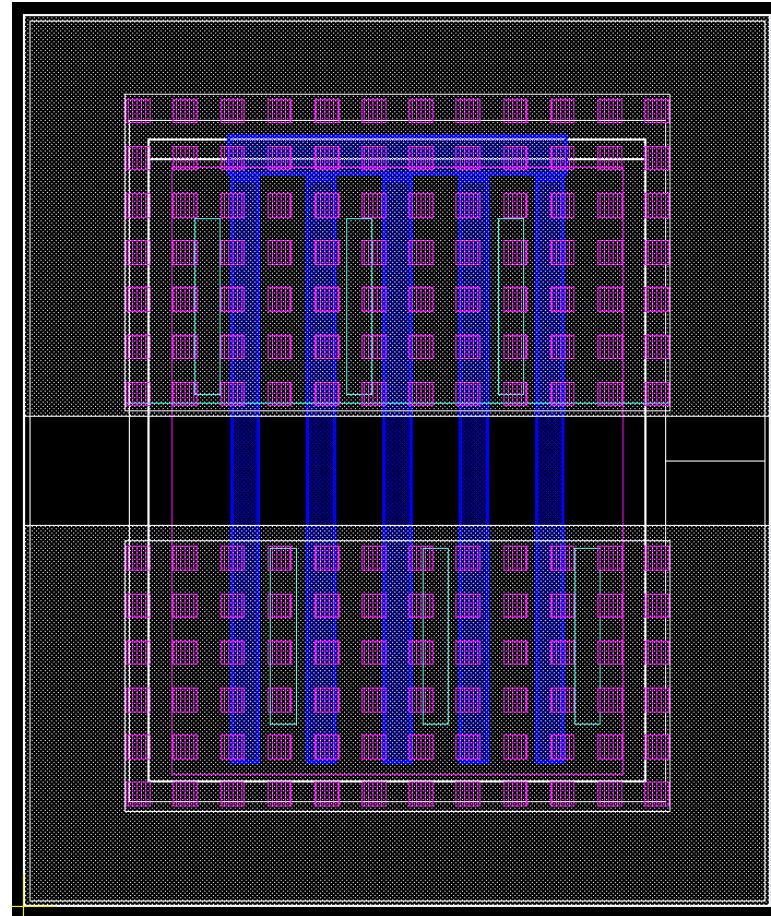


# Power MOS Layout Example

## ◆ Power PMOS cell



Metal2~3 + via2

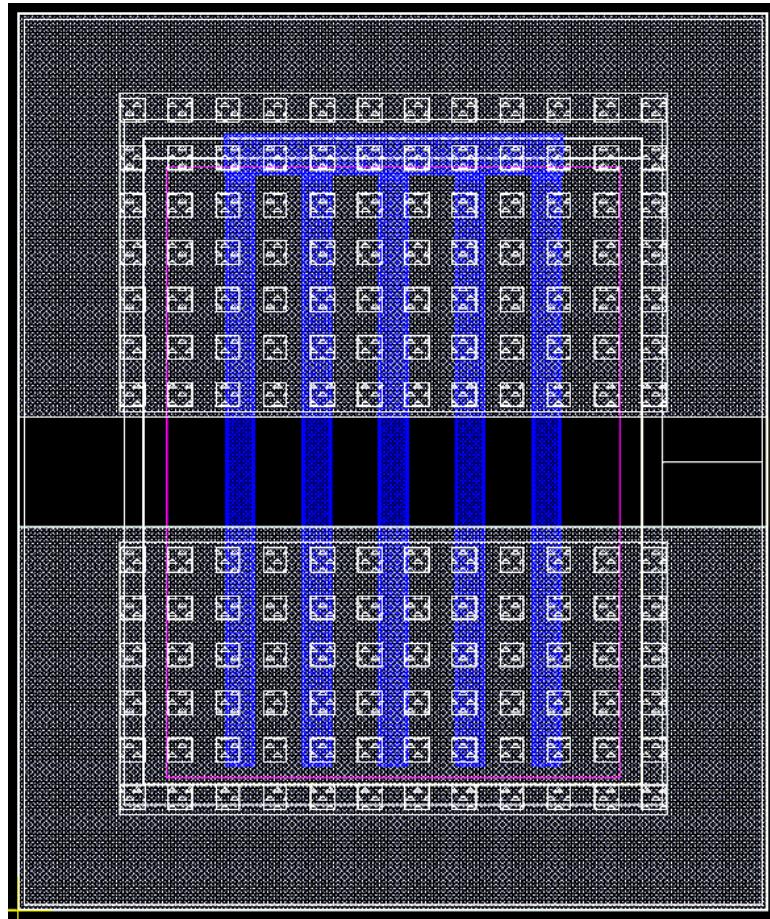


Metal3~4 + via3

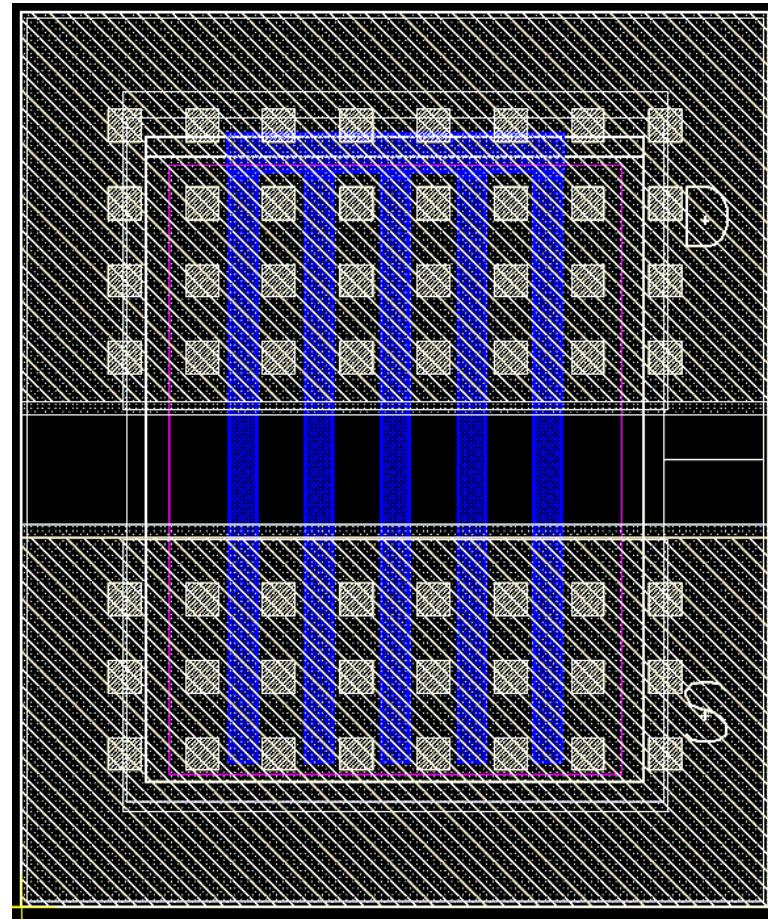


# Power MOS Layout Example

## ◆ Power PMOS cell



Metal4~5 + via4

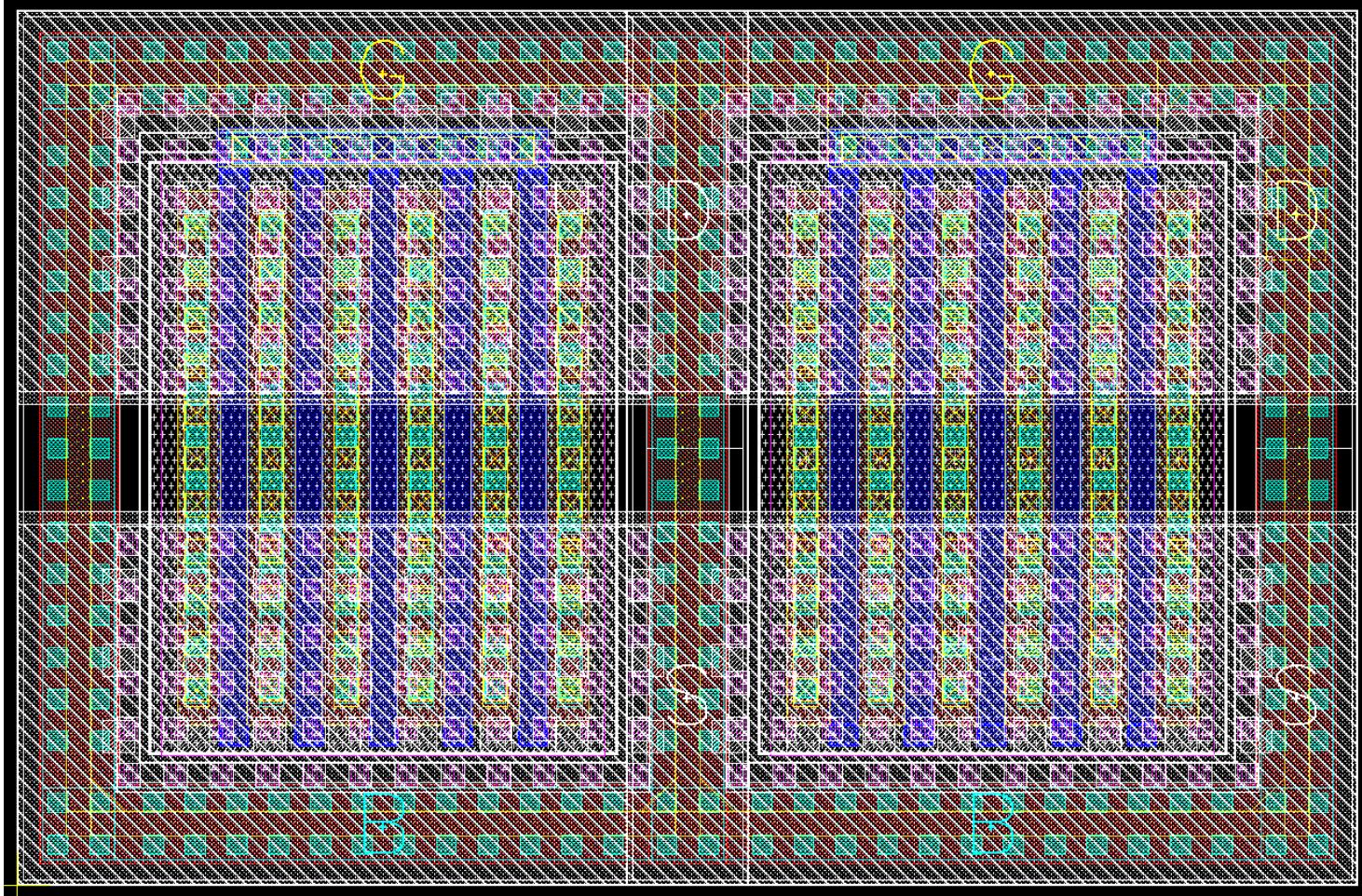


Metal5~6 + via5

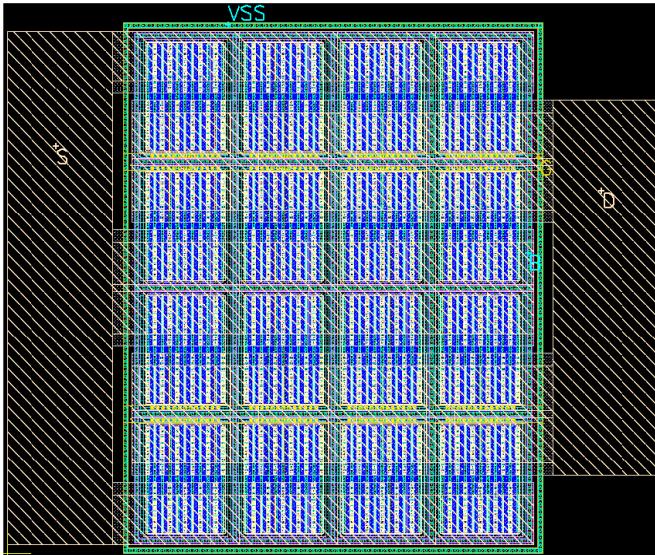


# *Power MOS Layout Example*

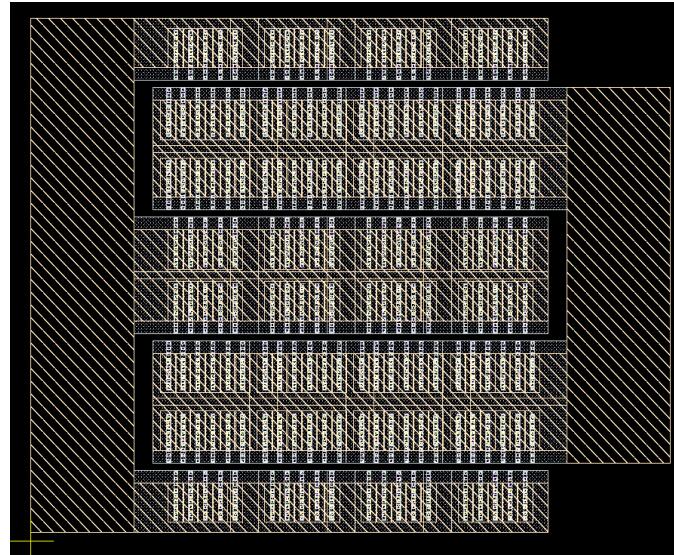
- ◆ Combine two power PMOS cells



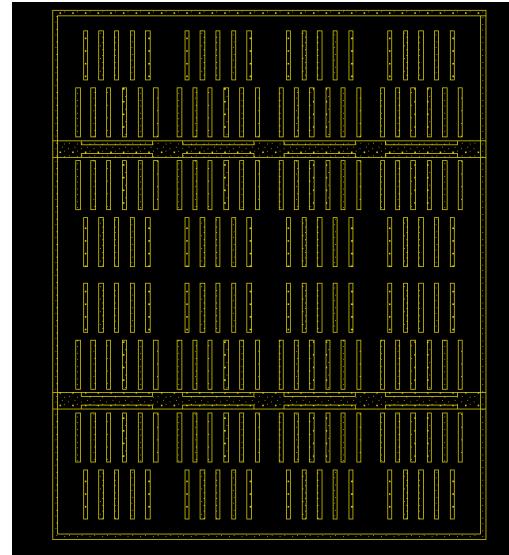
# Power MOS Layout Example



Power PMOS 4x4



Source and Drain



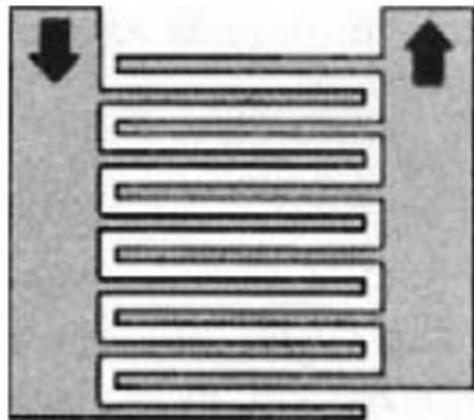
Gate

- ◆ **Power line layout concern:** ( $\sim 1\mu\text{m} = 1\text{mA}$ )
  - Large current tolerance → enough wider power line
  - Metal parasitic resistance →  $10\sim 30\mu\text{m}$  or more
- ◆ **Gate width layout concern:**
  - Gate parasitic capacitance & Switching loss

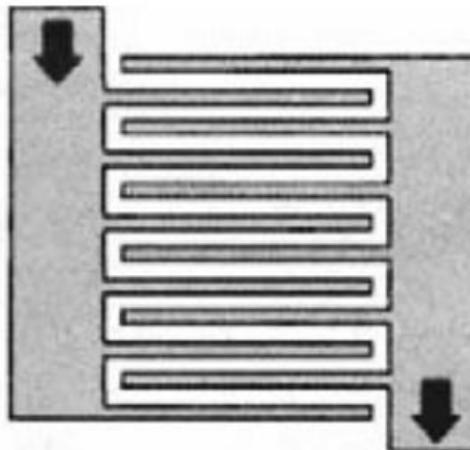


# S/D Metallization of Power MOS

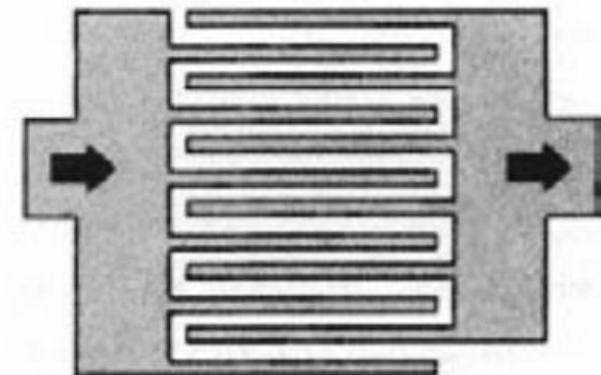
## ◆ Power MOS: Current flow direction in S/D



(A)



(B)



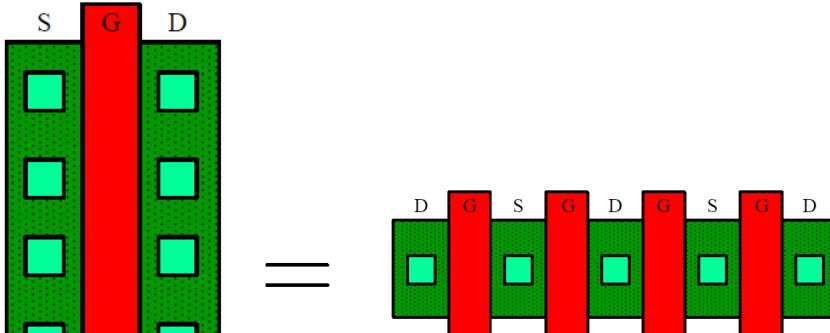
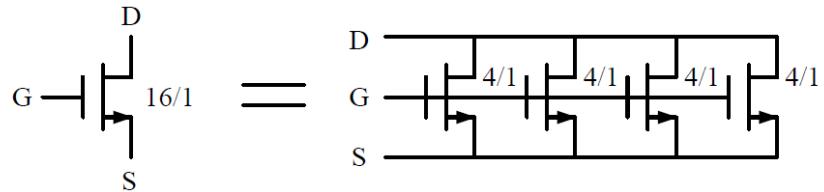
(C)

- **A** -common arrangement, excessive voltage drop, uneven current distribution
- **B** -better arrangement and lower total R than A, even current distribution
- **C** -not have to flow full length of bus, minimizes R, uneven current distribution



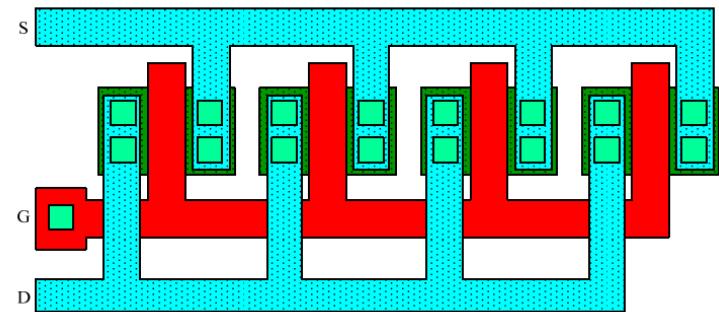
# Layout Styles of MOS Transistor

## ◆ MOS並聯等效

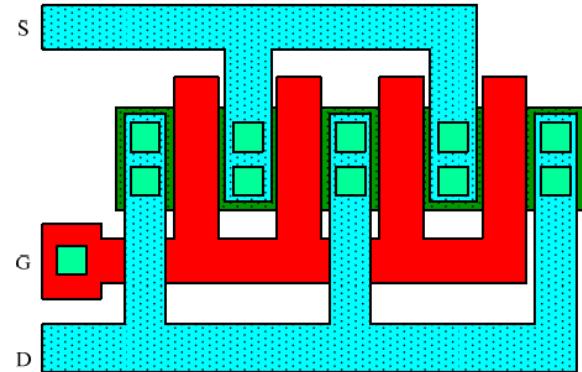


由於讓S/D面積共用，因此減小S/D端的寄生電容

## ◆ 相鄰端不共用

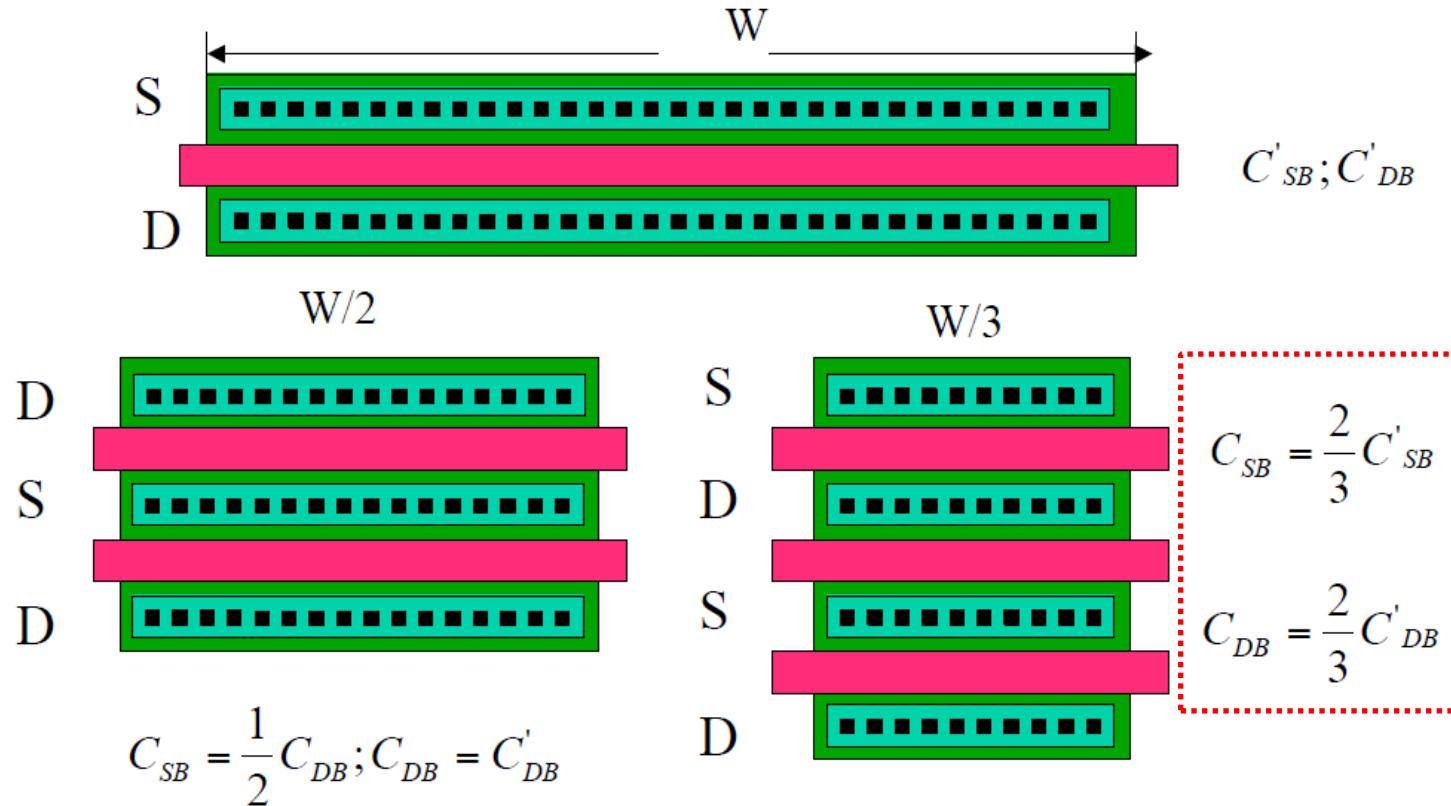


## ◆ 相鄰端共用



# Use of Multiple Fingers

- ◆ 畫Power MOS若使用越多Fingers, 寄生電容越小
  - 但Drain/Source供給電流Path的線寬則越窄



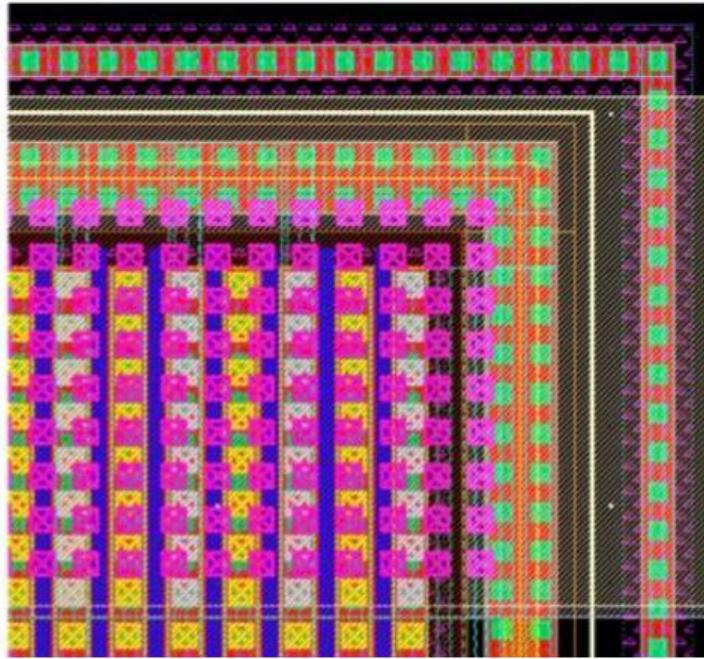
Source: F. Maloberti – Layout of Analog CMOS IC



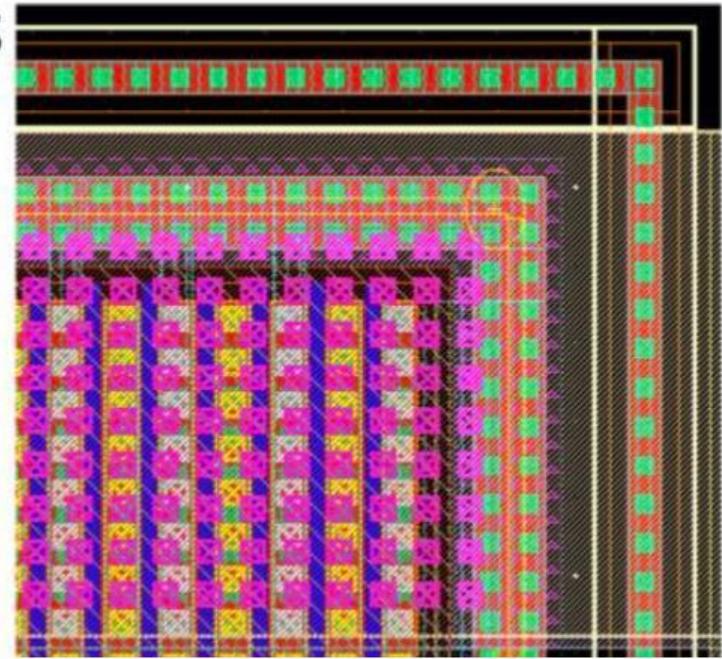
# *Double Guard-ring*

- ◆ PMOS需要先圍nplus diffusion(接vdd)再圍pplus diffusion(接地)
- ◆ NMOS需要先圍pplus diffusion(接地)再圍nplus diffusion(接vdd)並加上deep n-well

PMOS



NMOS



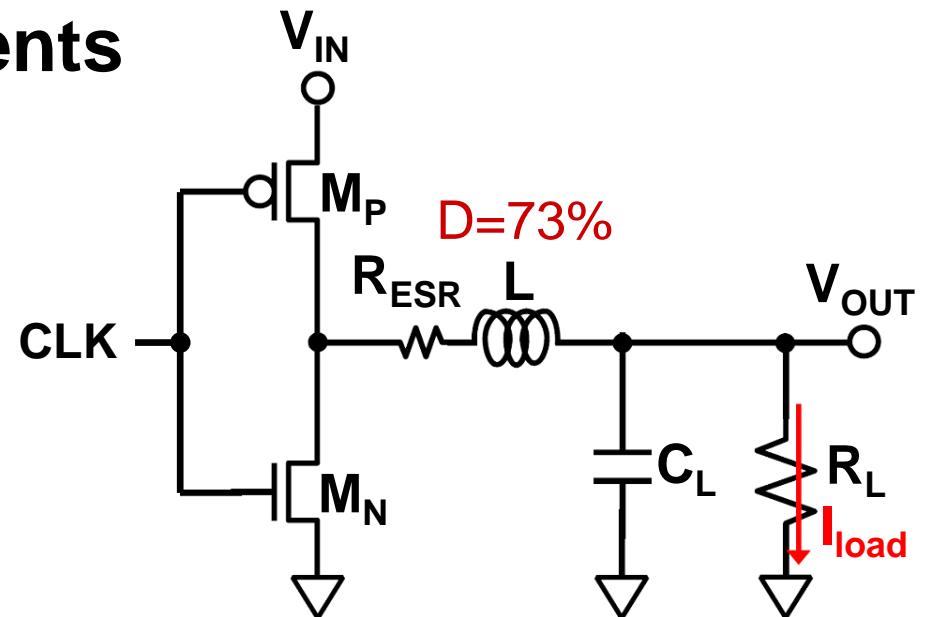
# Lab 3 - Open Loop Buck Converter

## ◆ Power stage components

- $M_P$ :  $(10\mu\text{m}/0.18\mu\text{m}) * 120$
- $M_N$ :  $(10\mu\text{m}/0.18\mu\text{m}) * 60$
- $R_{ESR}$ :  $0.26\Omega$
- $L$ :  $10\mu\text{H}$
- $C_L$ :  $10\mu\text{F}$
- $R_L$ :  $650\Omega$

**CLK:**

- voltage =  $1.8\text{V}$
- rising time =  $1\text{ps}$
- falling time =  $1\text{ps}$
- duty =  $27\%$

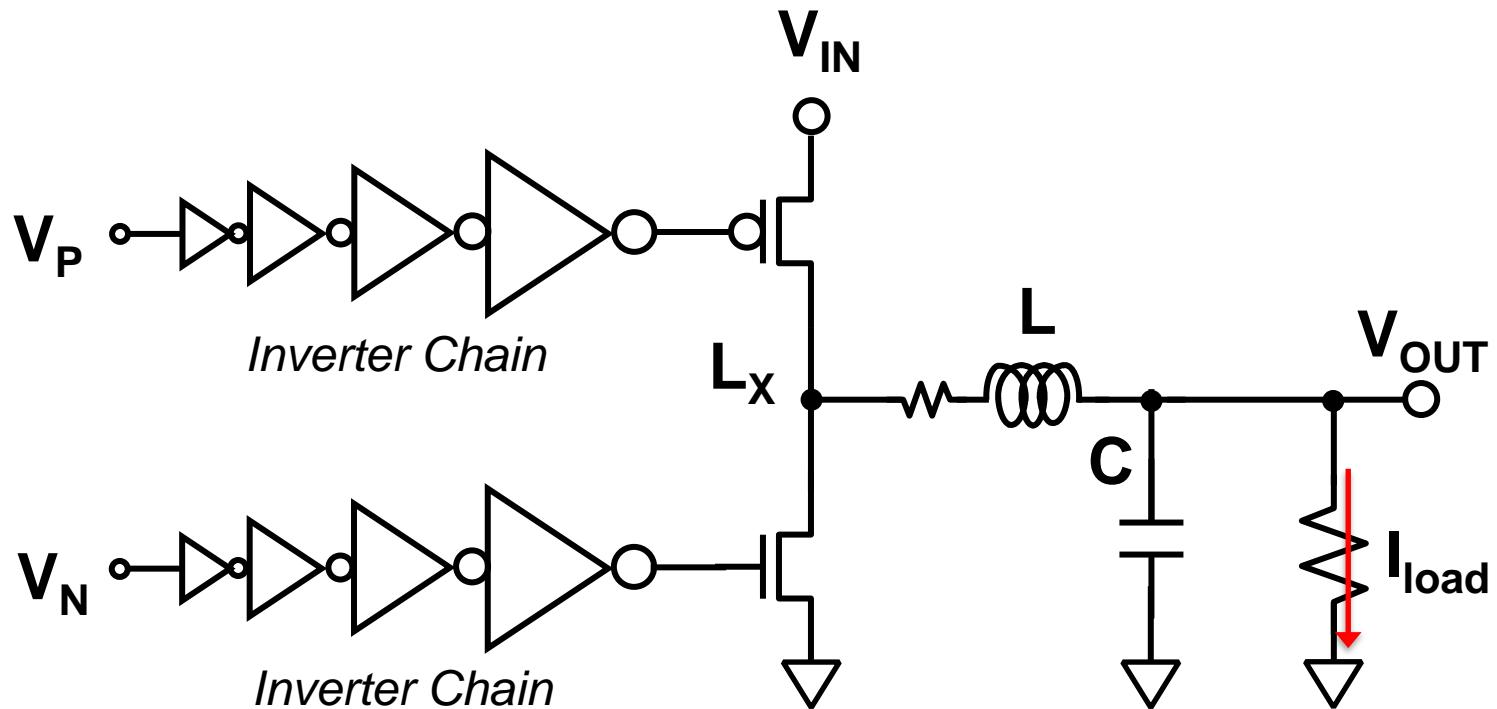


Parameters	$I_{load} = 2\text{mA (BCM)}$		Unit
Input Voltage ( $V_{IN}$ )	1.8		V
Output Voltage ( $V_{OUT}$ )	1.3		V
Switching Frequency ( $F_{SW}$ )	10		MHz
Power Conversion Efficiency	Pre-sim.	Post-sim.	%
	94.6%	>92%	



# PMIC Project1

## □ Design a buck converter



# PMIC Project1

## □ Specifications

Parameters	SPEC.	Design	Unit
Input Voltage ( $V_{IN}$ )	1.8		V
Output Voltage ( $V_{OUT}$ )	1.2 (1.19~1.21)		V
Load Current ( $I_{LOAD}$ )	10, 90, 180		mA
Inverter Chain	>5		stage
Output Capacitance	10		uF
Output Ripple	< 20 (10mA, 90mA, 180mA)		mV
Power Conversion Efficiency (post-layout)	>92 (10mA, 90mA, 180mA)		%

- External sources: Only “one” power source ( $V_{in}$ ), “one” control signal ( $V_{CLK}$ ).



# PMIC Project1 (Loss Calculation)

TABLE I

Estimated percentage of total losses from pre-layout simulation data (  $V_{IN}=1.8V$ ,  $V_{out}=1.2V$  )

Source of Losses	$I_{load} = 10\text{mA}$ (CCM)	$I_{load} = 90\text{ mA}$ (CCM)	$I_{load} = 180\text{mA}$ (CCM)
Inductor series resistance			
nFET gate driver			
nFET channel resistance			
pFET gate driver			
pFET channel resistance			
$L_x$ node capacitance			
Others?			

\*Efficiency should be optimized at each condition.  
\*Conduction loss (%) should increase as output load increases.



## □ Specifications

- 只有一個輸入電壓 $V_{IN}$ , 以及一個控制訊號 $V_{CLK}$
- 電感L大小 $1\mu H \sim 100\mu H$ , ESR 從規格表找
- 電容 C 使用 $10\mu F$ 理想元件,  $I_{load}$ 使用理想電流源
- 電感電流須恆為正值( $> 0$ )
- 開關頻率選擇請用整數( $0.1, 0.2, \dots, 1, 2, \dots, 10$  (MHz))
- 設計功率電晶體大小 ( $w, m$ )
- 不同輸出電流下的duty cycle不一樣
- Buffer第一級INV之NMOS必須使用最小size, PMOS size須為NMOS之兩倍
- 計算效率請取0.5ms至1ms的完整整數週期的輸出/輸入功率進行計算



# Chip Inductor Specification

產品規格 (ELJEA Series)			
大小	L.3.2 W.2.5 H.2.2 (mm)		
操作溫度範圍	-20 → +85 ° C		
型號	電感值 ( μH)	直流阻抗(Ω)	額定電流(mA)
ELJEA1R0MF	1	0.07	500
ELJEA1R5MF	1.5	0.08	390
ELJEA2R2MF	2.2	0.1	350
ELJEA3R3MF	3.3	0.12	270
ELJEA4R7MF	4.7	0.14	240
ELJEA6R8MF	6.8	0.19	200
ELJEA100KF	10	0.26	160
ELJEA150KF	15	0.32	145
ELJEA220KF	22	0.5	115
ELJEA330KF	33	0.7	95
ELJEA470KF	47	1	80
ELJEA680KF	68	1.5	60
ELJEA101KF	100	2.4	50

<http://jp.rs-online.com/mobile/search/searchBrowseAction.html?method=getProduct&R=6654388>



# PMIC Project1

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## □ Demo

- 繳交2頁報告、列出Specification、Table I 兩張表，並於8/22（二）之前上傳至e3平台。
- **Deadline: 8/22(二) 上機時直接Demo給助教看**
- **抄襲0分**
- 總分10分: Spec.全部達到9分，少一項扣1分，報告1分
- 評分項目為10mA 90mA 180mA 平均輸出電壓、輸出漣波及轉換效率(Post-layout simulation, 共九項)



# *Project 1 Notification*

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- ◆ 注意事項1: 於Lab3上機時所畫的Power MOS layout可延用於Project 1
- ◆ 注意事項2: 需在整顆組起來的Power PMOS及NMOS圍上guard ring, 以防Latch-up及雜訊
- ◆ 注意事項3: PEX驗證請萃取“R+C+CC”，提早設計避免Post-sim.時間太久
- ◆ 注意事項4: DRC驗證最後只能有"4.29NOTICE"的錯誤
- ◆ 注意事項5: 可在電感與負載電容上設定initial condition以縮短模擬時間，電感電流設為負載電流，電容電壓設為輸出電壓。
- ◆ 注意事項6: 報告中的table-I 請填入Pre-layout simulation結果，並以百分比表示。寄生電容大小使用capacitance table的total值，並使用 $0.5 \times fcv^2$ 去計算loss. conduction loss需將 $I_D$ 與 $V_{DS}$ 的波形相乘並取穩態的平均值。
- ◆ 注意事項7: 電感電流需保證在正值，負載為10mA時需特別注意。

# *Project 1 Notification*

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- ◆ 設計提示1: 按"O"可加入Contact+Metal, 在按"O"後把下方"Compute"取消打勾, 即可調整Metal寬度。(寬度0.08um也能通過DRC)
- ◆ 設計提示2: Density錯誤 Ex:" The ME? coverage must be larger than 30% of.....", 請在空餘的面積加入對應缺少的Dummy Metal, 即可解掉。



# Hint for PIC Project 1 (1/2)

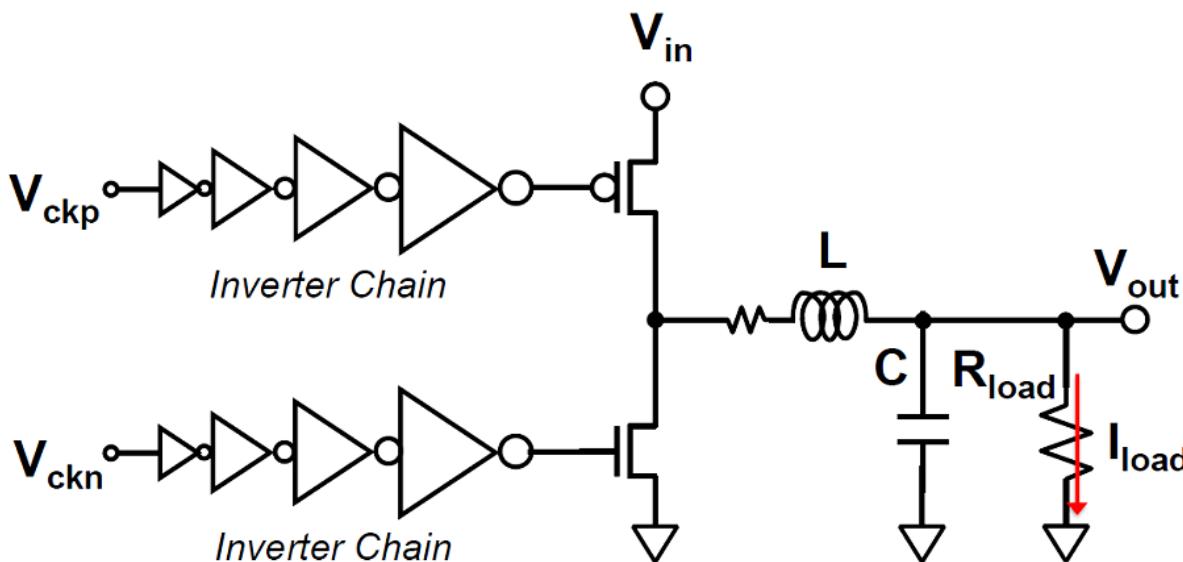
## ◆ Trade-off between loss

- L : ESR loss

- f<sub>sw</sub> : switching loss

- R<sub>ON</sub> : conduction loss

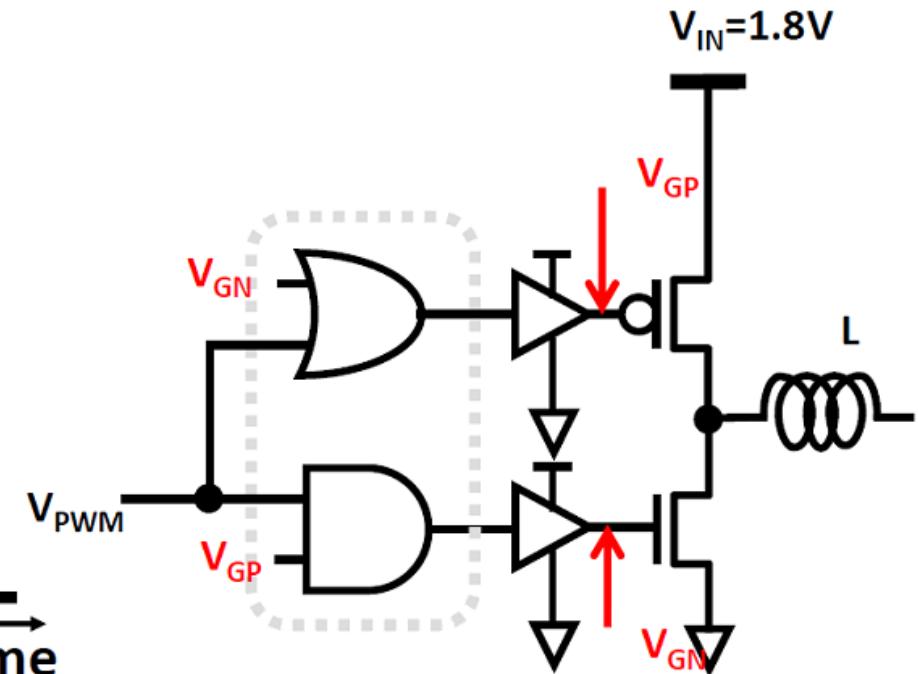
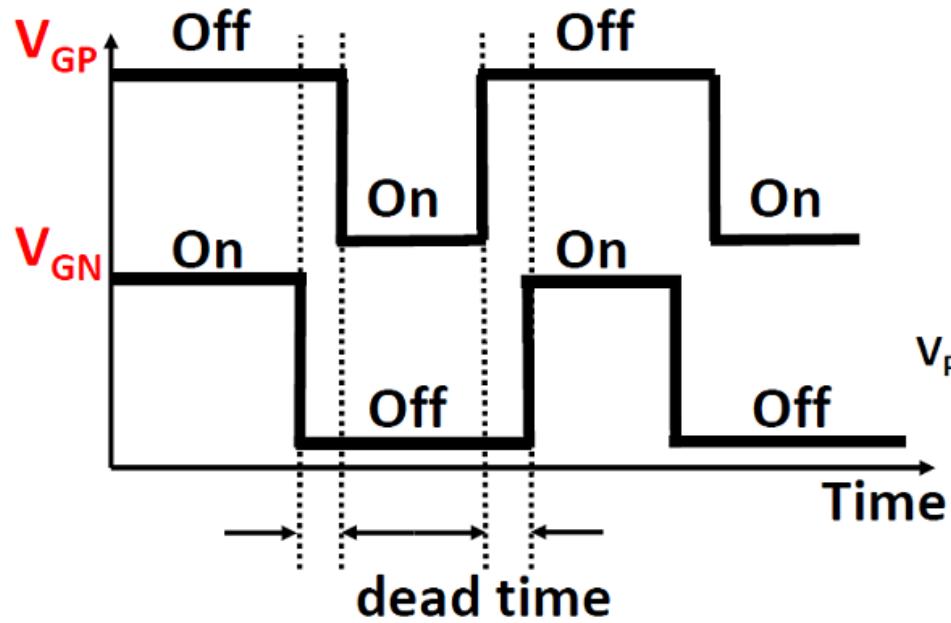
Trade-off between switching loss, conduction loss, ESR loss, etc. Is there any relationship?



# *Hint for PIC Project 1 (2/2)*

## ◆ Dead time generator

## ◆ Logics



# Node Capacitance

## ◆ 觀察節點電容值

打開PEX，點選Start RVE

Calibre Interactive - PEX v2013.3\_28.19 : PEX\_set

File Transcript Setup

Rules  
Inputs  
Outputs  
Run Control  
Transcript  
Run PEX  
**Start RVE**

```
// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.  
//  
// Mentor Graphics software executing under x86-64 Linux  
//  
// Running on Linux linux05 2.6.32-573.el6.x86_64 #1 SMP Thu Jul 23 15  
// 64 bit virtual addressing enabled  
// Running calibre/pkgsrc/icv/pvt/calibre.alt -nowait -rve -pex /misc/RA  
Process ID: 24873  
//  
Starting time: Tue Mar 14 15:54:54 2017  
//  
Running on 1 CPU  
//  
// Graphical User-Interface startup.... Complete.  
//  
calibreddb license acquired.  
RVE authorized.
```

28 Warnings

As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2008.3, the following SVRF command is deprecated: PEX TEMPERATL  
**As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRA'**  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2008.3, the following SVRF command is deprecated: PEX TEMPERATL  
As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRA'

觀察節點電容值

Calibre - RVE v2013.3\_28.19 : svdb.inv

File View Highlight Tools Window Setup

Navigator ERC Results ERC Summary

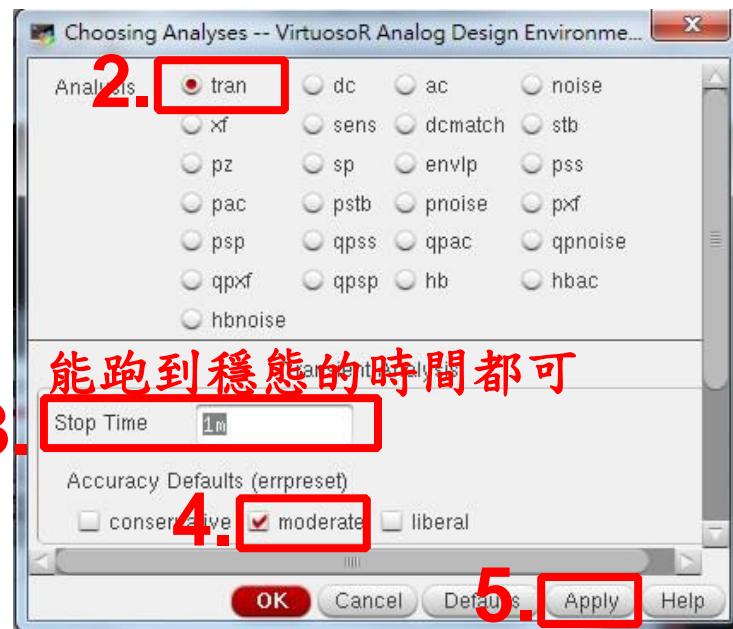
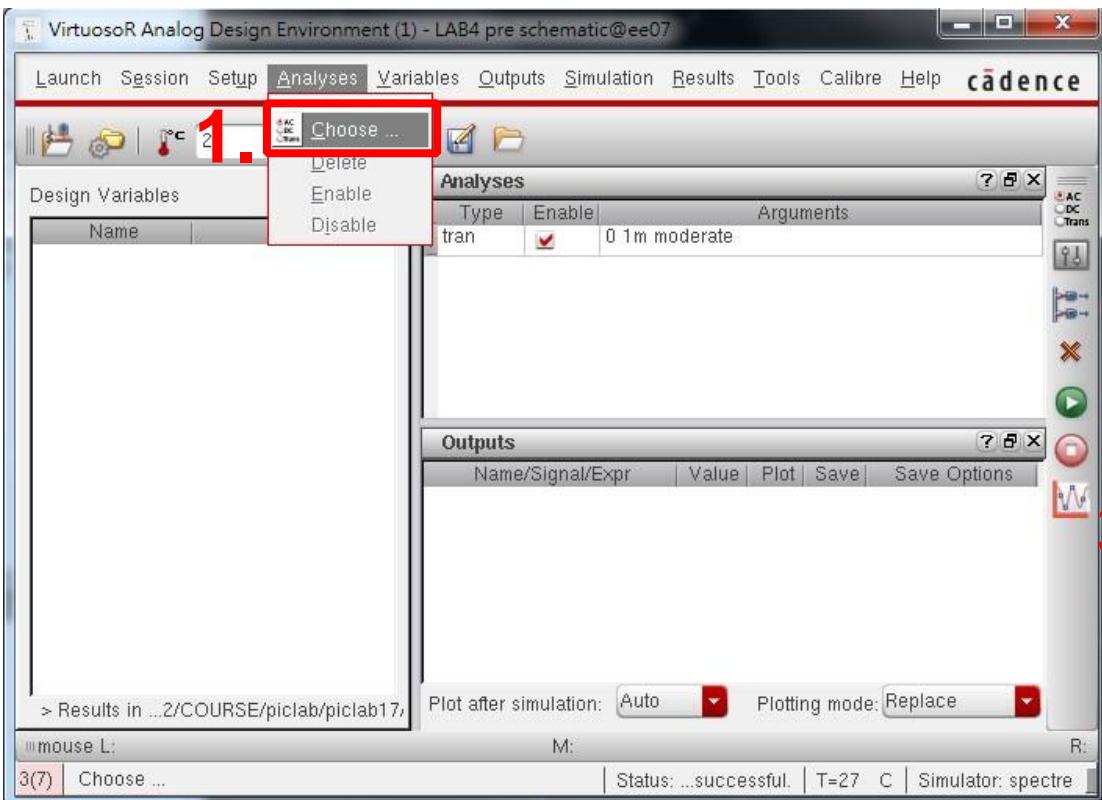
No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	IN	IN	34	8.18701E-16	2.35528E-15	3.05398E-15
2	OUT	OUT	37	2.07692E-16	3.36234E-15	3.57003E-15
3	VSS	VSS	44	7.65706E-16	1.45378E-15	2.21949E-15
4	VDD	VDD	52	7.50061E-16	2.52390E-15	3.27476E-15

C: 對地的寄生電容值  
CC: metal間寄生耦合電容值



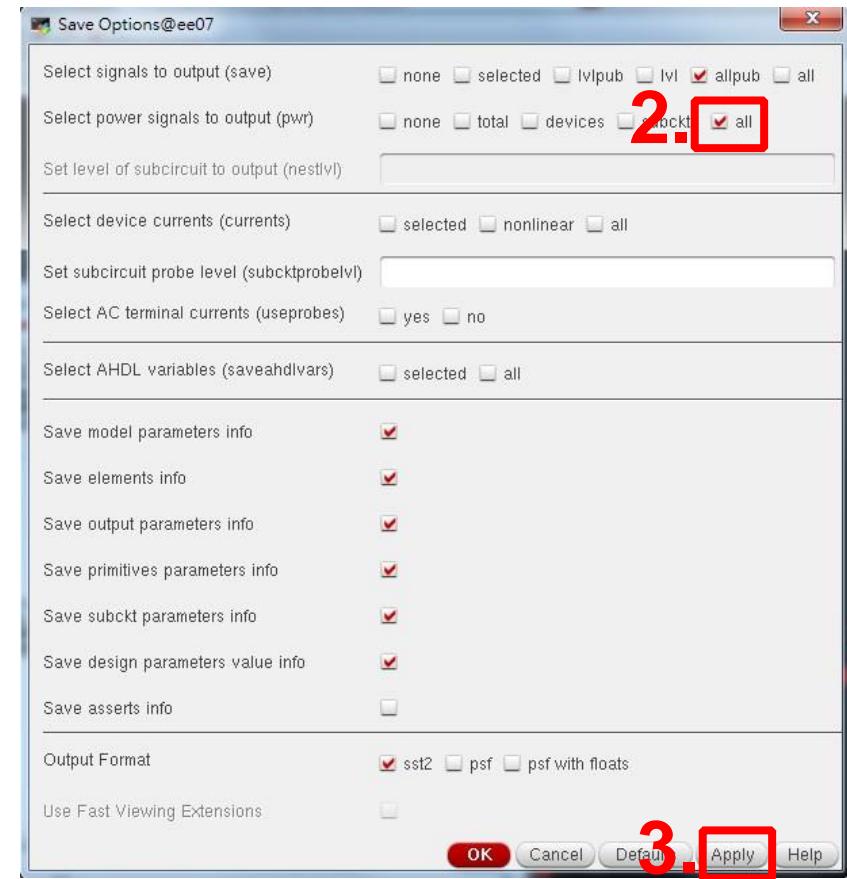
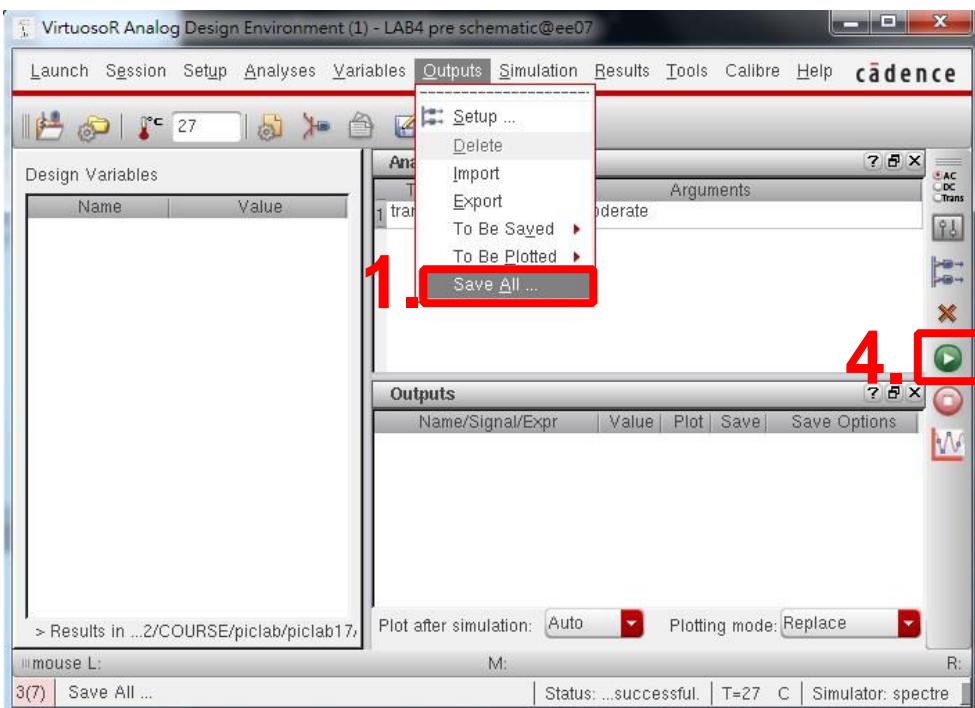
# Power & Efficiency Simulation

## ◆ 首先電路圖畫好先跑 .tran模擬 (ADE L tool)



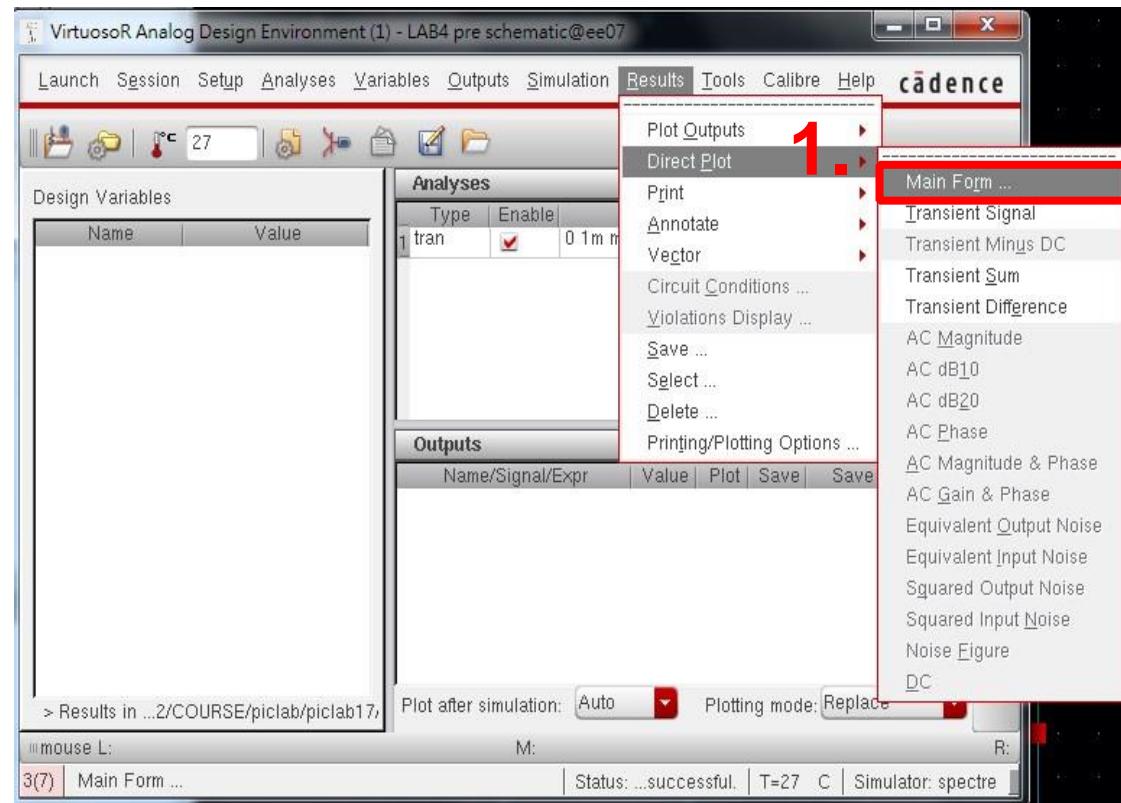
# Power & Efficiency Simulation

◆ 選擇模擬Power的Option後，即可進行模擬。



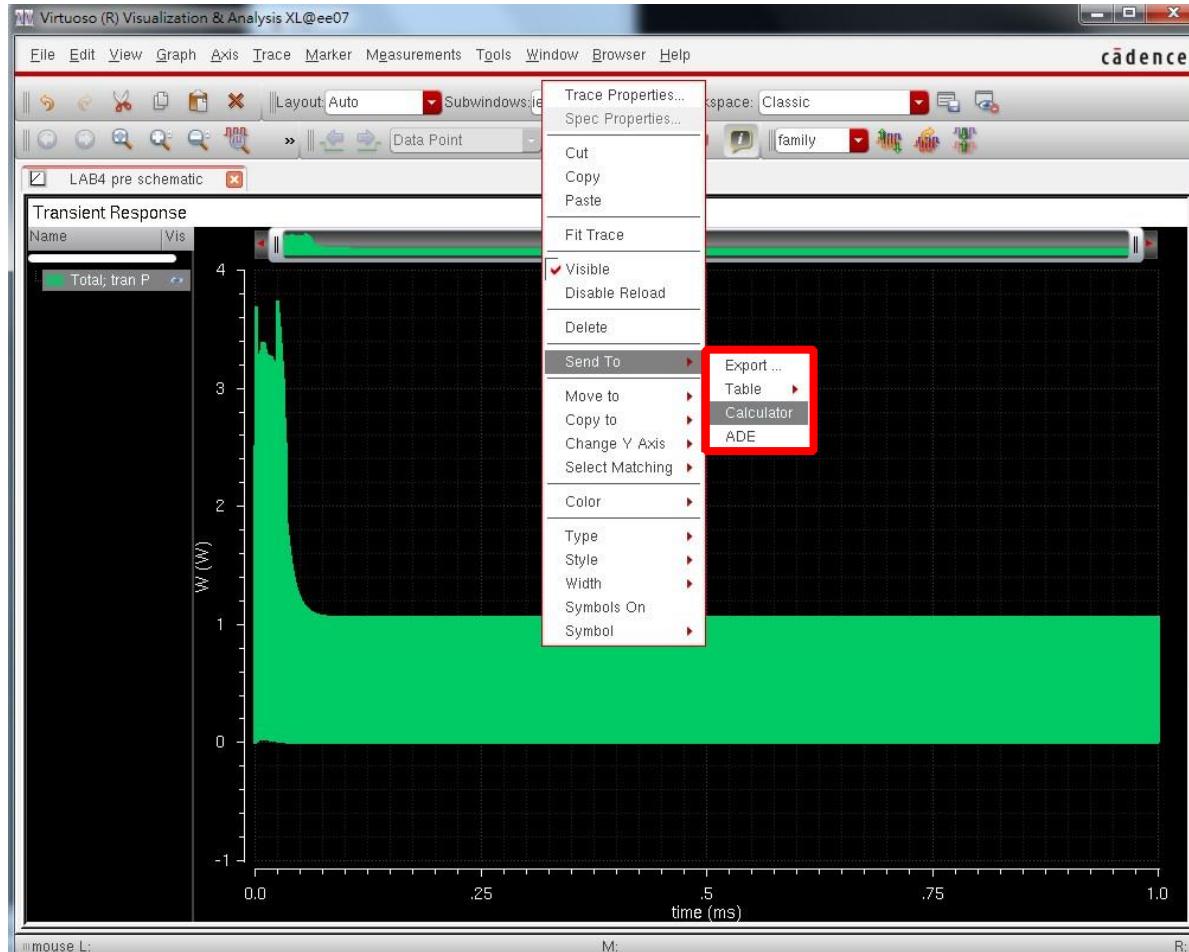
# Power & Efficiency Simulation

◆ 模擬完成後，於電路中選擇欲看Power的截點



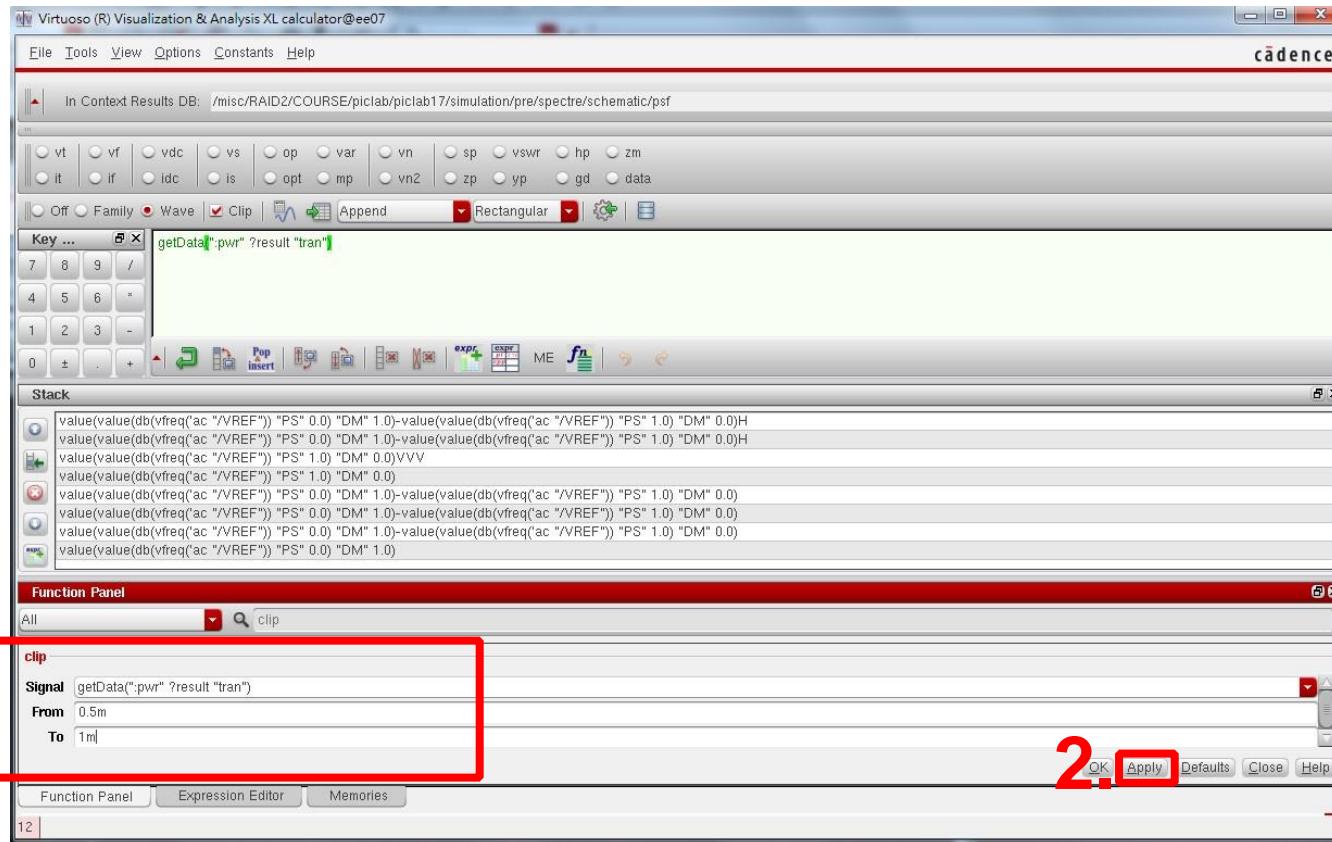
# Power & Efficiency Simulation

◆ 在波形圖點選右鍵，使用Calculator計算平均功率



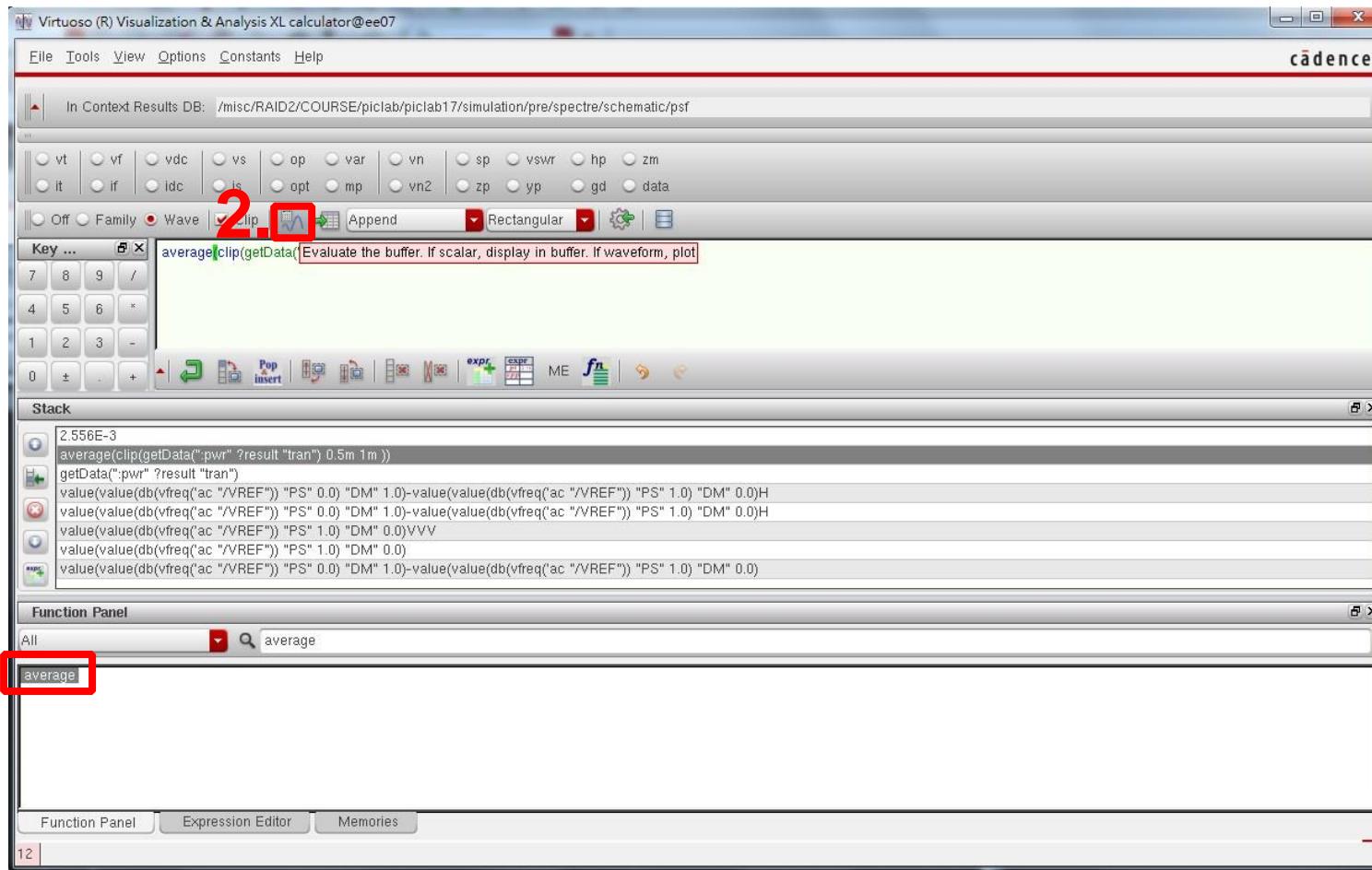
# Power & Efficiency Simulation

- ◆ 由於欲計算**穩態時的平均功率**, 因此使用”**Clip**”公式  
, 僅選取**穩態時的時間來做運算** (Ex: 0.5ms~1ms)



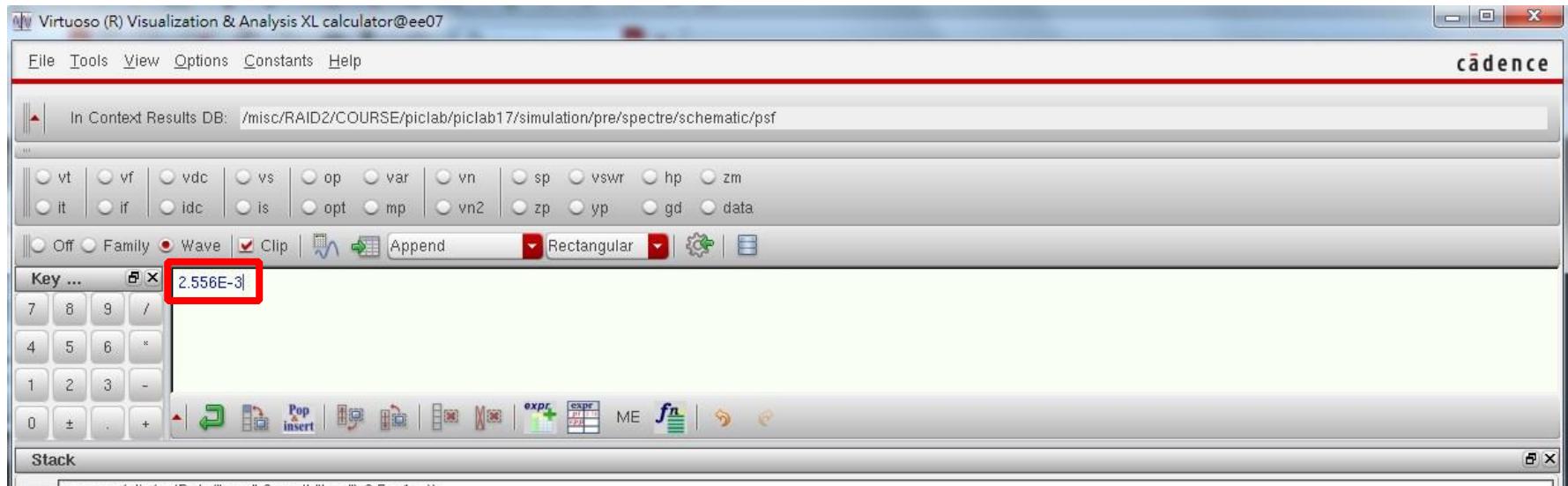
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◆ “Clip”公式選取穩態時間後，即可“Average”做平均。



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- ◆ 即可得知穩態平均功率為2.556mW



- ◆ 輸入及輸出的穩態平均功率求出後，即可運算效率。



# Power Line 注意事項

- ◆ 若Power Line畫太大片或太寬，會出現DRC Error  
(Ex: 6.A.1 ...等等的錯誤)
- ◆ Power Line 中間可以加入一些空洞，可使用上方工具列剪刀功能，或者利用方形Metal圍出空洞。Ex:

