
電源管理晶片設計與實作

Lab 2

Layout Skills & Constant-gm

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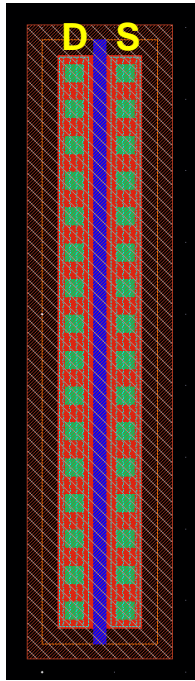
August 1st, 2023

National Yang Ming Chiao Tung University



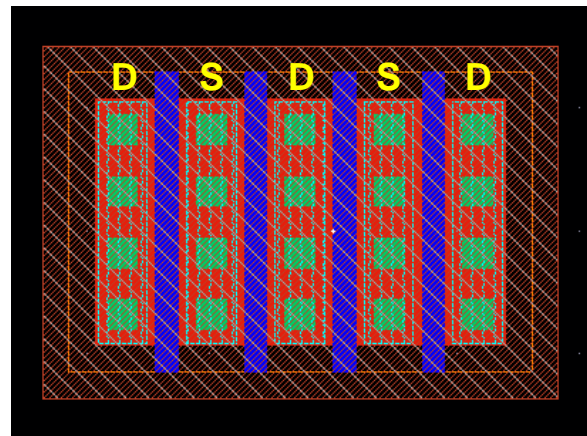
Finger Number

◆ Single Finger / Multiple Fingers Schematic View



Total Width = 8um
Finger Width = 8um
L = 180nm
Finger Number = 1

更改Finger Number時，Finger Width會自動計算為Total Width/Finger Number



Total Width = 8um
Finger Width = 2um
L = 180nm
Finger Number = 4

CDF Parameter	Value	Display
Model Name	n_18_mm	off
Total Width	8u M	off
Finger Width	8u M	off
Length	180.0n M	off
Finger Number	1	off
mis_flag	1	off
Source Drain Metal Width	400.0n M	off
AD AS PD PS Editable	<input type="checkbox"/>	off
Drain diffusion area (m^2)	3.92e-12	off
Source diffusion area (m^2)	3.92e-12	off
Drain diffusion periphery	16.98u M	off
Source diffusion periphery	16.98u M	off
Multiplier	1	off

更改Multiplier時，上面的數值皆不會更動，要自行計算Total Width

Layout View

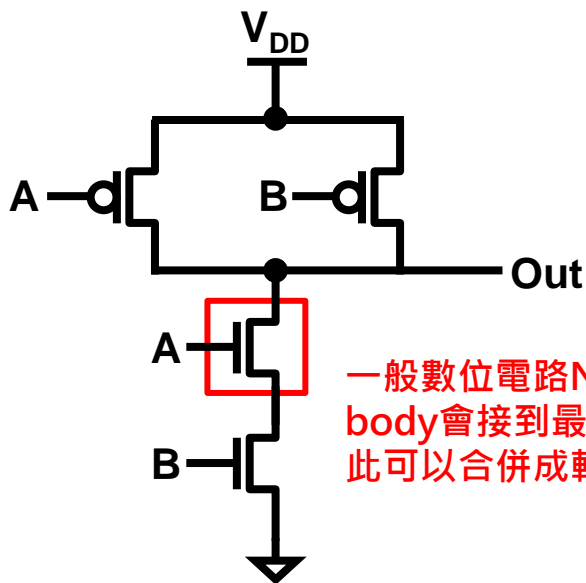
Parameters	
Model Name	n_18_mm
Total Width	8u M
Finger Width	8u M
Length	180.0n M
Finger Number	1

設定Layout所需的Finger Number



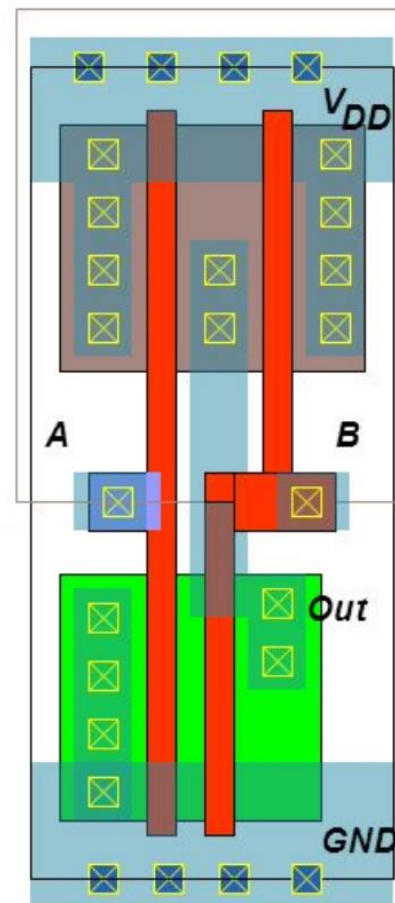
Layout

◆ Example: NAND layout



一般數位電路NMOS/PMOS的body會接到最高/最低電位，因此可以合併成較精簡的layout

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

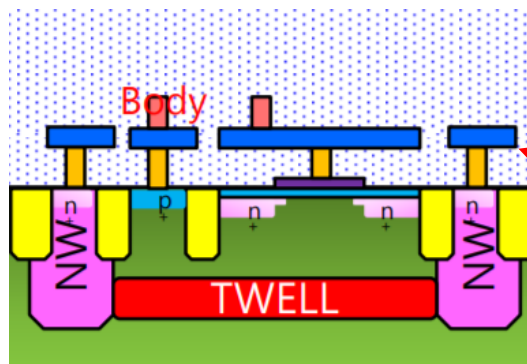
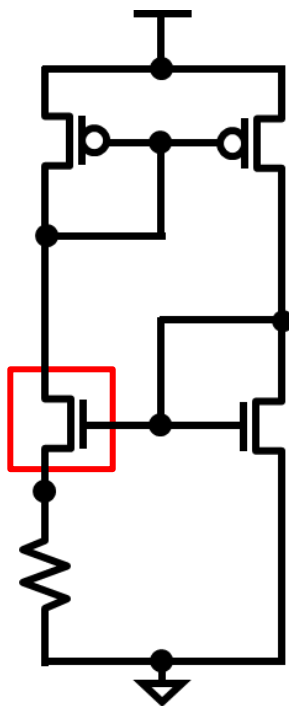


Reference: <http://2.zqwx.ffbayreuth-ost.de/kuy/figure-1-schematic-and-stick-diagram-of-a-two-inputnand-gate.html>

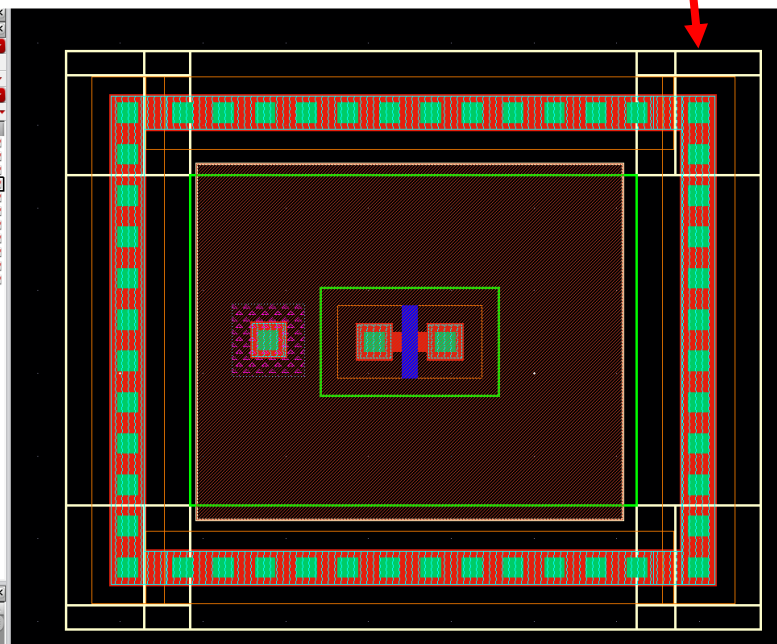
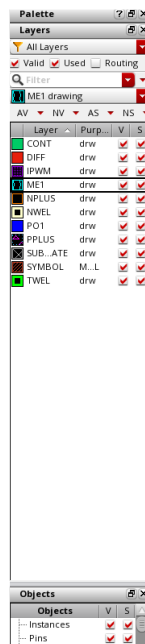


Layout

◆ Deep N-Well



N-Well接最高電位



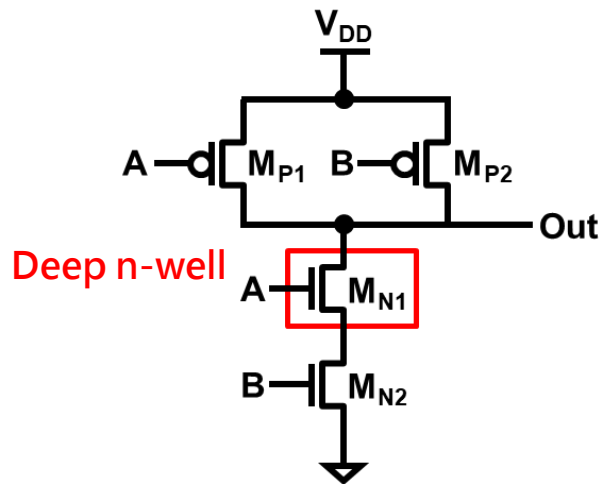
類比電路為了避免body effect造成的影響

$$V_{TH} = V_{TH0} + \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{2\Phi_F} \right)$$

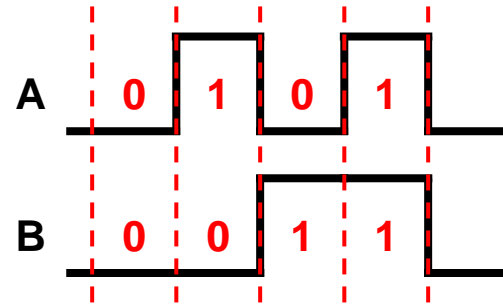
因此會將body接到source，而layout上則需加上deep n-well來區隔電位

Lab 2

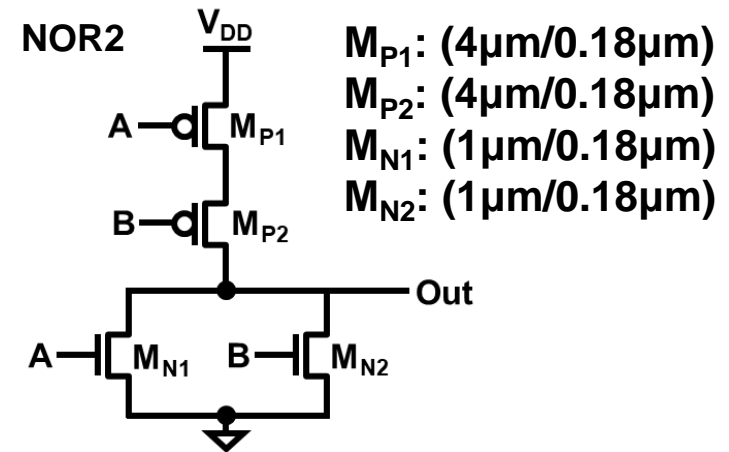
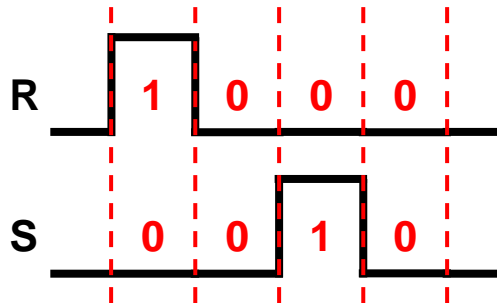
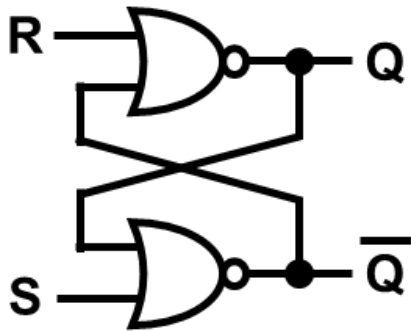
◆ NAND2



M_{P1} : ($2\mu\text{m}/0.18\mu\text{m}$)
 M_{P2} : ($2\mu\text{m}/0.18\mu\text{m}$)
 M_{N1} : ($2\mu\text{m}/0.18\mu\text{m}$)
 M_{N2} : ($2\mu\text{m}/0.18\mu\text{m}$)



◆ SR Latch



M_{P1} : ($4\mu\text{m}/0.18\mu\text{m}$)
 M_{P2} : ($4\mu\text{m}/0.18\mu\text{m}$)
 M_{N1} : ($1\mu\text{m}/0.18\mu\text{m}$)
 M_{N2} : ($1\mu\text{m}/0.18\mu\text{m}$)



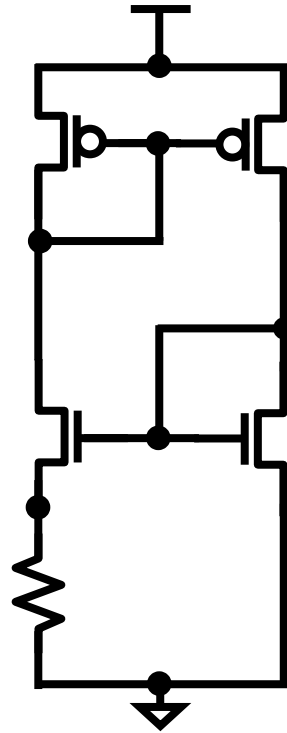
Current Reference Circuit

◆ Current Reference / Current Generator

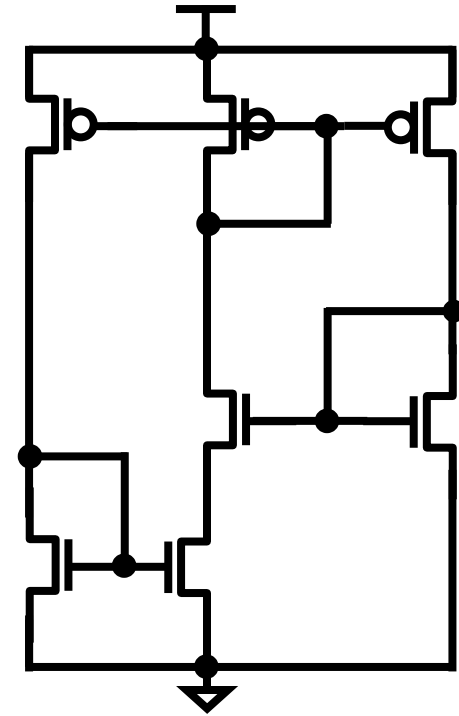
Ideal current reference



Constant- g_m
with Resistance

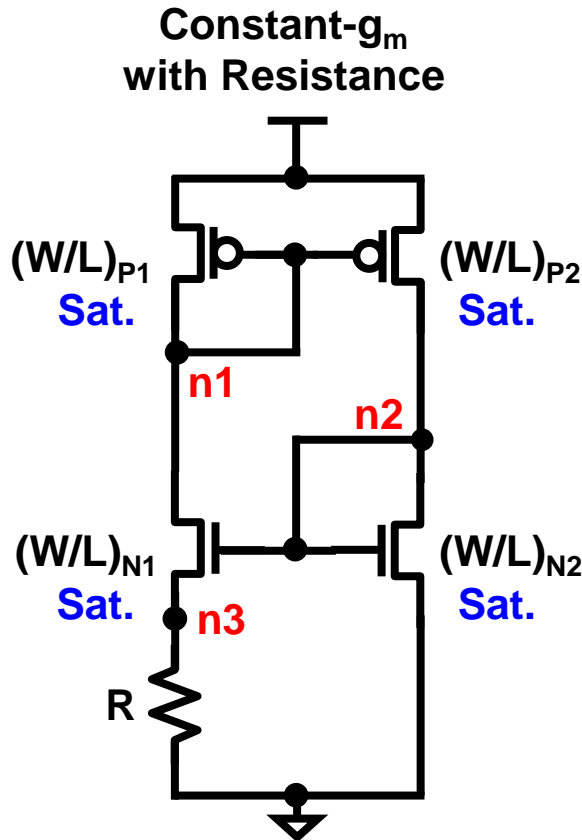


Constant- g_m
without Resistance



Current Reference Circuit

◆ Current Reference / Current Generator



$$(W/L)_{P1} = (W/L)_{P2}, (W/L)_{N1} = K(W/L)_{N2}, K > 1$$

$$V_{gs, MP1} = V_{gs, MP2} \text{ (} M_{P1} \text{ and } M_{P2} \text{ in Saturation Region)}$$

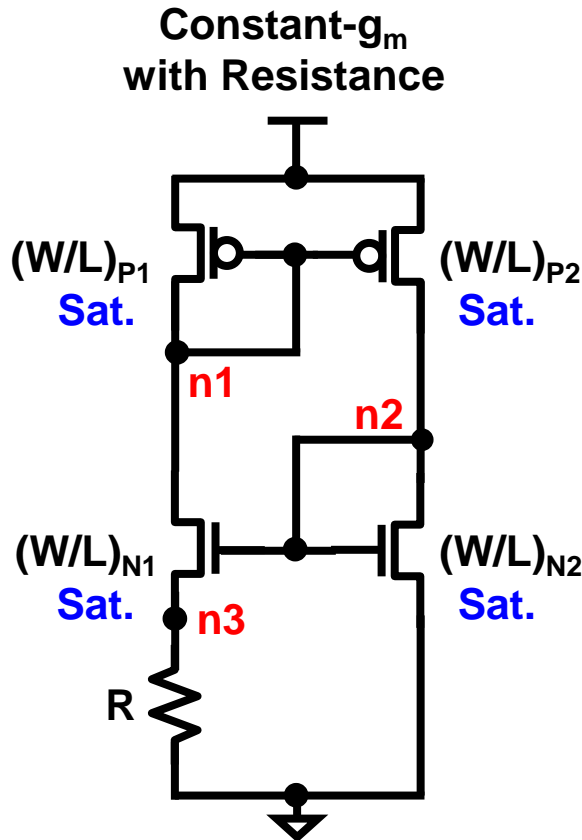
$$I_{ds, MP1} = I_{ds, MP2} = I_{ds, MN1} = I_{ds, MN2} = I_{REF}$$

$$V_{gs, MN1} + I_{ds, MN1} * R = V_{gs, MN2}$$

$$(I_{ds, sat} = \frac{1}{2} \mu C_{ox} \frac{W}{L} V_{ov}^2, V_{ov} = V_{gs} - V_{th})$$

Current Reference Circuit

◆ Current Reference / Current Generator



$$V_{th, MN1} + \left(\frac{2I_{REF}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N1}} \right)^{1/2} + I_{REF} * R = V_{th, MN2} + \left(\frac{2I_{REF}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N2}} \right)^{1/2}$$

$$I_{REF} * R = \left(\frac{2I_{REF}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N2}} \right)^{1/2} - \left(\frac{2I_{REF}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N1}} \right)^{1/2}$$

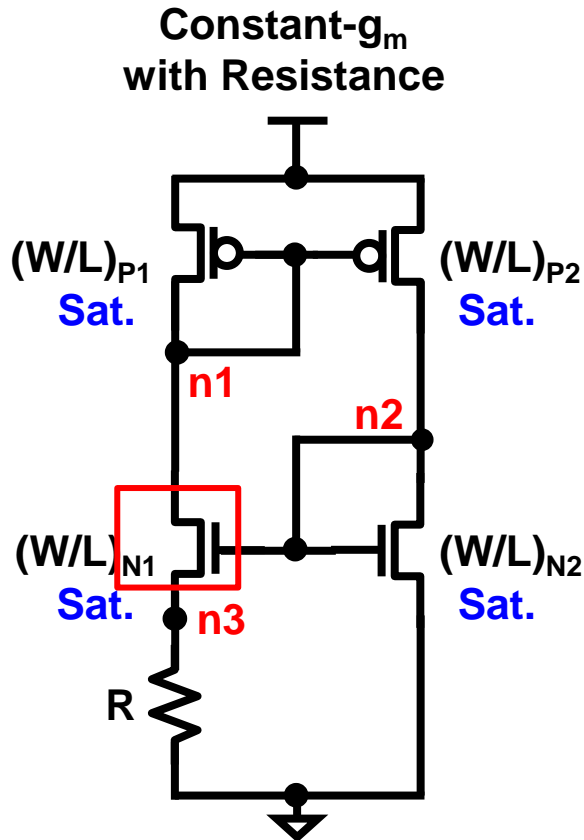
$$I_{REF} * R = \left(1 - \frac{1}{\sqrt{K}} \right) \left(\frac{2I_{REF}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N2}} \right)^{1/2}$$

$$I_{REF} * R^2 = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N2}} \left(1 - \frac{1}{\sqrt{K}} \right)^2$$

$$I_{REF} = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L} \right)_{N2}} \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2$$

Current Reference Circuit

◆ Current Reference / Current Generator



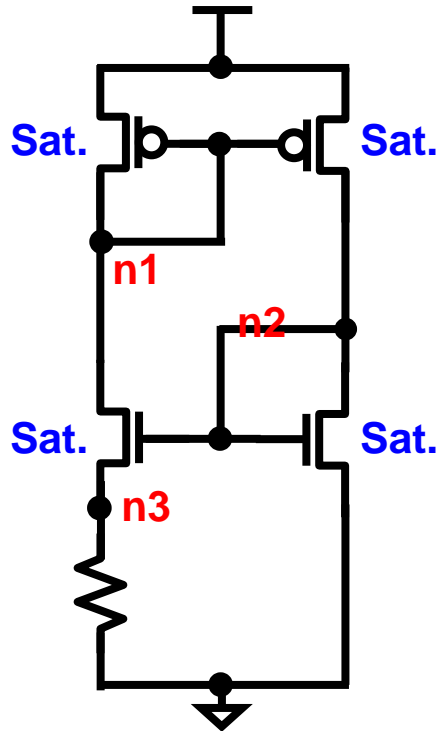
$$V_{TH} = VT_{H0} + \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{2\Phi_F} \right)$$

$$\Phi_F = \left(\frac{kT}{q} \right) \ln \left(\frac{N_{SUB}}{n_i} \right)$$

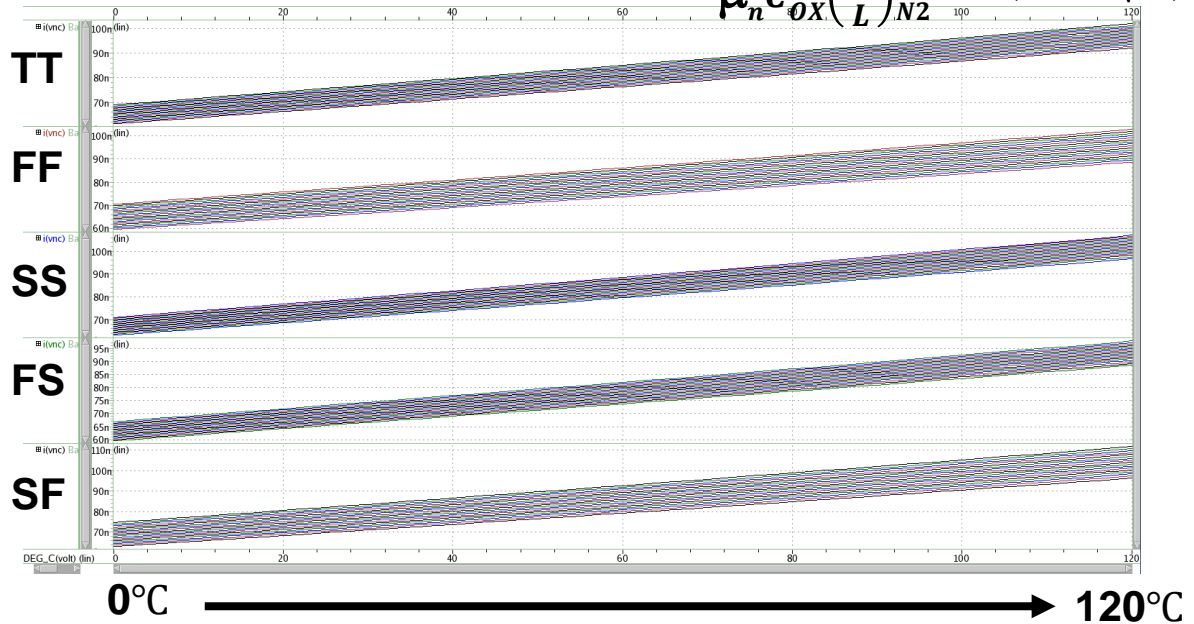
The body of N₁ needs to be connected to n₃ for the cancellation of V_{TH} .

Current Reference Circuit

◆ Constant- g_m with Resistance



$$I_{REF} = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{N2}} \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$



Corner	TT	FF	SS	FS	SF
$I_{D,0^\circ C}$ (@ $V_{DD}=1$ V)	61	60	63	60	63
$I_{D,120^\circ C}$ (@ $V_{DD}=1$ V)	92	89	97	86	96
$I_{D,0^\circ C}$ (@ $V_{DD}=1.8$ V)	69	71	71	67	75
$I_{D,120^\circ C}$ (@ $V_{DD}=1.8$ V)	102	103	107	98	112

The magnitude of mobility is complimentary to absolute temperature



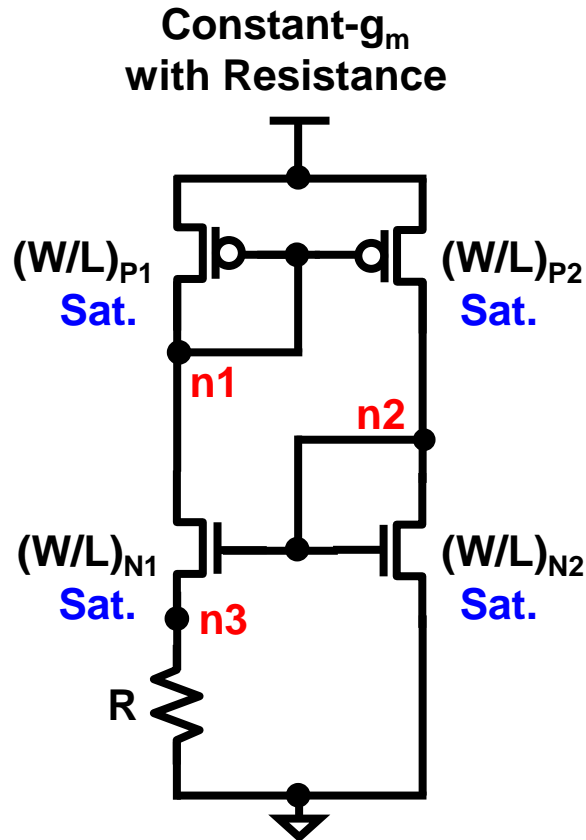
◆ Current Reference / Current Generator



- 

Current Reference Circuit

◆ Current Reference / Current Generator



- 特別留意

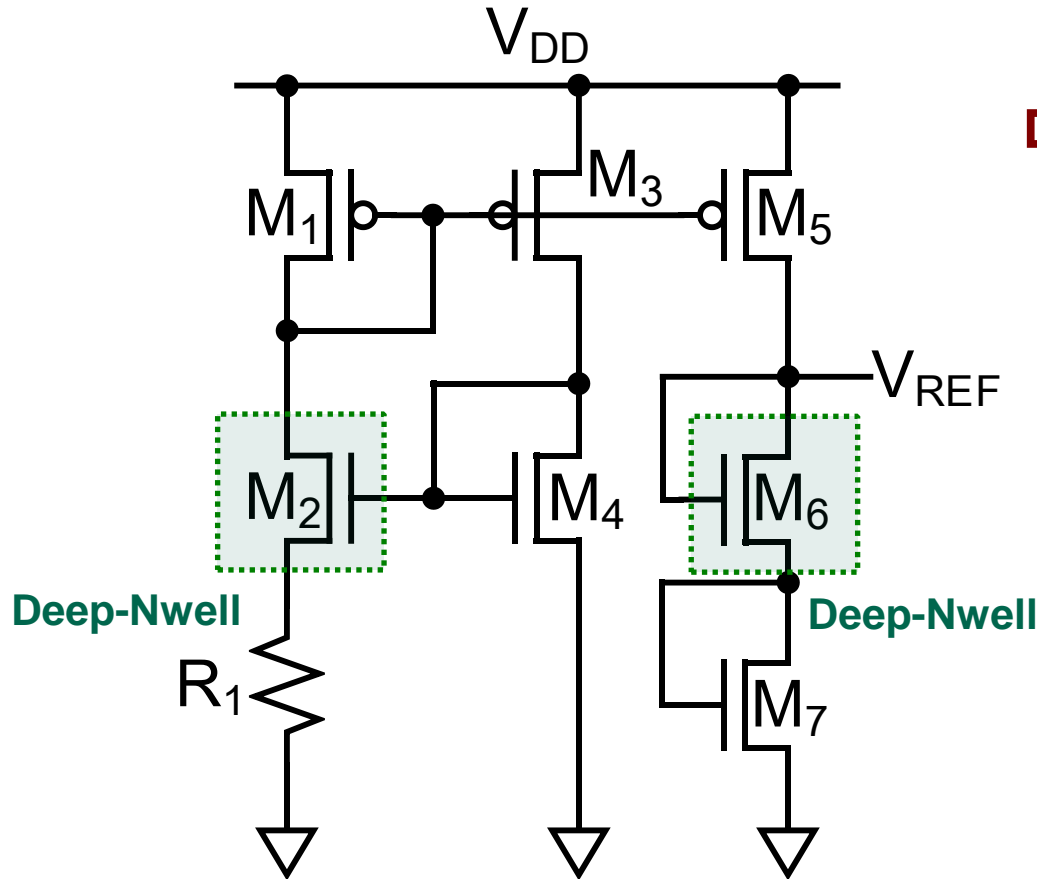
決定MOSFET操作在Saturation region與否，與drain電壓有關， $n2$ 太高、 $n1$ 太低，將使 M_{N1} 及 M_{P2} 進入Triode region。

調整參數過程需考慮到layout時的對稱性， M_{N1} 及 M_{N2} 的width和length相同，應改變 m (或finger)數來調整total width而非改變width大小。

跑dc若發現電路沒有正常運作，可在 $n1$ 到 $n2$ 之間，接一或多個diode-connected的MOS，但**不可讓MOS導通**。(不可給initial condition)

HW 2

◆ Architecture and specification



□ Constant g_m :

M_1 : $(4\mu\text{m}/0.5\mu\text{m}) * 12$

M_2 : $(1\mu\text{m}/0.5\mu\text{m}) * 4$

M_3 : $(4\mu\text{m}/0.5\mu\text{m}) * 12$

M_4 : $(1\mu\text{m}/0.5\mu\text{m})$

M_5 : $(4\mu\text{m}/0.5\mu\text{m}) * 12$

M_6 : $(? \mu\text{m}/0.5\mu\text{m})$

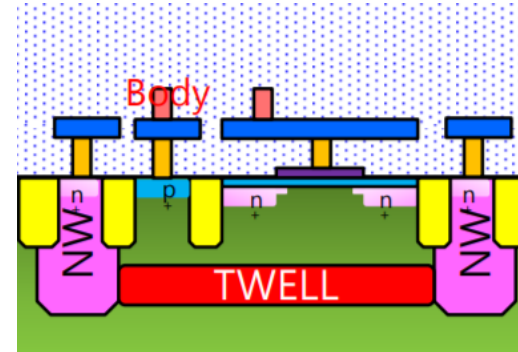
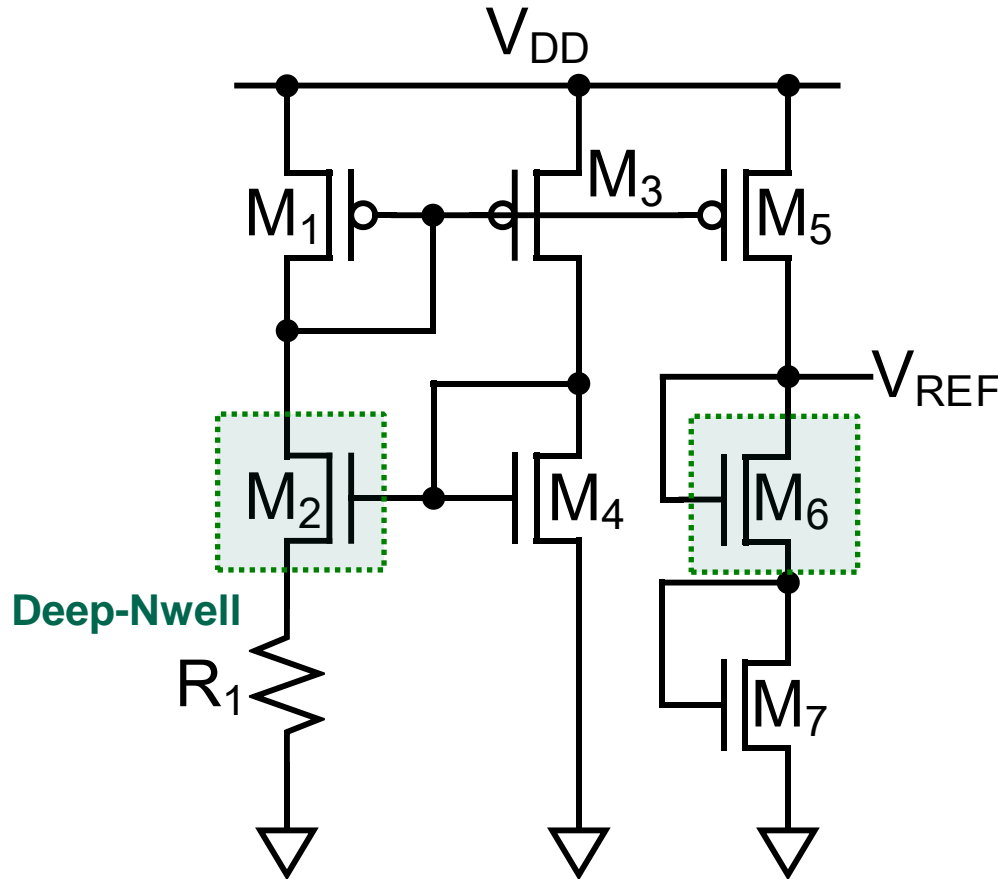
M_7 : $(? \mu\text{m}/0.5\mu\text{m})$

R_1 : ? $\text{K}\Omega$ [RNNPO_MM]

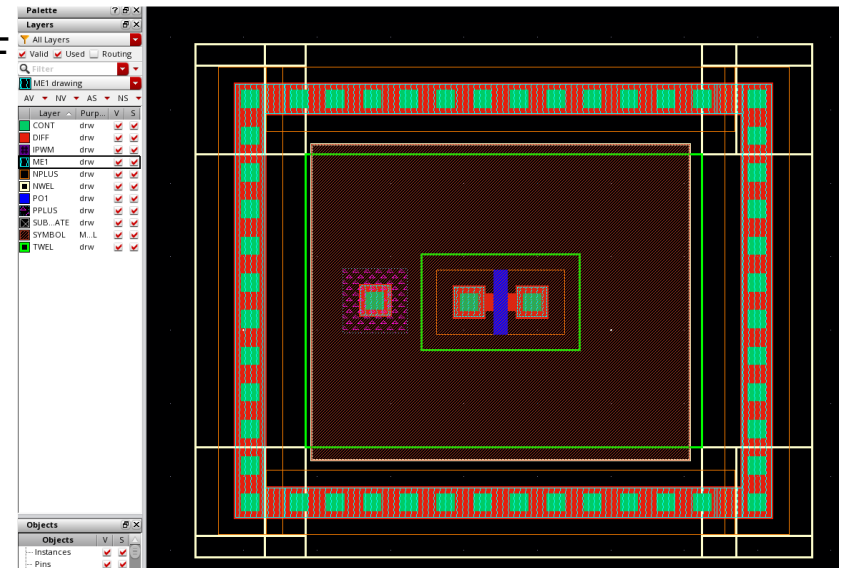
➤ All bodies of NMOS and PMOS are connected to source.

HW 2

◆ Layout Concern



N-Well接最高電位



➤ All bodies of NMOS and PMOS are connected to source.



HW 2

◆ Specifications

Parameters	Target spec.		Pre-sim.	Post-sim.
V_{REF}	1.2V (+/- 1%) @ $V_{DD}=1.8V$	Value (V)		
		Error (%)		
V_{REF}	1.2V (+/- 1%) @ $V_{DD}=1.7V-1.9V$	Value (V)		
		Error (%)		
I_{REF}	10 μ A (+/- 1%) @ $V_{DD}=1.8V$	Value (V)		
		Error (%)		
I_{REF}	10 μ A (+/- 5%) @ $V_{DD}=1.7V-1.9V$	Value (V)		
		Error (%)		
P_{VDD}	<150uW @ $V_{DD}=1.8V$	Power (uW)		

誤差計算方式如下：
$$\frac{V_{REF} - 1.2}{1.2} \times 100\%$$



HW 2

- 繳交一份電子檔。
- 請在報告中加入**Pre-sim.**和**Post-sim.**模擬結果，**Layout**圖，**DRC**及**LVS**結果。報告中的波形圖請改用白底，並將線條加粗。
- **Pre-sim.**和**Post-sim.**模擬結果需包括 V_{REF} (和 I_{REF})對 V_{DD} (1.7V~1.9V)的圖，以及 V_{REF} (和 I_{REF})對溫度(0°C~120°C)的圖($V_{DD}=1.8V$)。
- 並請於報告中簡單說明 M_6/M_7 及 R_1 尺寸設計的考量
- 作業繳交時間為**2023/08/07(一)晚上12點前**，請將作業報告上傳至e3

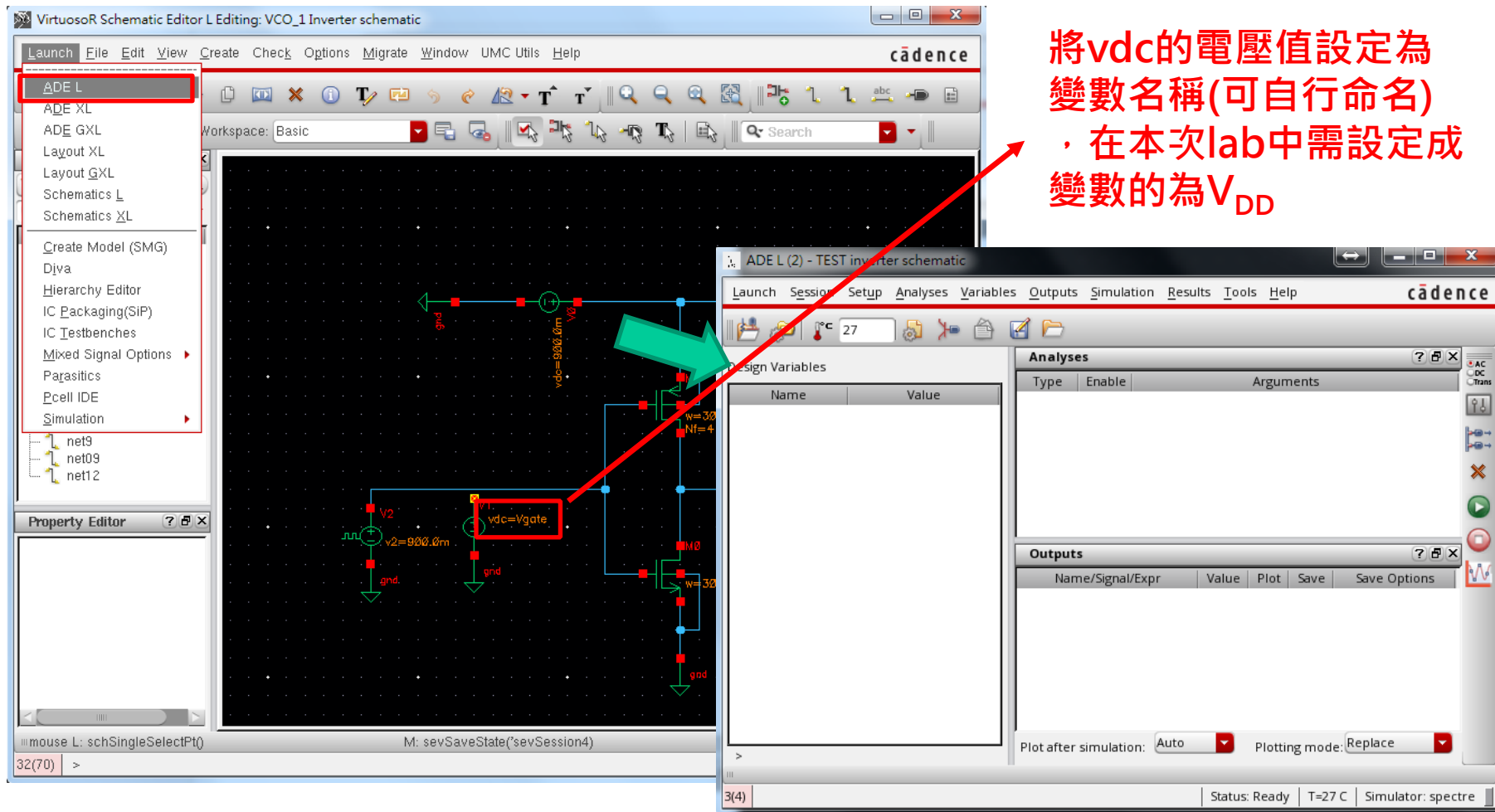


Thanks for your attention !



DC simulation (1)

- 開啟Analog Design Environment視窗



將vdc的電壓值設定為變數名稱(可自行命名)
，在本次lab中需設定成變數的為 V_{DD}

ADE L (2) - TEST inverter schematic

Name	Value
------	-------

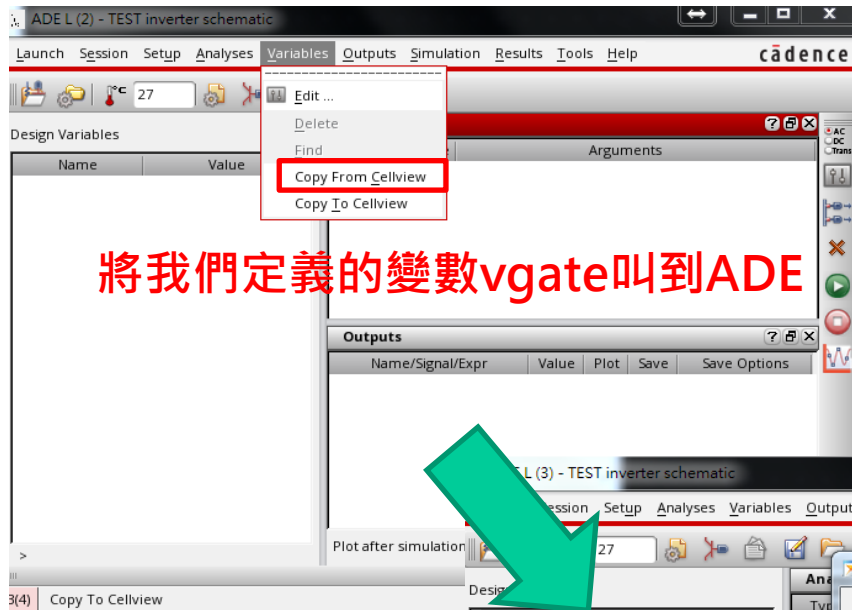
Type	Enable	Arguments
------	--------	-----------

Name/Signal/Expr	Value	Plot	Save	Save Options
------------------	-------	------	------	--------------

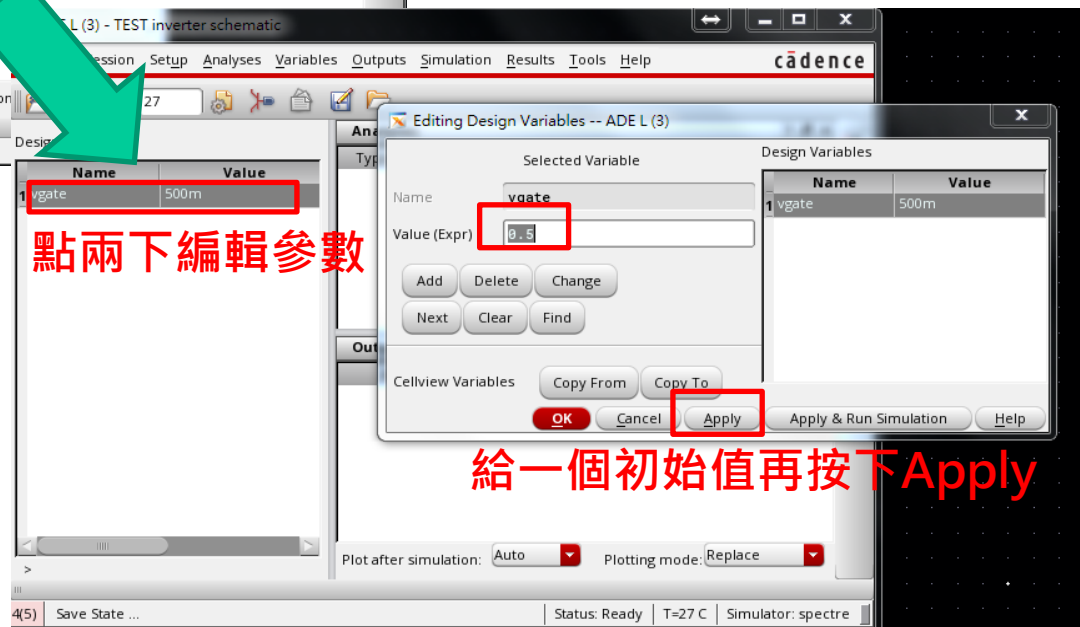
Plot after simulation: Auto Plotting mode: Replace

Status: Ready T=27 C Simulator: spectre

DC simulation (2)



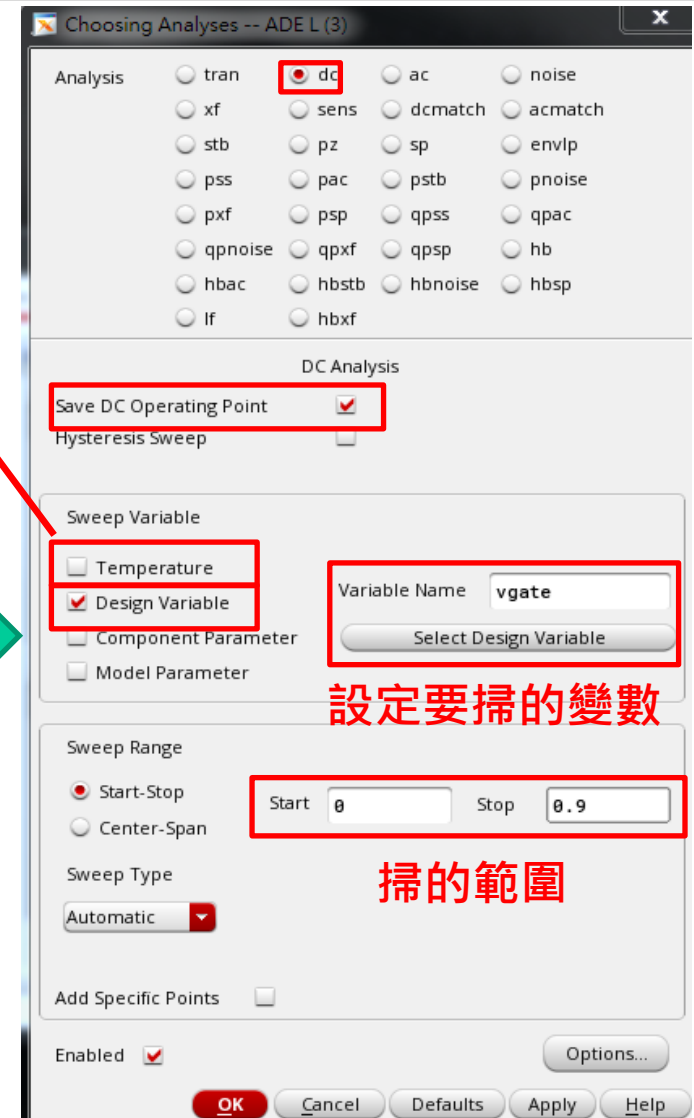
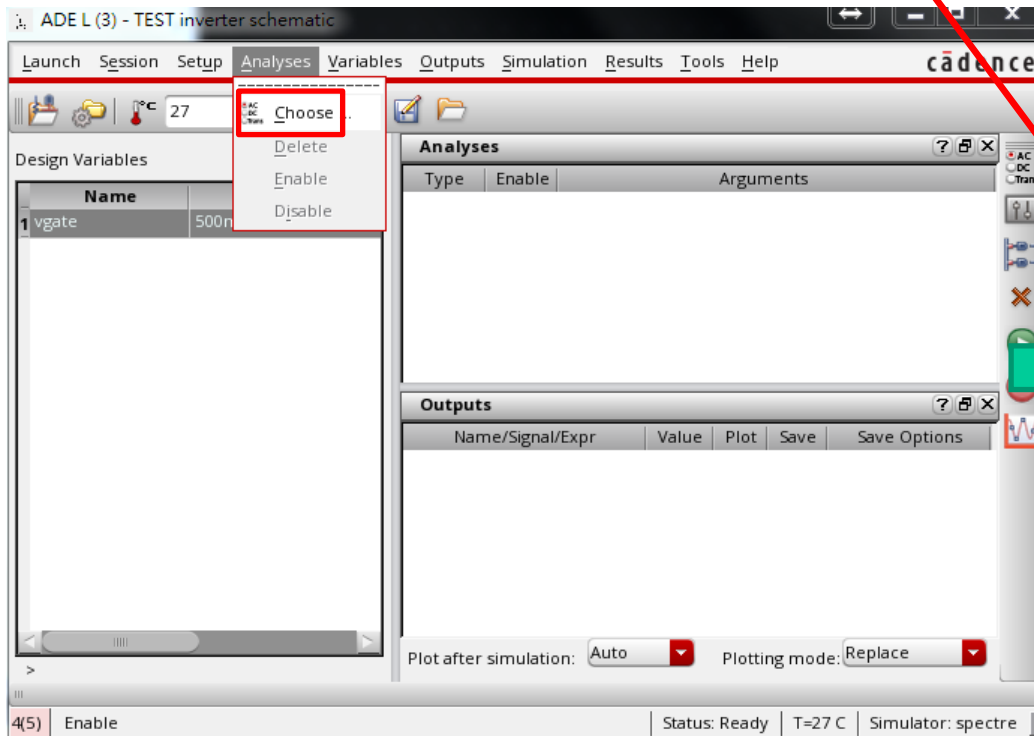
點兩下編輯參數



DC simulation (3)

- 選擇DC analysis

若要sweep溫度則勾選Temperature，接著設定要掃的溫度範圍



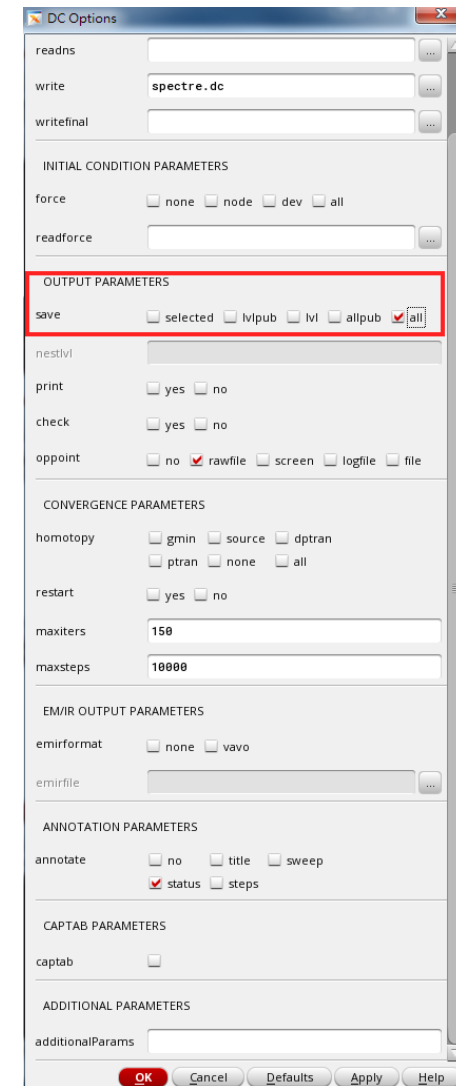
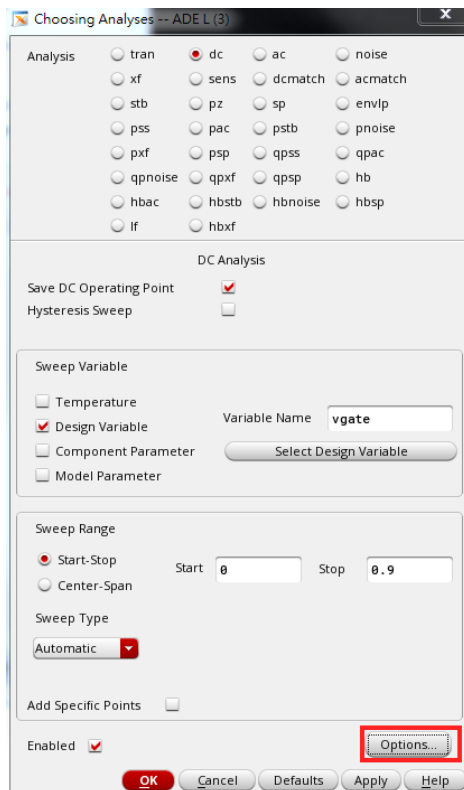
設定要掃的變數

掃的範圍



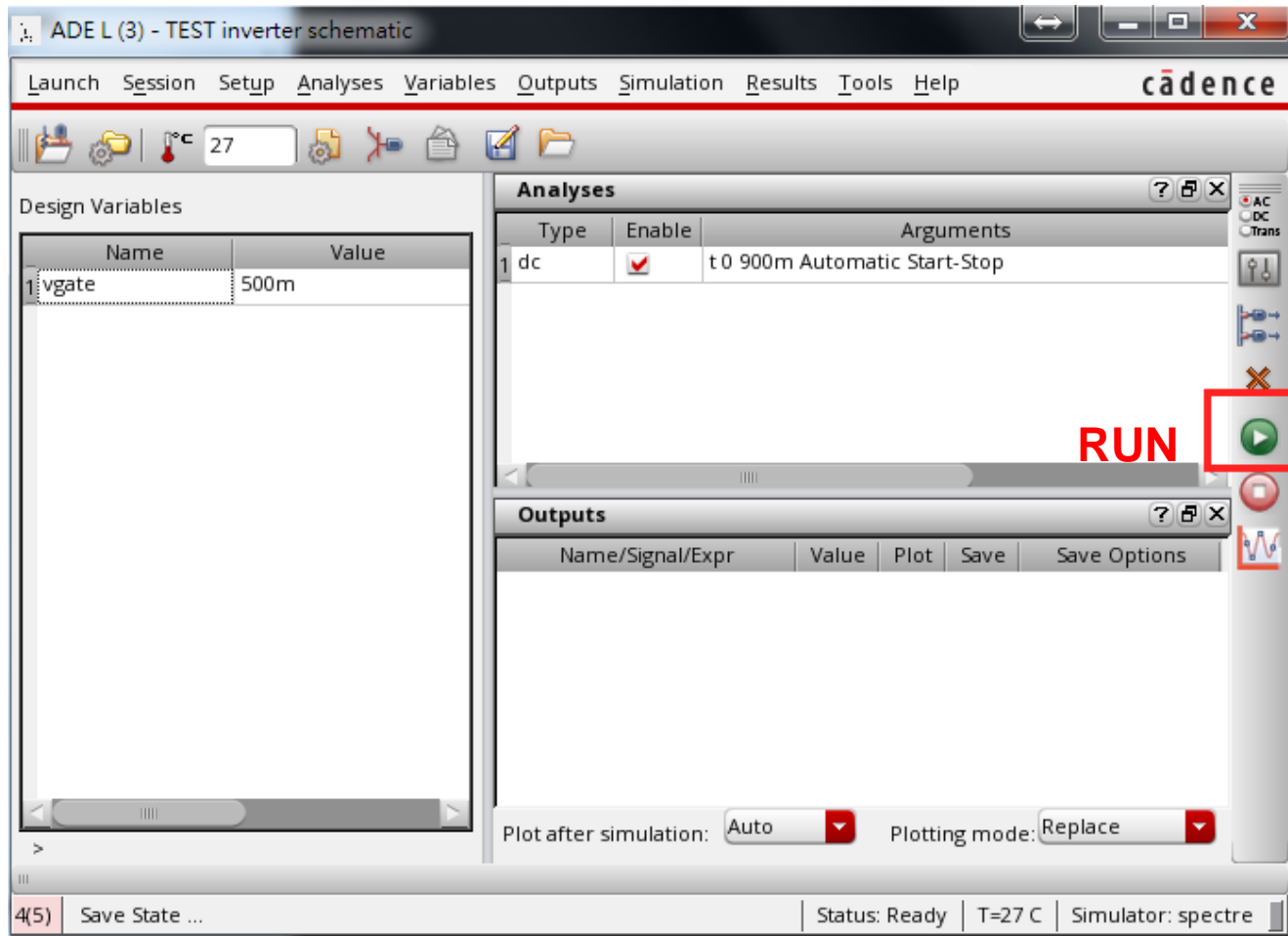
DC simulation (4)

- 如果要看component的parameter，要在option裡面點output parameter選all (若電路複雜度較高，通常不會選擇all，因為會佔用太多硬碟容量)



DC simulation (5)

- 設定好就可以按netlist and run開始跑模擬



DC simulation (6)

- Output log

```

/home/RAID2/COURSE/aiclab/aiclabta05/simulation/inverter/spect...
File Edit View Help cadence
dc: vgate = 594e-03 (66 %), step = 18e-03 (2 %)
dc: vgate = 612e-03 (68 %), step = 18e-03 (2 %)
dc: vgate = 630e-03 (70 %), step = 18e-03 (2 %)
dc: vgate = 648e-03 (72 %), step = 18e-03 (2 %)
dc: vgate = 666e-03 (74 %), step = 18e-03 (2 %)
dc: vgate = 684e-03 (76 %), step = 18e-03 (2 %)
dc: vgate = 702e-03 (78 %), step = 18e-03 (2 %)
dc: vgate = 720e-03 (80 %), step = 18e-03 (2 %)
dc: vgate = 738e-03 (82 %), step = 18e-03 (2 %)
dc: vgate = 756e-03 (84 %), step = 18e-03 (2 %)
dc: vgate = 774e-03 (86 %), step = 18e-03 (2 %)
dc: vgate = 792e-03 (88 %), step = 18e-03 (2 %)
dc: vgate = 810e-03 (90 %), step = 18e-03 (2 %)
dc: vgate = 828e-03 (92 %), step = 18e-03 (2 %)
dc: vgate = 846e-03 (94 %), step = 18e-03 (2 %)
dc: vgate = 864e-03 (96 %), step = 18e-03 (2 %)
dc: vgate = 882e-03 (98 %), step = 18e-03 (2 %)
dc: vgate = 900e-03 (100 %), step = 18e-03 (2 %)
DC simulation time: CPU = 256.96 ms, elapsed = 2.89886 s.
Total time required for 'dc analysis -dc': CPU = 4.999 ms, elapsed = 11.
Time accumulated: CPU = 257.96 ms, elapsed = 2.90254 s.
Peak resident memory used = 42.6 Mbytes.

modelParameter: writing model parameter values to rawfile.

Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.

Opening the PSF file ../psf/element.info ...
outputParameter: writing output parameter values to rawfile.

Opening the PSF file ../psf/outputParameter.info ...
designParamVals: writing netlist parameters to rawfile.

Opening the PSFASCII file ../psf/designParamVals.info ...
primitives: writing primitives to rawfile.

Opening the PSFASCII file ../psf/primitives.info.primitives ...
subckts: writing subcircuits to rawfile.

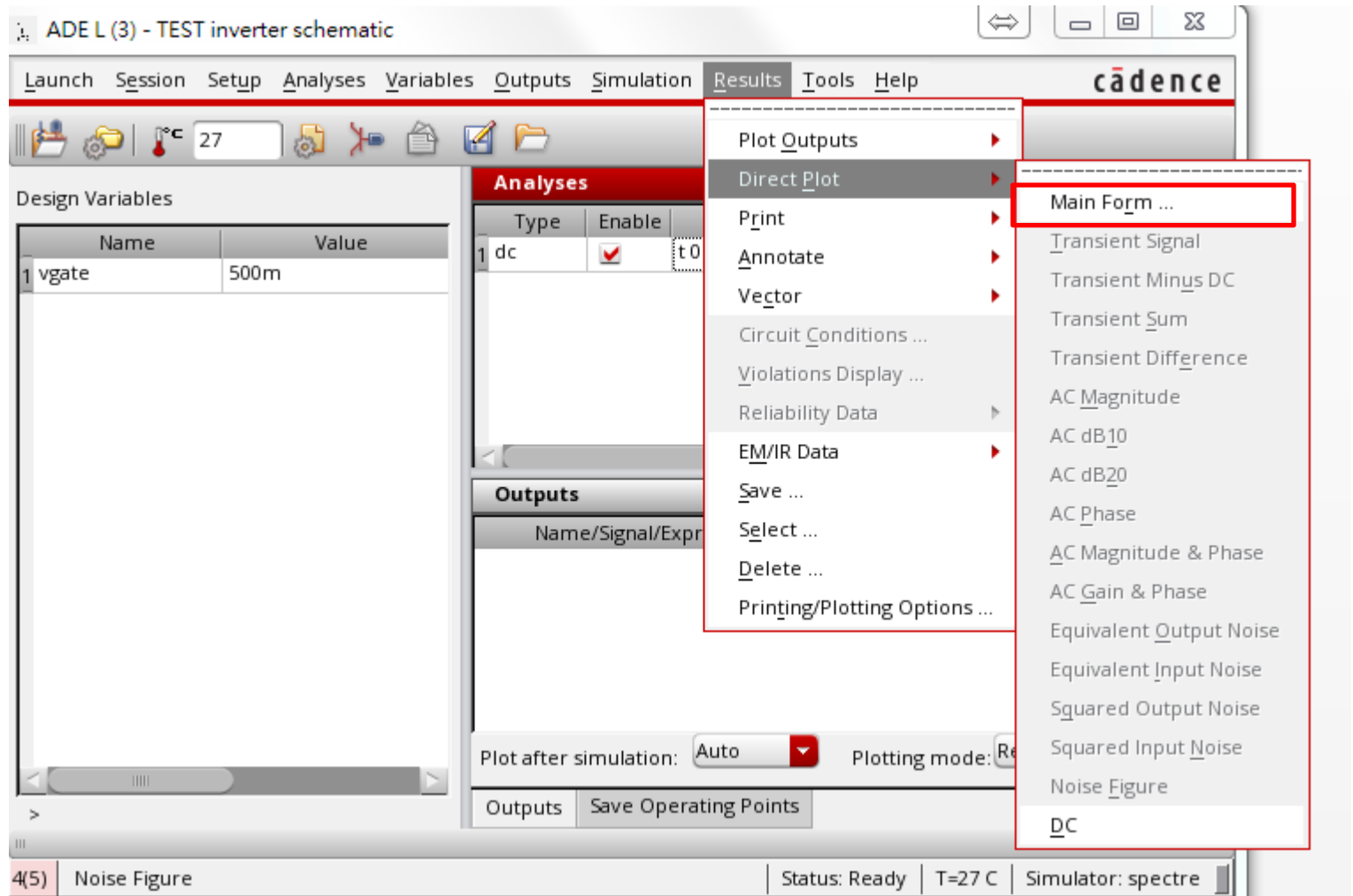
Opening the PSFASCII file ../psf/subckts.info.subckts ...
4 > L297 C58
```

跑完了

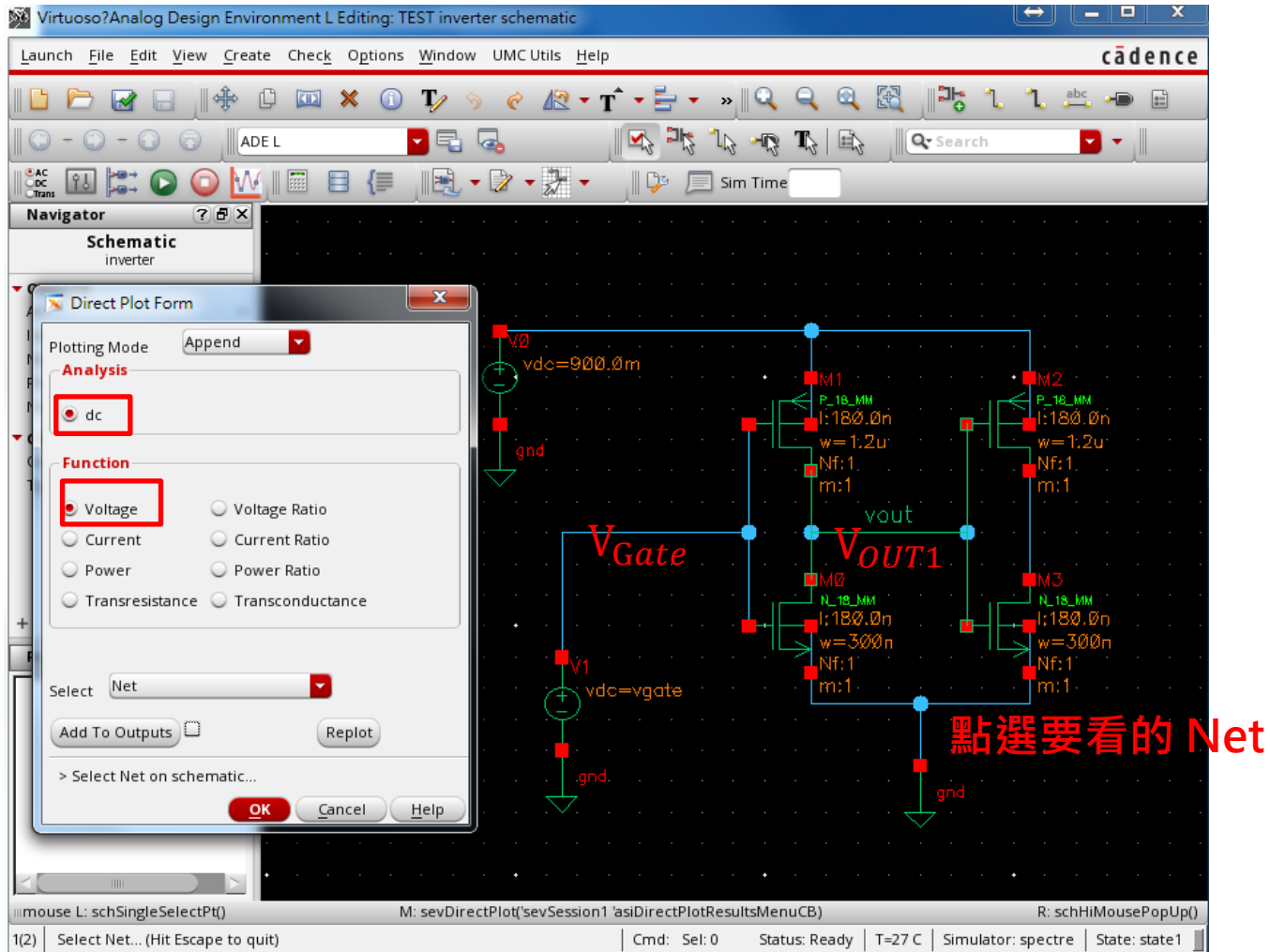


DC simulation (7)

查看模擬結果

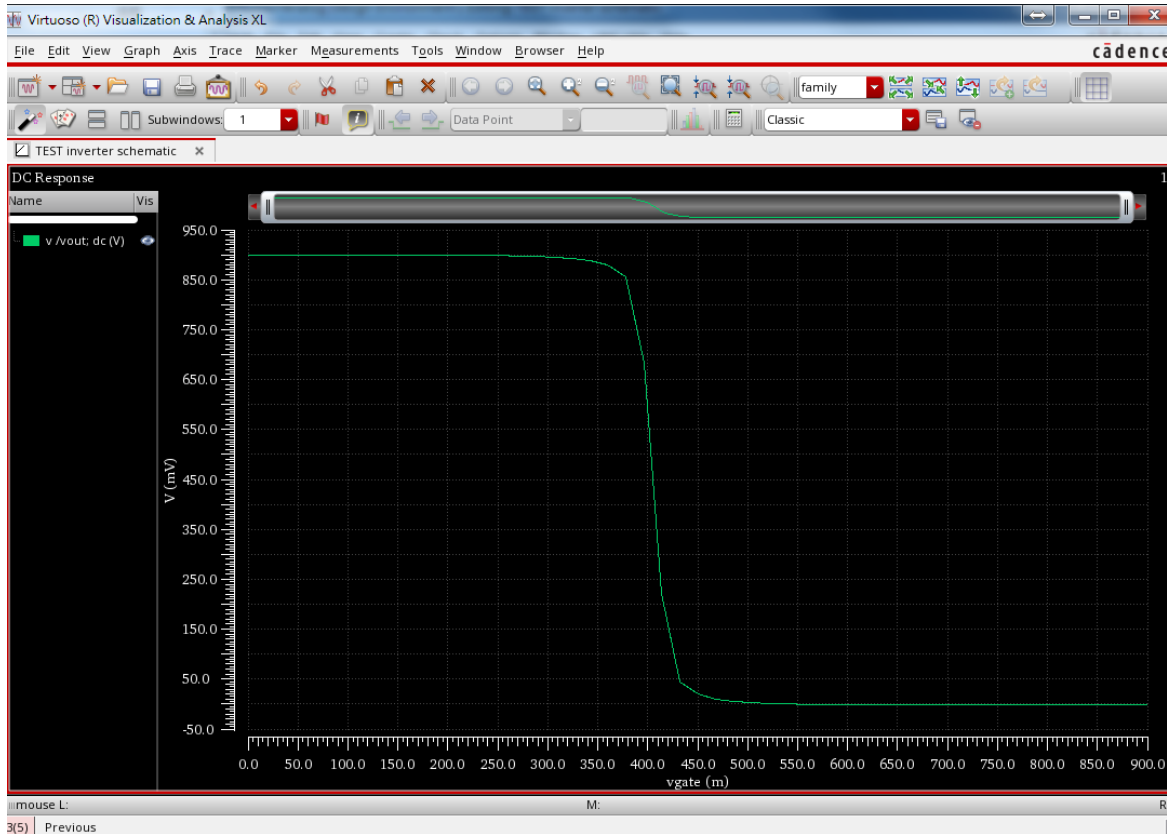


DC simulation (8)



DC simulation (9)

DC Transfer Curve



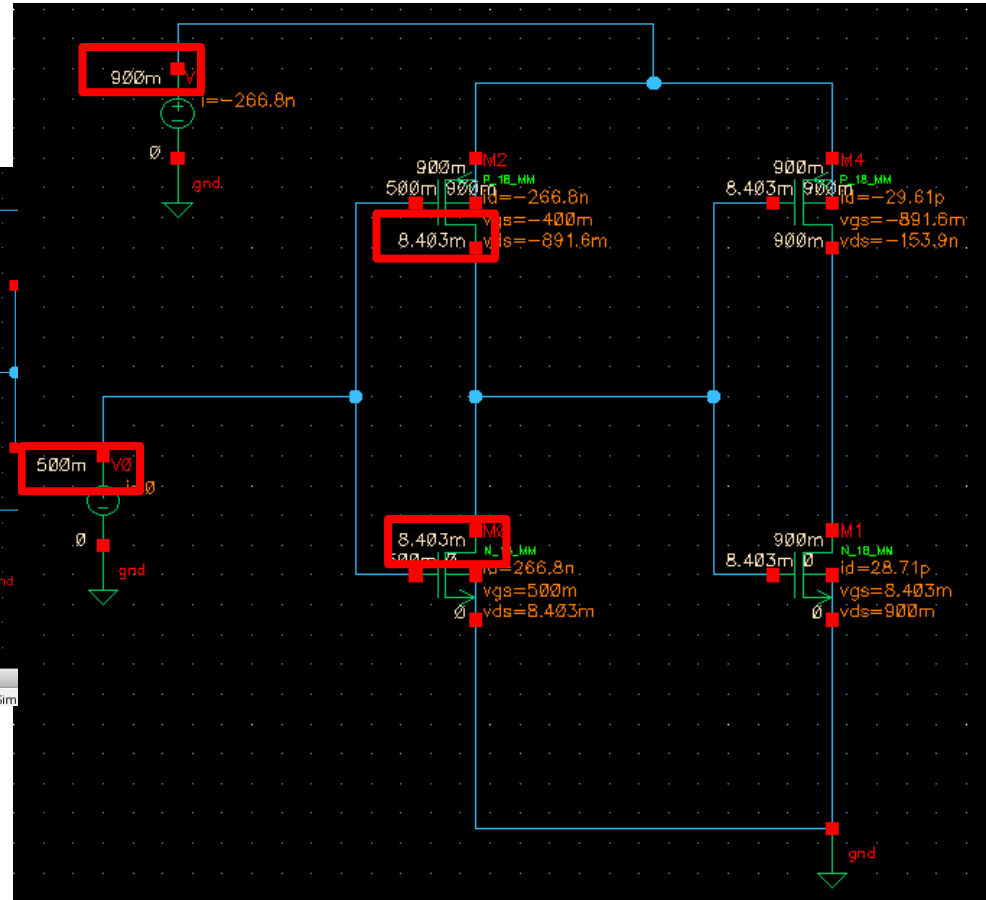
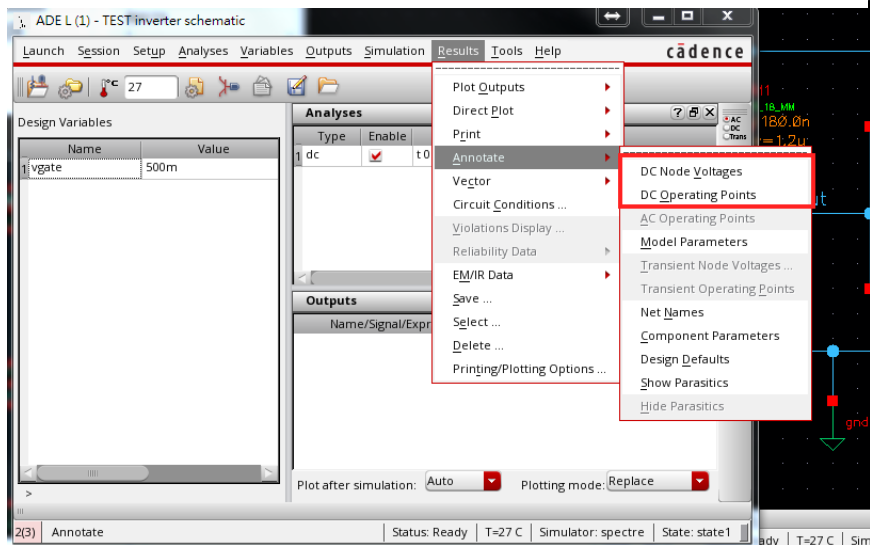
更改背景顏色:
Graph → Edit
→ Foreground/Background

加入marker:
Marker → Place
→ Trace Marker (t)



DC simulation (10)

- 選擇DC Node Voltage以及DC Operating Points可以將目前的DC 操作電壓或電流標示在schematic



DC simulation (11)

- 利用Results Browser去看device的參數

