電源管理晶片設計與實作

Lab 2

Layout Skills & Constant-gm

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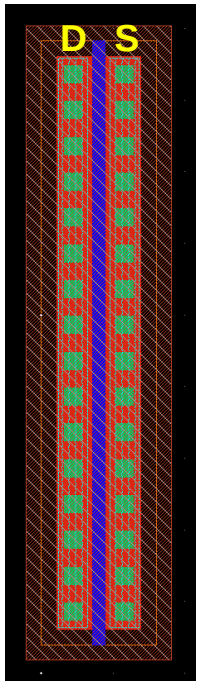
August 1st, 2023

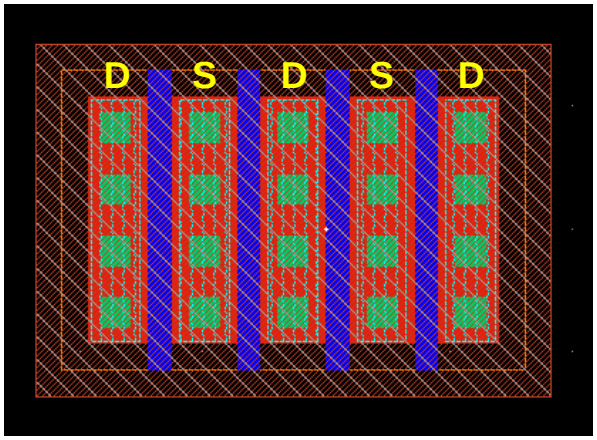
National Yang Ming Chiao Tung University

Finger Number

◆Single Finger / Multiple Fingers



更改Finger Number時，Finger Width會自動計算為Total Width/Finger Number



Total Width = 8um
Finger Width = 8um
L = 180nm
Finger Number = 1

Total Width = 8um
Finger Width = 2um
L = 180nm
Finger Number = 4

Schematic View

CDF Parameter	Value	Display
Model Name	n_18_mm	off
Total Width	8u M	off
Finger Width	8u M	off
Length	180.0n M	off
Finger Number	1	off
mis_flag	1	off
Source Drain Metal Width	400.0n M	off
AD AS PD PS Editable		off
Drain diffusion area (m^2)	3.92e-12	off
Source diffusion area (m^2)	3.92e-12	off
Drain diffusion periphery	16.98u M	off
Source diffusion periphery	16.98u M	off
Multiplier	1	off

更改Multiplier時，上面的數值皆不會更動，要自行計算Total Width

Layout View

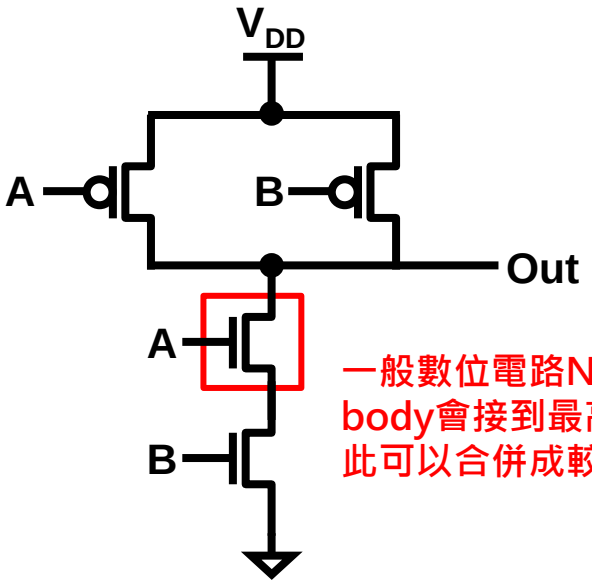
Parameters

Model Name	n_18_mm
Total Width	8u M
Finger Width	8u M
Length	180.0n M
Finger Number	1

設定Layout所需的Finger Number

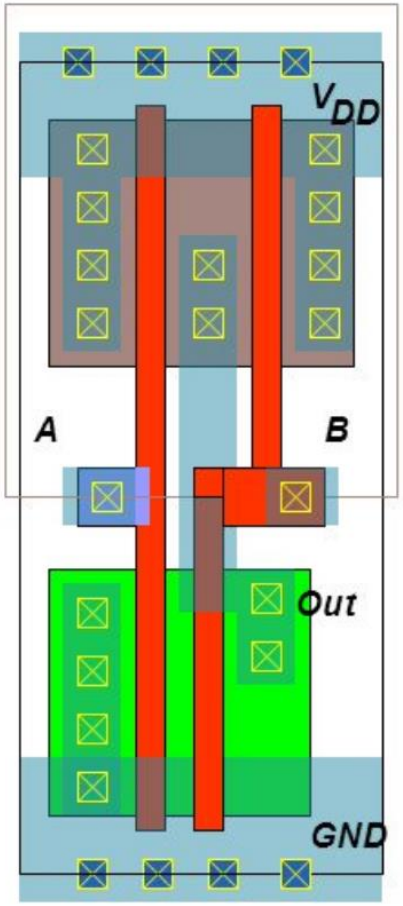
Layout

◆Example: NAND layout



一般數位電路NMOS/PMOS的body會接到最高/最低電位，因此可以合併成較精簡的layout

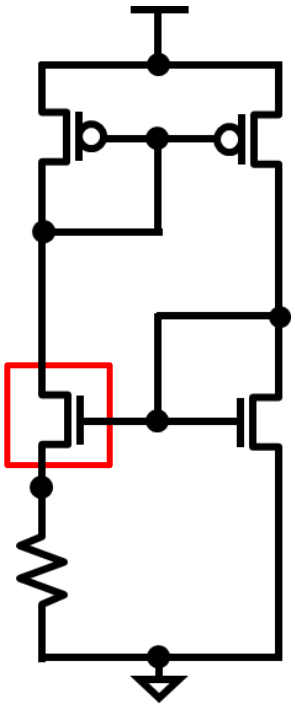
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

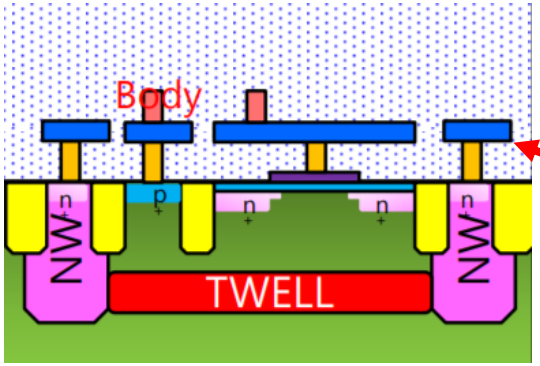


Reference: http://2.zqxw.ffbayreuth-ost.de/kuy/figure-1-schematic-and-stick-diagram-of-a-two-inputnand-gate.html

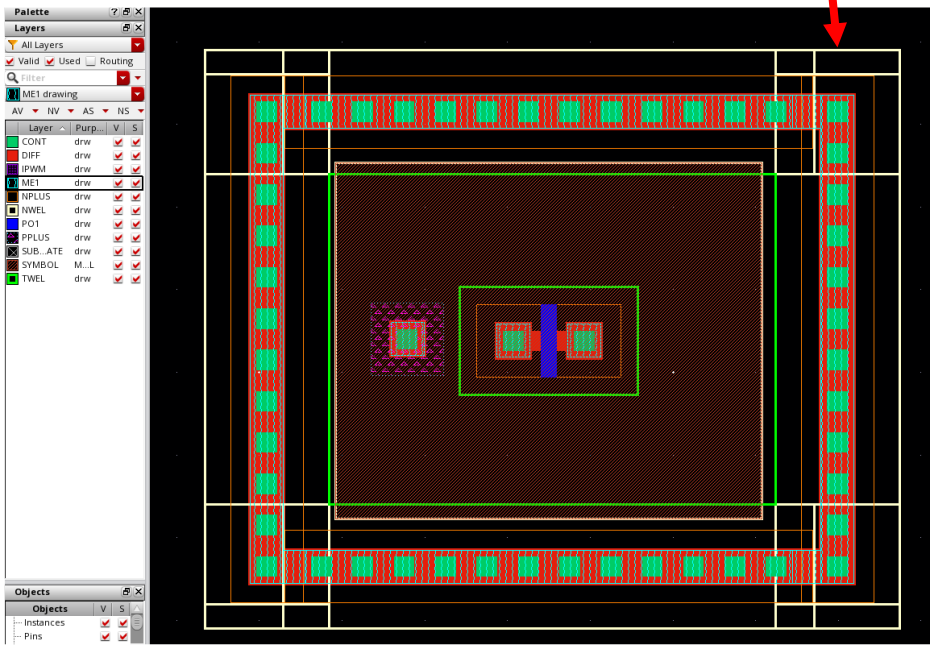
Layout

◆Deep N-Well





N-Well接最高電位



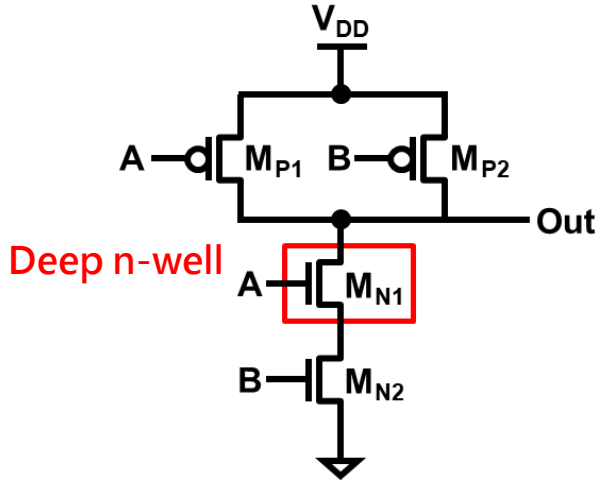
類比電路為了避免body effect造成的影響

$$V_{TH} = VTH_0 + \left(\sqrt{|2\Phi_F + VSB|} - \sqrt{2\Phi_F}\right)$$

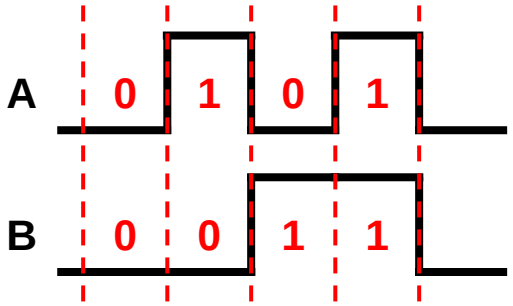
因此會將body接到source，而layout上則需加上deep n-well來區隔電位

Lab 2

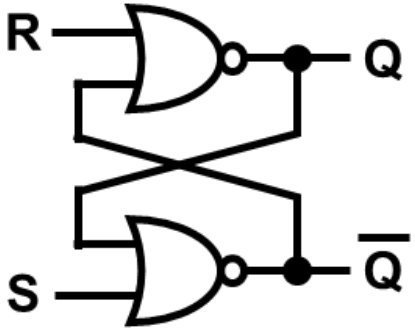
◆NAND2

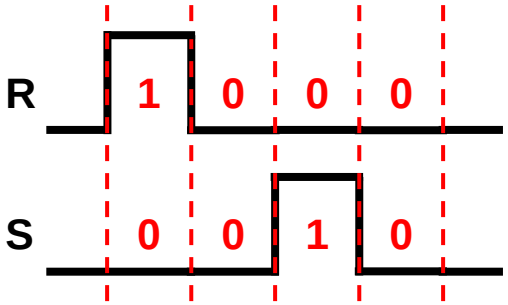


M_{P1}: (2μm/0.18μm)
M_{P2}: (2μm/0.18μm)
M_{N1}: (2μm/0.18μm)
M_{N2}: (2μm/0.18μm)

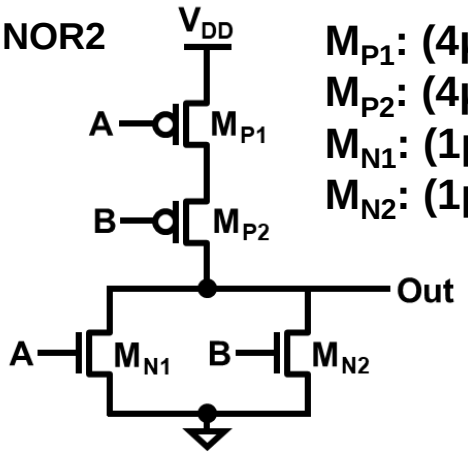


◆SR Latch





NOR2



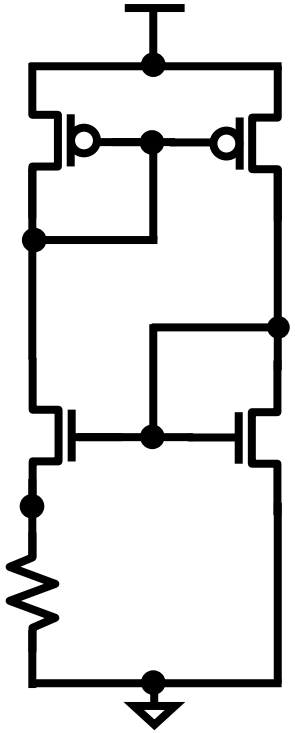
M_{P1}: (4μm/0.18μm)
M_{P2}: (4μm/0.18μm)
M_{N1}: (1μm/0.18μm)
M_{N2}: (1μm/0.18μm)

Current Reference Circuit

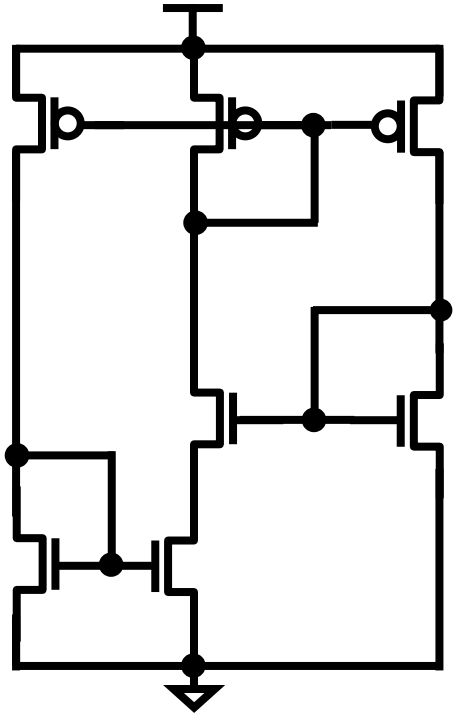
◆Current Reference / Current Generator

Ideal current reference

Constant-g_m with Resistance

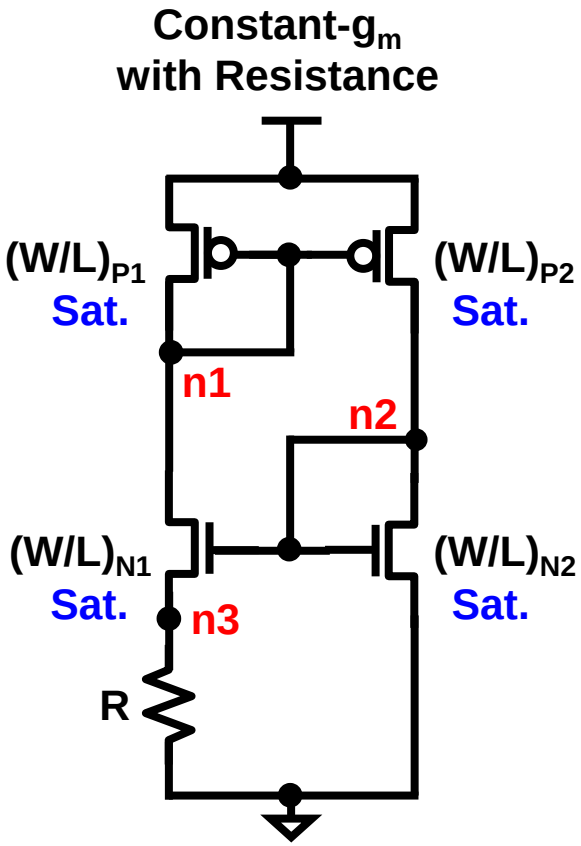


Constant-g_m without Resistance



Current Reference Circuit

◆Current Reference / Current Generator



$$(W/L)_{P1} = (W/L)_{P2}\,,\ (W/L)_{N1} = K^*(W/L)_{N2}\,,\ K>1$$

$V_{gs,\,MP1} = V_{gs,\,MP2}$ (M_{P1} and M_{P2} in Saturation Region)

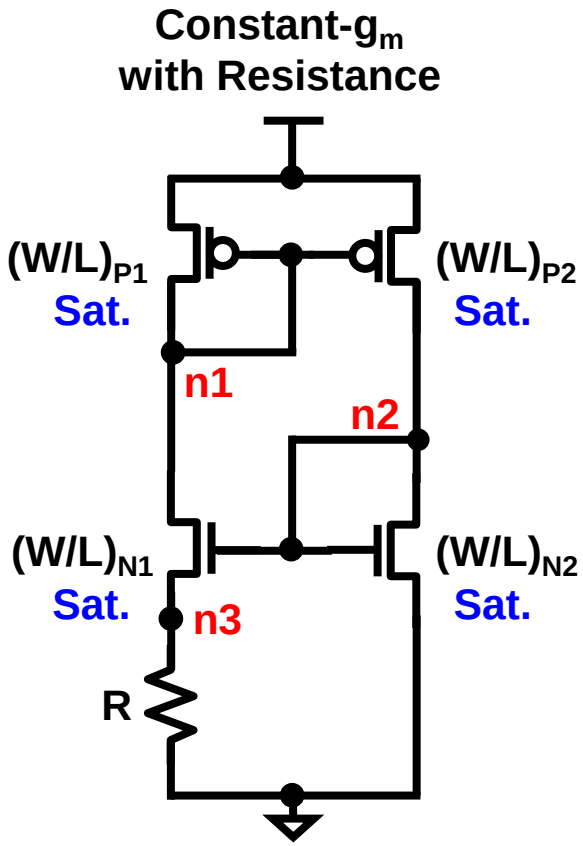
$$I_{ds,\,MP1} = I_{ds,\,MP2} = I_{ds,\,MN1} = I_{ds,\,MN2} = I_{REF}$$

$$V_{gs,\,MN1} + I_{ds,\,MN1}{}^*R = V_{gs,\,MN2}$$

$$\left(I_{ds,\,sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{ov}{}^2\,,\ V_{ov} = V_{gs}\text{-}V_{th}\right)$$

Current Reference Circuit

◆Current Reference / Current Generator



$$V_{th,MN1} + \left(\frac{2I_{REF}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N1}}\right)^{1/2} + I_{REF}*R = V_{th,MN2} + \left(\frac{2I_{REF}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}\right)^{1/2}$$

$$I_{REF}*R = \left(\frac{2I_{REF}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}\right)^{1/2} - \left(\frac{2I_{REF}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N1}}\right)^{1/2}$$

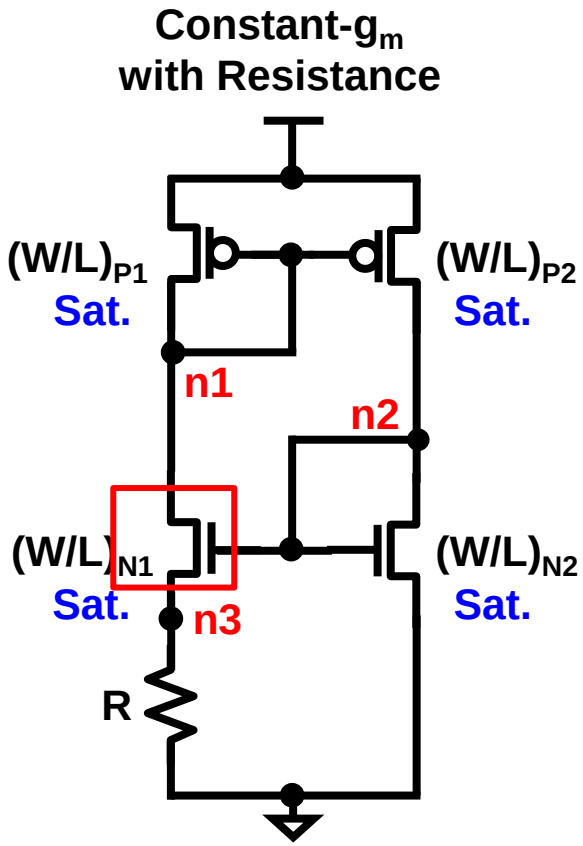
$$I_{REF}*R = \left(1 - \frac{1}{\sqrt{K}}\right)\left(\frac{2I_{REF}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}\right)^{1/2}$$

$$I_{REF}*R^2 = \frac{2}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$$I_{REF} = \frac{2}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}\frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

Current Reference Circuit

◆Current Reference / Current Generator



$$V_{TH} = VT_{H0} + \left(\sqrt{|2\Phi_F + VSB|} - \sqrt{2\Phi_F}\right)$$

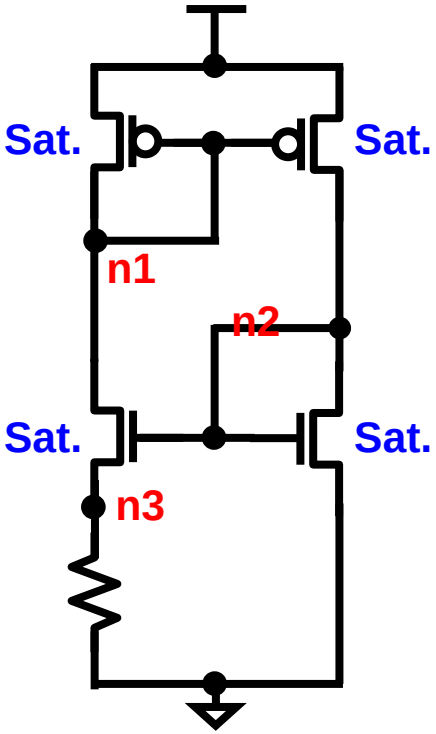
$$\Phi_F = \left(\frac{kT}{q}\right) ln\left(\frac{N_{SUB}}{n_i}\right)$$

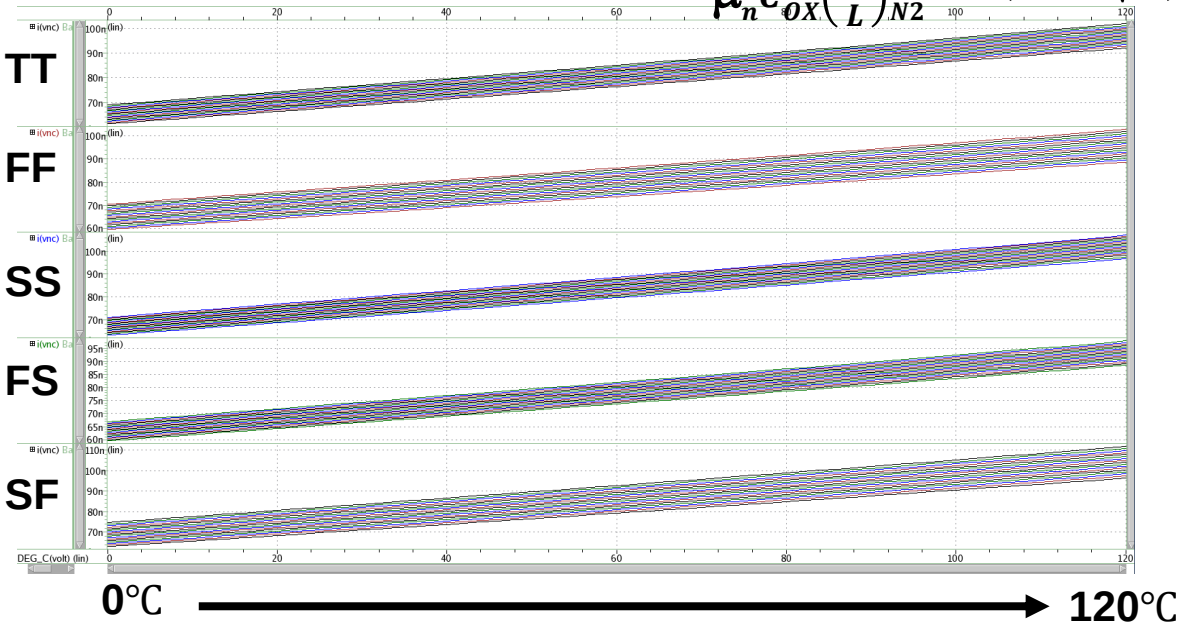
The body of N_1 needs to be connected to n_3 for the cancellation of V_{TH}.

Current Reference Circuit

◆Constant-g_m with Resistance

$$I_{REF} = \frac{2}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}} \frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$



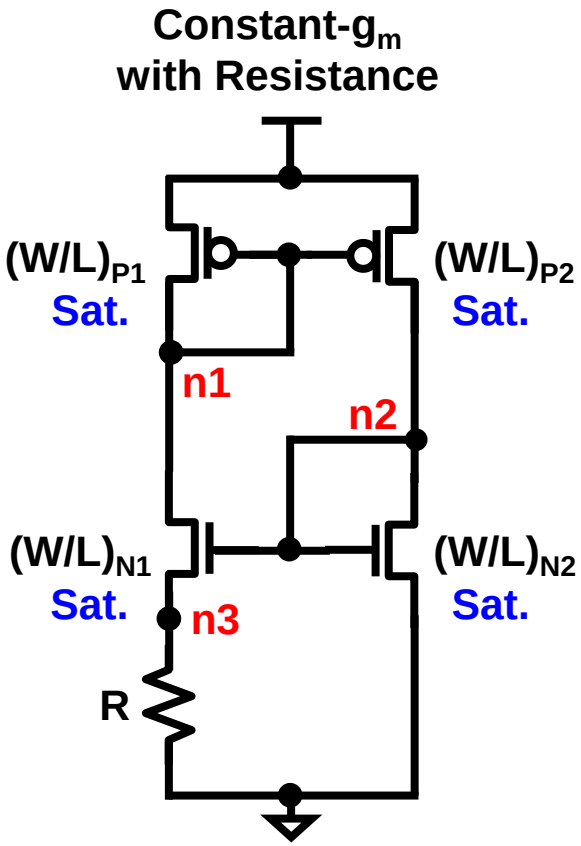


The magnitude of mobility is complimentary to absolute temperature

Corner	TT	FF	SS	FS	SF
$I_{D,0℃}$ (@V_{DD}=1 V)	61	60	63	60	63
$I_{D,120℃}$ (@V_{DD}=1 V)	92	89	97	86	96
$I_{D,0℃}$ (@V_{DD}=1.8 V)	69	71	71	67	75
$I_{D,120℃}$ (@V_{DD}=1.8 V)	102	103	107	98	112

Current Reference Circuit

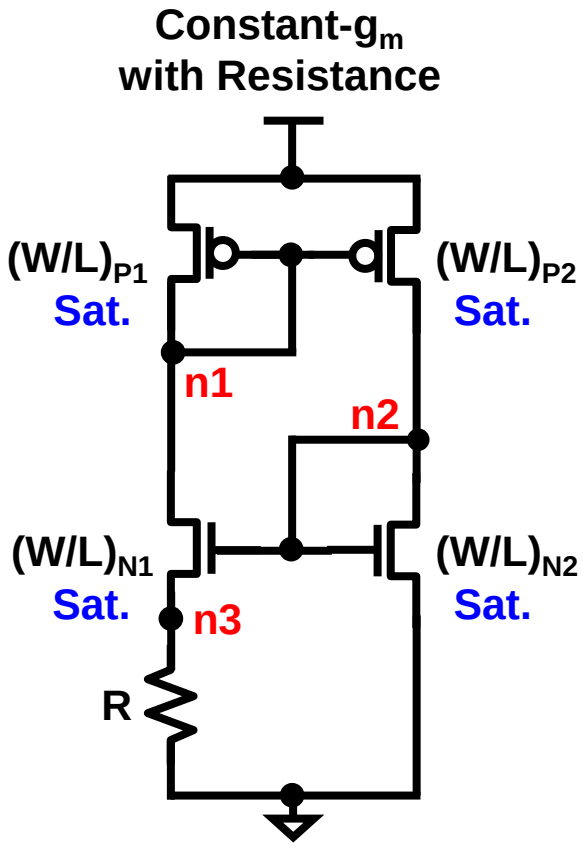
◆Current Reference / Current Generator



- 簡單的設計流程：
  1. 選定I_{REF}大小 (功耗,效能)
  2. 根據I_{REF}選擇適合的n2大小和M_{N2}大小
  3. 根據I_{REF}選擇適合的n1大小和M_{P1} ,M_{P2}大小，需保證M_{P2}可以工作在飽和區
  4. 調整M_{N1}大小（K值）和R值以達到所需電流
  5. 再次檢查所有電晶體的工作區間，若需要可微調電晶體大小

Current Reference Circuit

◆Current Reference / Current Generator



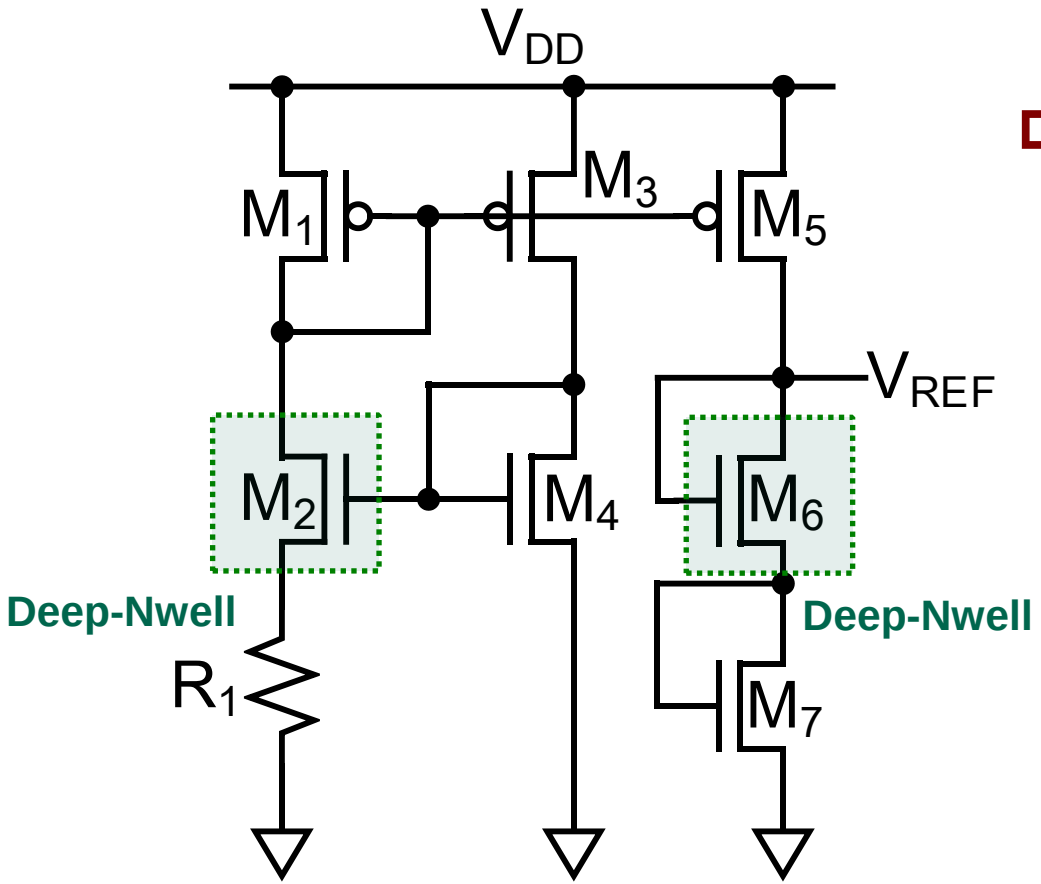
- 特別留意
  決定MOSFET操作在Saturation region與否，與drain電壓有關，n2太高、n1太低，將使M_{N1}及M_{P2}進入Triode region。

  調整參數過程需考慮到layout時的對稱性，M_{N1}及M_{N2}的width和length相同，應改變m(或finger)數來調整total width而非改變width大小。

  跑dc若發現電路沒有正常運作，可在n1到n2之間，接一或多個diode-connected的MOS，但不可讓MOS導通。(不可給initial condition)

HW 2

◆ Architecture and specification

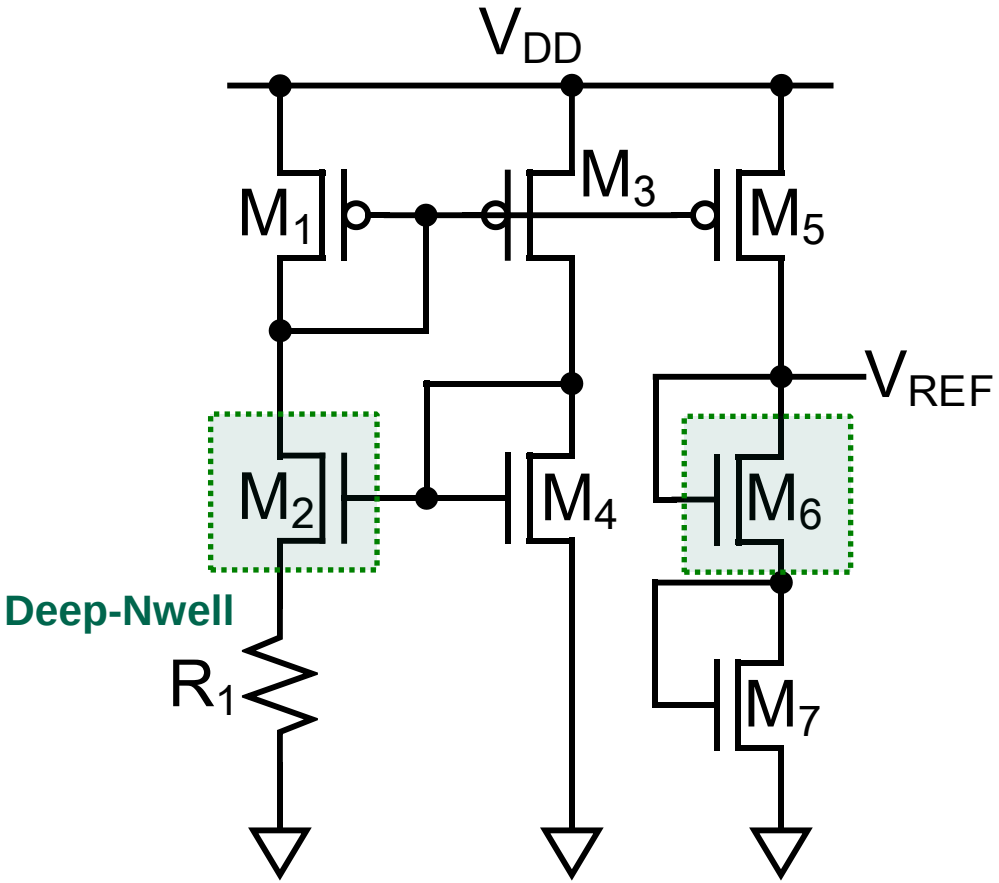


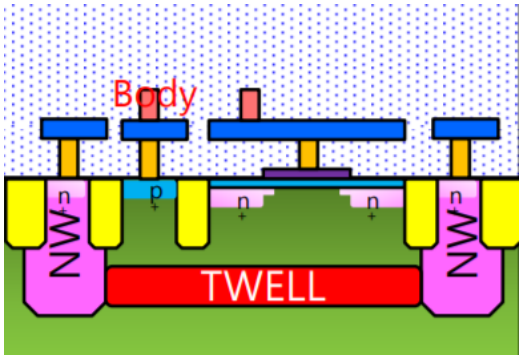
- **Constant g_m:**
  - **M_1: (4μm/0.5μm)*12**
  - **M_2: (1μm/0.5μm)*4**
  - **M_3: (4μm/0.5μm)*12**
  - **M_4: (1μm/0.5μm)**
  - **M_5: (4μm/0.5μm)*12**
  - **M_6: (? μm/0.5μm)**
  - **M_7: (? μm/0.5μm)**
  - **R_1: ? KΩ [RNNPO_MM]**

➢ All bodies of NMOS and PMOS are connected to source.

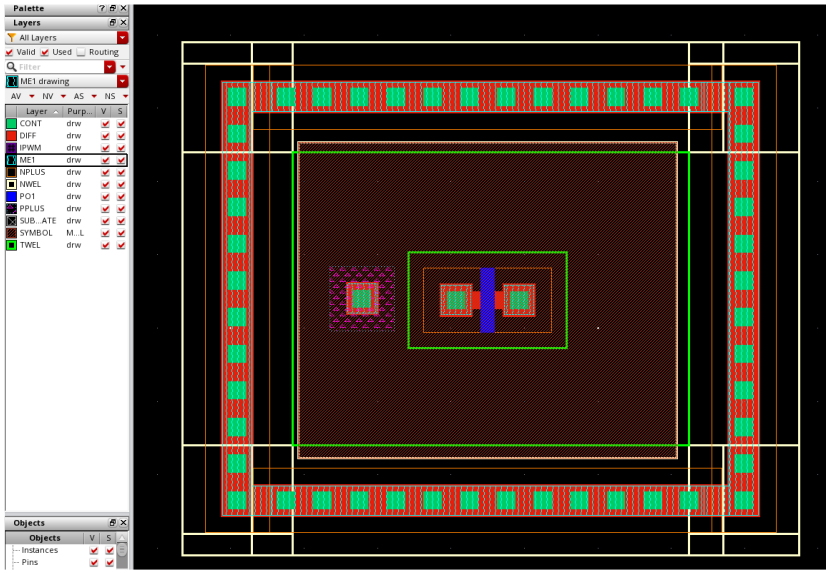
HW 2

◆ Layout Concern





N-Well接最高電位



➢ All bodies of NMOS and PMOS are connected to source.

HW 2

◆Specifications

Parameters	Target spec.		Pre-sim.	Post-sim.
V_{REF}	1.2V (+/- 1%) @ V_{DD}=1.8V	Value (V)		
		Error (%)		
V_{REF}	1.2V (+/- 1%) @ V_{DD}=1.7V-1.9V	Value (V)		
		Error (%)		
I_{REF}	10μA (+/- 1%) @ V_{DD}=1.8V	Value (V)		
		Error (%)		
I_{REF}	10μA (+/- 5%) @ V_{DD}=1.7V-1.9V	Value (V)		
		Error (%)		
P_{VDD}	<150uW @ V_{DD}=1.8V	Power (uW)		

誤差計算方式如下：

$$\frac{V_{REF} - 1.2}{1.2} \times 100\%$$

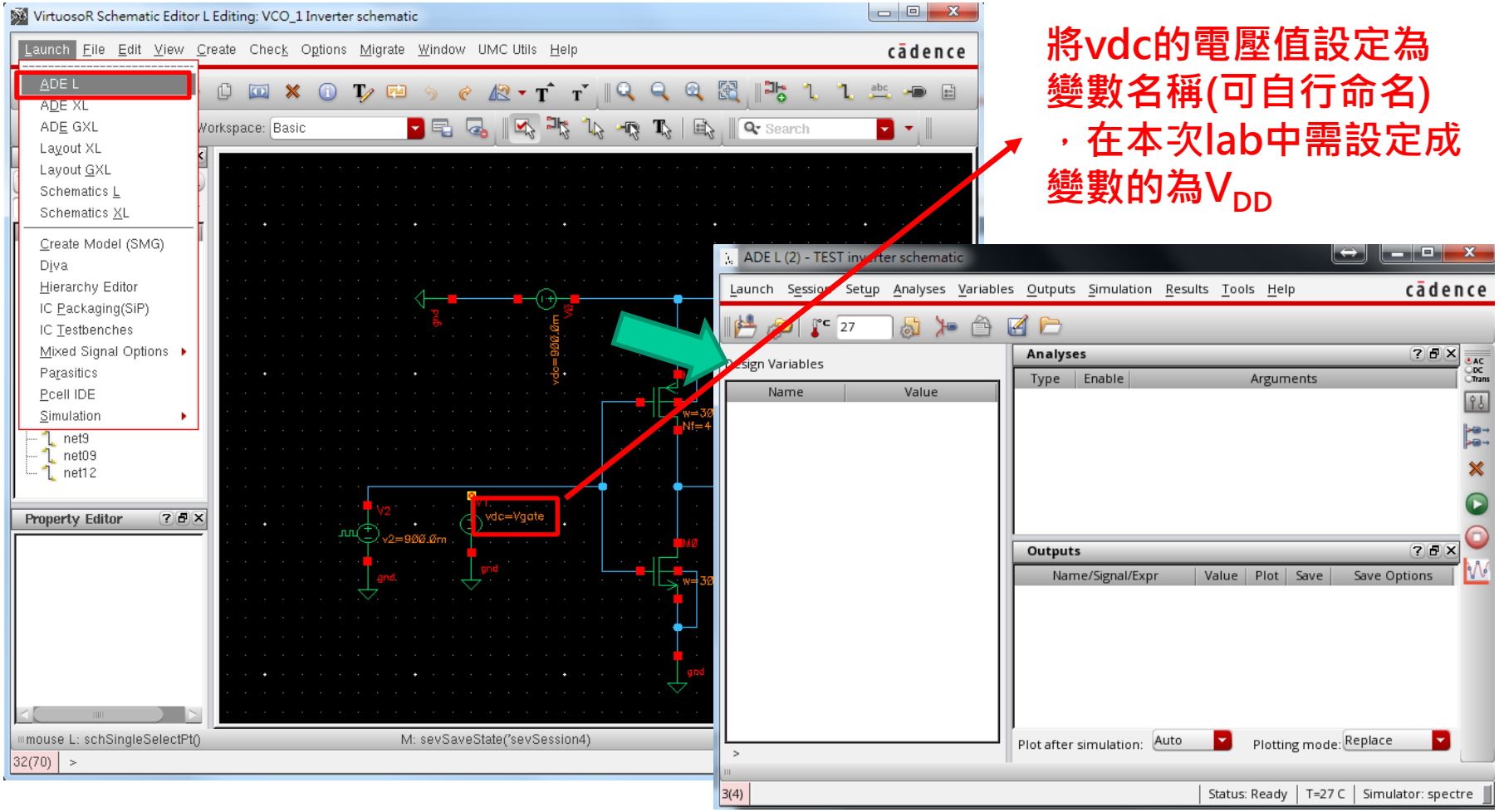
HW 2

- 繳交一份電子檔。
- 請在報告中加入**Pre-sim.**和**Post-sim.**模擬結果，**Layout**圖，**DRC**及**LVS**結果。報告中的波形圖請改用白底，並將線條加粗。
- **Pre-sim.**和**Post-sim.**模擬結果需包括V_{REF}(和I_{REF})對V_{DD}(1.7V~1.9V)的圖，以及V_{REF}(和I_{REF})對溫度(0℃~120℃)的圖(V_{DD}=1.8V)。
- 並請於報告中簡單說明M_6/M_7及R_1尺寸設計的考量
- 作業繳交時間為**2023/08/07(一)晚上12點前**，請將作業報告上傳至**e3**

Thanks for your attention !

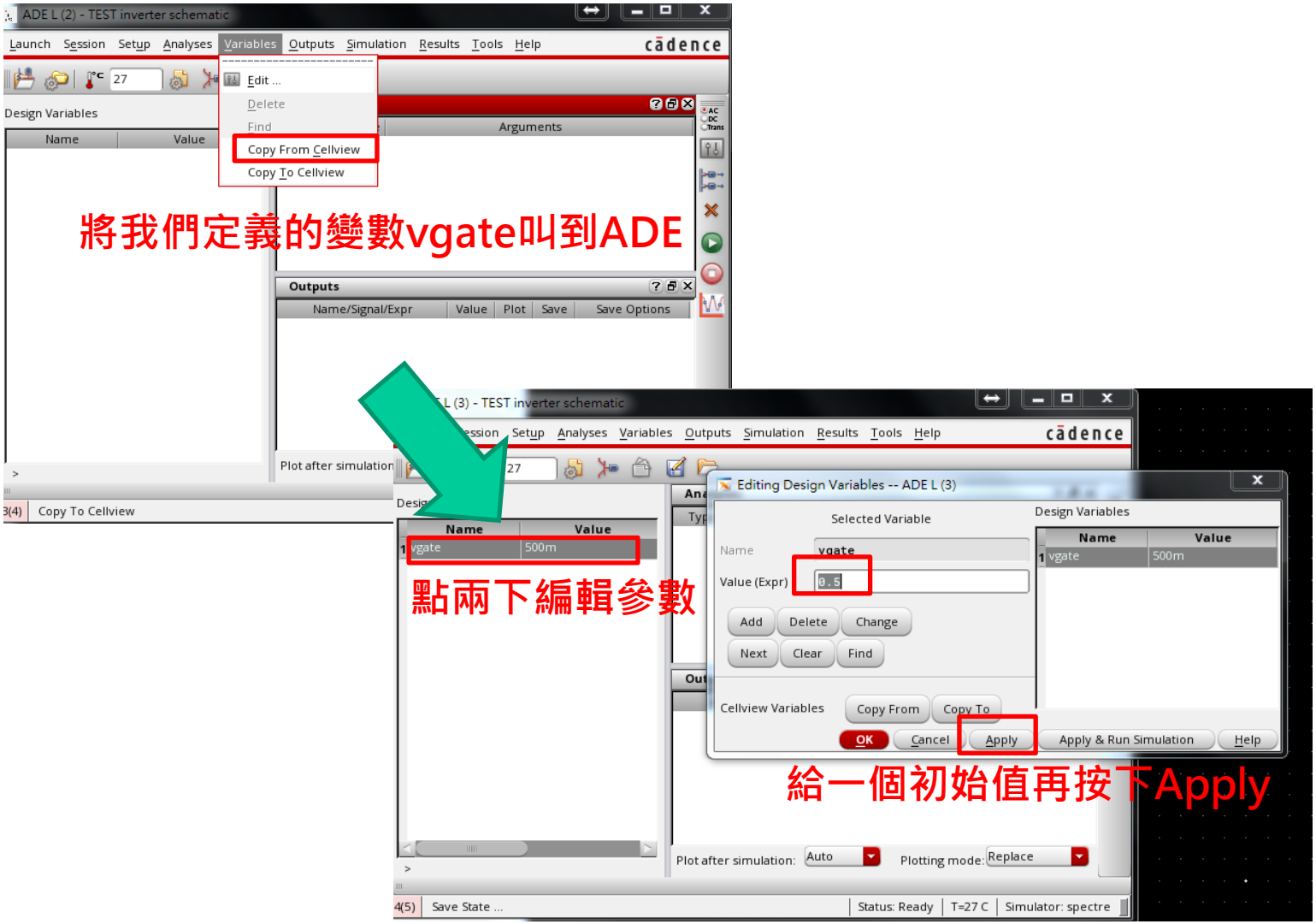
DC simulation (1)

- 開啟Analog Design Environment視窗



將vdc的電壓值設定為變數名稱(可自行命名)，在本次lab中需設定成變數的為V_{DD}

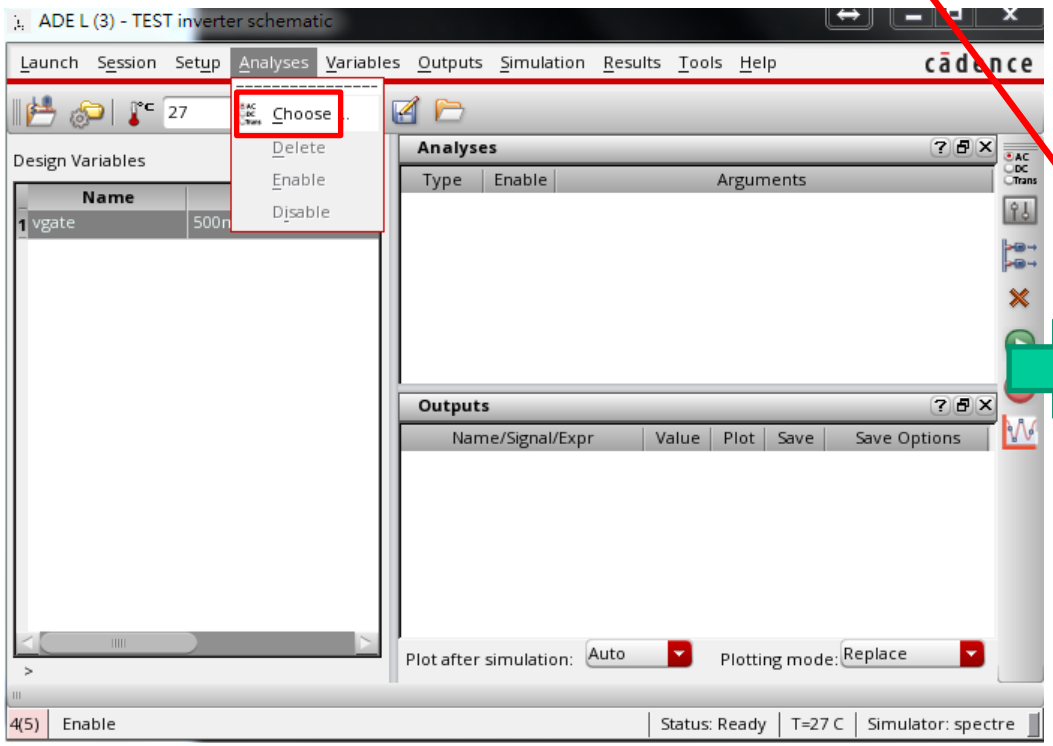
DC simulation (2)

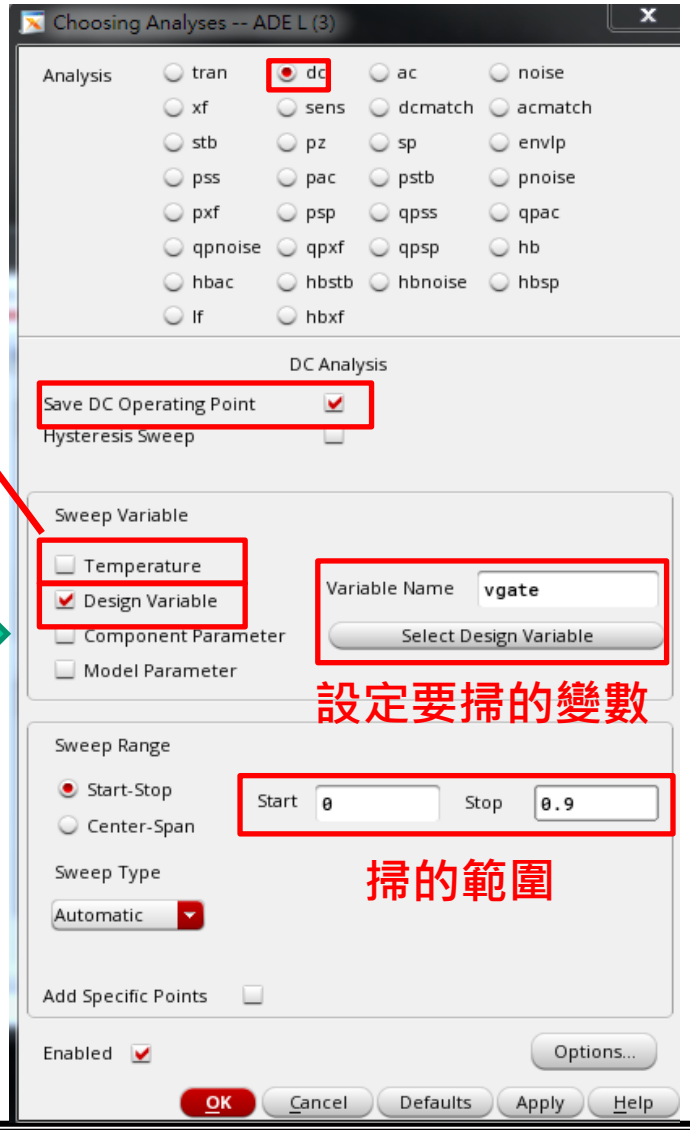


DC simulation (3)

- 選擇DC analysis

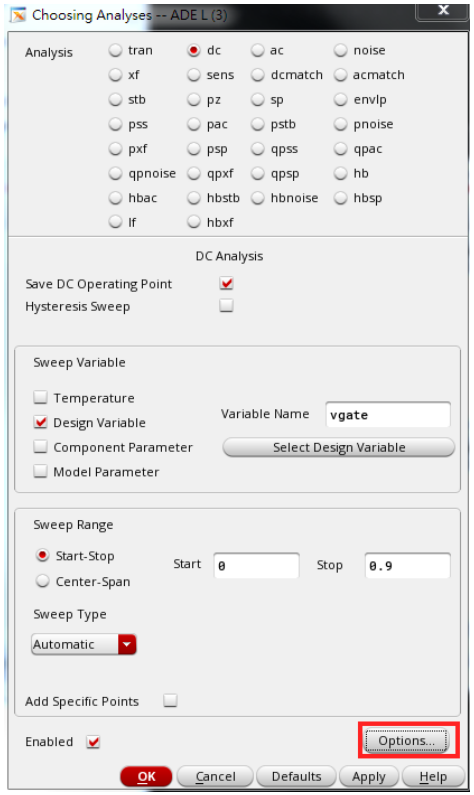
若要sweep溫度則勾選Temperature，接著設定要掃的溫度範圍

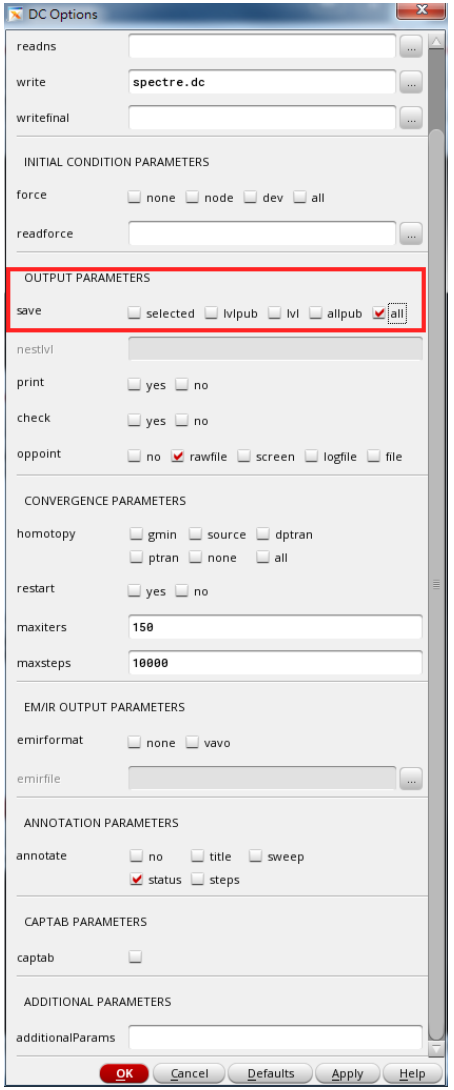




DC simulation (4)

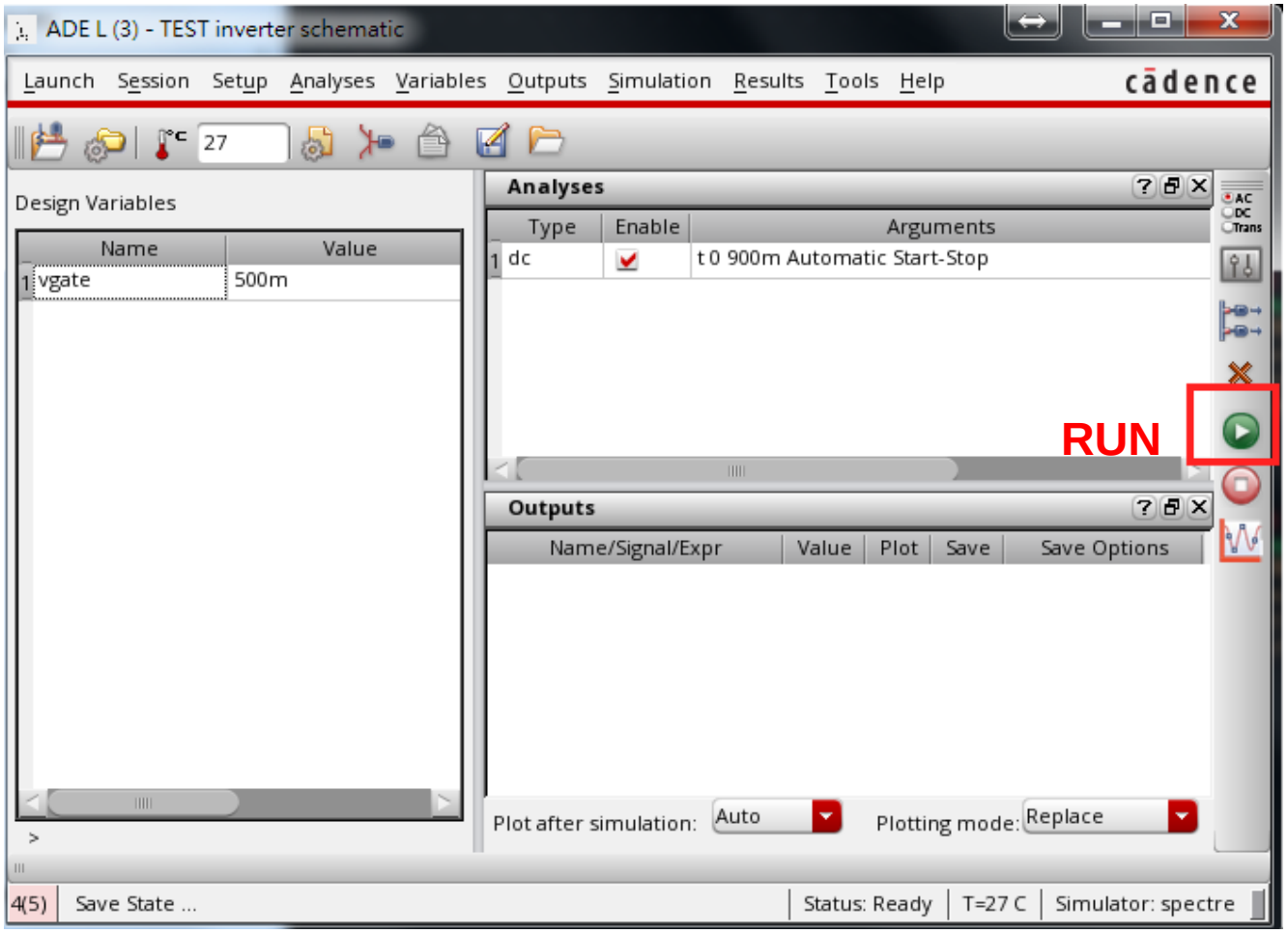
- 如果要看component的parameter，要在option裡面點output parameter選all (若電路複雜度較高，通常不會選擇all，因為會佔用太多硬碟容量)





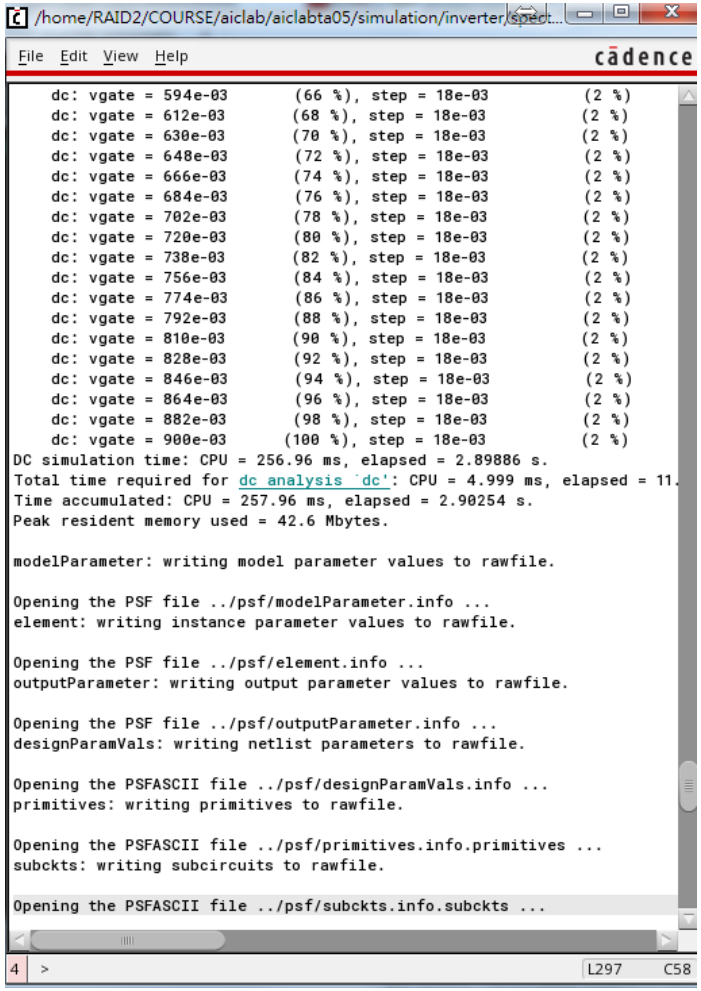
DC simulation (5)

- 設定好就可以按netlist and run開始跑模擬



DC simulation (6)

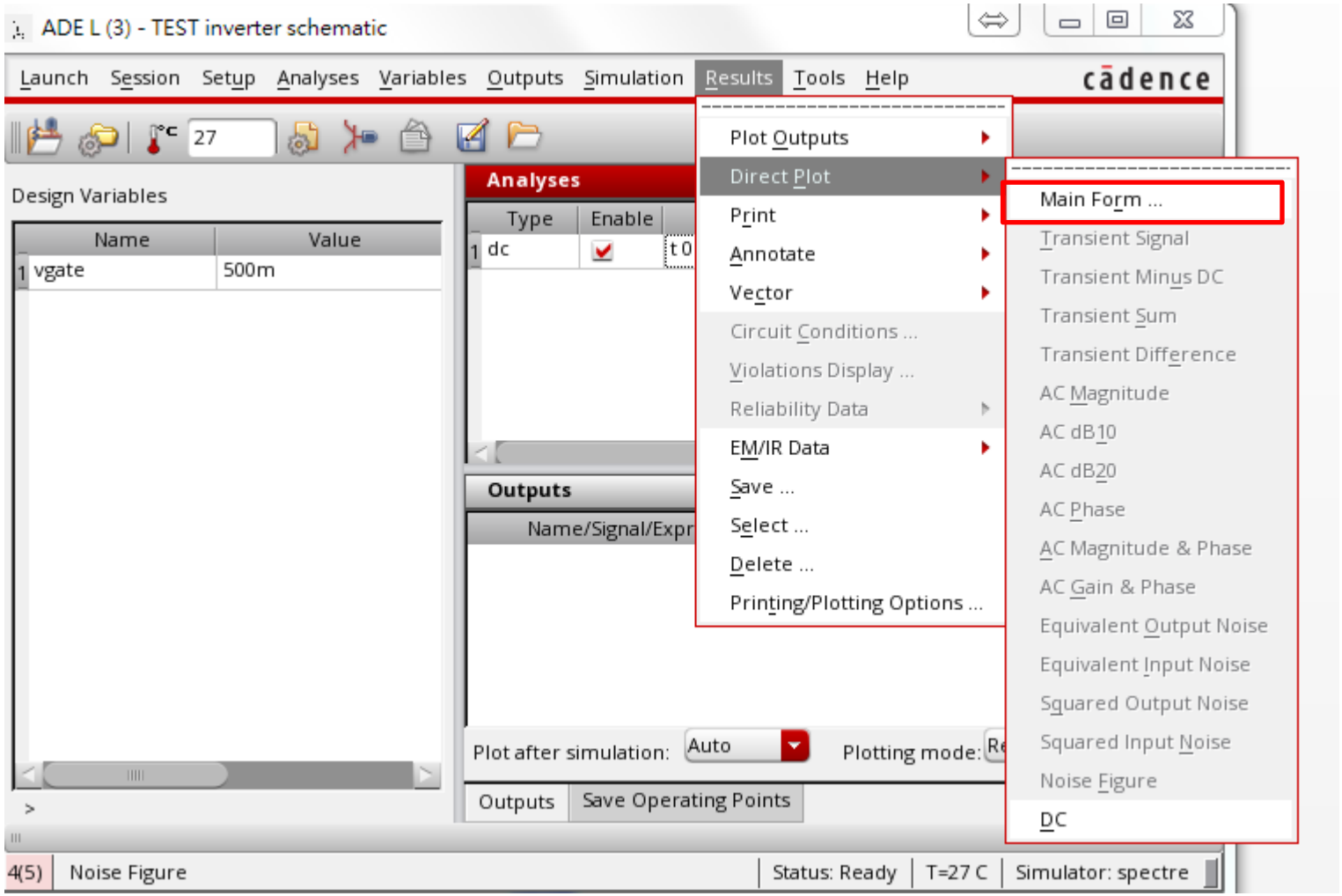
- **Output log**



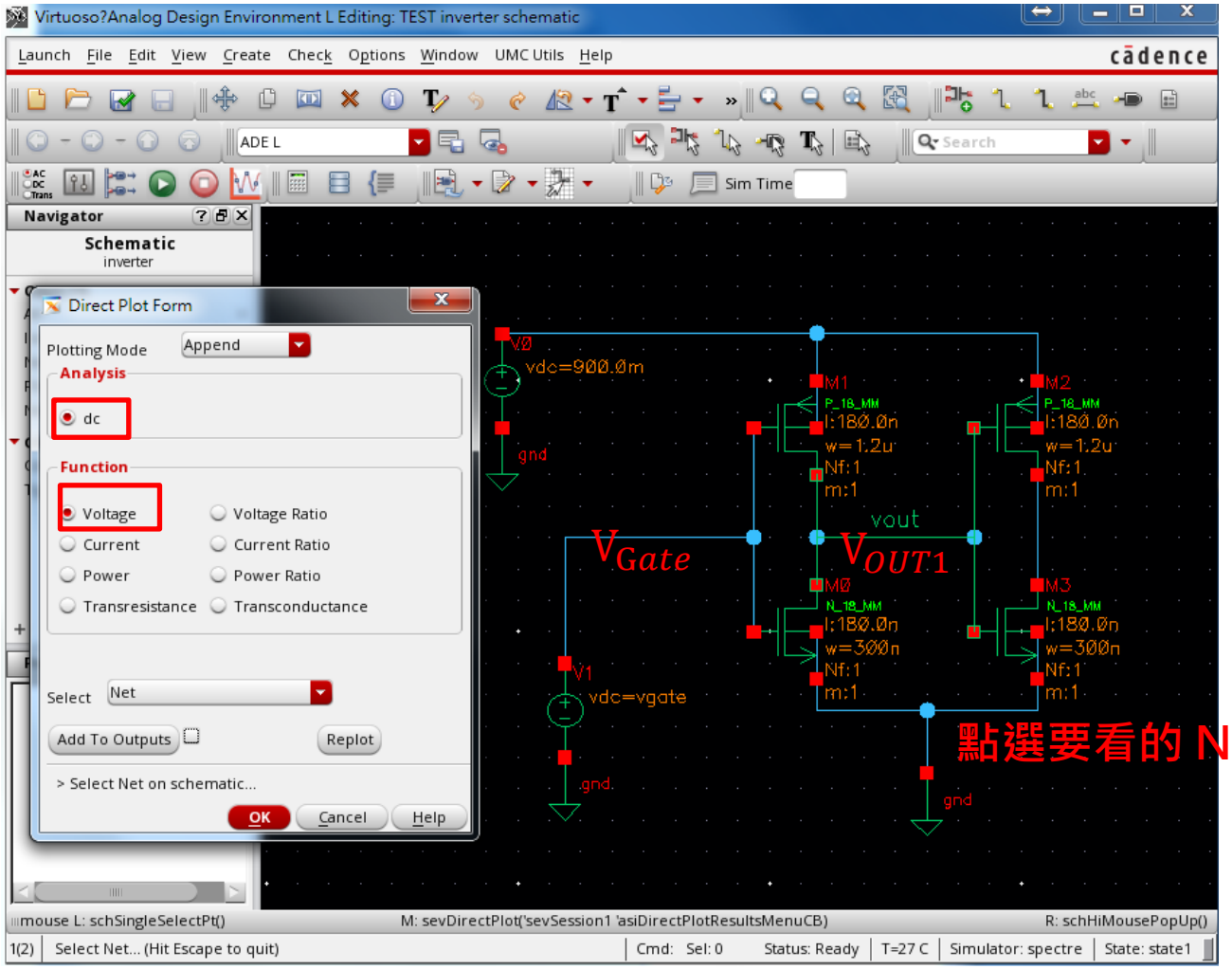
跑完了

DC simulation (7)

查看模擬結果

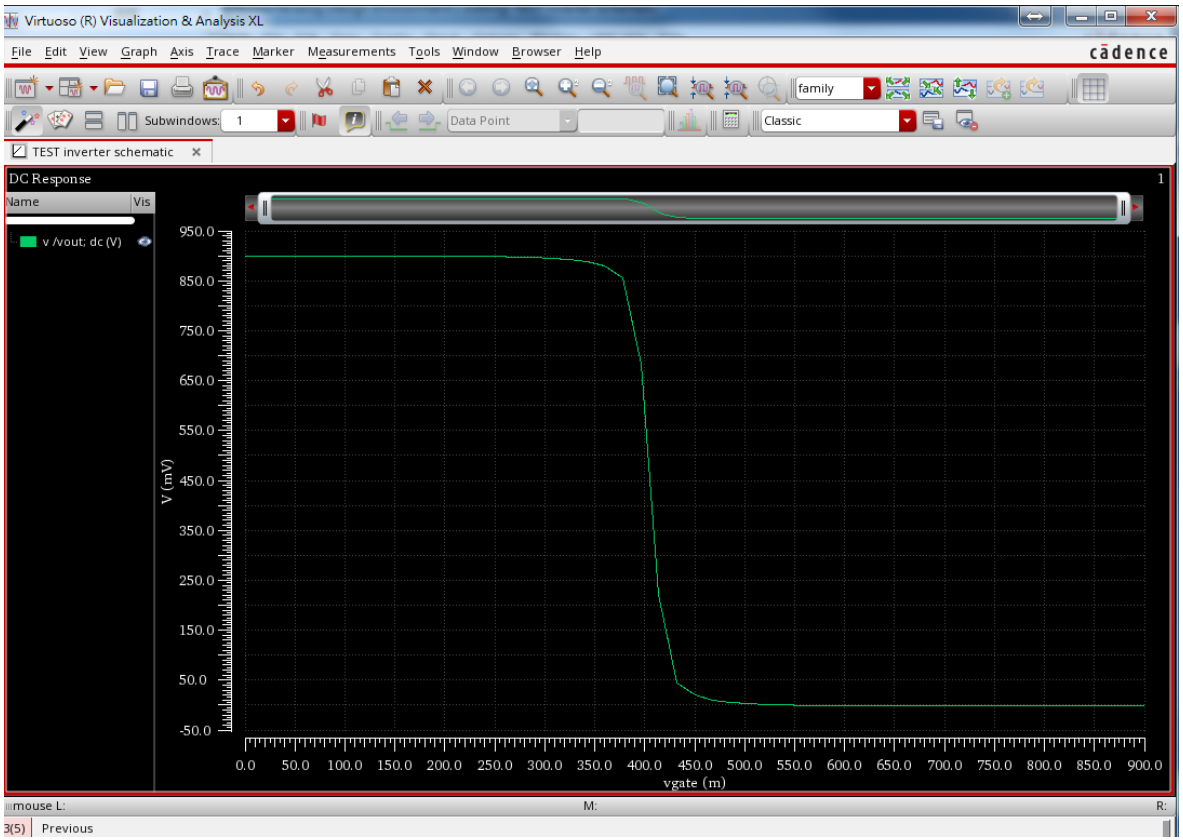


DC simulation (8)



DC simulation (9)

DC Transfer Curve

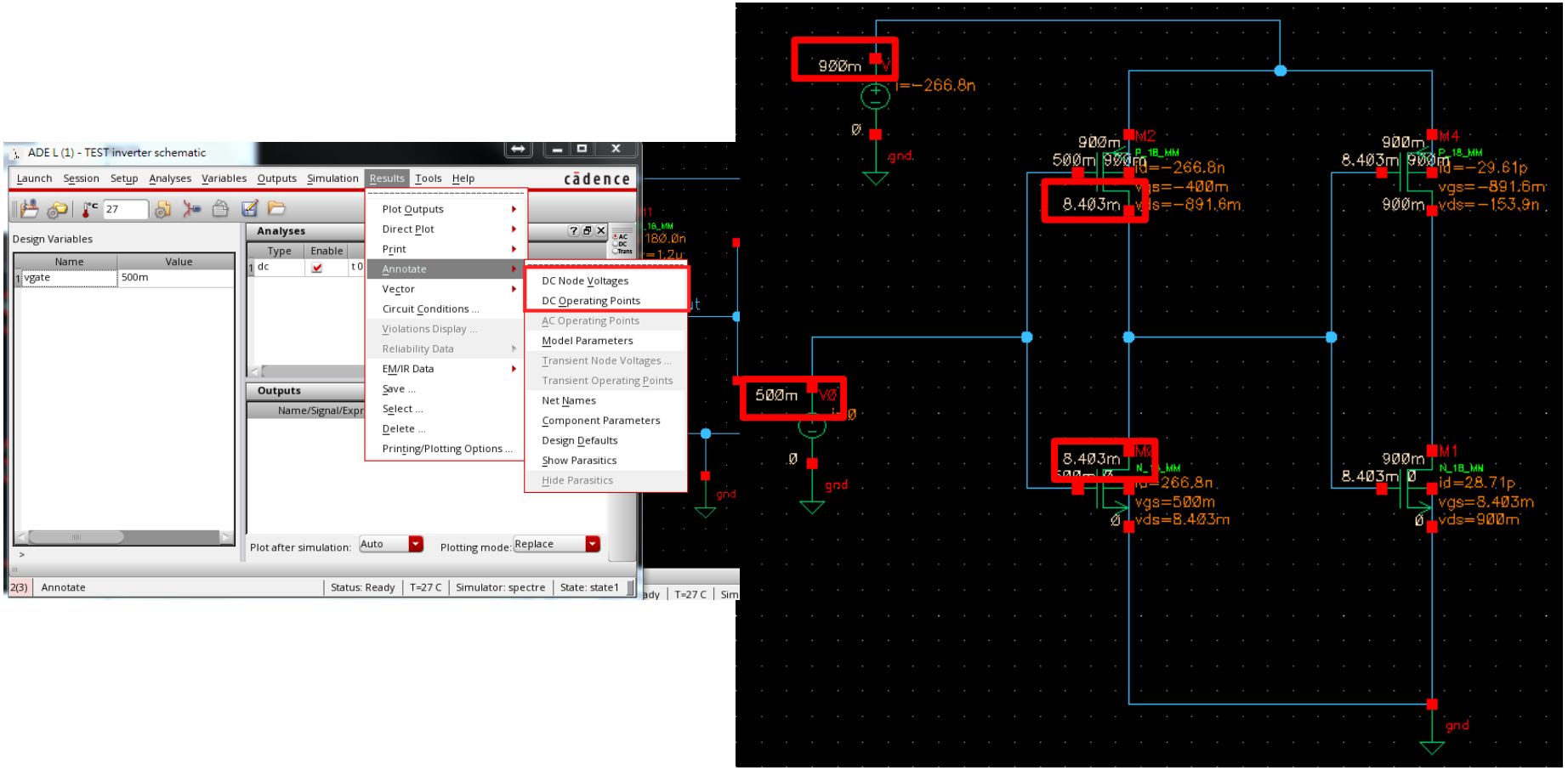


更改背景顏色:
Graph→Edit
→Foreground/Background

加入marker:
Marker →Place
→Trace Marker (t)

DC simulation (10)

- 選擇DC Node Voltage以及DC Operating Points可以將目前的DC 操作電壓或電流標示在schematic



DC simulation (11)

- 利用Results Browser去看device的參數