

# 電源管理晶片設計與實作

## *Pre-Layout Simulation* Workstation Setup

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*National Yang Ming Chiao Tung University*



# *Workstation Log-in Information*

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- ◆ 可用機台：[\[ee21~ee35\].ee.nctu.edu.tw](http://[ee21~ee35].ee.nctu.edu.tw) (不一定連號)
- ◆ 學員帳號：[pmic001~050](#)
- ◆ 預設密碼：[pmic](#) (請登入機台使用passwd指令更改密碼)
- ◆ 有效期限：2023/10/07
- ◆ 提供實驗室無法提供工作站的同學使用，請向助教領取工作站帳號。
- ◆ 未向助教領取帳號者，請勿自行使用工作站帳號。



# *Workstation Log-in Information*

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## 一、違規行為：

1. 任意重開或關閉電腦及工作站，未告知系統管理者。
2. 鎖住電腦螢幕後離開實驗室，妨礙他人使用主機。
3. 過量使用實驗室主機資源，影響其他人正常使用。
4. **將修課帳號借給他人使用，或借用他人帳號。**
5. 使用本實驗室電腦設備用於非課程教學用途。
6. 破壞系統或實驗室設備，或任何影響系統運作的行為。
7. 入侵系統或盜取、盜用他人帳號。
8. 其他違規事宜，經個案討論認定違規者。

## 二、罰則：

1. 如使用者有前項1,2,3 點的違規行為，初犯帳號停權兩星期，累犯取消課程帳號。
2. 如使用者有前項4,5,6,7 點的違規行為，使用者帳號立即取消，並登記使用者資料至黑名單內，違規的使用者不得再申請使用本實驗室電腦設備。
3. 其他違規事宜，個案討論認定其罰則。

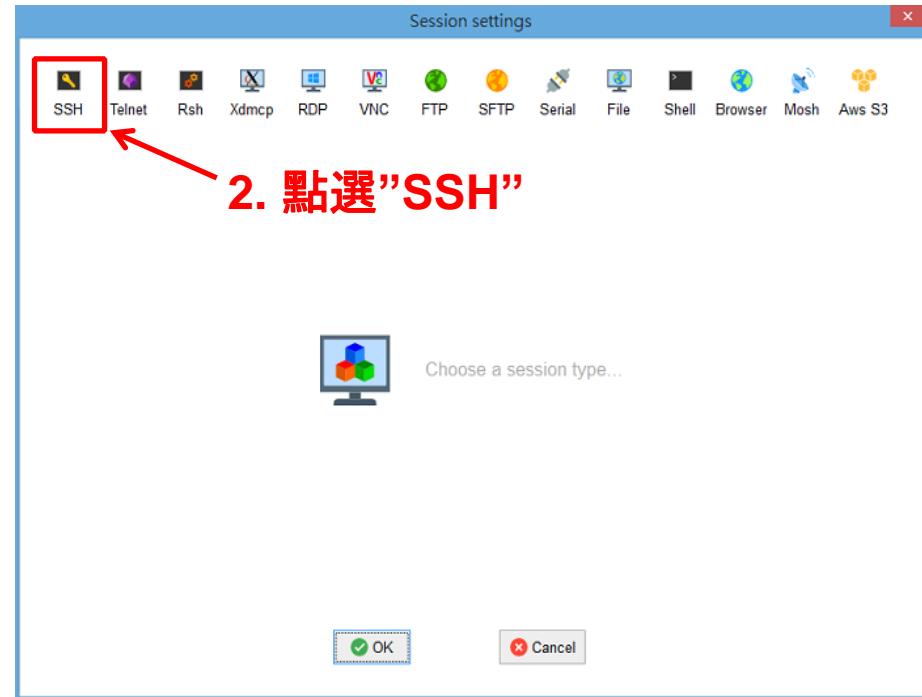
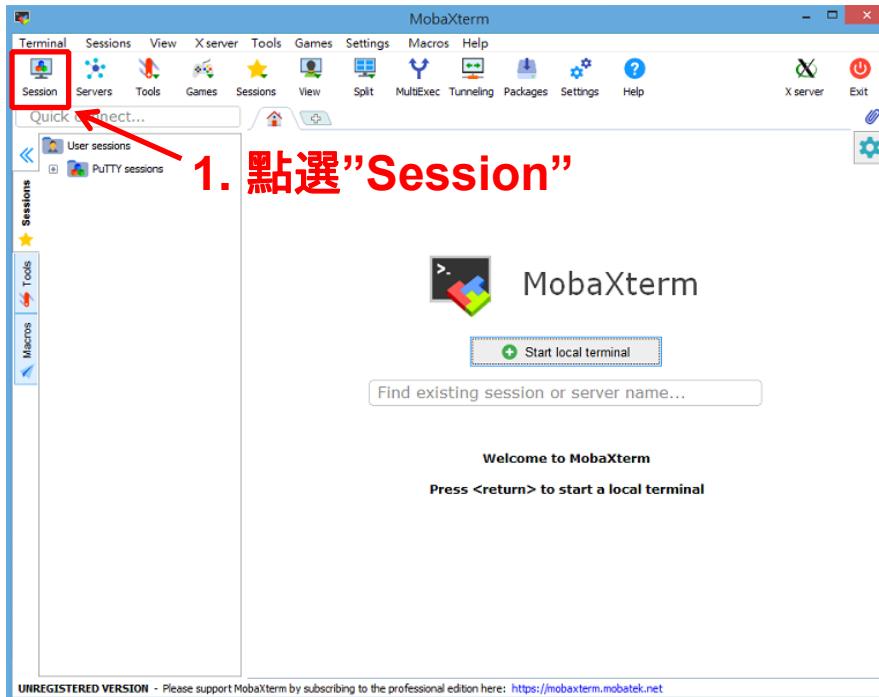
## 三、注意事項：

1. 登入時，請先關閉螢幕鎖定設定。
2. 請勿攜帶食物進入教室以維持教室清潔。
3. 離開時，請記得先登出工作站。



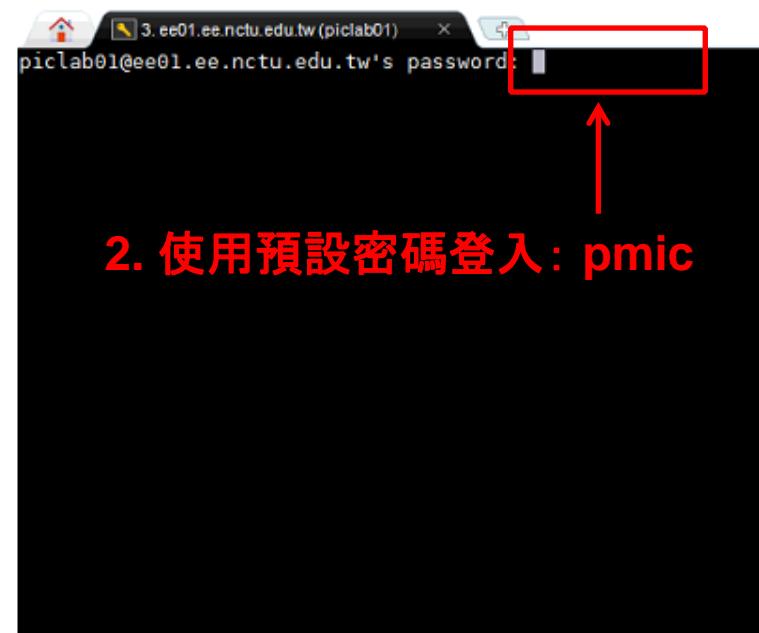
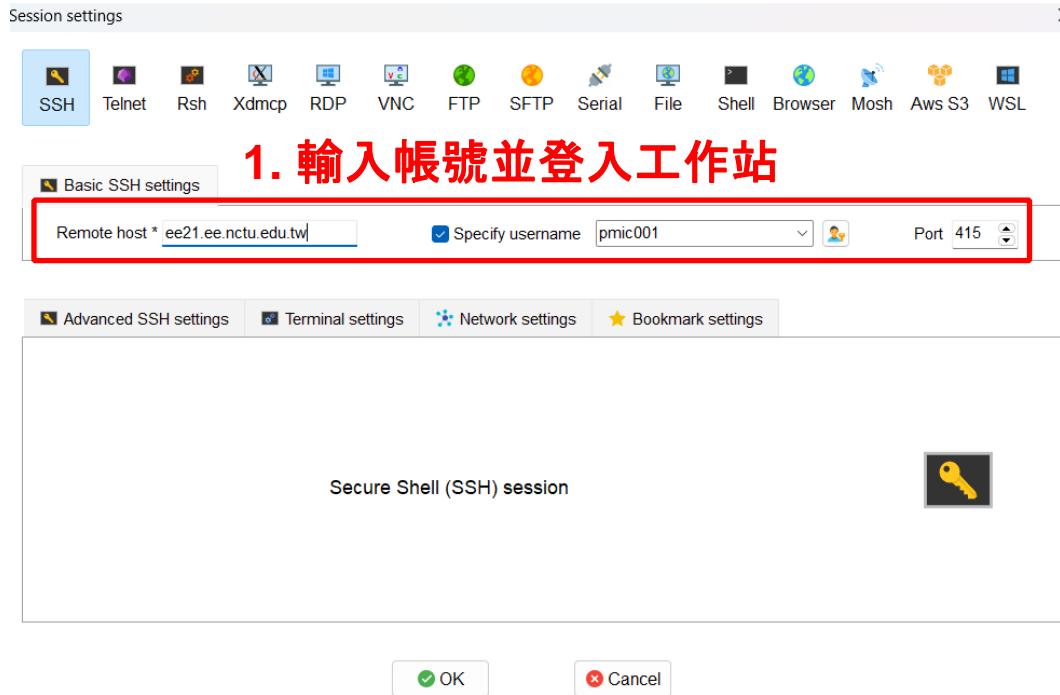
# MobaXterm Software Setup

- ◆ VPN連回交大( <https://it.nycu.edu.tw/itservices/networks/ssl-vpn/> )
- ◆ Download MobaXterm ( <https://mobaxterm.mobatek.net/> )
  - 使用Putty、Xmanager、UltraVNC...等平台皆可, 依個人喜好



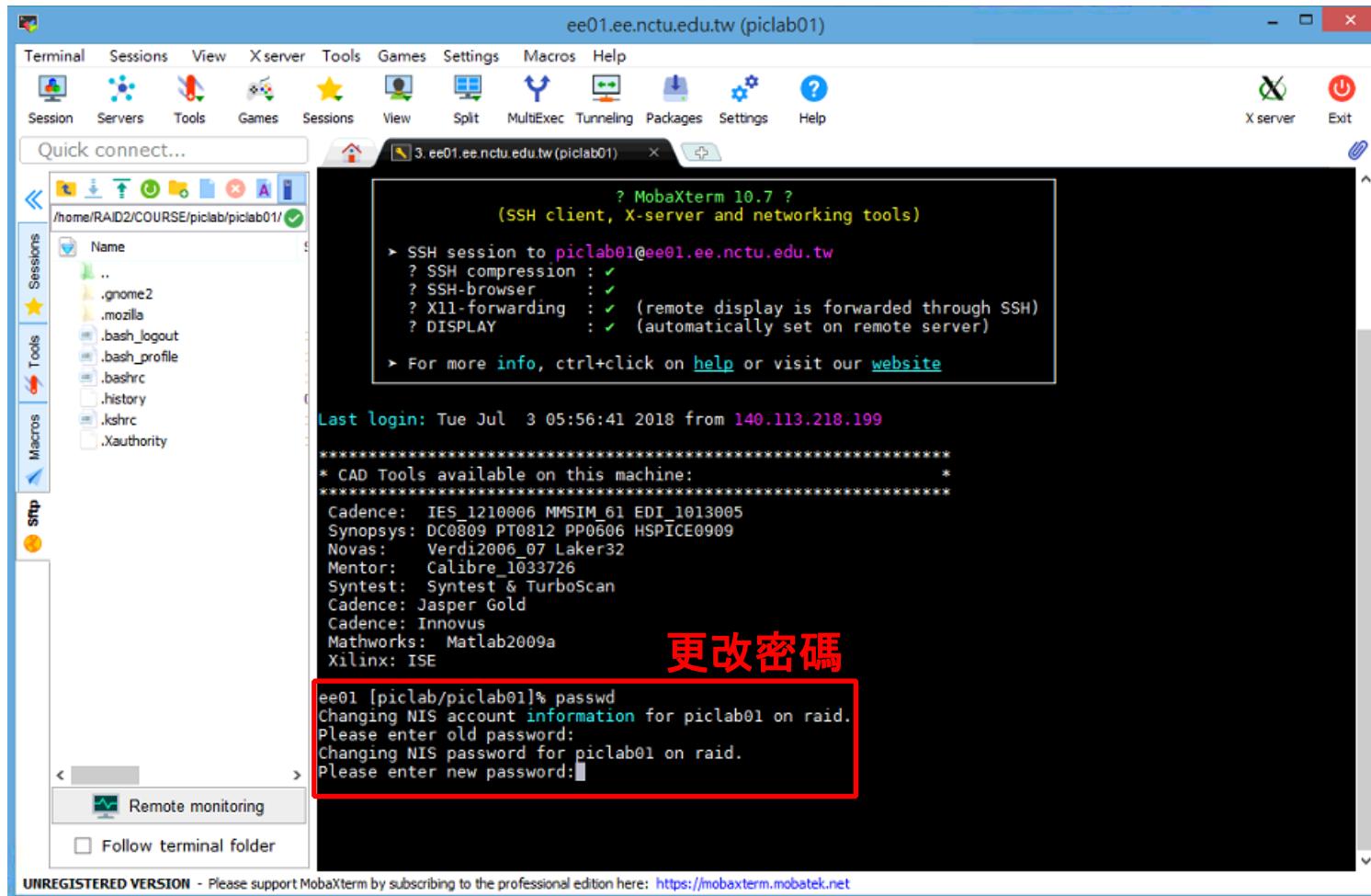
# Login to Workstation

- ◆ Remote host 欄位，選擇其中一個輸入  
**[ee21~ee35].ee.nctu.edu.tw**
- ◆ Specific name 欄位打勾，輸入分配的工作站帳號，並輸入密碼



# Change Password

- ◆ 指令: **passwd**, 輸入舊預設密碼, 及兩次新設定密碼



# Basic Linux Instructions

## ◆ 其餘指令可參考

([http://linux.vbird.org/linux\\_basic/redhat6.1/linux\\_06command.php](http://linux.vbird.org/linux_basic/redhat6.1/linux_06command.php))

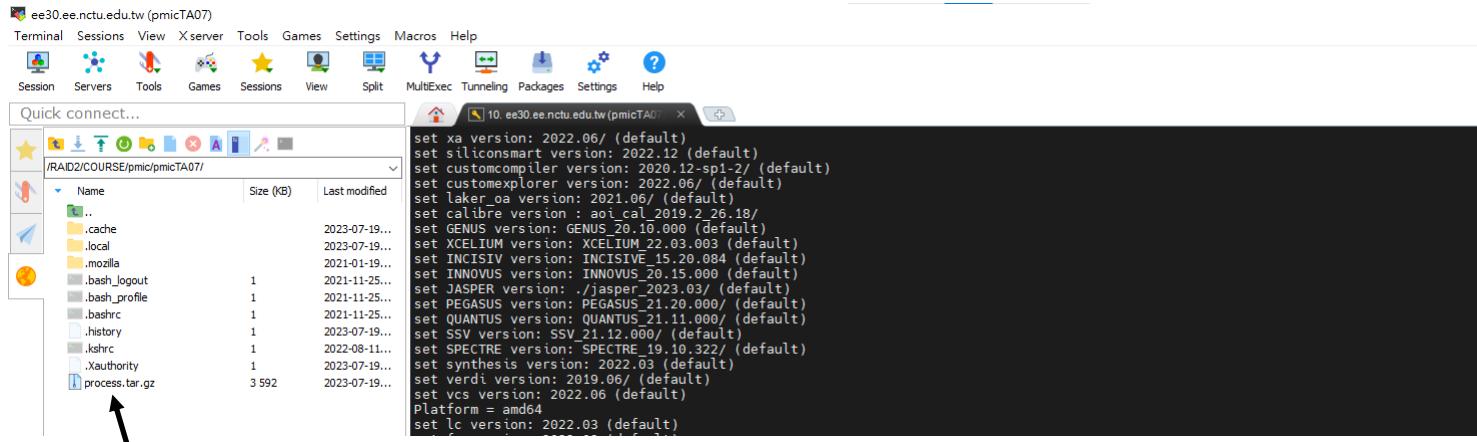
➤ 圖形化介面指令：**nautilus** (結束可使用ctrl+c指令)

ls	顯示所有非隱藏的資料夾與檔案
ls -a	顯示所有的資料夾與檔案
cd ~	回到主目錄
cd name	進入名稱為 name 的資料夾
cd ..	回到上一層資料夾
pwd	顯示當前的資料夾路徑
mkdir name	建立名稱 name 的空白資料夾
rm –ir name	刪除名稱為 name 的檔案或資料夾
mv fileA fileB	將檔案fileA更名為fileB
cp fileA newfolderB/.	複製檔案fileA至目錄newfolderB中
du	檢視硬碟中資料檔使用的容量



# Workstation Setup with Process File

## ◆ 將製程檔案拖至HOME底下



把檔案拖進來

## ◆ ls

列出HOME下有**process.tar.gz**  
(檔案名稱會依各實驗室不同)



# Workstation Setup with Process File

## ◆ tar -zxvf process.tar.gz

解壓縮檔並放在自己 HOME底下。

```
pmicTA08@ee30[~]$ tar -zxvf process.tar.gz
```

## ◆ rm process.tar.gz

移除之前多餘的壓縮檔。

```
UM180FDKMFC_C05_PB/.cadence/dfII/workspaces/Layout/  
UM180FDKMFC_C05_PB/.cadence/dfII/workspaces/Schematics/  
UM180FDKMFC_C05_PB/libManager.log  
UM180FDKMFC_C05_PB/.cdsinit  
UM180FDKMFC_C05_PB/.cdsenv  
UM180FDKMFC_C05_PB/cds.lib  
12:53 pmicTA08@ee30[~]$ rm process.tar.gz  
12:53 pmicTA08@ee30[~]$
```

## ◆ ls -a

列出HOME下有  
**UM180FDKMFC\_C05\_PB**資料夾。

```
13:07 pmicTA08@ee30[~]$ ls -a  
. .Xauthority .bash_profile .cache .kshrc .mozilla  
.. .bash_logout .bashrc .history .local UM180FDKMFC_C05_PB
```

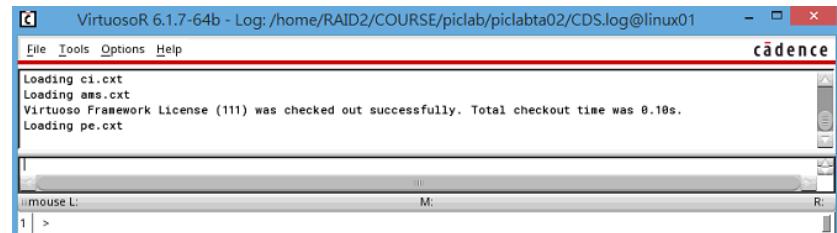


# Open Cadence

- ◆ 指令cd UM180FDKMFC\_C05\_PB進入資料夾
- ◆ 接著輸入virtuoso &進入cadence軟體
- ◆ 在UM180FDKMFC\_C05\_PB資料夾下主要含有：

```
13:07 pmicTA08@ee30[~]$ cd UM180FDKMFC_C05_PB/
13:09 pmicTA08@ee30[~/UM180FDKMFC_C05_PB]$ ls
0.18um_techfile.tf  Models      calview.cellmap  display.drf  libManager.log
Calibre              UMC_18_CMOS  cds.lib        icc.rules   stream.map
13:09 pmicTA08@ee30[~/UM180FDKMFC_C05_PB]$ virtuoso &
```

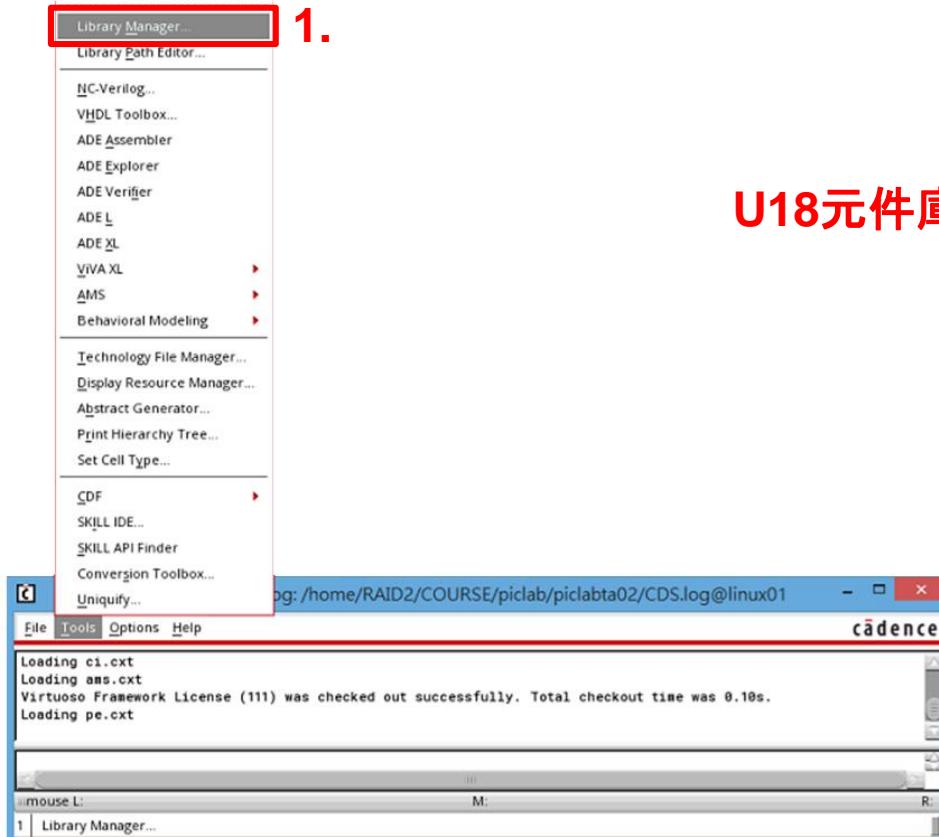
- 0.18um\_techfile.tf: U18製程技術檔
- displaydrf: icfb顯示設定檔
- cds.lib: icfb定義目錄檔
- Calibre: DRC, LVS, XRC等rule檔
- Models: HSPICE, Spectre等所需lib檔
- UMC\_18\_CMOS: 標準元件庫



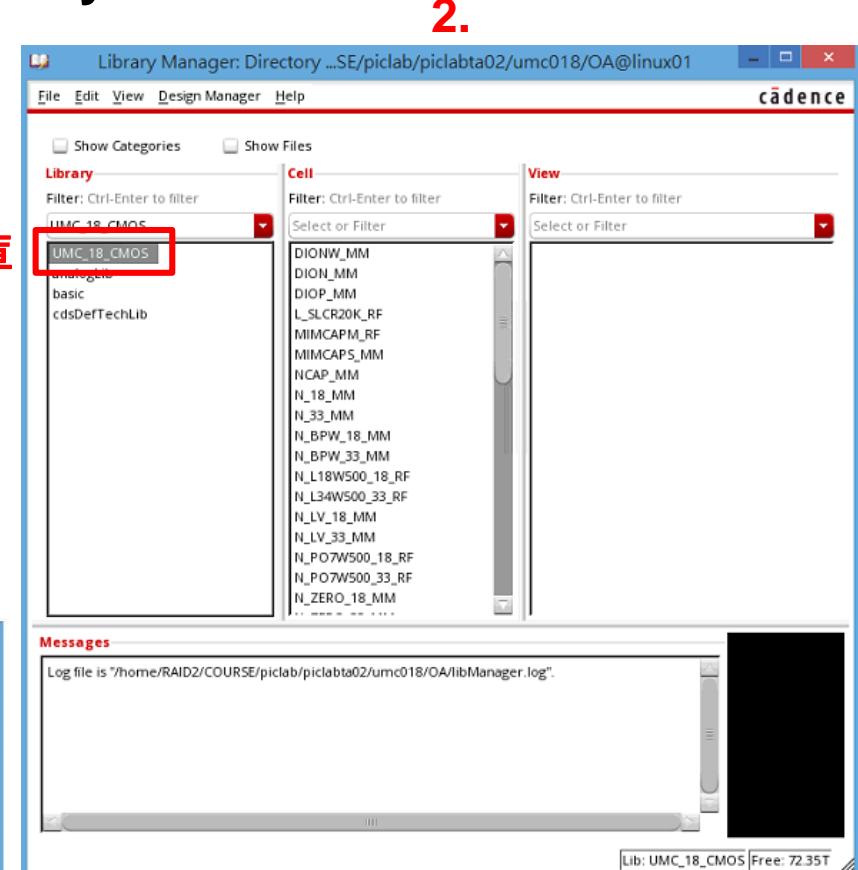
# Library Manager

## ◆ Tools → Library Manager

➤ 可於Library Manager管理各項Library及Cell

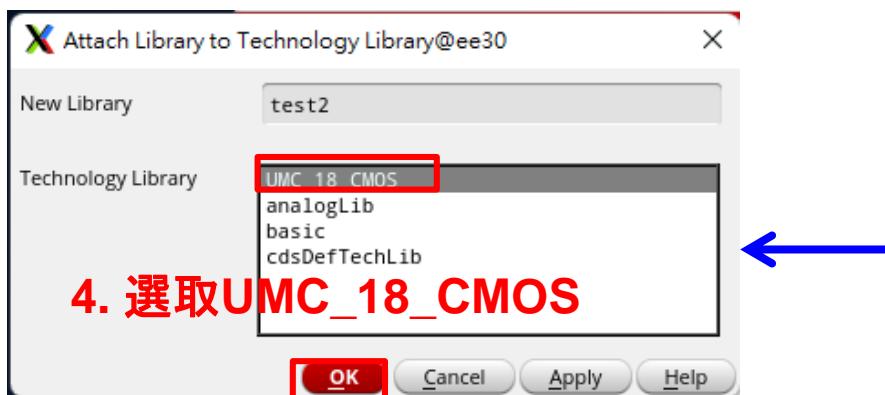
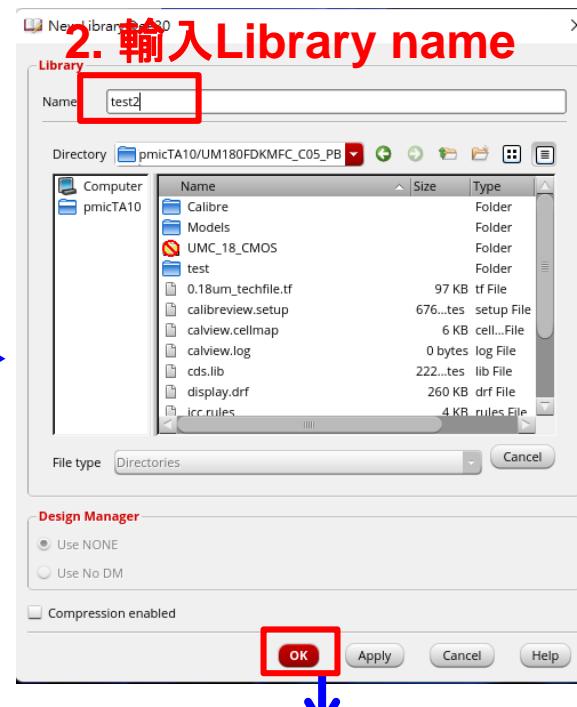
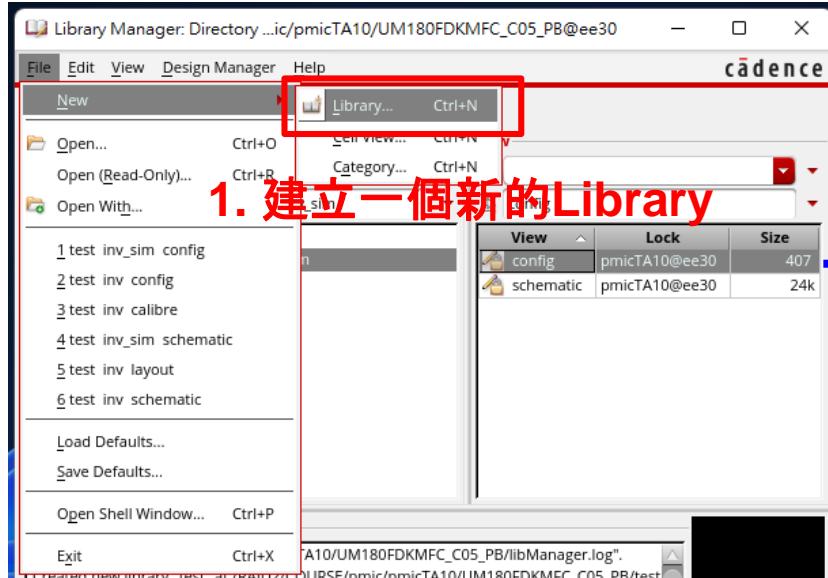


U18元件庫



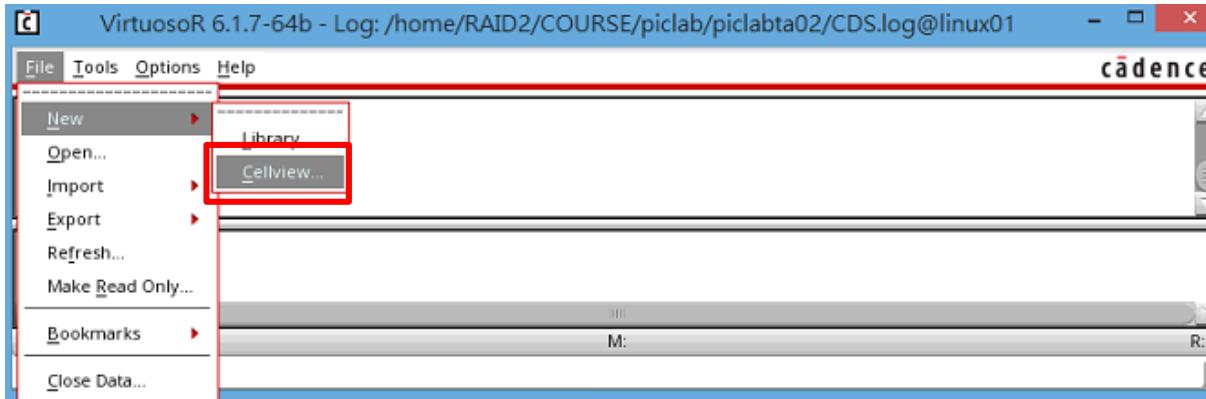
# Establish New Library

◆ File → New → Library



# Establish New Cellview under Library

## ◆ Establish a cellview under your Library

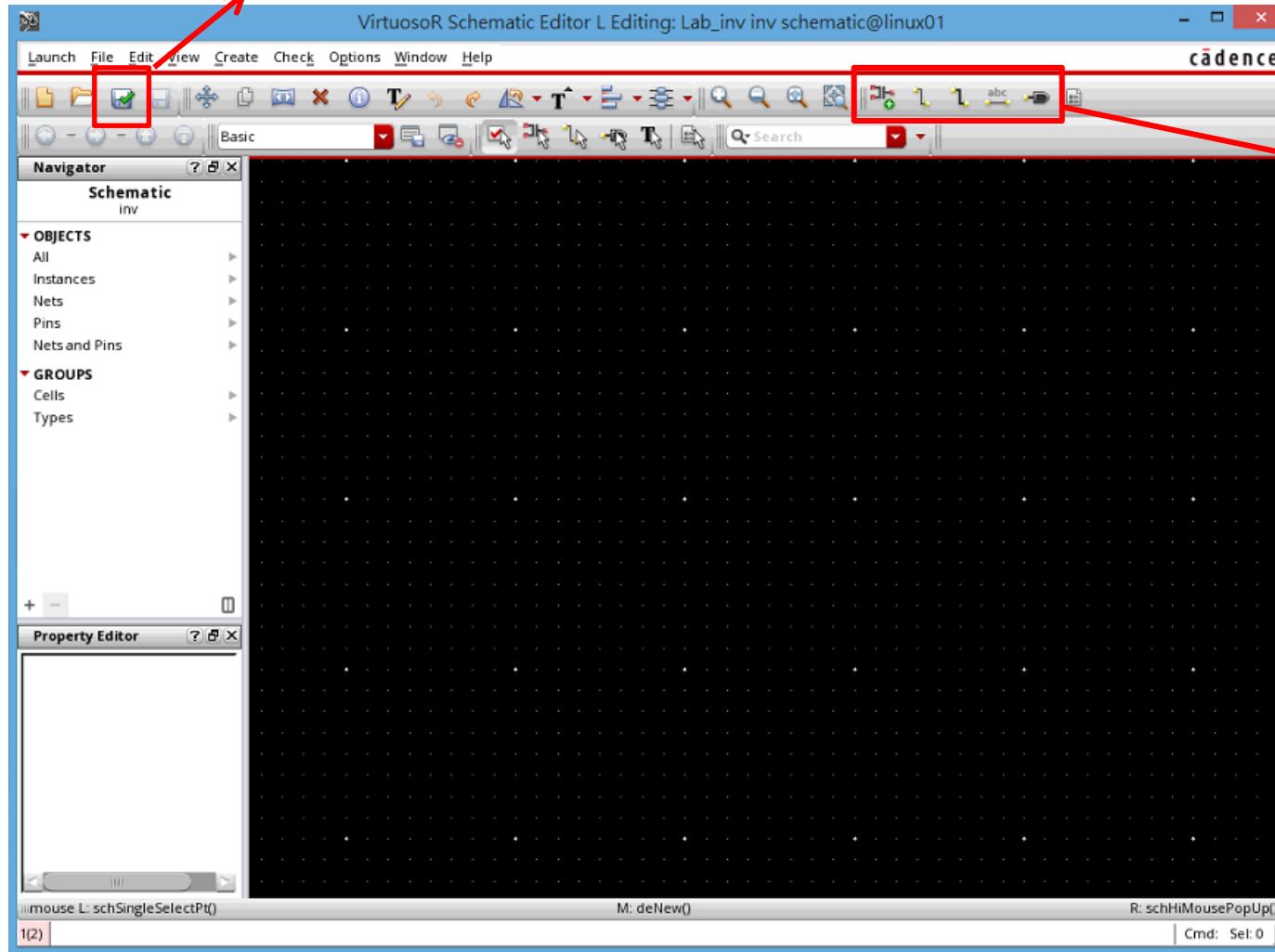


1. Choose library
2. Name of cellview
3. Choose type –**Schematic**



# Schematic Editor

Check and Save



Instance (Shortcut: i)

加入元件

Delete (Shortcut: Delete)

刪除

Property (Shortcut: q)

修改元件參數

Wire (Shortcut: w)

新增線條

Wire name (Shortcut: l)

命名線條

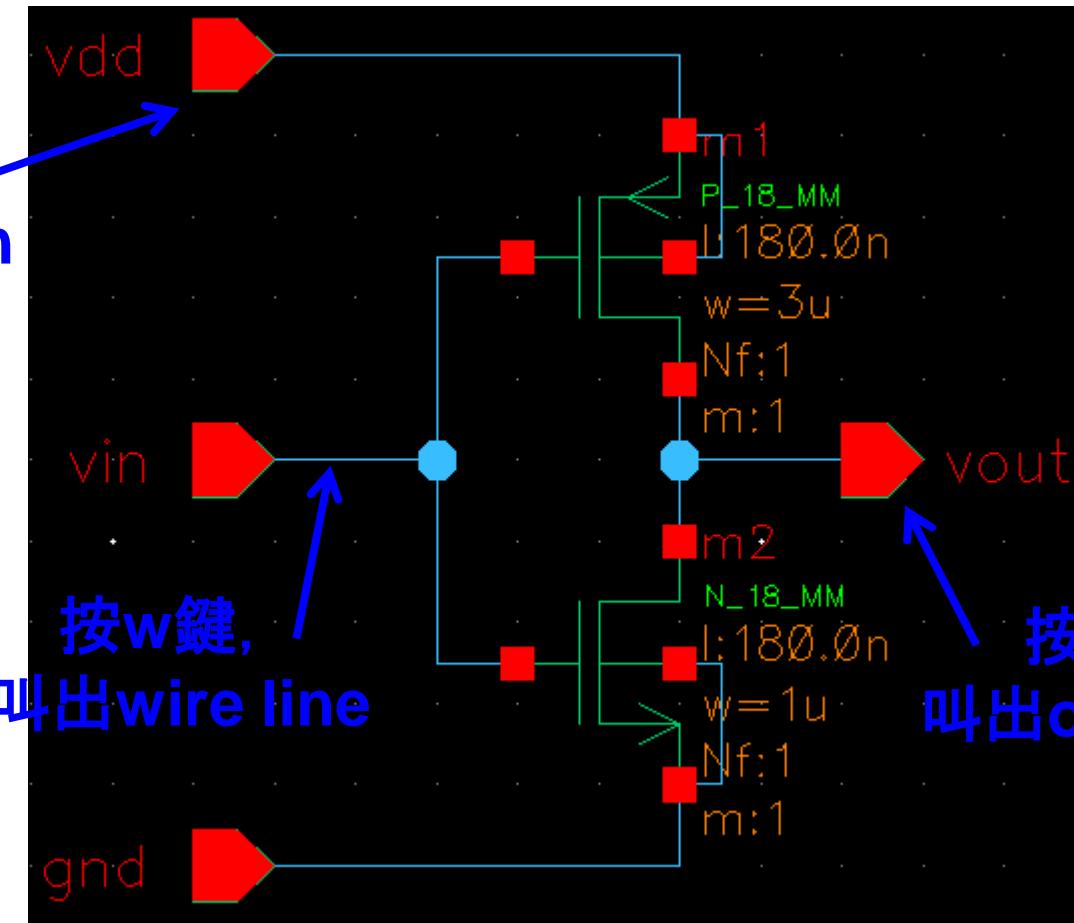
Pin (Shortcut: p)

新增Pin



# Example: Inverter

按p鍵,  
叫出input pin



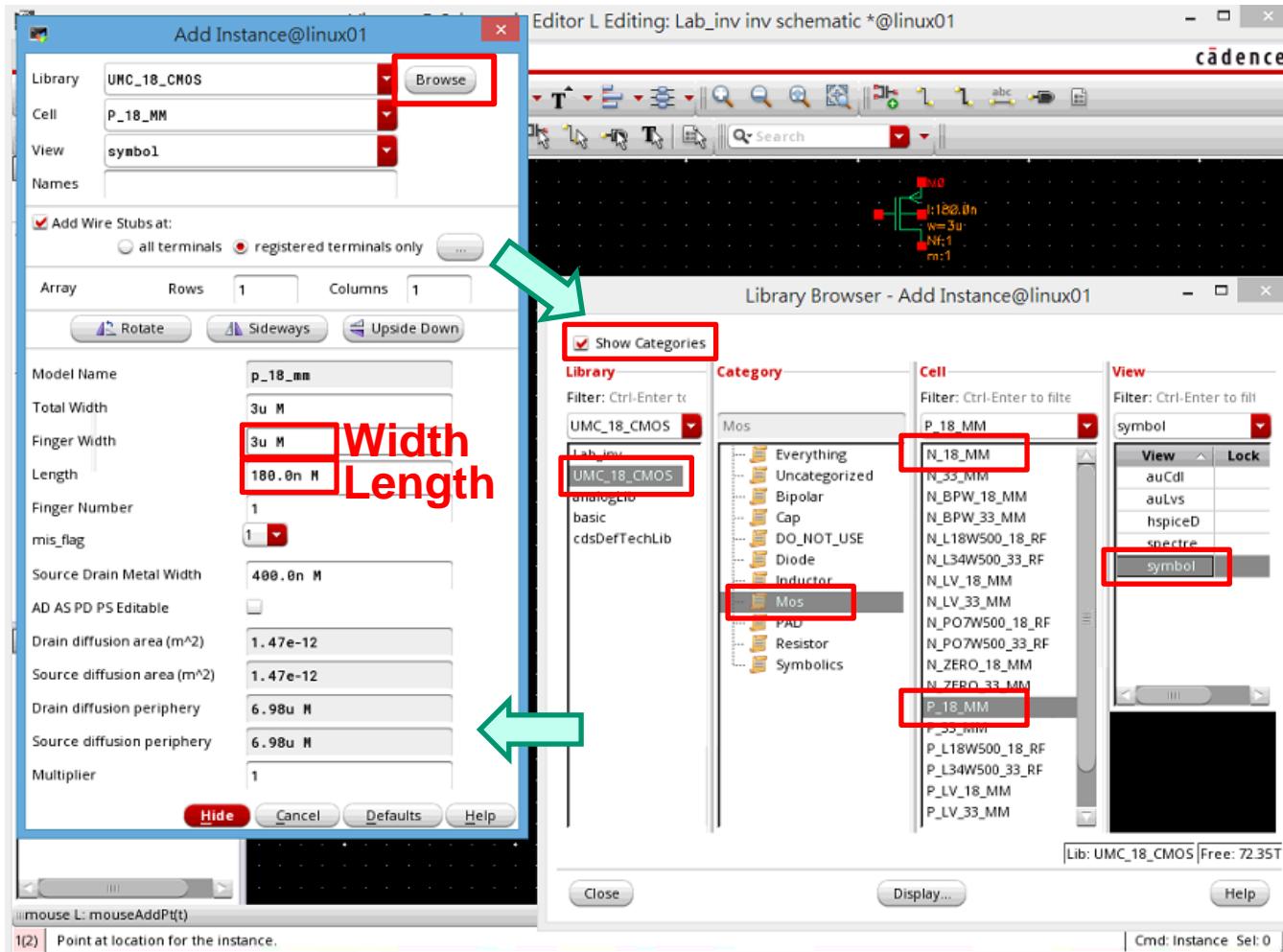
按w鍵,  
叫出wire line

按p鍵,  
叫出output pin



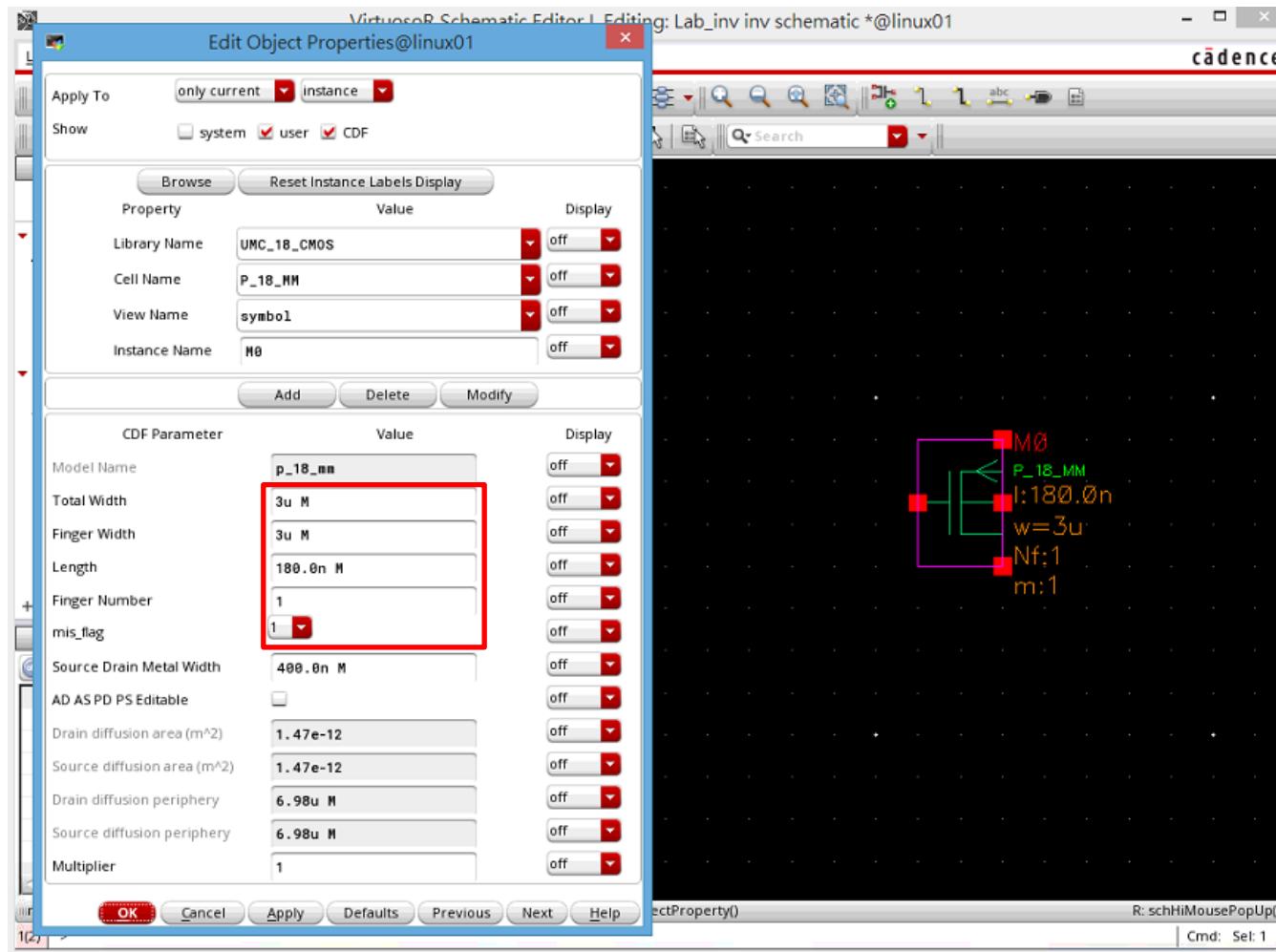
# Add Instance

◆ Click instance (shortcut: i) 按i, instance一個新的物件



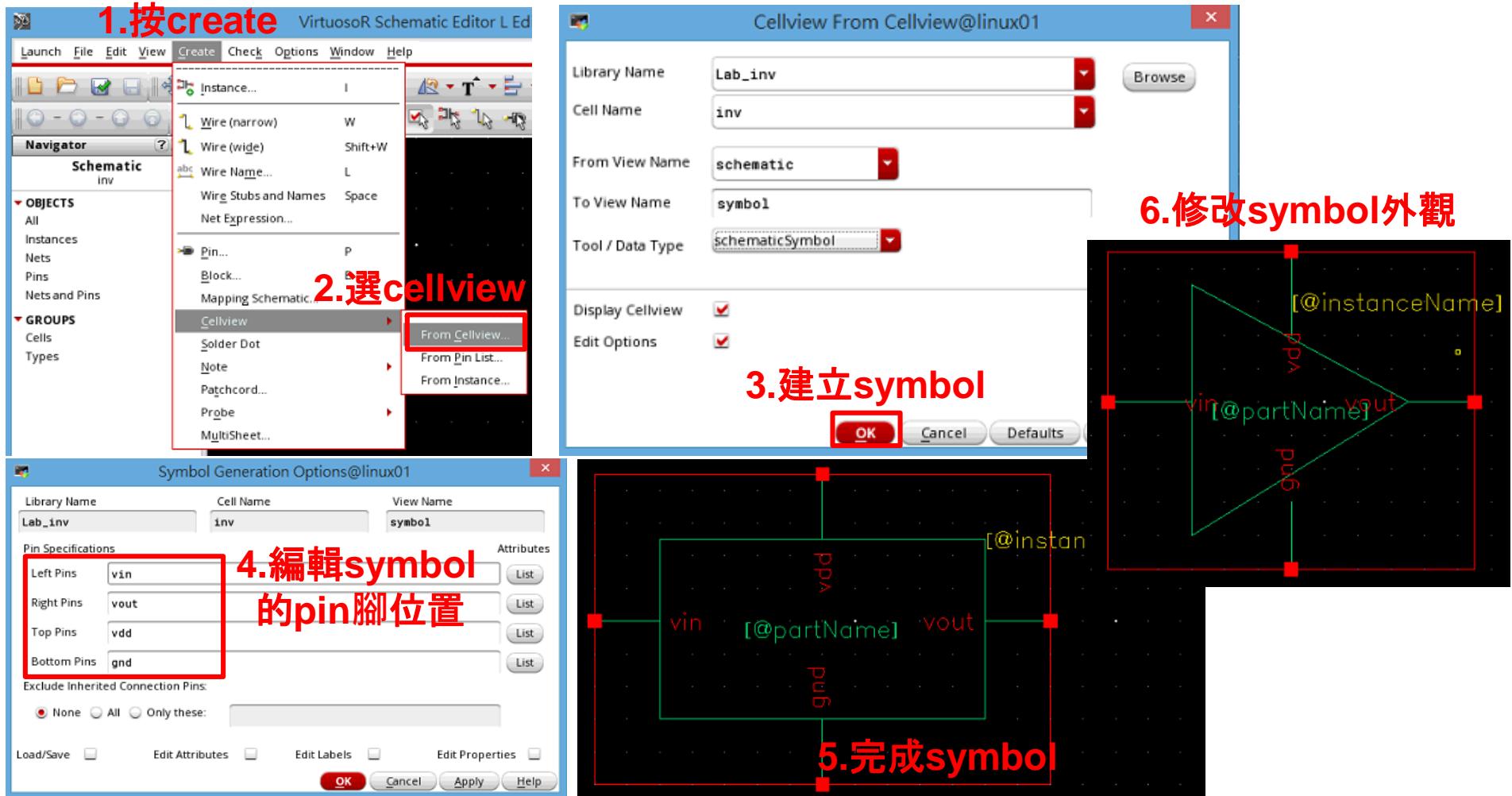
# Edit Object Parameter

◆ Choose object and click property (shortcut: q)



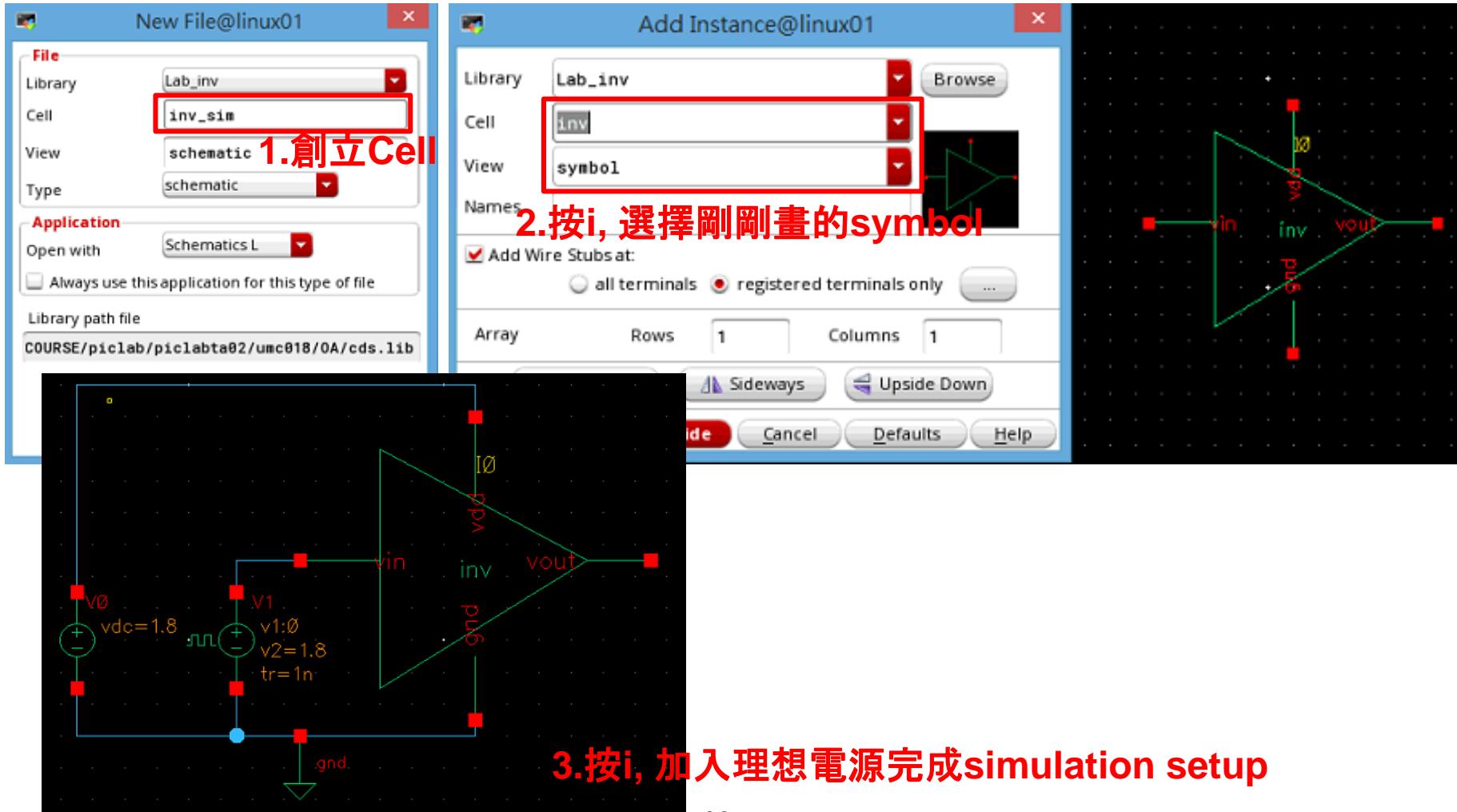
# Create Symbol

◆ Create → Cellview → From Cellview



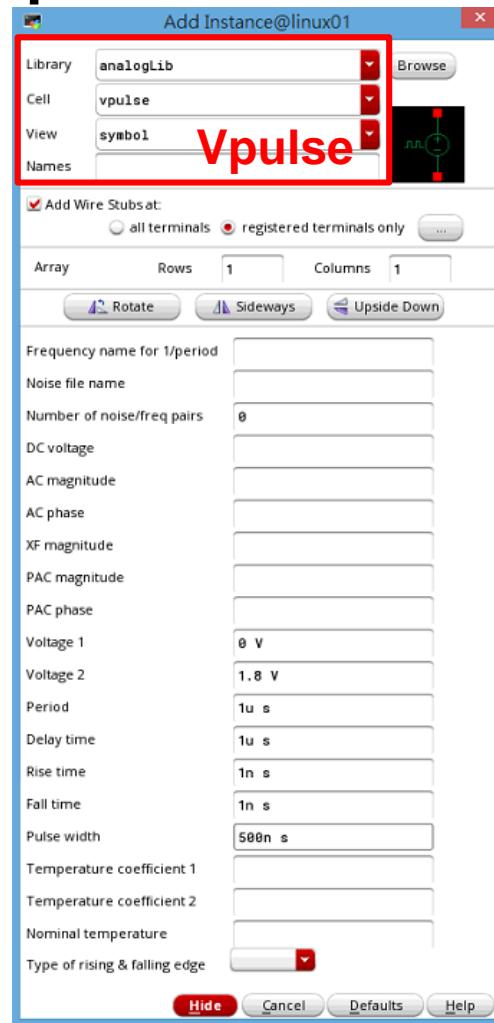
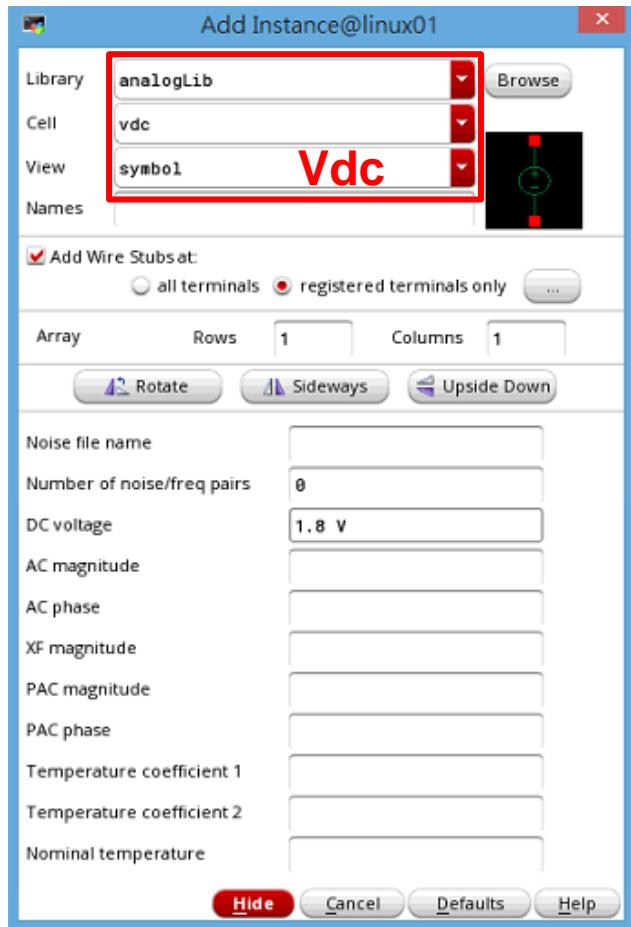
# Create Simulation Model

◆ 再同一層Library下，創另一個Cell給Simulation使用



# Add Voltage Source and Ground

- ◆ Voltage source component are in **analogLib library**



vdc: DC voltage source

gnd: ground

vsin: sin wave voltage source

vpulse: square wave voltage source

res: resistor

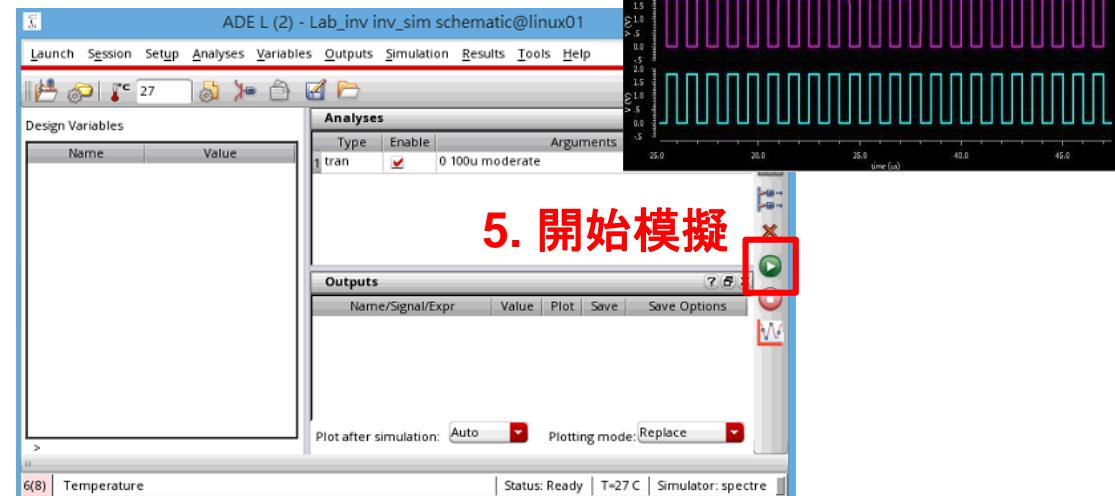
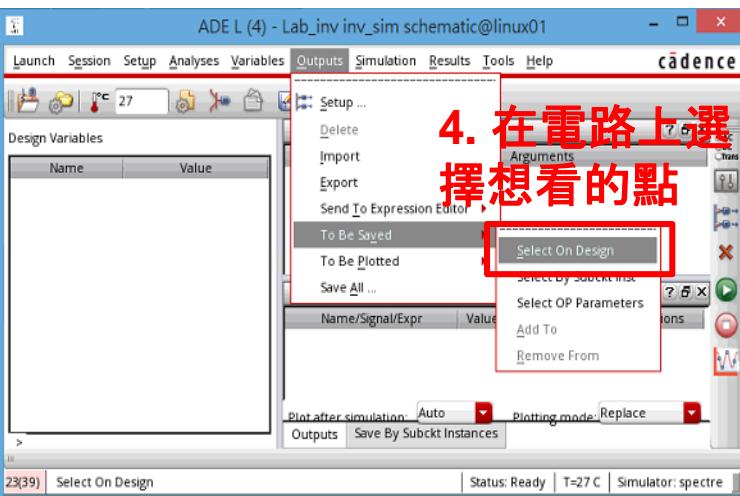
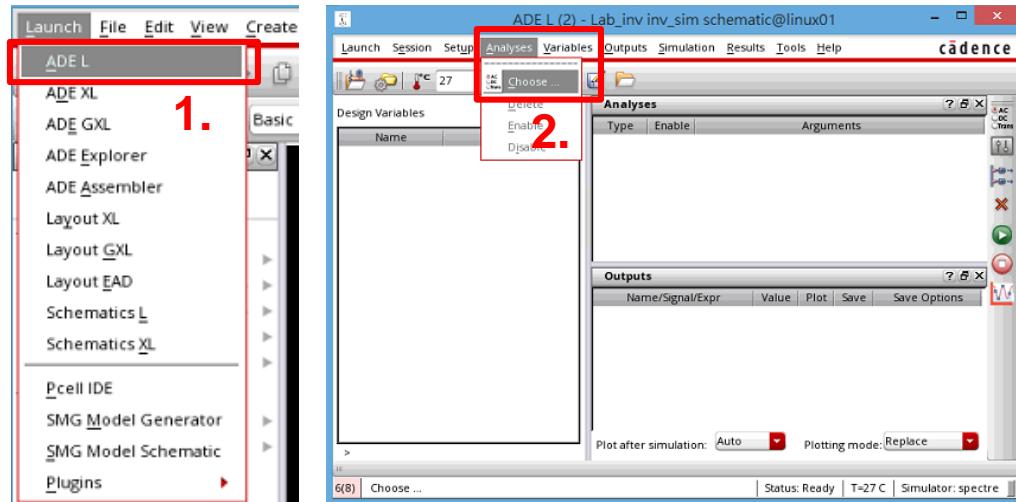
cap: capacitor

ind: inductor



# Transient Simulation

## ◆ 跑transient模擬



# 電源管理晶片設計與實作

## *Post-Layout Simulation* Cadence Tool – Virtuoso

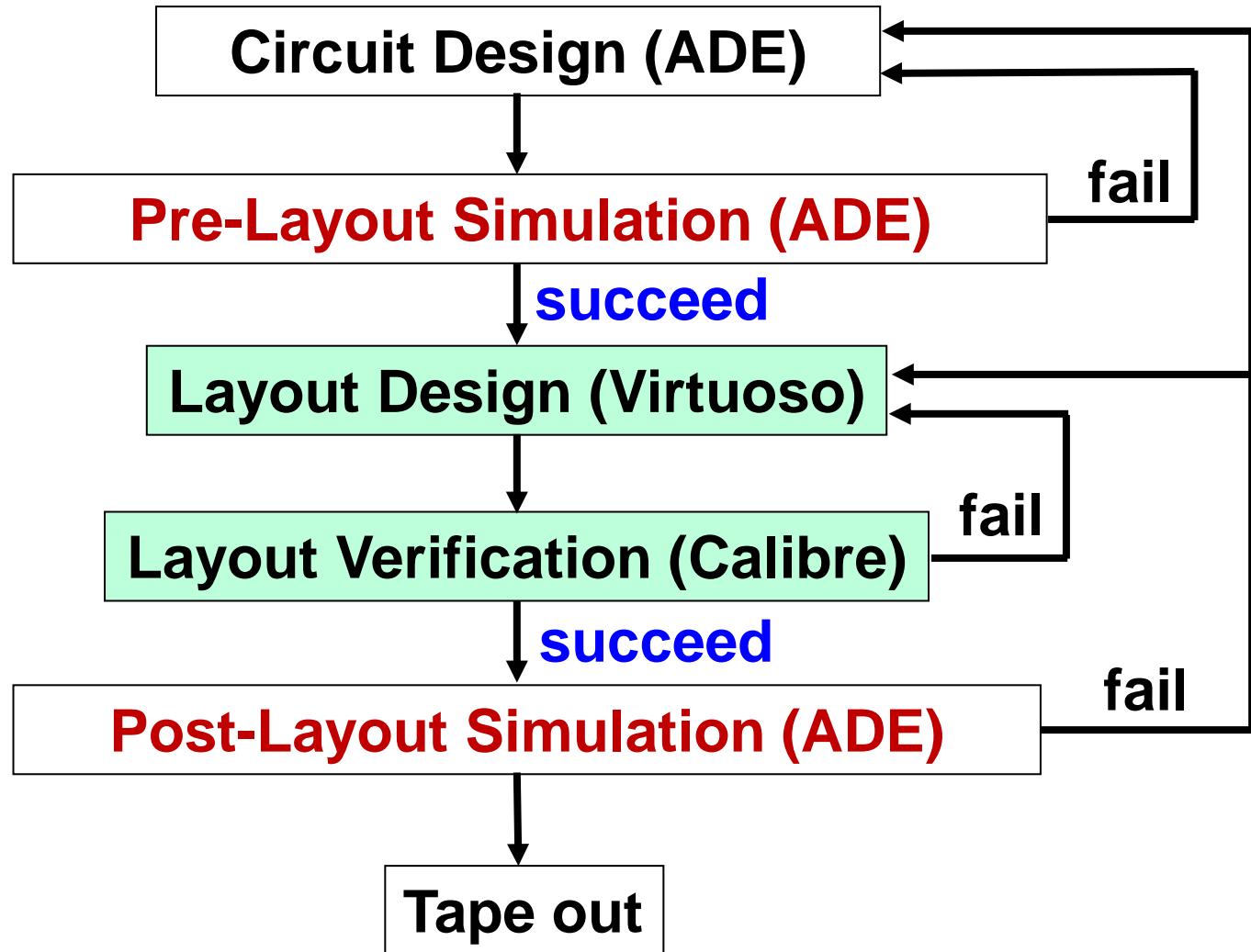
TA: 溫晨羽, 劉子寧

July 25th, 2023

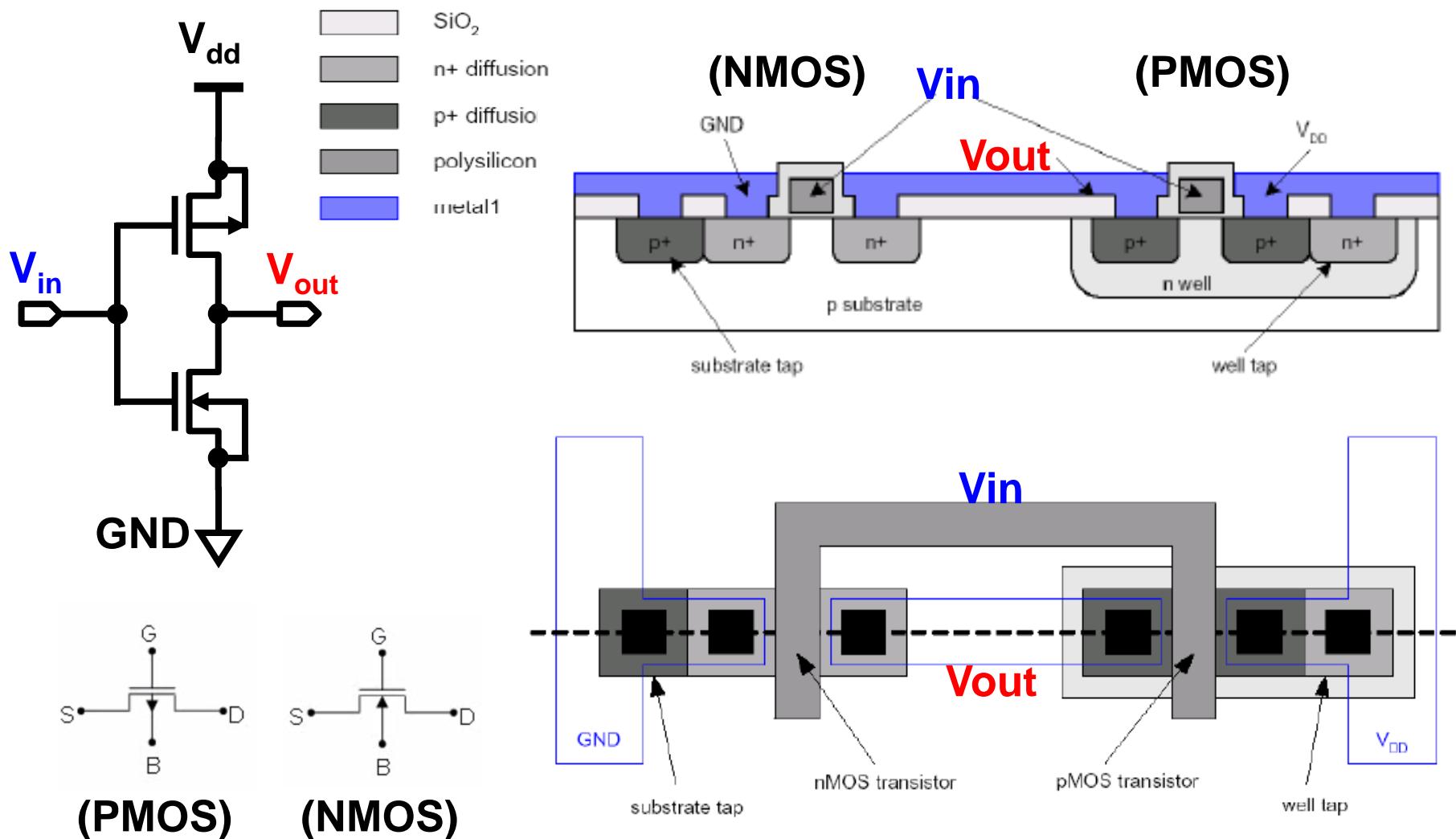
*National Yang Ming Chiao Tung University*



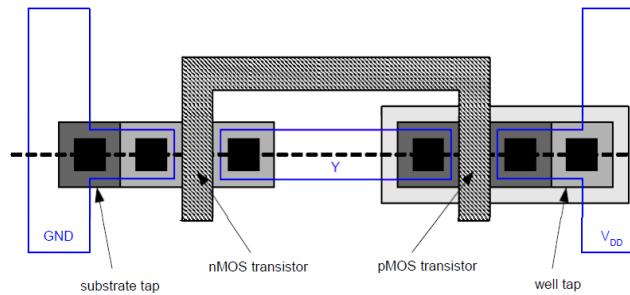
# Design Flow



# CMOS Layout Structure



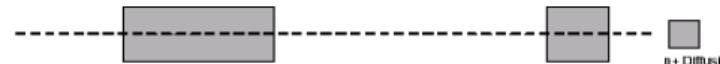
# CMOS Layout Structure



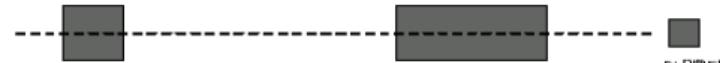
**NWELL**



**Polysilicon**



**N<sup>+</sup> Diffusion**



**P<sup>+</sup> Diffusion**



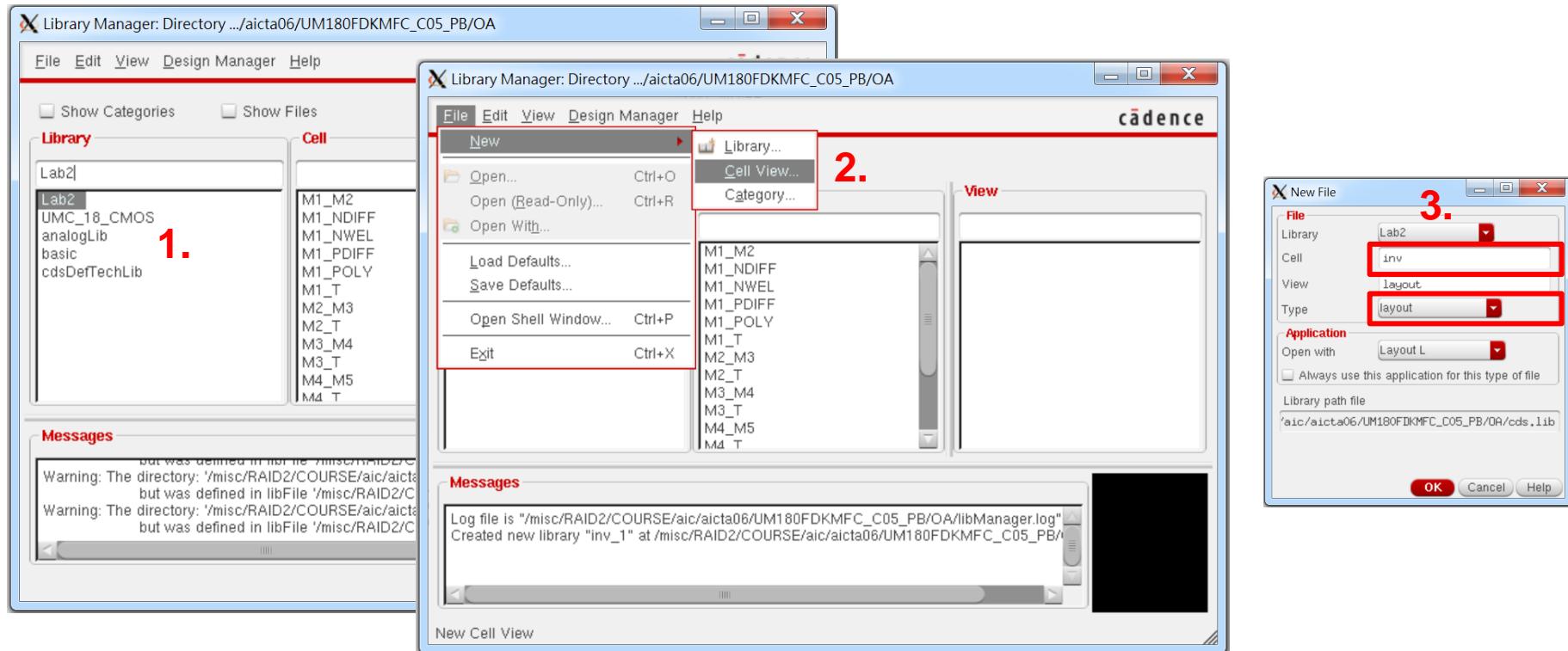
**Contact**



**Metal**

# Create Layout Cellview

- ◆ 選擇 library
- ◆ File → New → Cell View
- ◆ 輸入cell name, 選擇type為layout, 此時view name顯示layout



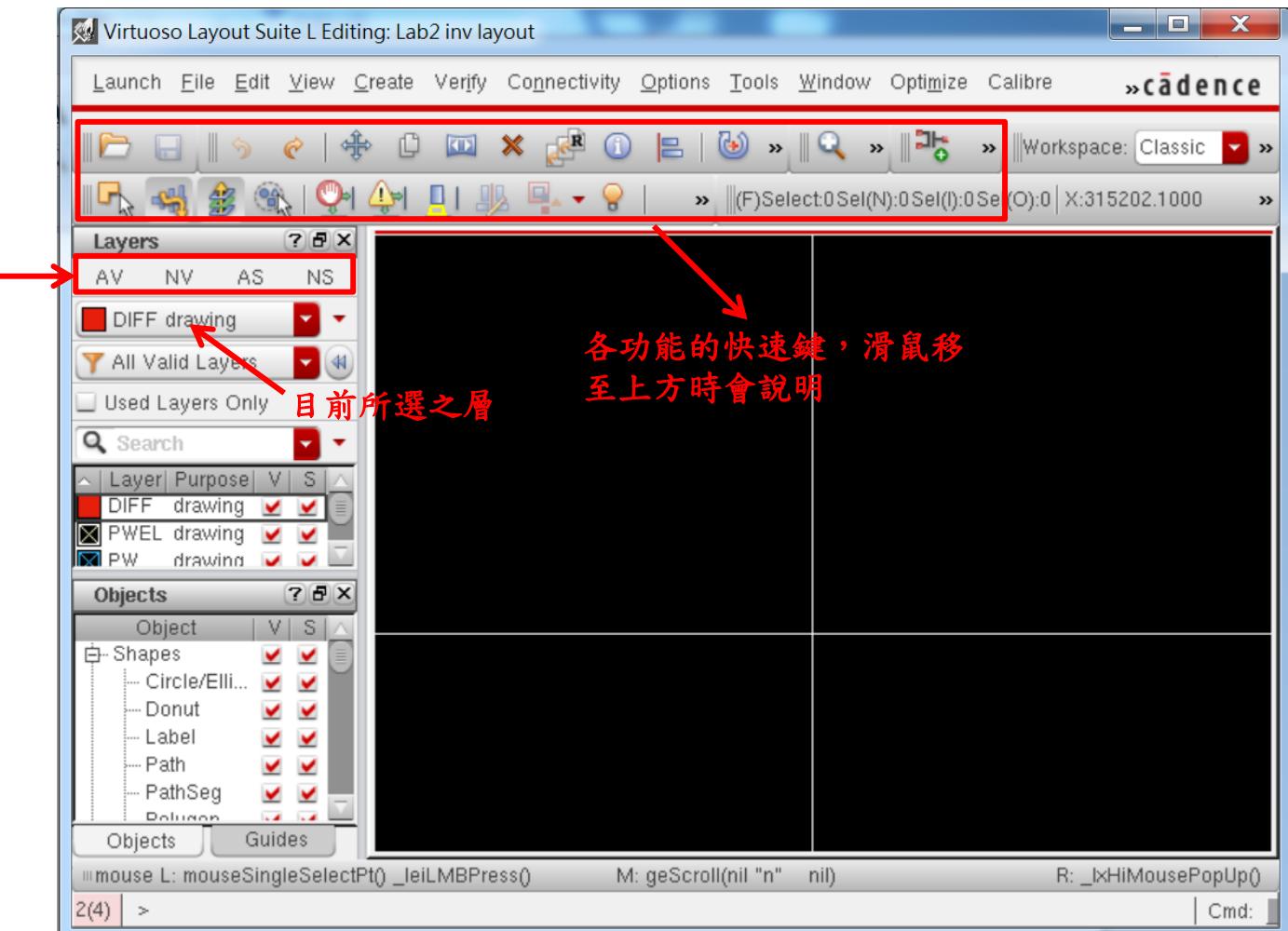
# Layout Editor

**AV:**所有層皆顯示  
於layout cellview 中

**NV:**除所選之層外  
於layout cellview  
中皆不顯示

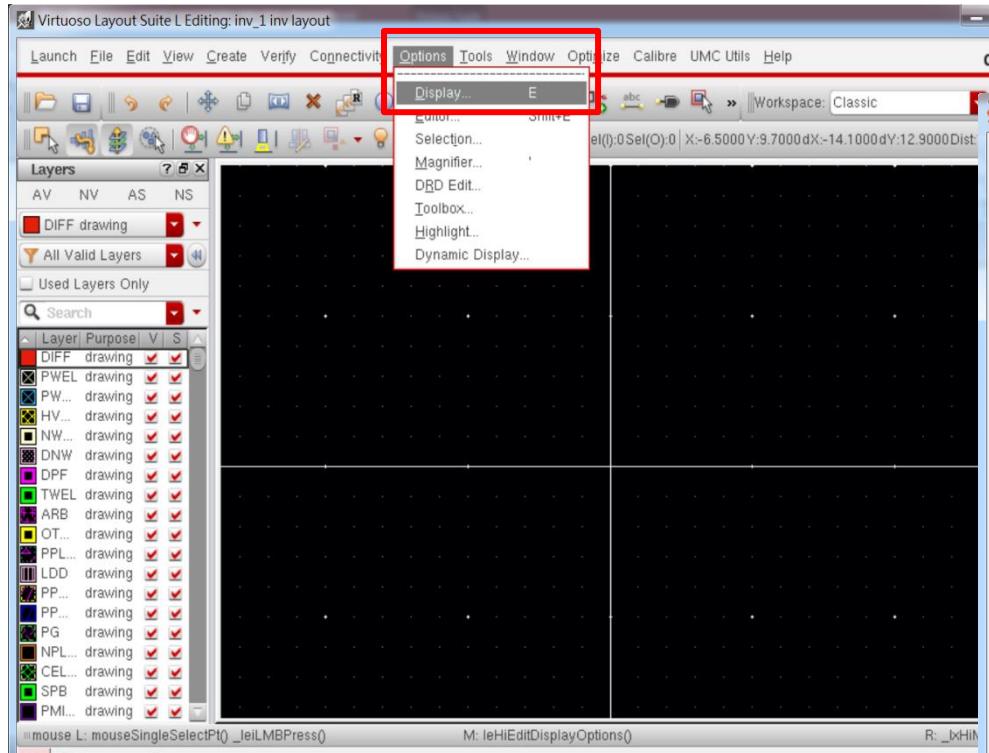
**AS:**所有圖層在  
layout cellview 中  
皆可被選取

**NS:**除所選之層外  
於layout cellview  
中皆不可被選取

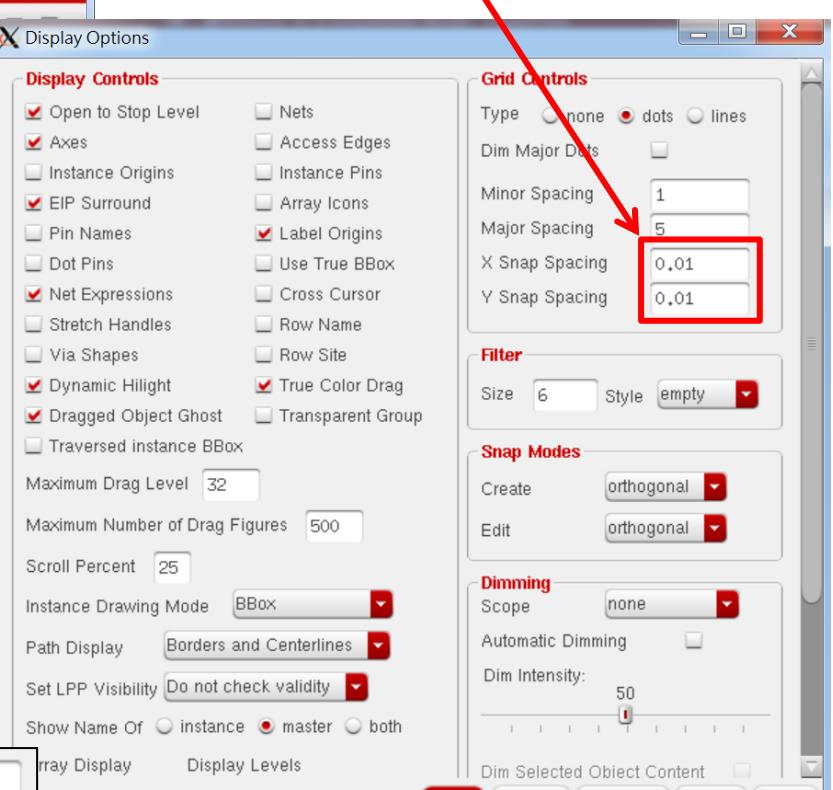


# Display Control Window

## ◆ Options → Display



此選項在頁面底下  
，請往下拉



改好後點選file，再按save to 儲存設定



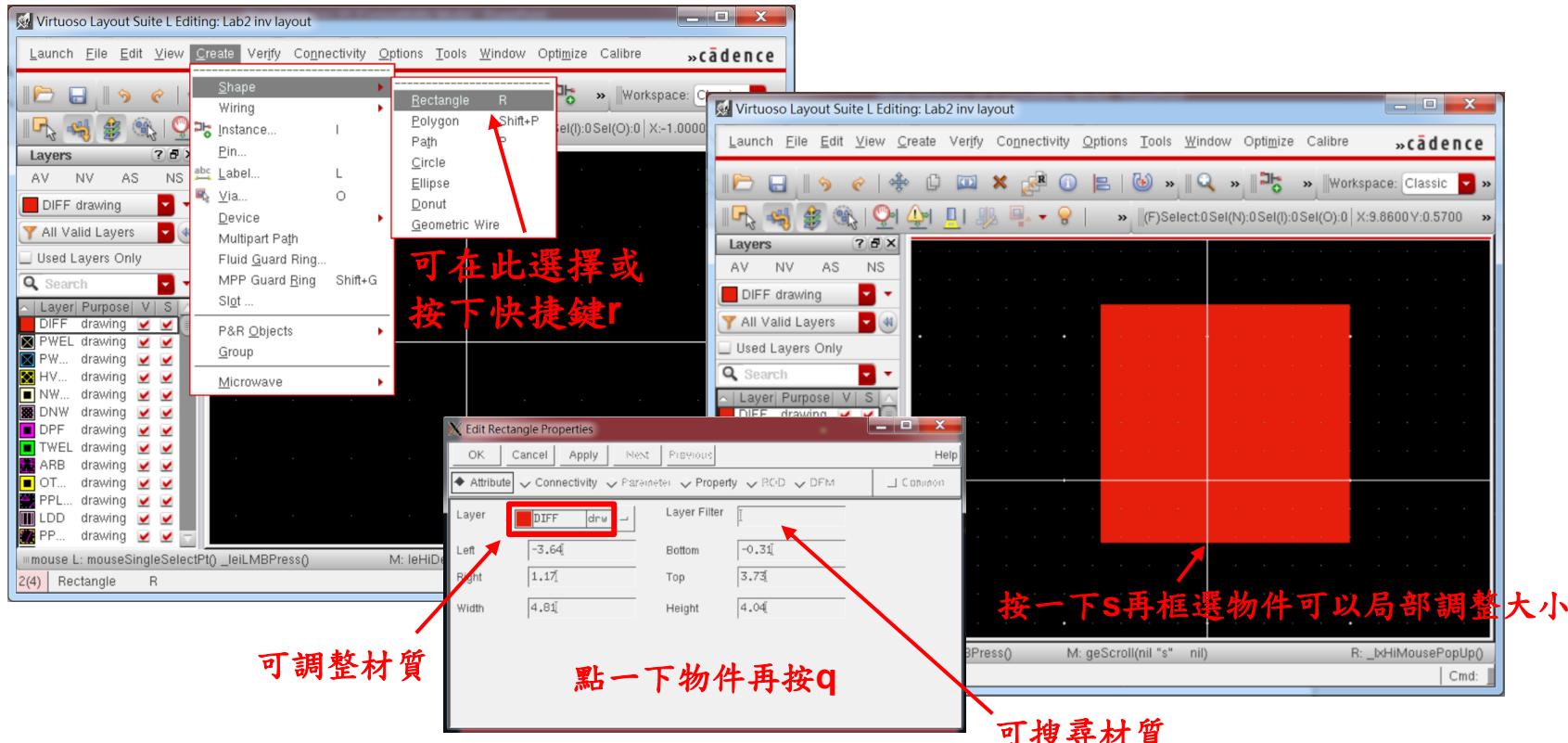
# *Layout Editor Bindkey*

## ◆ 快捷鍵

Virtuoso Hot-Key			
Key	Function	Key	Function
F2	Save	p	Create Path
m	Move	c	Copy
s	Stretch	Del	Delete
u	Undo	i	Create Instance
o	Create Contact	Ctrl+s	Split
Ctrl+z/Sfift+Z	Zoom In/Zoom Out	r	Rectangle
k/Shift+K	Ruler/Clear All Ruler	l	Label
q	Properties	f	Fit All

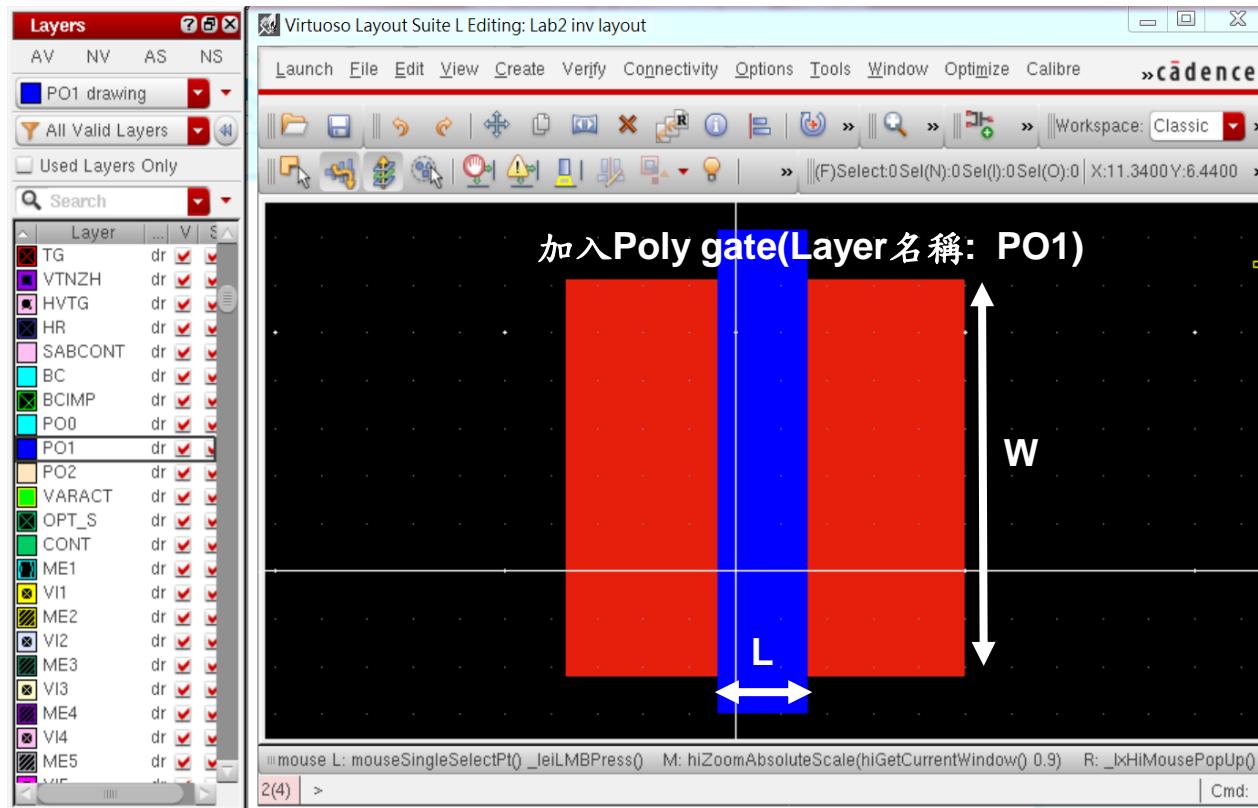
# Usage of Create and Edit (1)

- ◆ Create Rectangle (快捷鍵, r)
- ◆ Select a layer in Layers → Select function (按一下“r”)  
→ Draw an object in layout editor



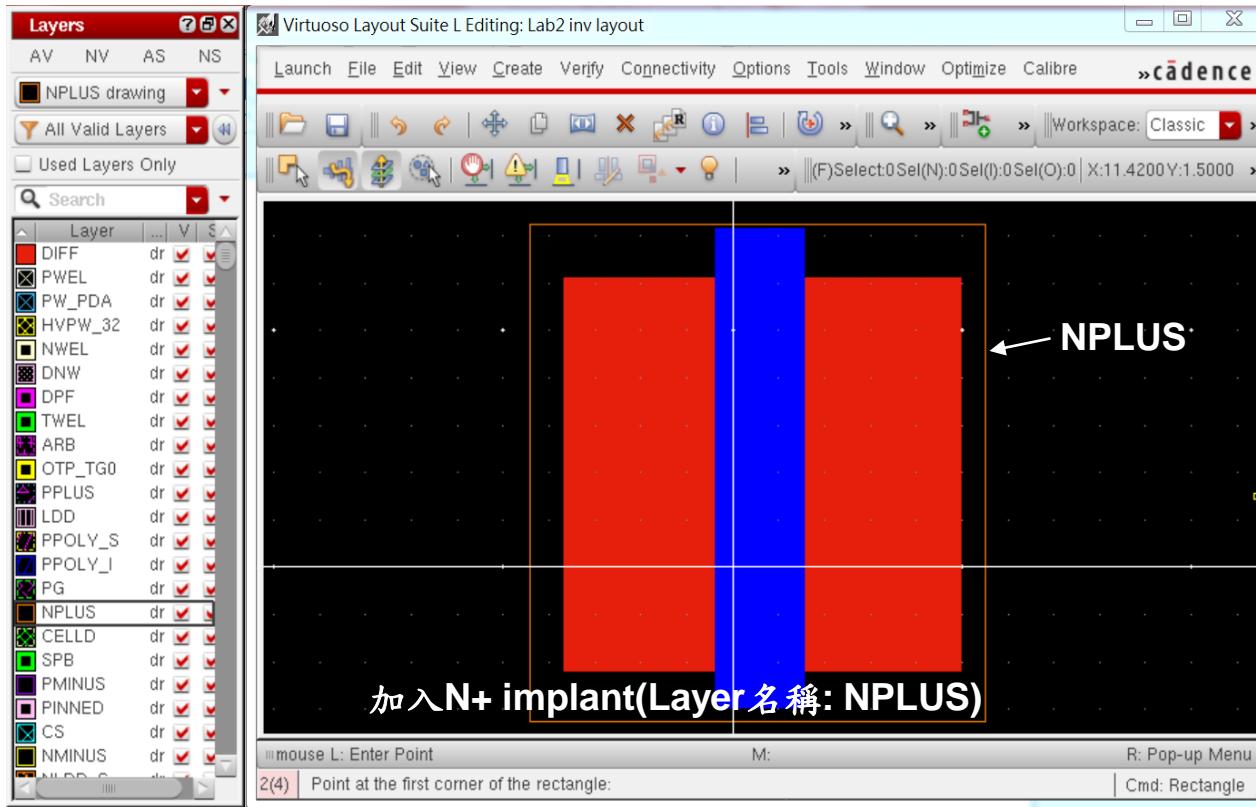
# Usage of Create and Edit (2)

- ◆ Create Rectangle (快捷鍵, r)
- ◆ Select a layer in Layers → Select function (按一下“r”)  
→ Draw an object in layout editor



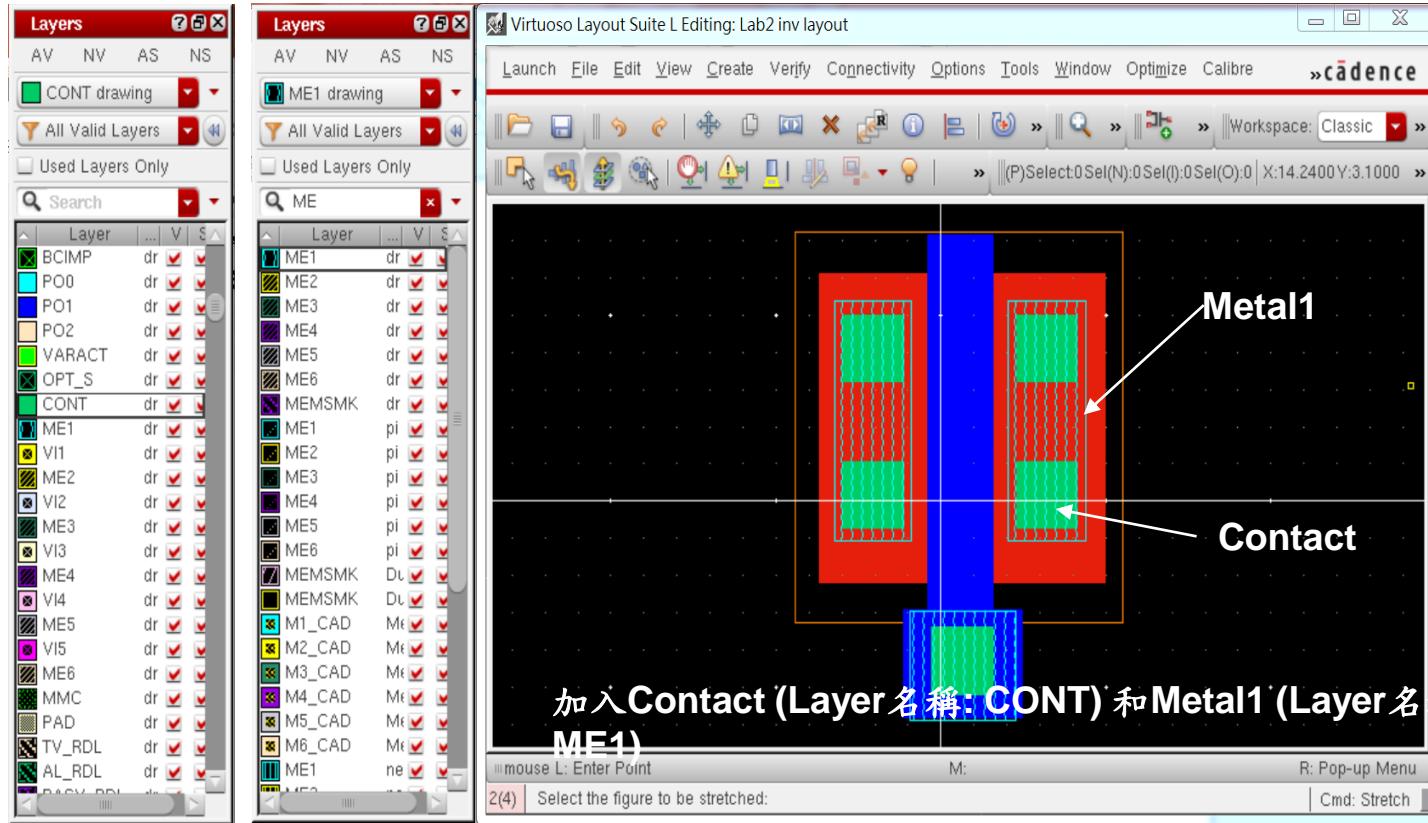
# Usage of Create and Edit (3)

- ◆ Create Rectangle (快捷鍵, r)
- ◆ Select a layer in Layers → Select function (按一下“r”)  
→ Draw an object in layout editor



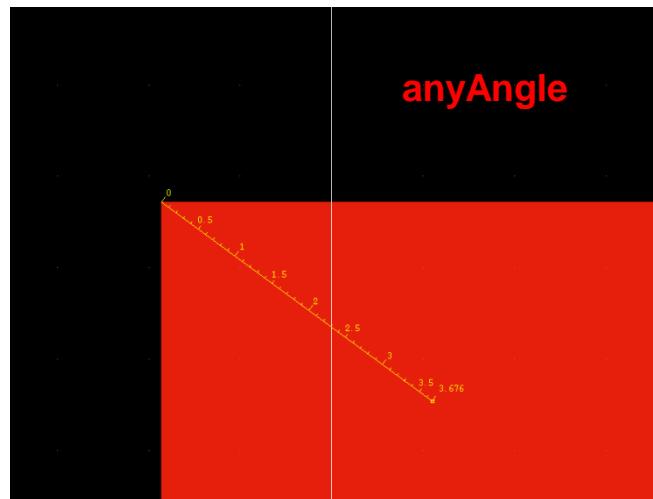
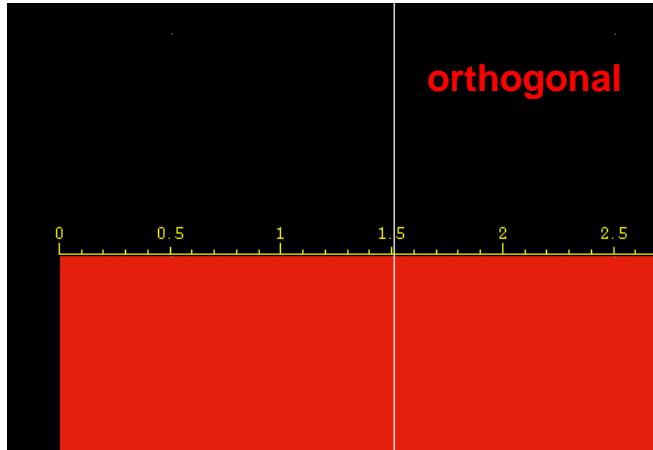
# Usage of Create and Edit (4)

- ◆ Create Rectangle (快捷鍵, r)
- ◆ Select a layer in Layers → Select function (按一下“r”)  
→ Draw an object in layout editor



# Usage of Create and Edit (5)

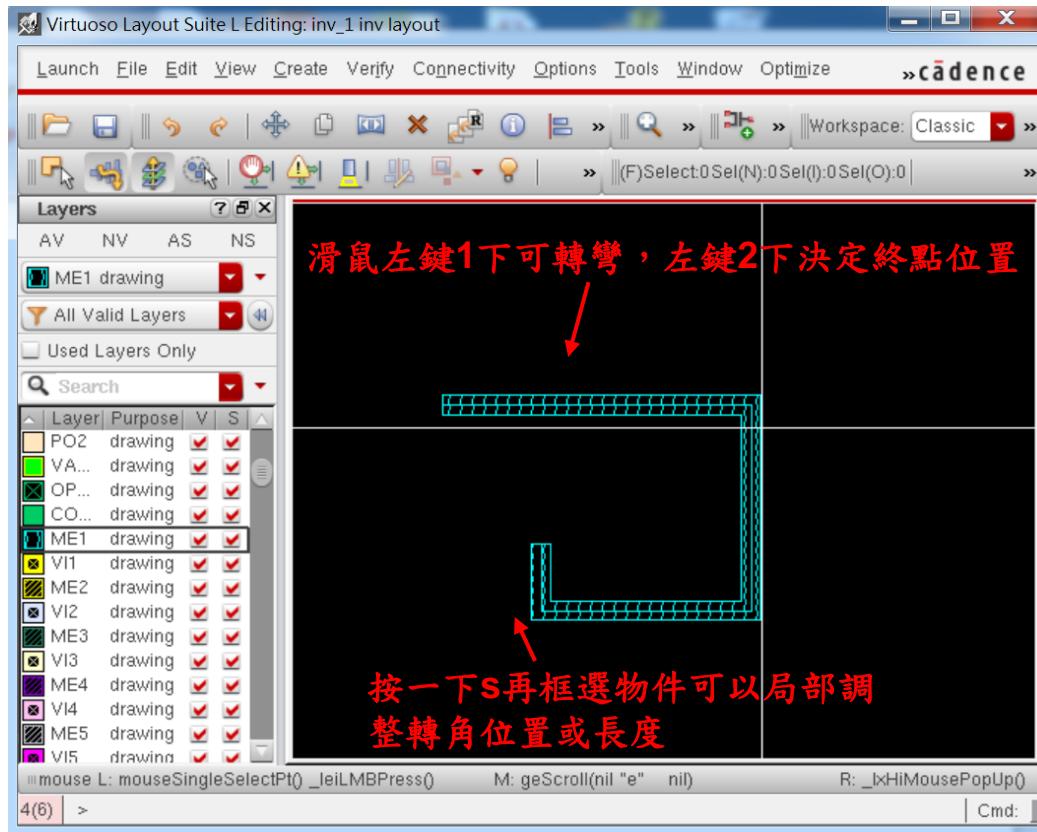
## ◆ Create Ruler (快捷鍵, k)



\*\*按Shift+k，可清除所有已存在版面的ruler

# Usage of Create and Edit (6)

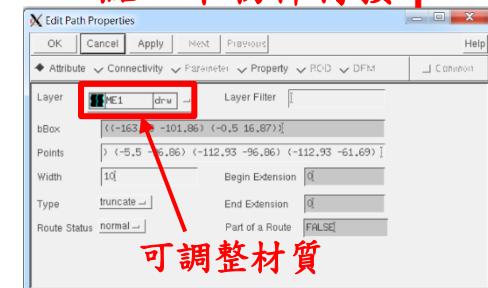
- ◆ Create Path (快捷鍵, p)
- ◆ Select a layer in layer → Select function (按一下“p”)  
→ Draw an object in layout editor



可再按F3進入調整頁面

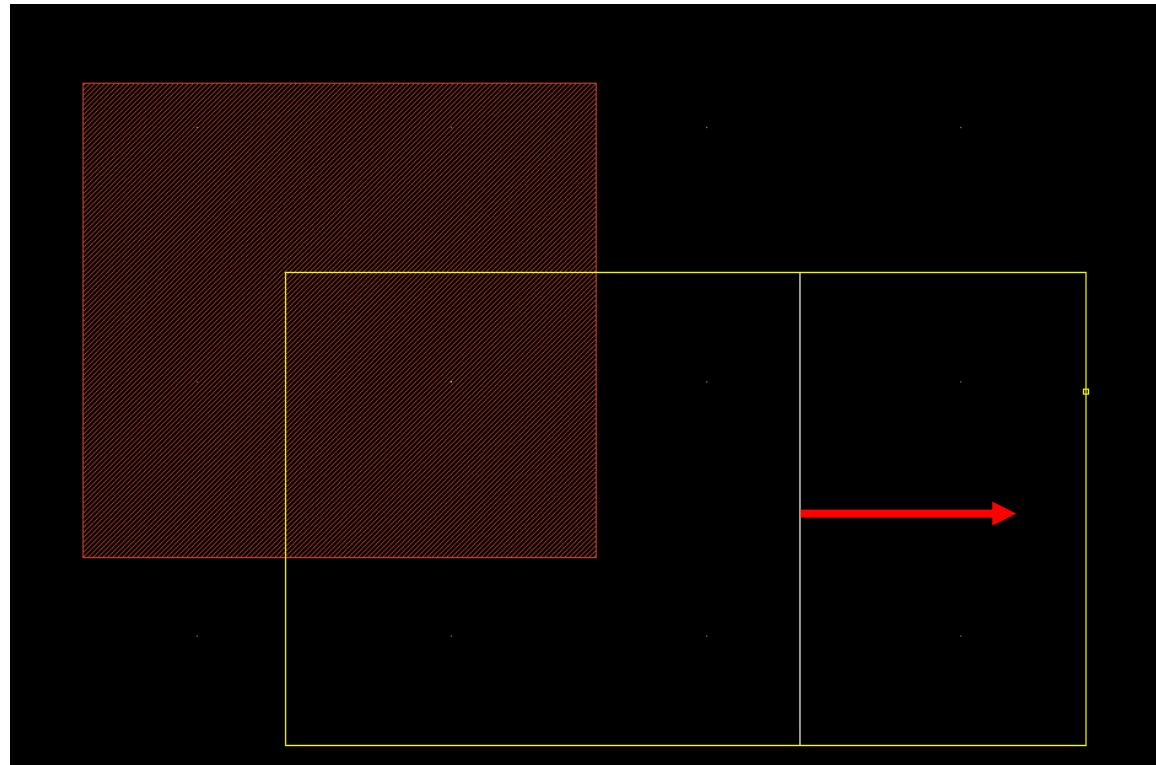


點一下物件再按q



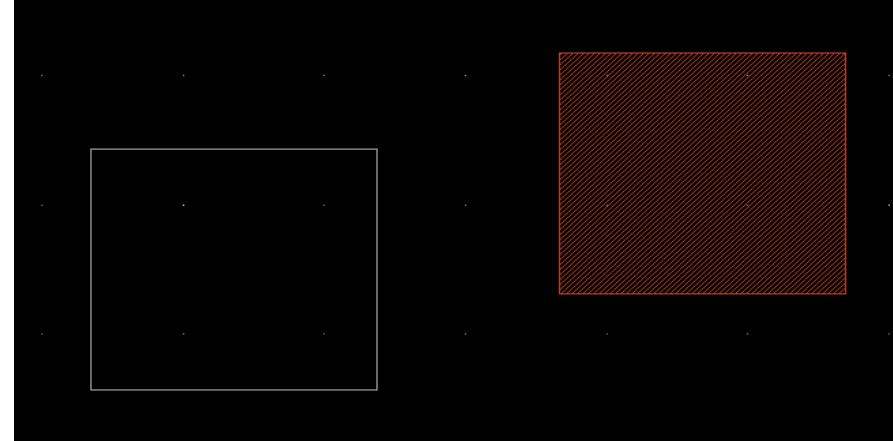
# *Usage of Create and Edit (7)*

- ◆ **Stretch** (快捷鍵, **s**)
- ◆ **Select function** (按一下“s”) → Select an area or one side of the object in layout editor



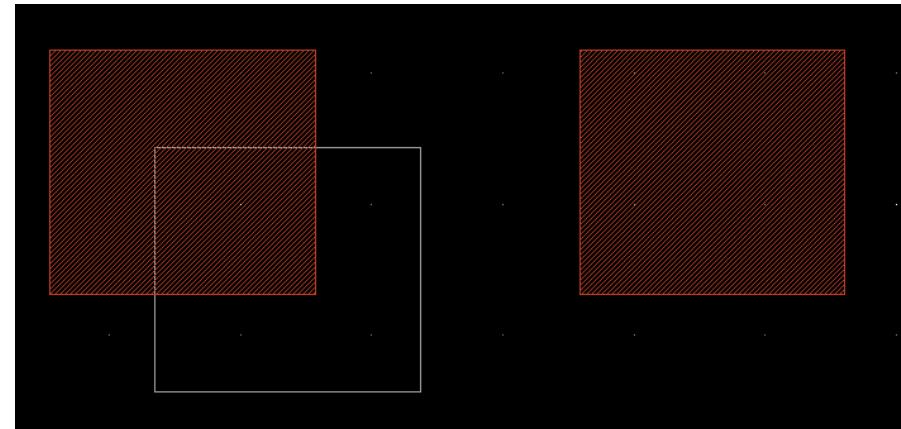
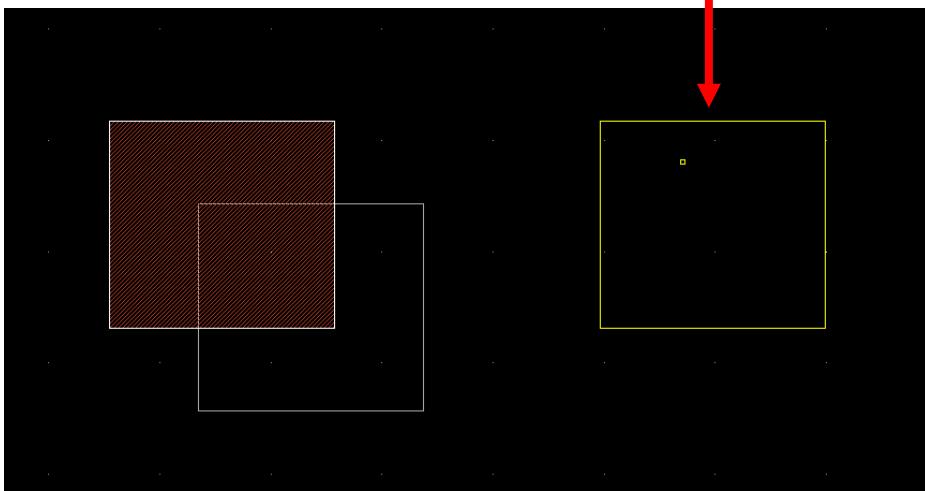
# *Usage of Create and Edit (8)*

- ◆ **Move** (快捷鍵, m)
- ◆ Select function (按一下“m”) → Select an object in layout editor → Move to the destination



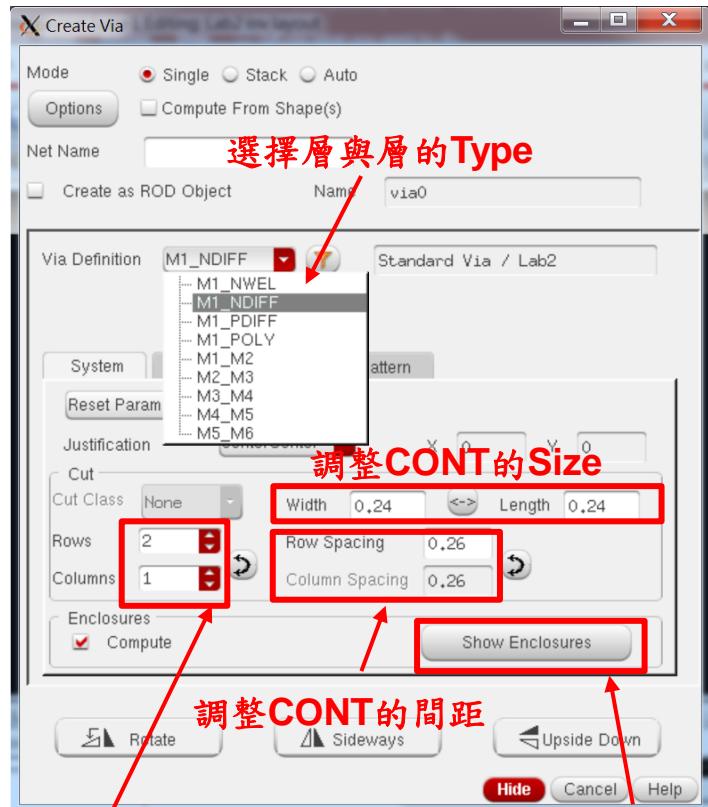
# *Usage of Create and Edit (9)*

- ◆ **Copy** (快捷鍵, c)
- ◆ **Select function** (按一下“c”) → Select an object in layout editor → Copy to the destination



# Usage of Create and Edit (10)

- ◆ Create Via/Contact (快捷鍵, o)
- ◆ Select function (按一下“o”) → Select an object in layout editor

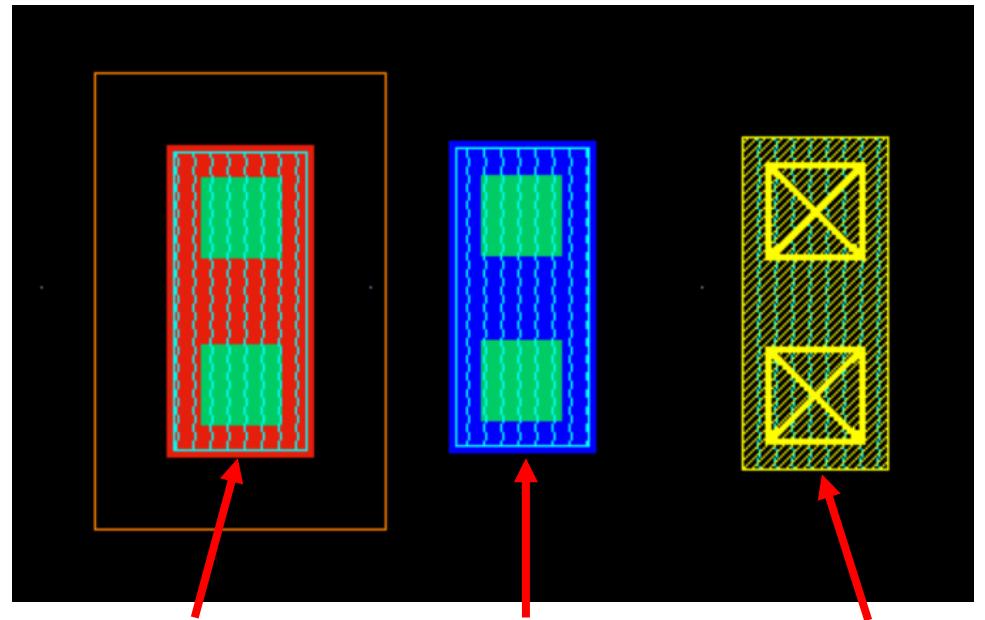


選擇層與層的Type

調整CONT的Size

調整CONT行或列的排列個數

調整層的Size



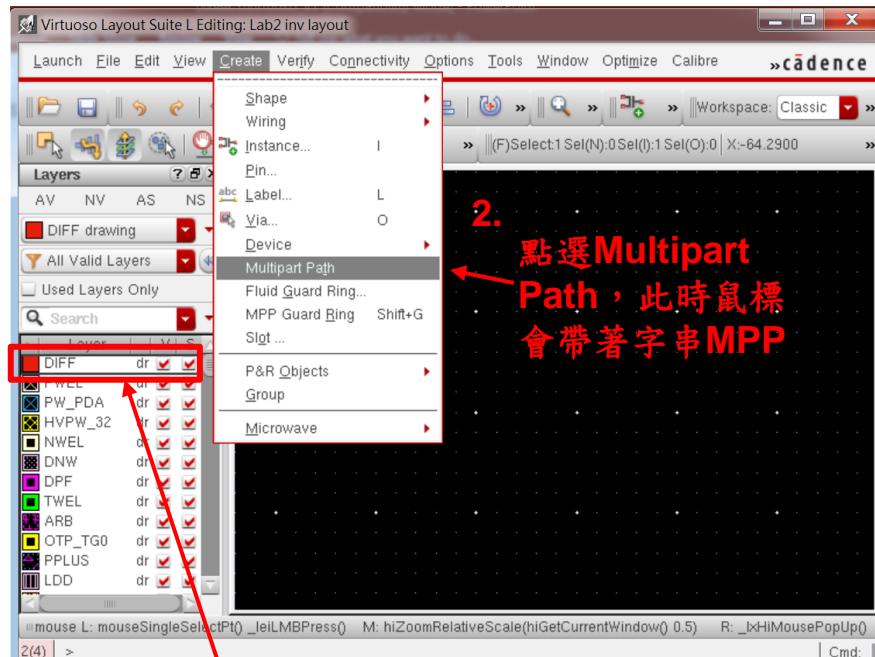
含 DIFF, NPLUS,  
CONT, ME1 的多  
層結構

含 Poly, CONT,  
ME1 的多層結構

含 ME1, Via1,  
ME2 的多層結構

# Usage of Create and Edit (11)

- ◆ Another way to create multi-layer (畫 P-type Pickup)
- ◆ Create → Multipart Path → F3 to adjust path parameters  
→ draw in Layout Editor



1. 先點選DIFF層當path基底材質



設定附屬path層的材質  
(\*接續下頁)



# Usage of Create and Edit (12)

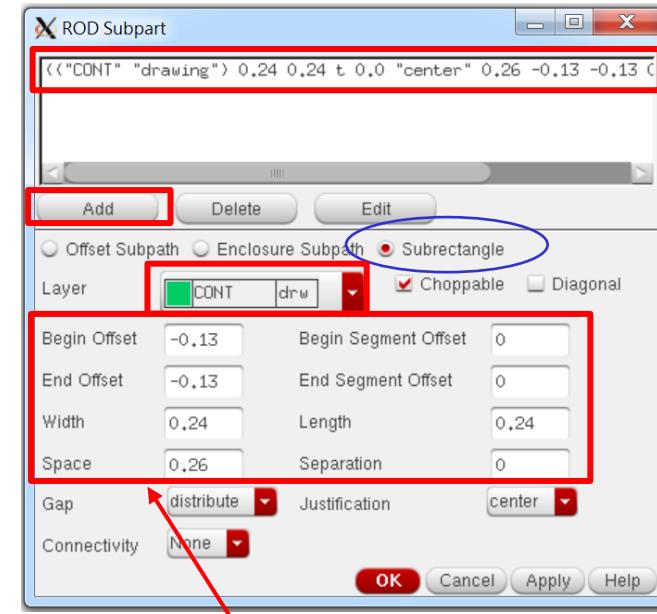
## ◆ Another way to create multi-layer (承續前頁)



設定材質 → 選上列已有物件再按edit編輯

按add後出現在上列才算有設定成功

Subrectangle: 可建立CONT或VIA等週期式陣列結構



設定CONT的大小與間距和偏移量，設定完記得按add，數值須符合design rule (請輸入圖中數值)

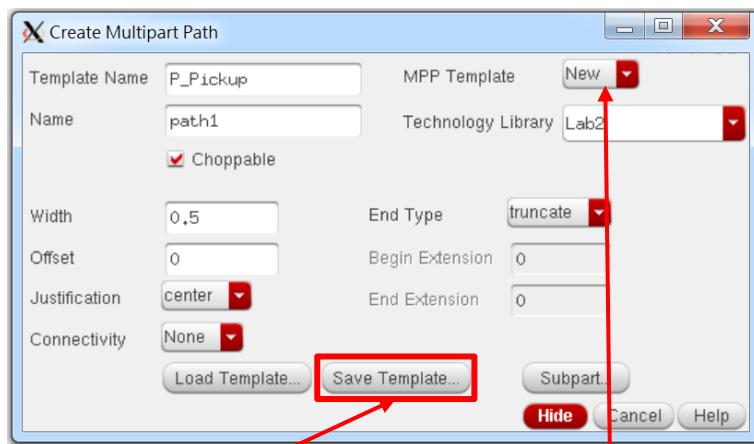
依據DIFF的寬度，設定Metal1和P+的寬度和偏移量，設定完記得按add，數值須符合design rule的間距

\*\*全部設定完，請確認白色視窗內數值是否設定正確，再按OK，會返回上一層頁面 (\*接續下頁)



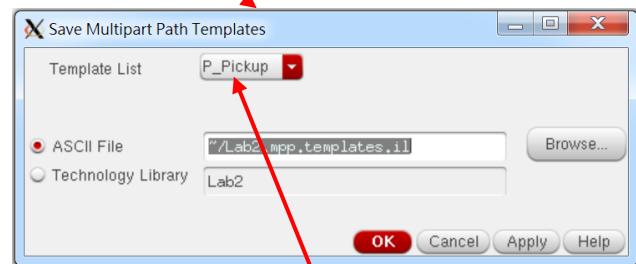
# Usage of Create and Edit (13)

## ◆ Another way to create multi-layer (承續前頁)



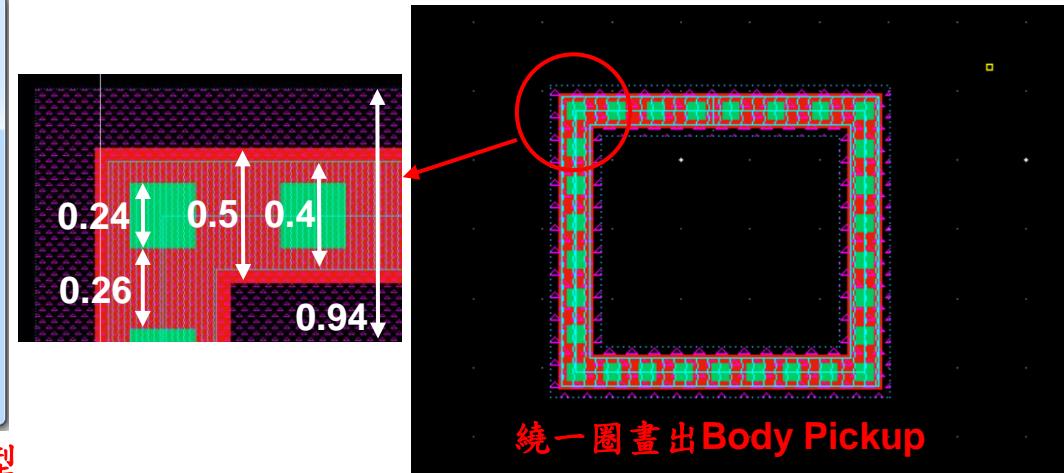
設定完記得存檔

存起來不同的path型  
式可以在這裡選擇

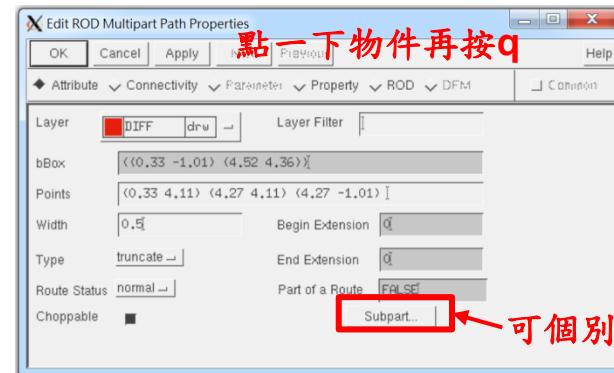


命名不同這裡名字會不同，N-type Pickup請另外設定保存

多層path設定完成，回到編輯版面，畫出下圖



繞一圈畫出Body Pickup

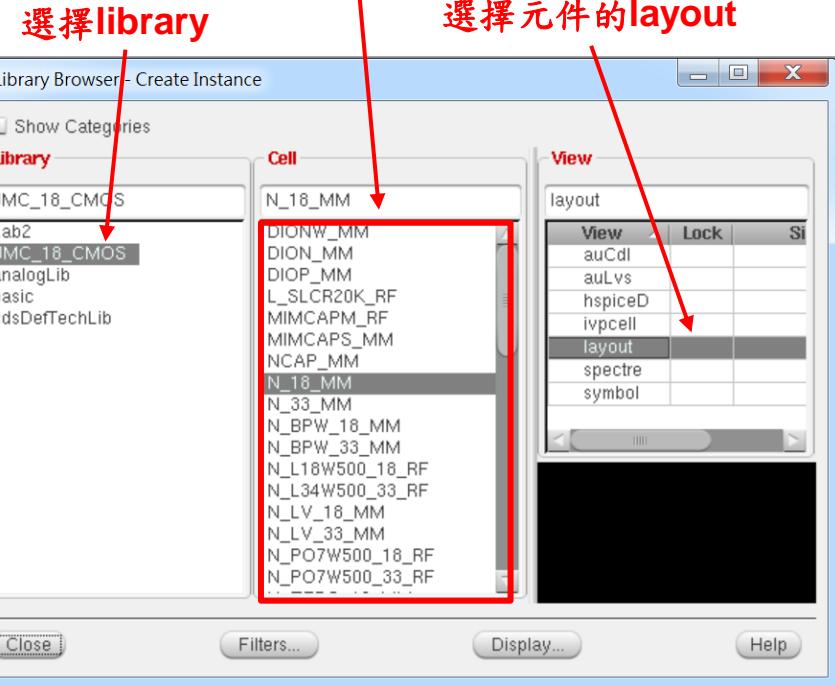
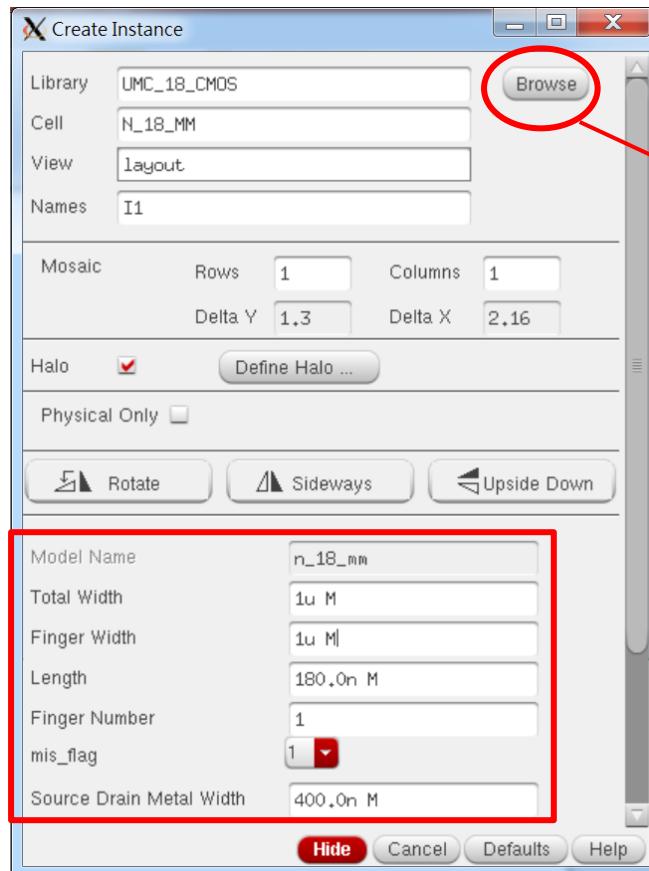


可個別再調整



# Usage of Create and Edit (14)

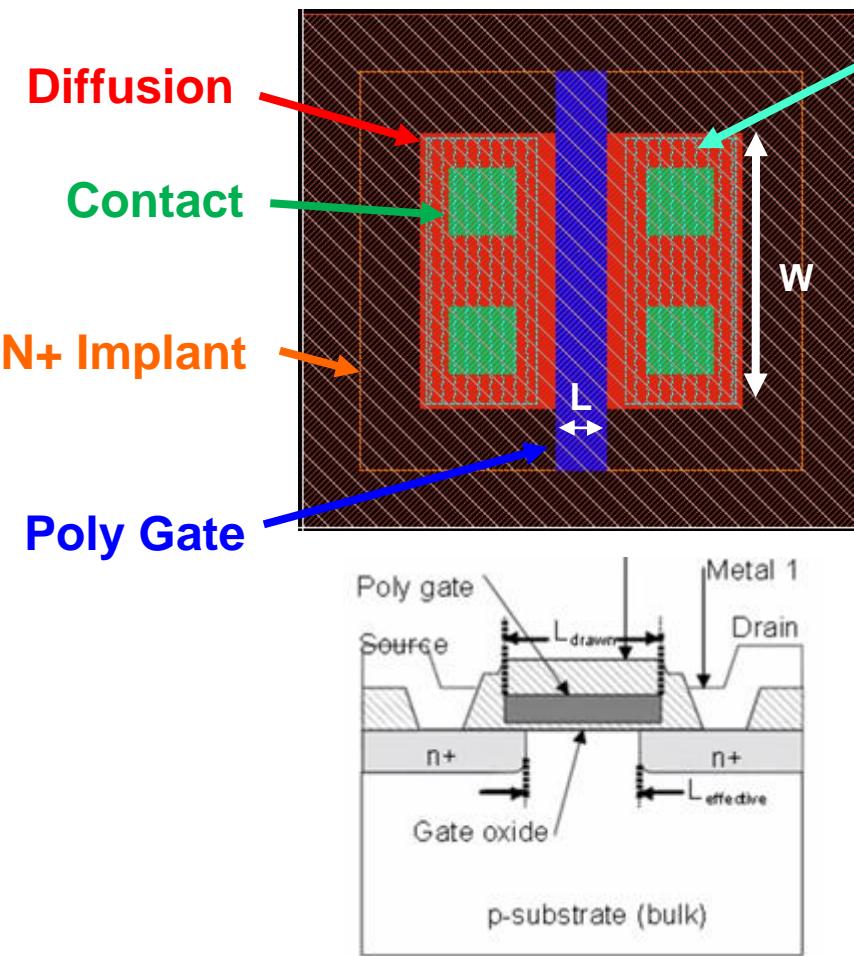
## ◆ Create instance (快捷鍵, i)



\*\*Foundry提供的元件庫內有參數化的主動或被動元件 (Pcells)，供設計者依需求使用

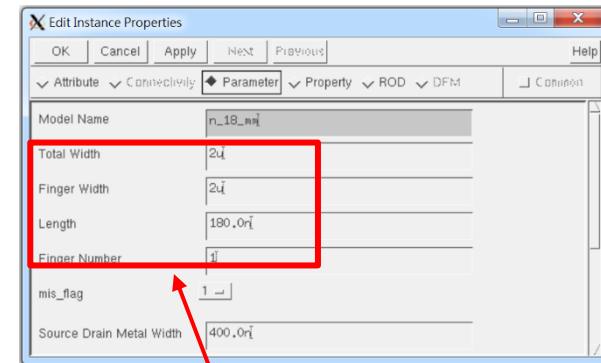


# Using Parameterized cell (Pcell) 1.8V NMOS



Metal1

點一下已生成的物件再按q

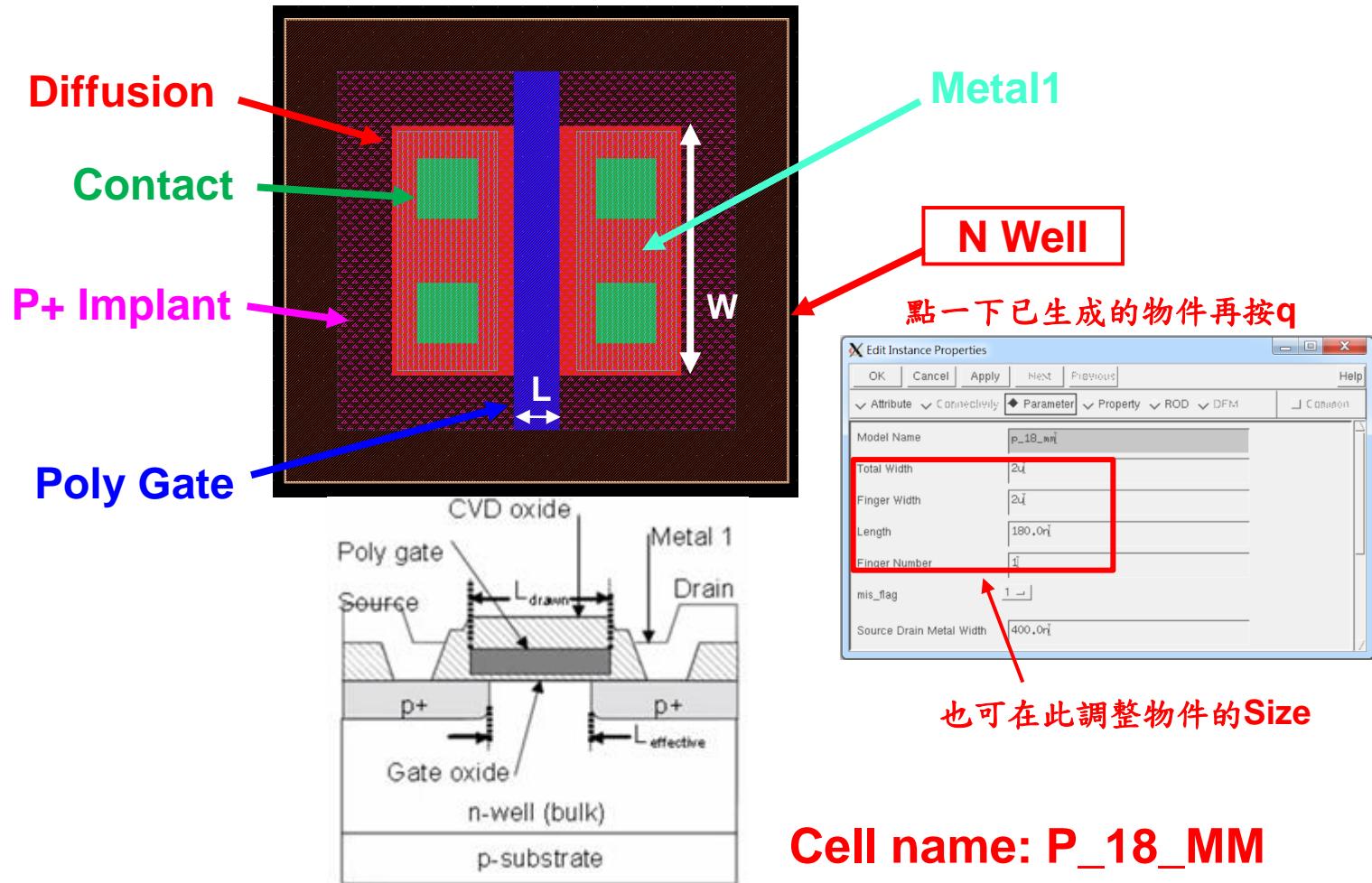


也可在此調整物件的Size

Cell name: N\_18\_MM

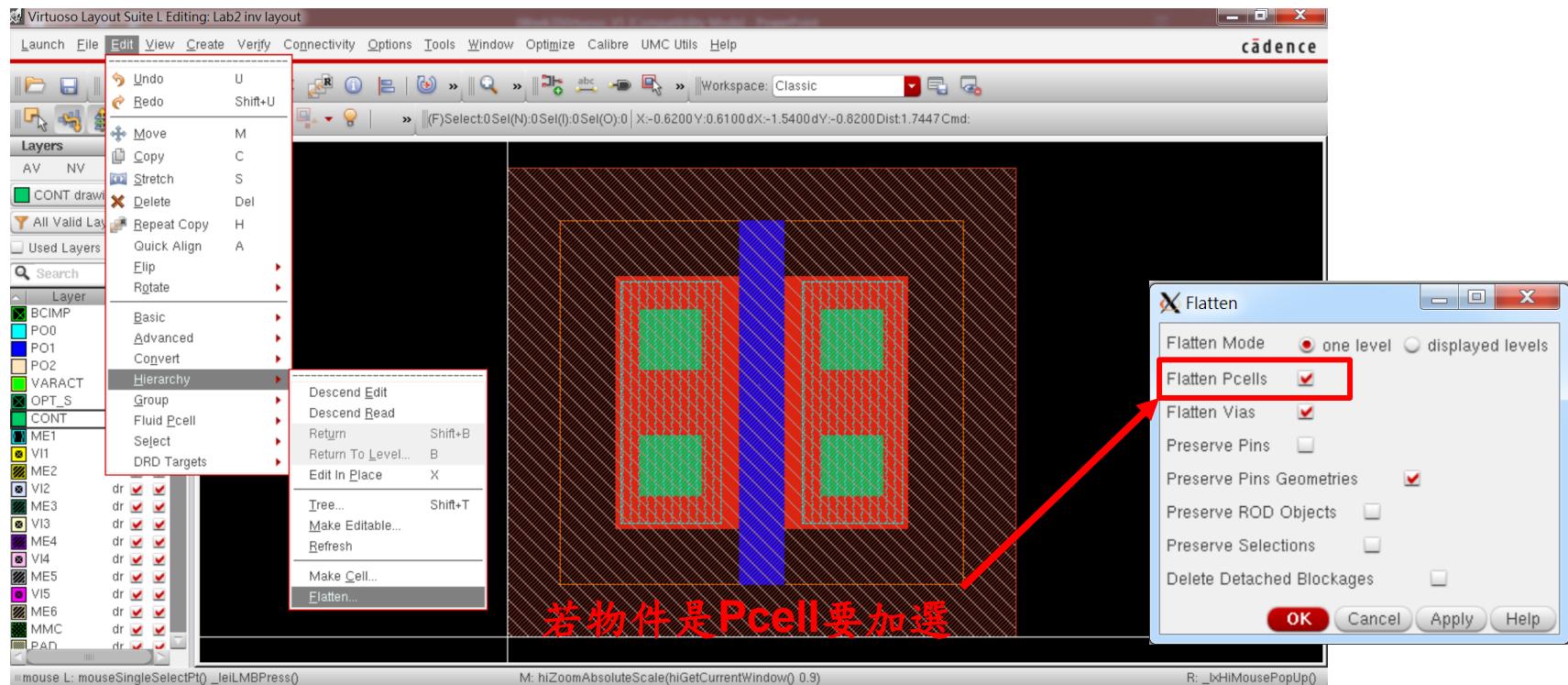


# Using Parameterized cell (Pcell) 1.8V PMOS



# Usage of Create and Edit (15)

- ◆ **Flatten Instance:** 把instance的群組解開，可觀察每一層之材質或間距，也可進行佈局調整
- ◆ **Edit → Hierarchy → Flatten**



# Usage of Create and Edit (16)

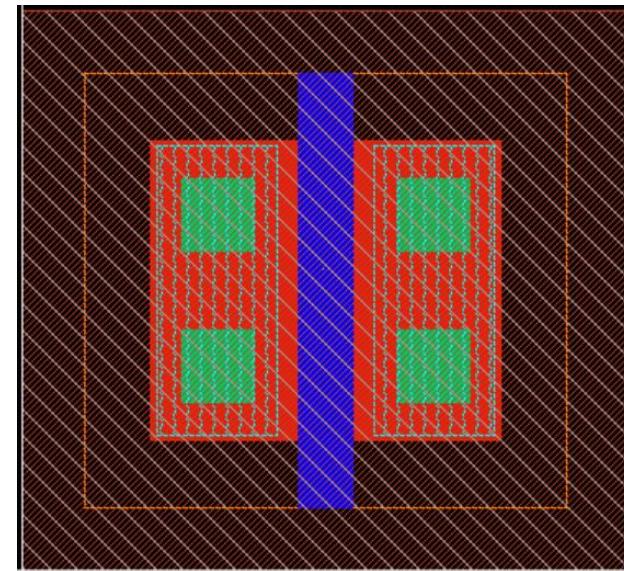
## ◆ Show Instance

- Shift+f: 顯示instance內容
- Ctrl+f: 隱藏instance內容



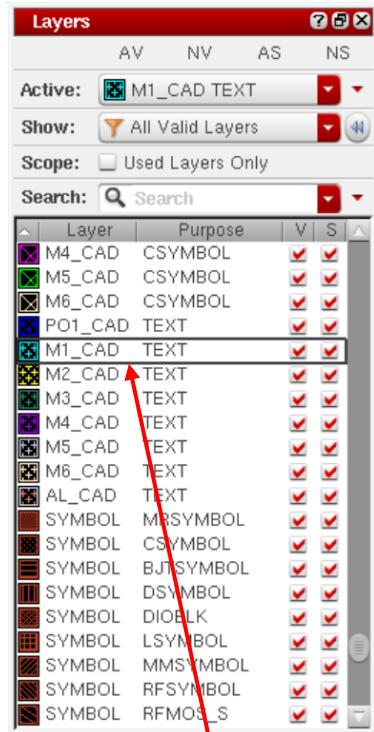
Shift+f

Ctrl+f

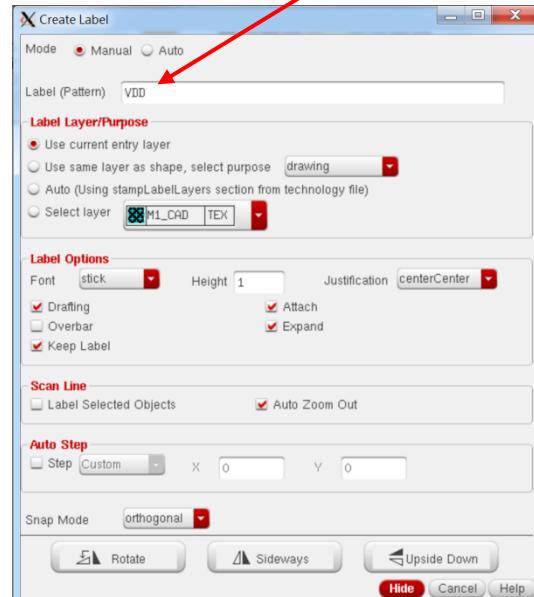


# Usage of Create and Edit (17)

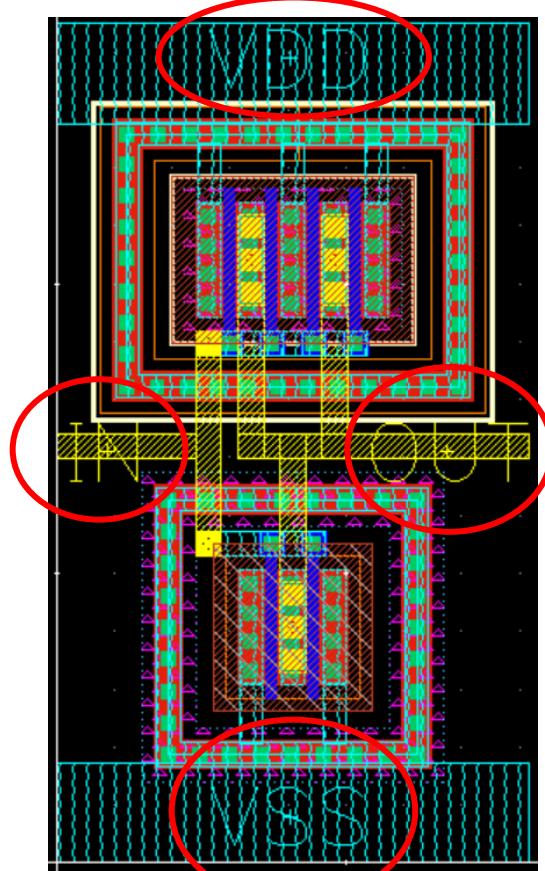
- ◆ Create label (快捷鍵, L)
- ◆ 使用TEXT layer 來命名節點名稱, 不同製程使用layer不同, 一般製程使用Pin layer (PN)



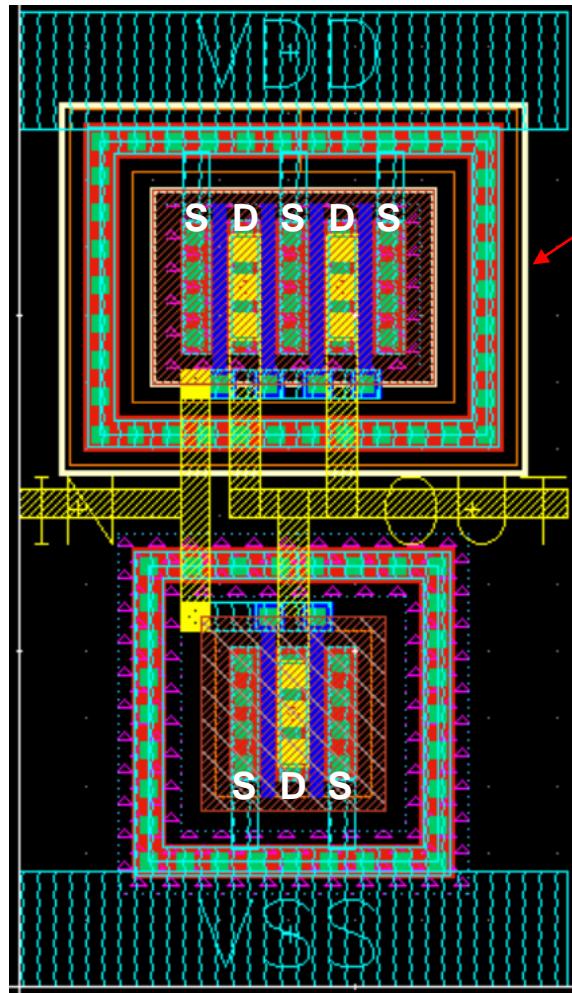
此 label 節點名稱即相對應於 schematic view 的 pin , 需相同以免後面的LVS出錯



使用的layer需對應到節點的金屬層，在這裡的M1\_CAD TEXT對應到Metal1(M1) layer

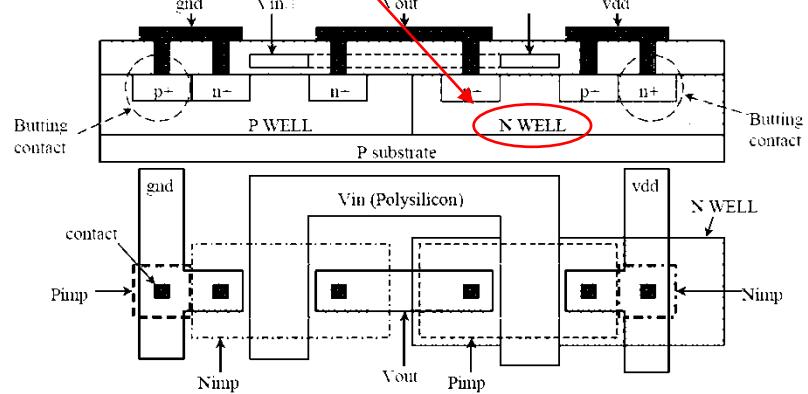
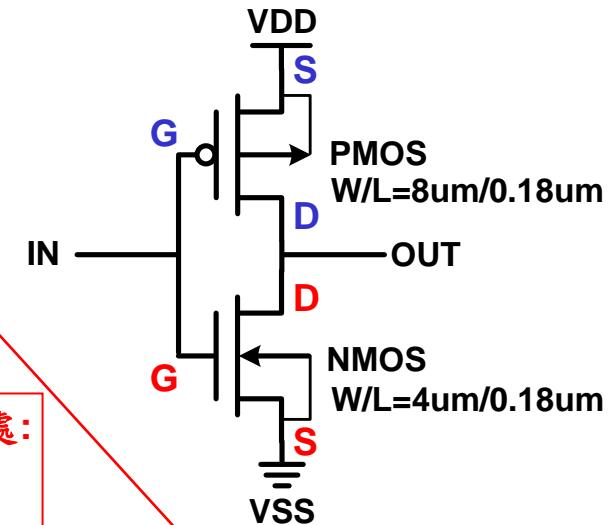


# Layout Structure of Inverter



請注意PMOS的N-type  
body pickup也須框入  
Nwell層!

Body pickup圍起來的好處：  
減少外部noise干擾  
避免latch-up發生



# *Layout Verification*

---

- ◆ **DRC (Design Rule Check)**

- To check physical layout data against fabrication-specific rules

- ◆ **LVS (Layout Versus Schematic)**

- To check the connectivity of a physical layout design to its related schematic

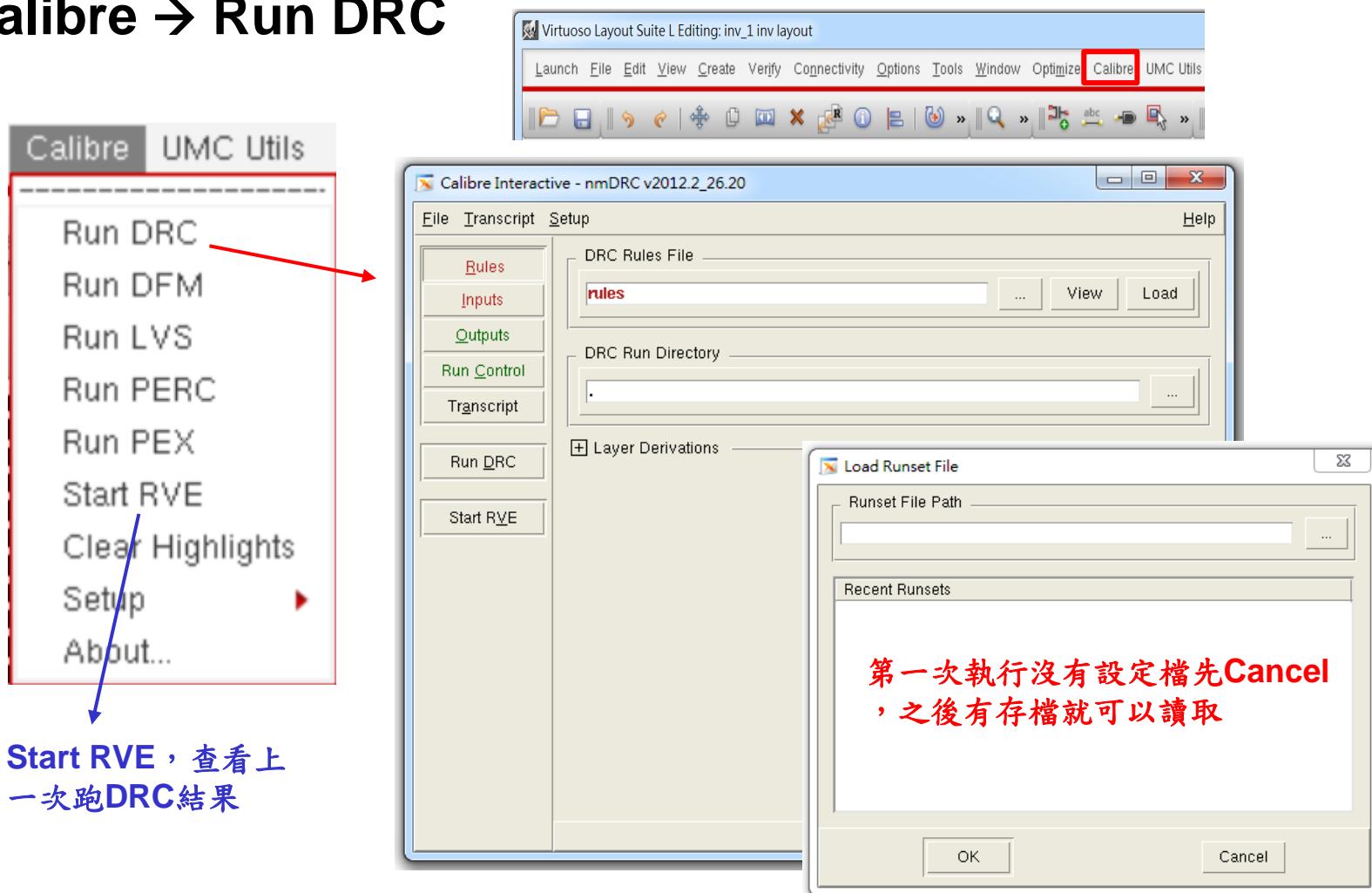
- ◆ **PEX (Parasitic Extraction)**

- To extract the parasitic effect from the interconnection of layout design



# Verification – DRC (1)

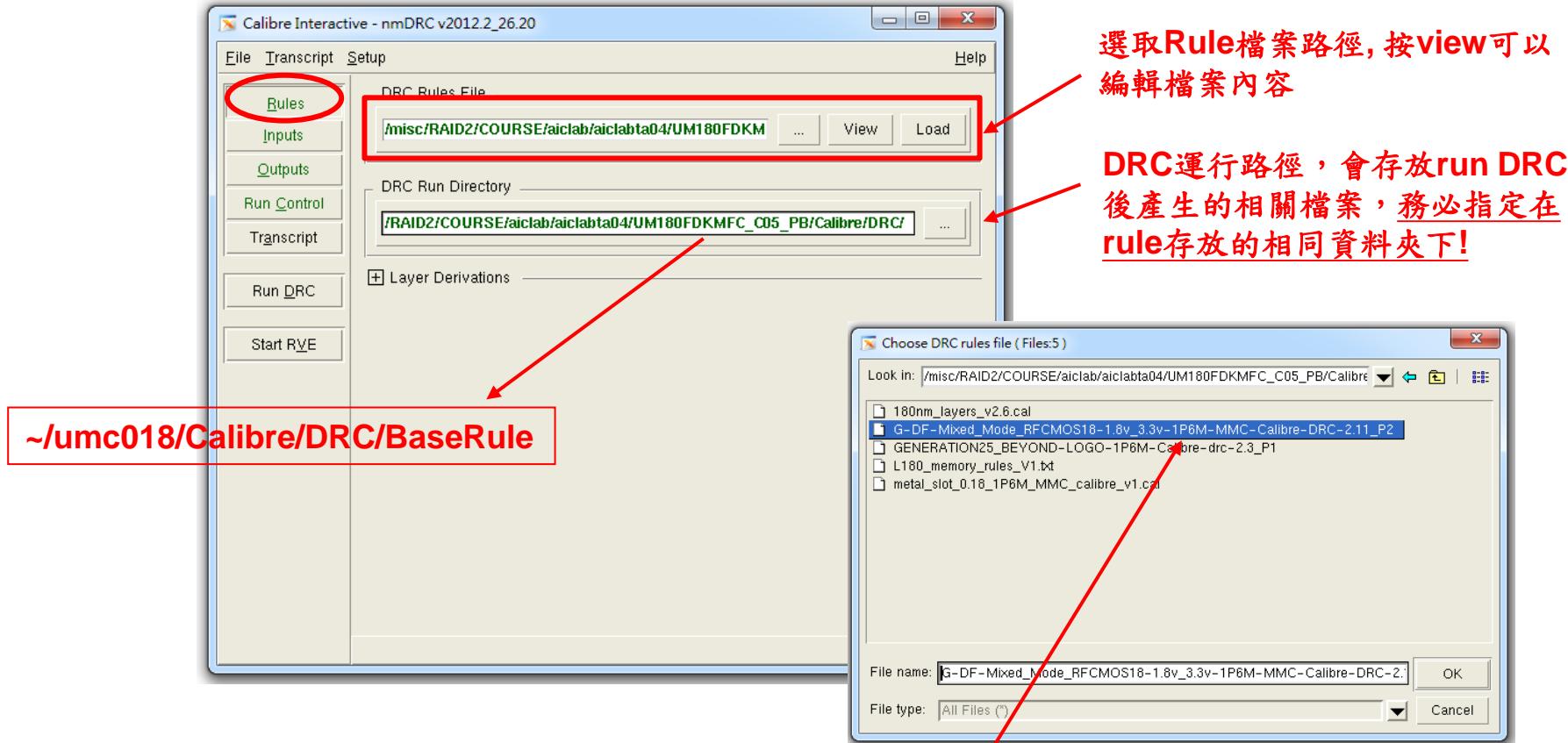
## ◆ Calibre → Run DRC



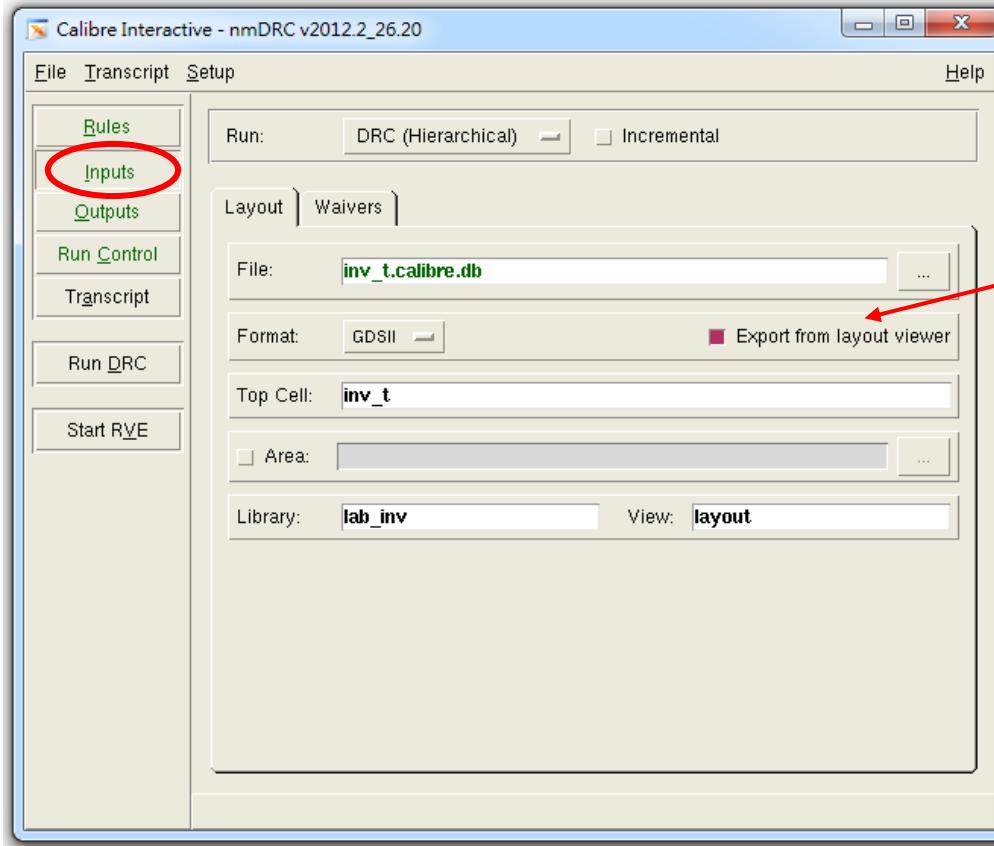
Start RVE，查看上  
一次跑DRC結果



# Verification – DRC (2)



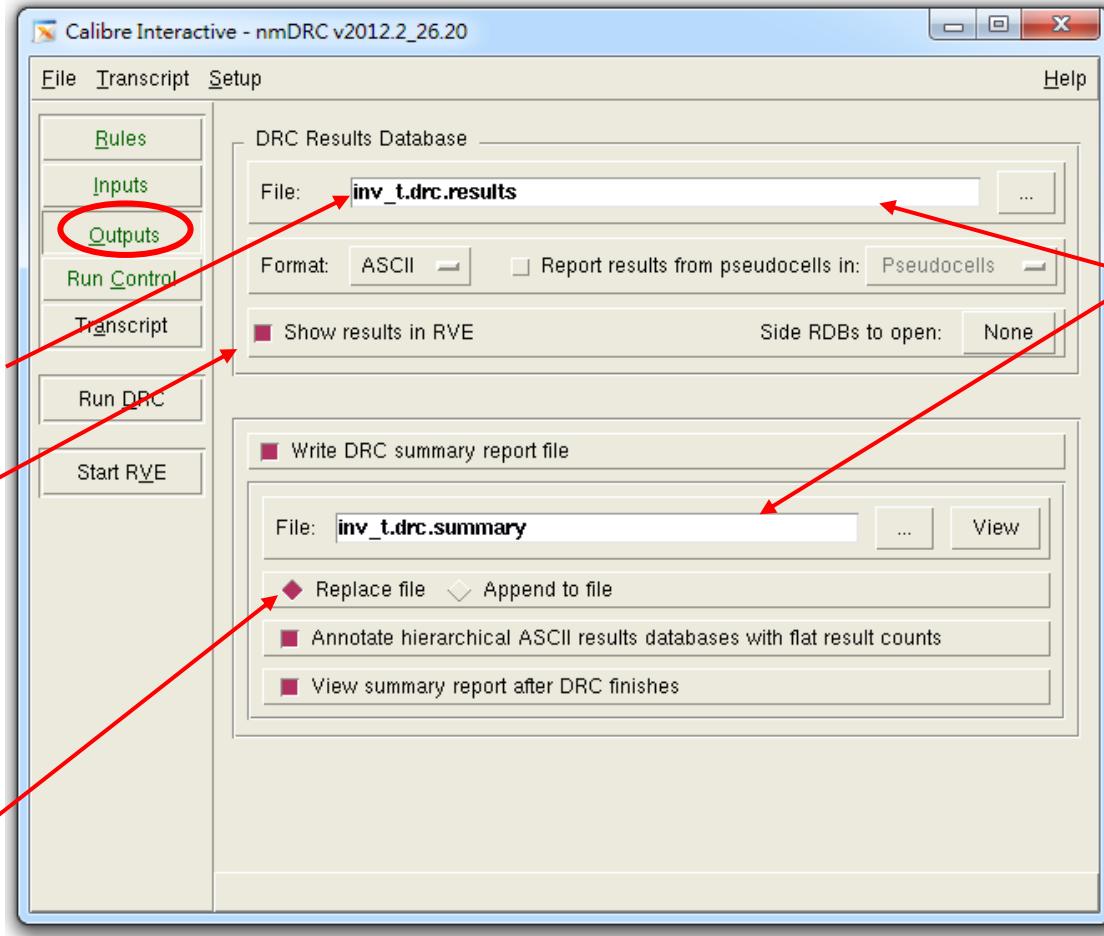
# Verification – DRC (3)



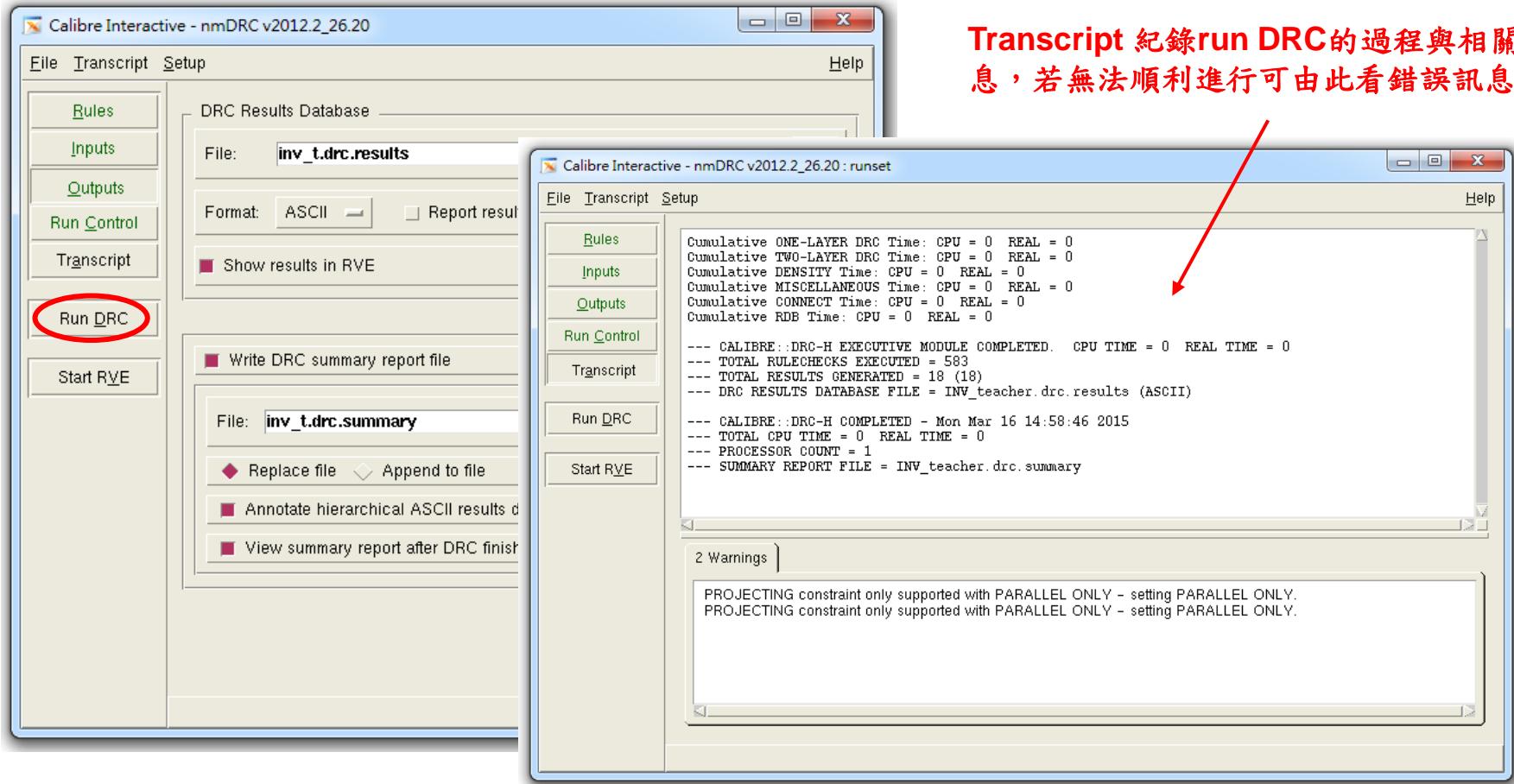
選擇使用當前layout視窗產生的gds檔，若已有現成的gds檔可不勾選，並自行輸入layout file名稱



# Verification – DRC (4)



# Verification – DRC (5)



Transcript 紀錄run DRC的過程與相關訊息，若無法順利進行可由此看錯誤訊息

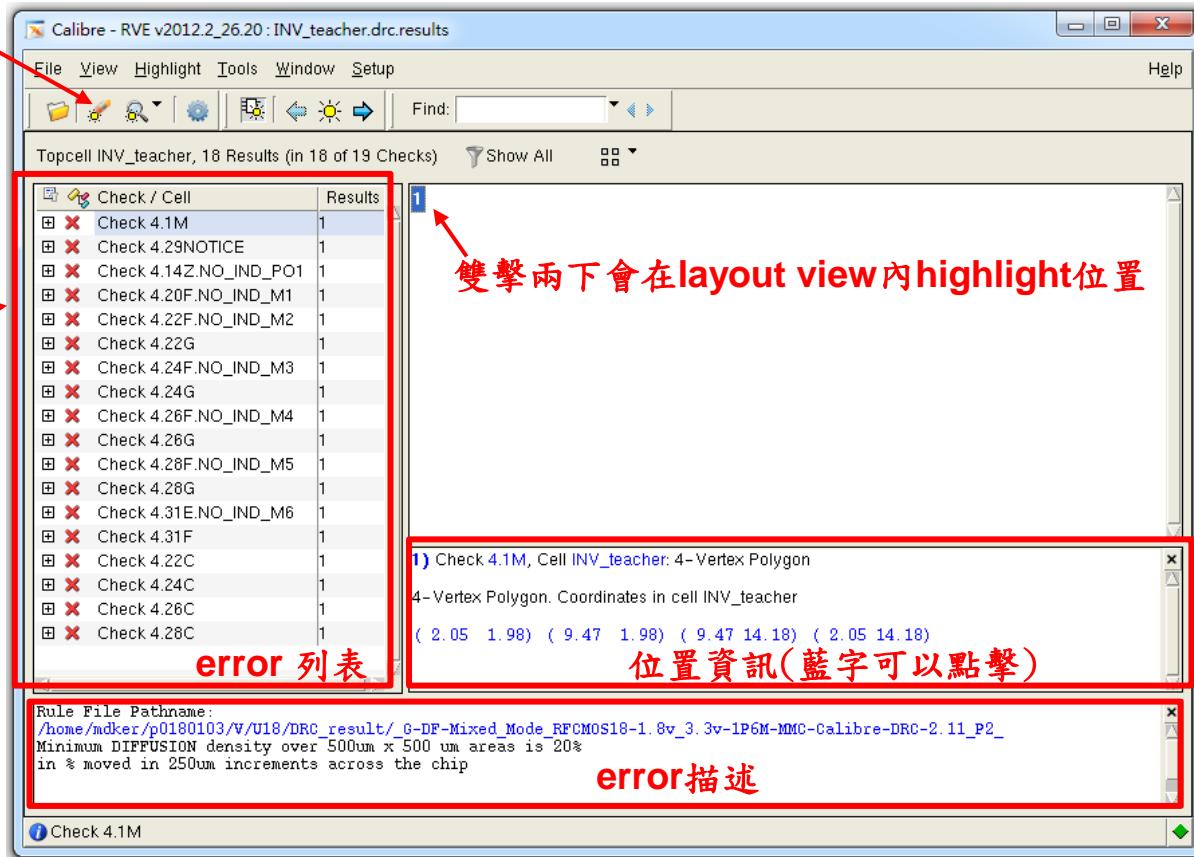


# Verification – DRC (6)

## Results Viewing Environment (RVE)

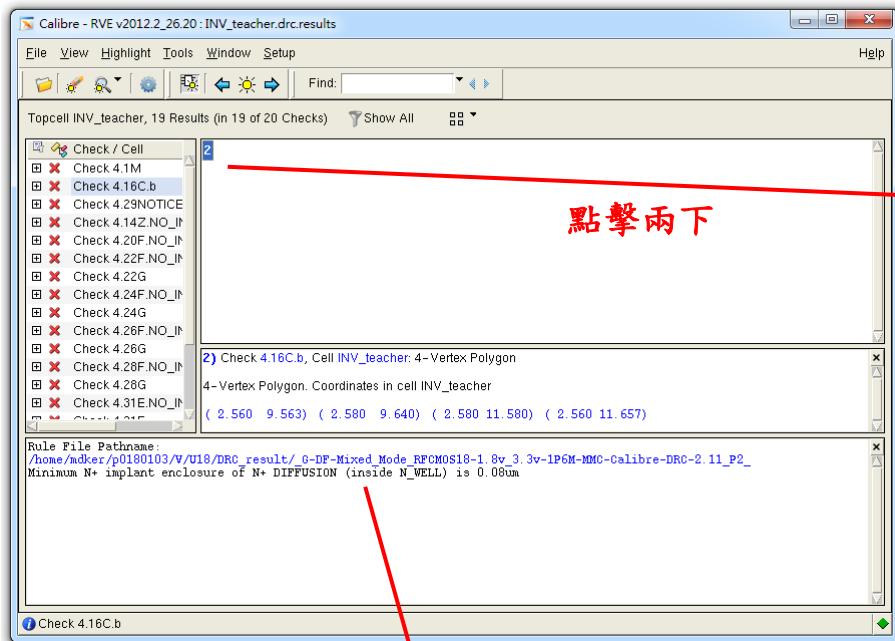
點此按鈕可清除高亮

大部分是density  
的問題，這些問  
題目前可以忽略



# Verification – DRC (7)

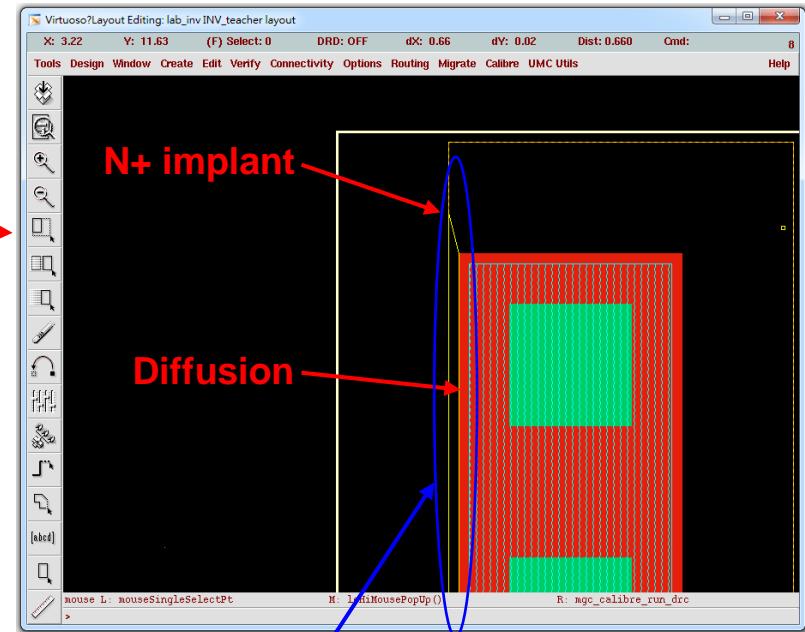
## ◆ DRC Error Example: minimum spacing



Rule File Pathname:

[/home/mdker/p0180103/V/U18/DRC\\_result/G-DF-Mixed\\_Mode RFCMOS18-1.8v\\_3.3v-1P6M-MMC-Calibre-DRC-2.11\\_P2\\_](/home/mdker/p0180103/V/U18/DRC_result/G-DF-Mixed_Mode RFCMOS18-1.8v_3.3v-1P6M-MMC-Calibre-DRC-2.11_P2_)

Minimum N+ implant enclosure of N+ DIFFUSION (inside N\_WELL) is 0.08um



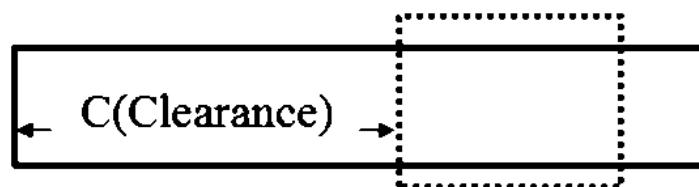
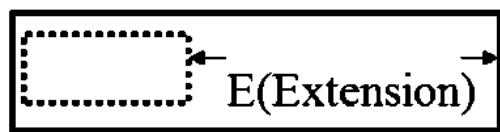
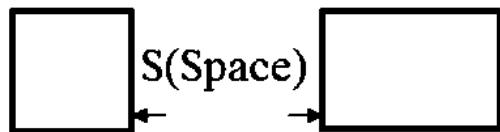
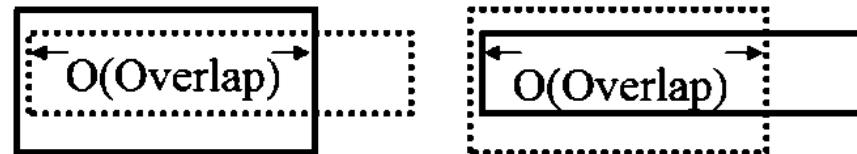
Error highlighted in layout



# *Verification – DRC (8)*

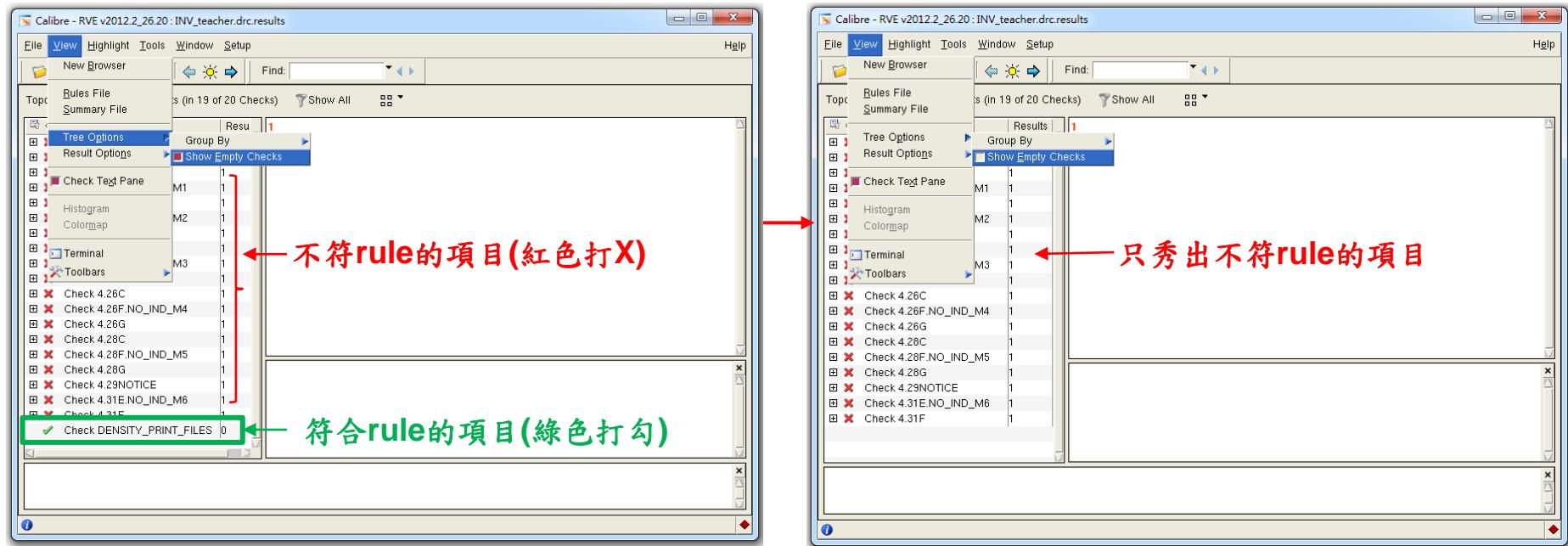
## ◆ DRC Error Examples:

- Width, Space, Extension, Overlap, Clearance, etc.



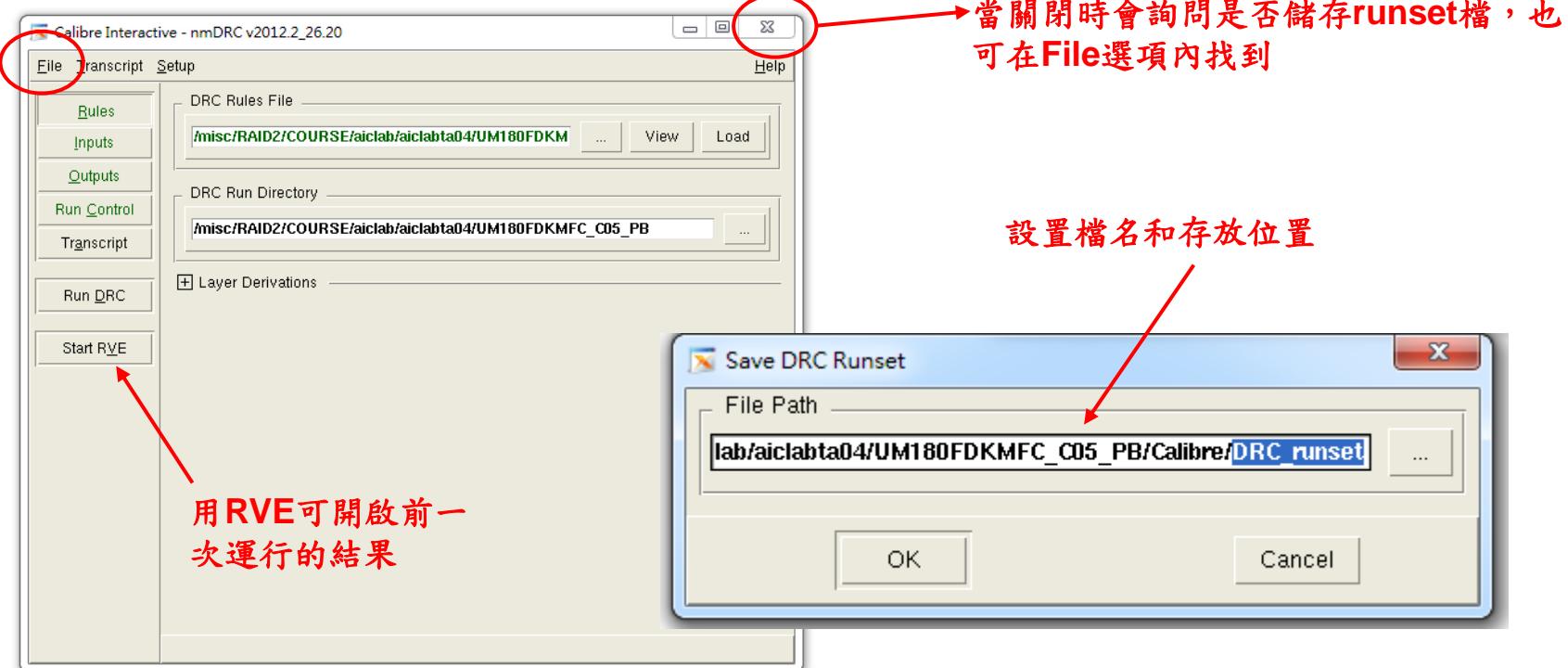
# Verification – DRC (9)

- ◆ 將符合rule的列表去除(綠色打勾選項), 幫助統整error
- ◆ View → Tree Options → cancel Show Empty Checks



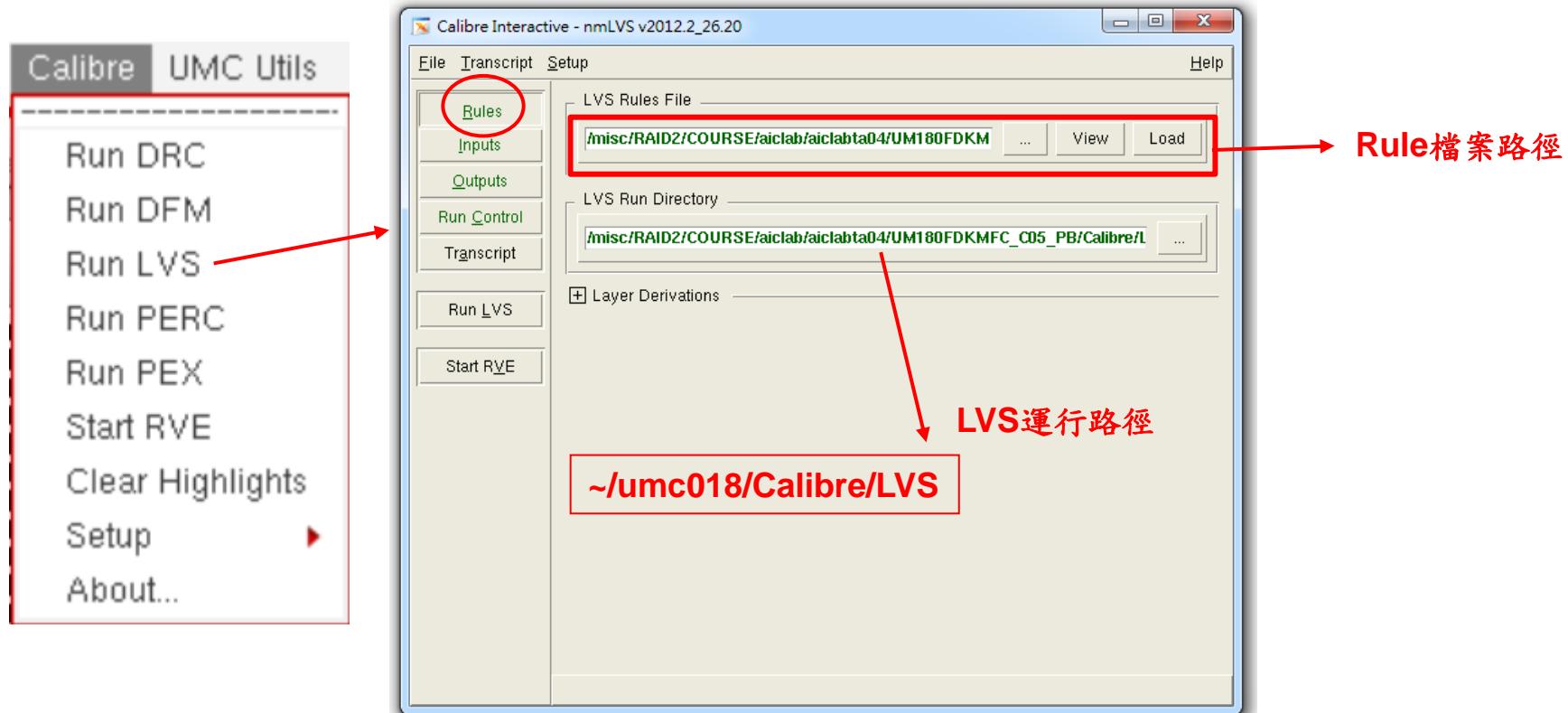
# Verification – DRC (10)

## ◆ Runset file setting



# Verification – LVS (1)

## ◆ Calibre → Run LVS

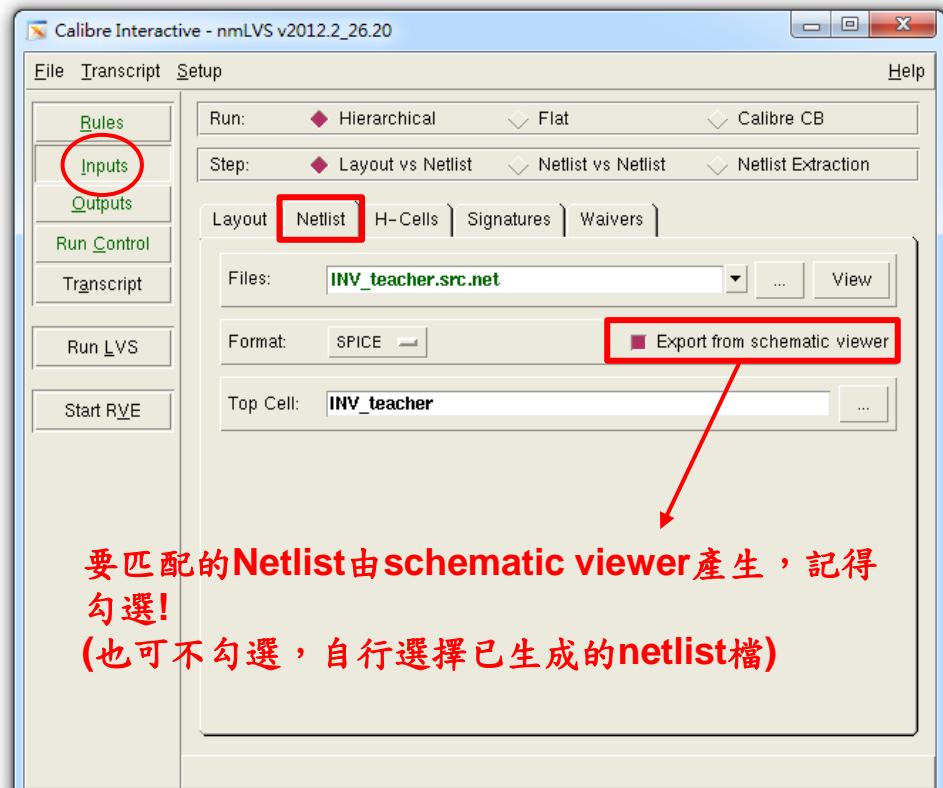
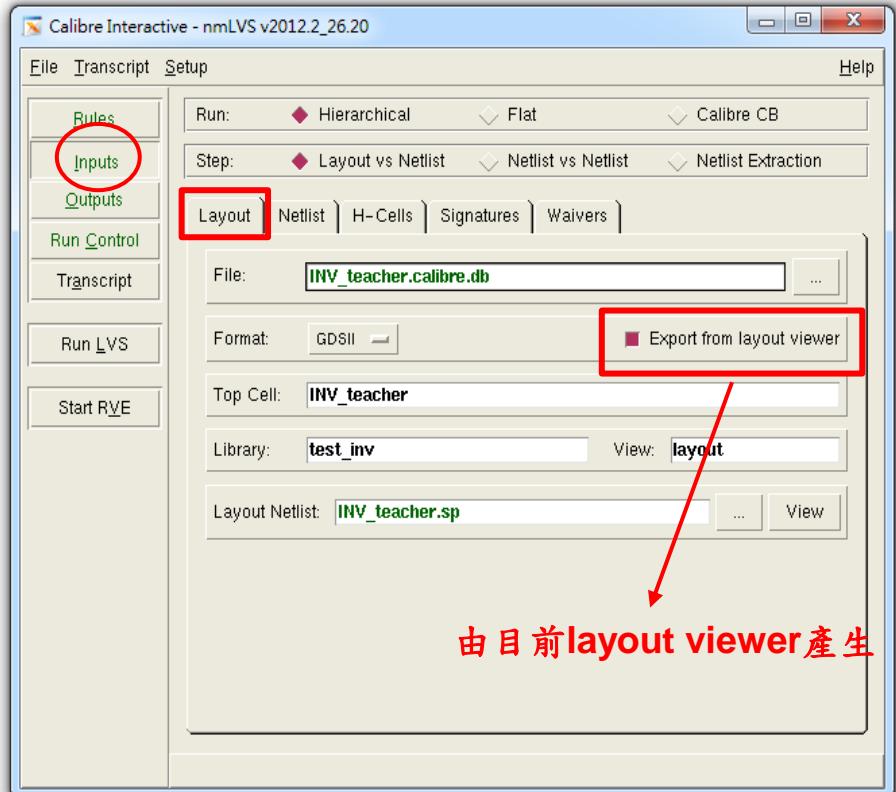


Rule檔案路徑:

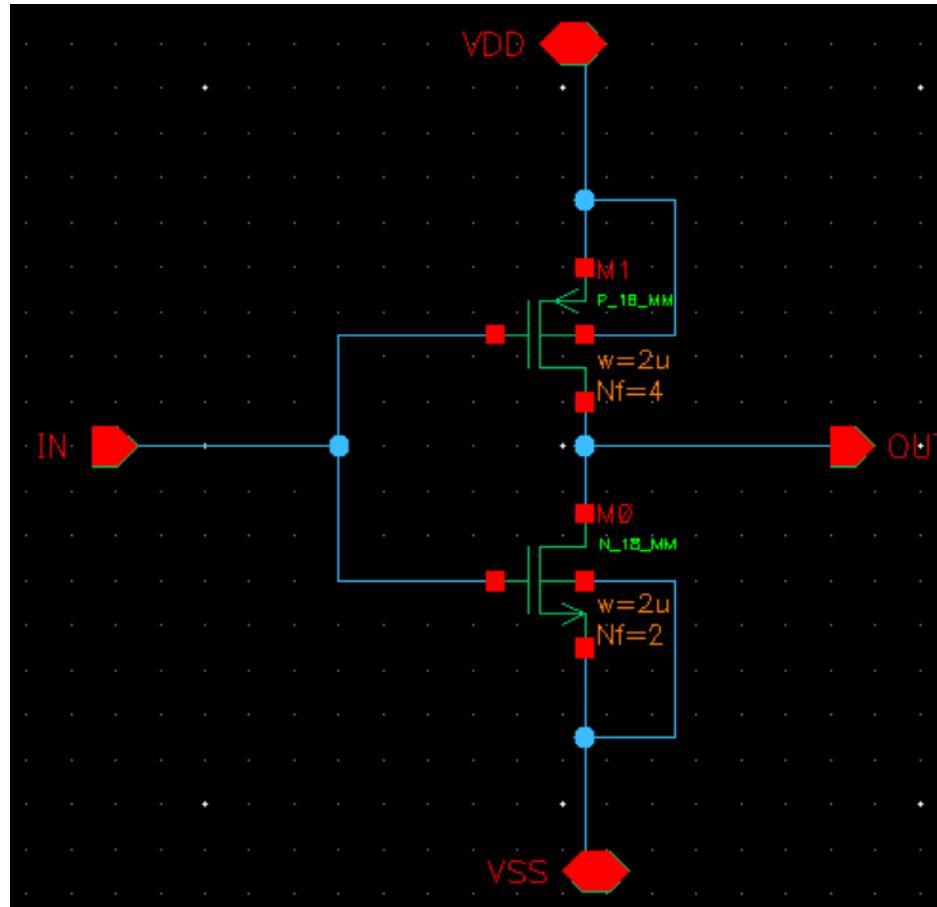
~/umc018/Calibre/LVS/G-DF-MIXED\_MODE\_RFCMOS18-1.8V\_3.3V-1P6M-MMC\_CALIBRE-LVS-2.1-P8.txt



# Verification – LVS (2)



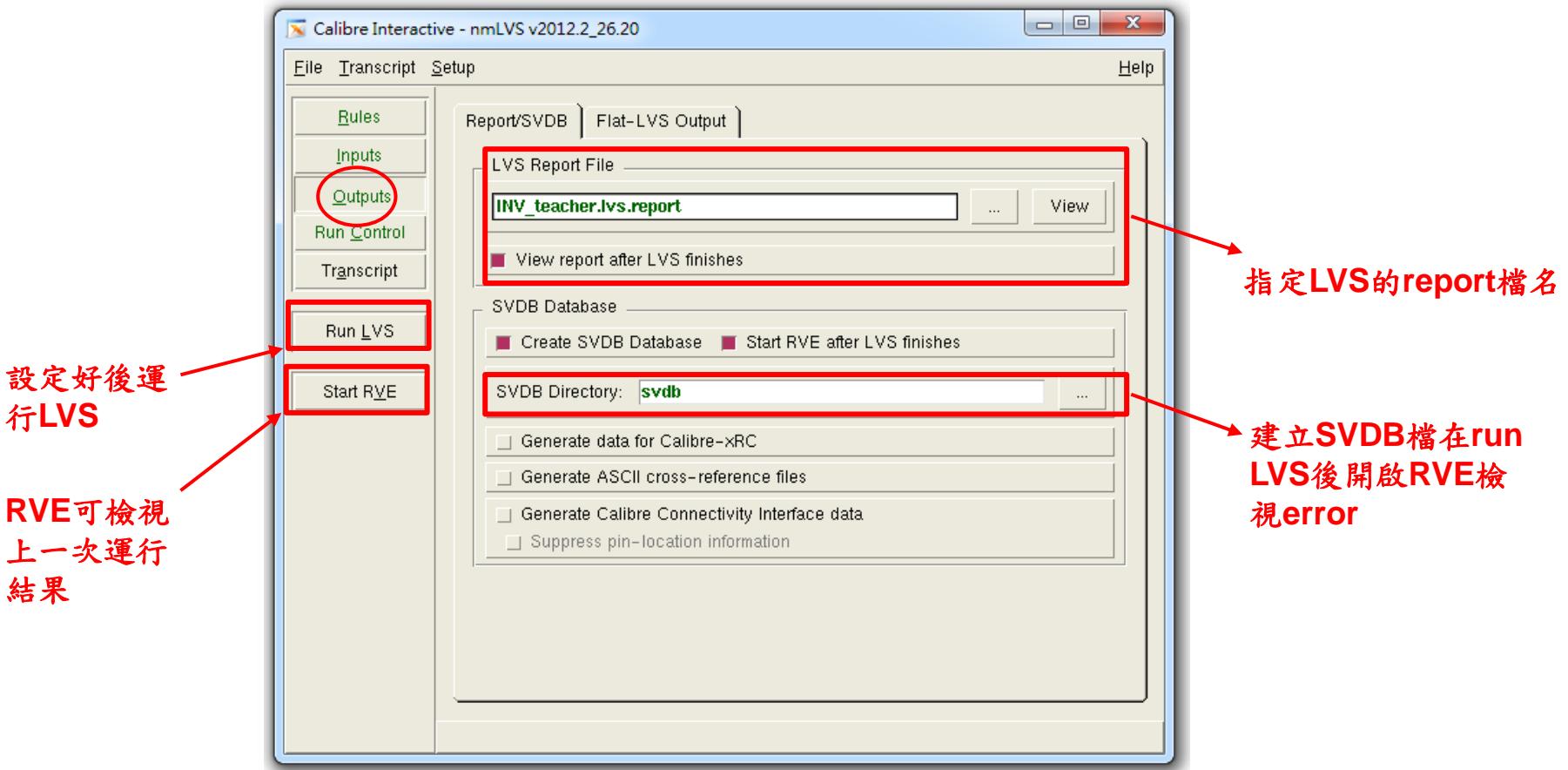
# Create Schematic of Inverter



Pin name 需與layout view的相同

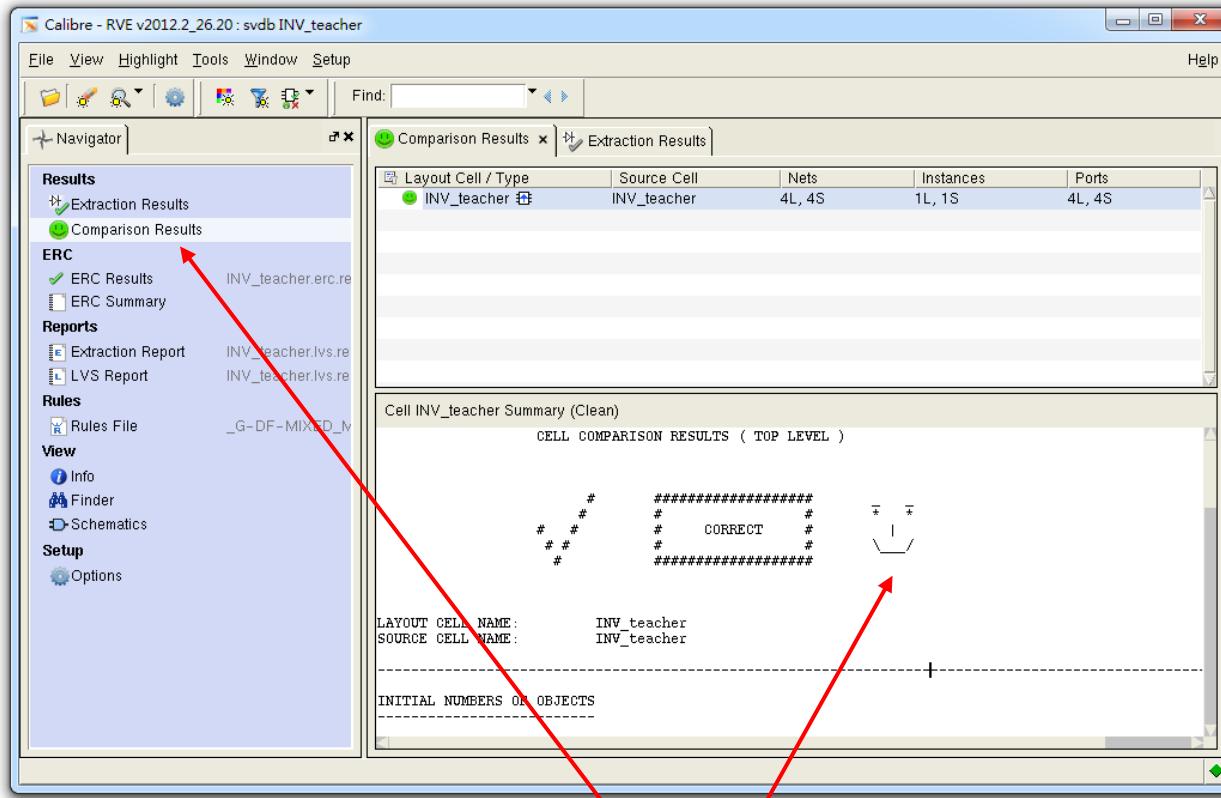


# Verification – LVS (3)



# Verification – LVS (4)

## Results Viewing Environment (RVE)

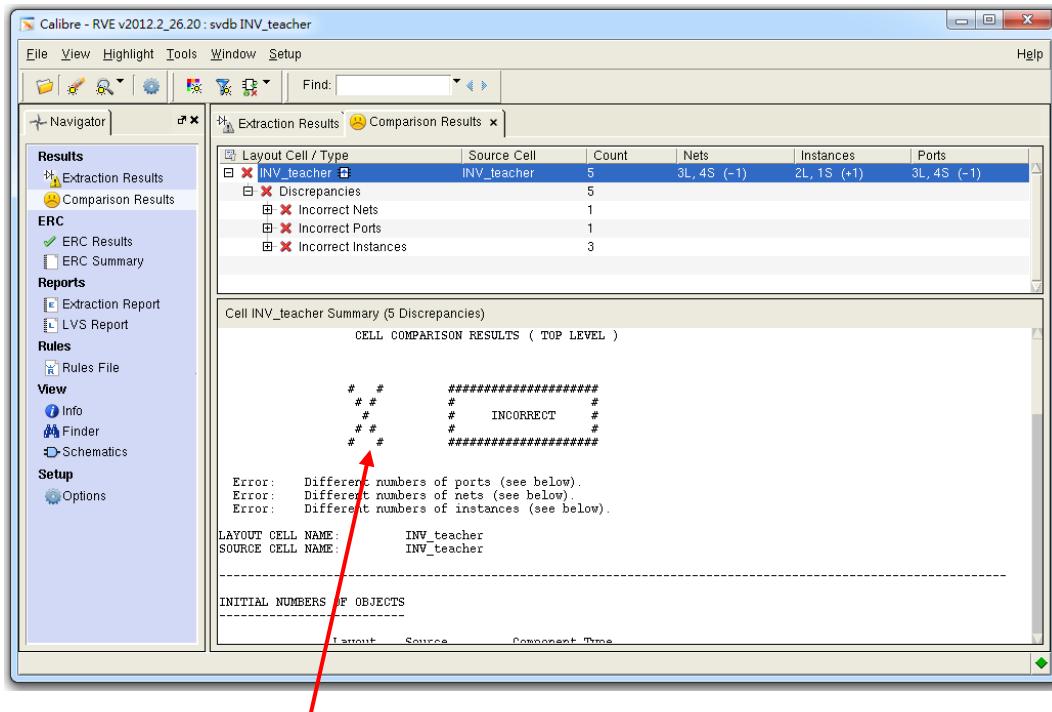


若correct會顯示勾勾和笑臉



# Verification – LVS (5)

## ◆ LVS Error Example: Short Circuits (1/3)



若incorrect會顯示X

CELL COMPARISON RESULTS ( TOP LEVEL )

#	#	##### <td>#</td> <td>#</td>	#	#
#	#	#	INCORRECT	#
#	#	#	#	#
#	#	#####	#####	#####

Error: Different numbers of ports (see below).  
Error: Different numbers of nets (see below).  
Error: Different numbers of instances (see below).

LAYOUT CELL NAME: INV\_teacher  
SOURCE CELL NAME: INV\_teacher

---

INITIAL NUMBERS OF OBJECTS

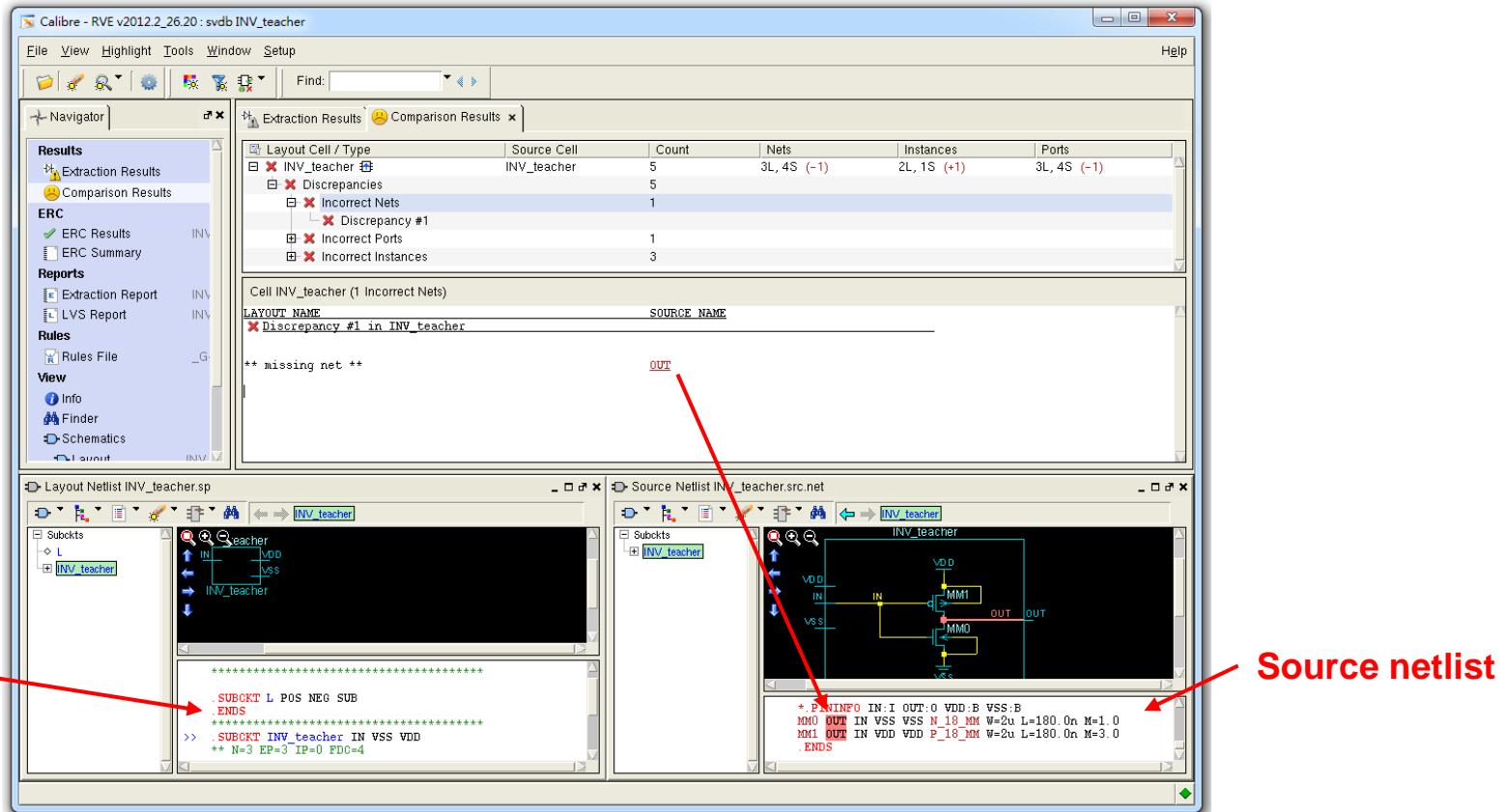
	Layout	Source	Component Type
Ports:	3	4	*
Nets:	3	4	*
Instances:	1	1	MN (4 pins)
	3	3	MP (4 pins)
Total Inst:	4	4	

layout有3個net，但Source確有4個  
net，表示layout有一處short



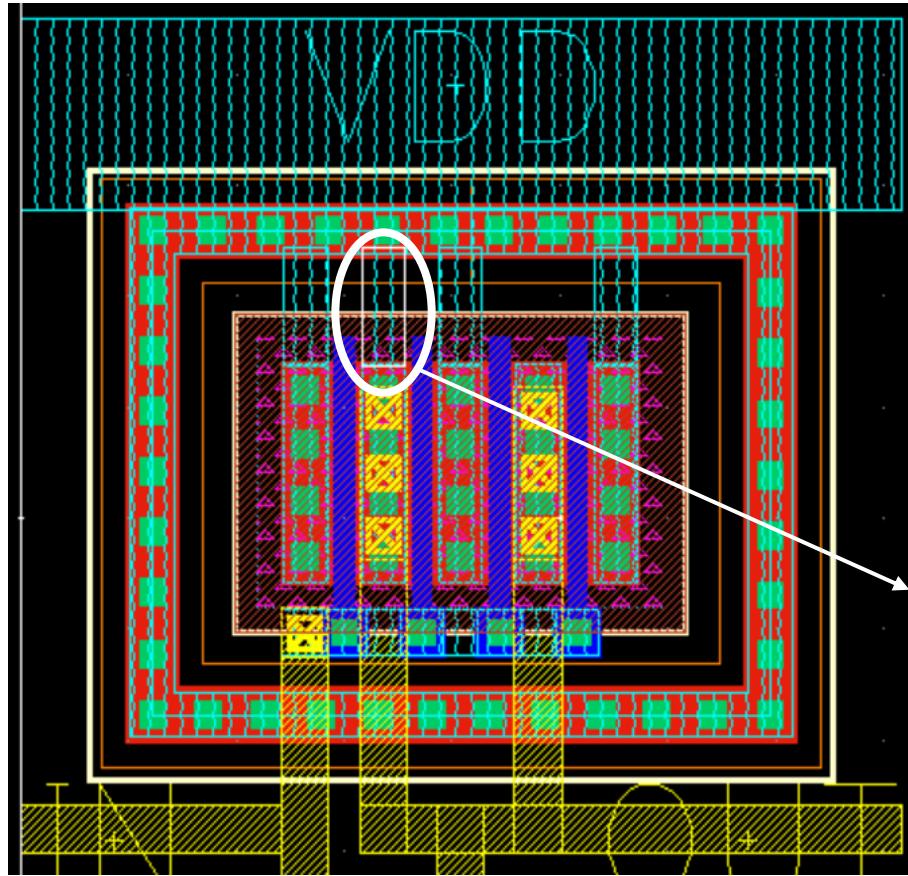
# Verification – LVS (6)

## ◆ LVS Error Example: Short Circuits (2/3)



# *Verification – LVS (7)*

## ◆ LVS Error Example: Short Circuits (3/3)

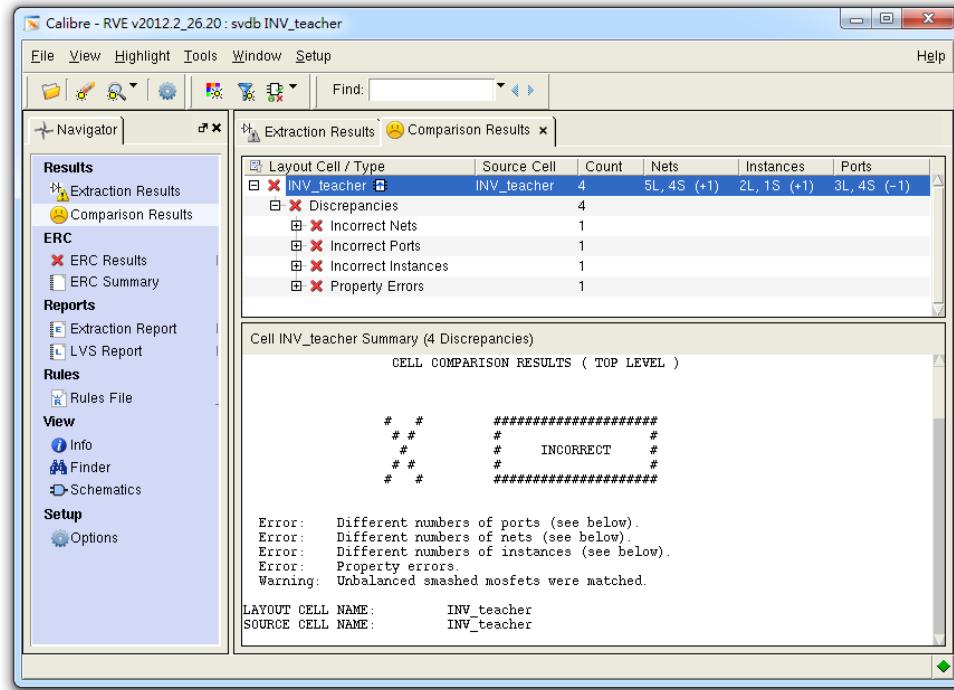


藉由接點找出短路處



# Verification – LVS (8)

## ◆ LVS Error Example: Open Circuits (1/3)



CELL COMPARISON RESULTS ( TOP LEVEL )

# # ##### # # # #  
# # # # INCORRECT #  
# # # #  
# # ##### # # # #

Error: Different numbers of ports (see below).  
Error: Different numbers of nets (see below).  
Error: Different numbers of instances (see below).  
Error: Property errors.  
Warning: Unbalanced smashed mosfets were matched.

LAYOUT CELL NAME: INV\_teacher  
SOURCE CELL NAME: INV\_teacher

### INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	3	4	*
Nets:	5	4	*
Instances:	1 3	1 3	MN (4 pins) MP (4 pins)
Total Inst:	4	4	

layout有5個net，但Source確有4個net，表示layout有一處Open



# Verification – LVS (9)

## ◆ LVS Error Example: Open Circuits (2/3)

The screenshot shows the Calibre LVS interface. The top window displays the 'Extraction Results' and 'Comparison Results' panes. The 'Results' pane lists 'ERC Results' (including 'INV\_results' and 'INV\_teacher.erc.results') and 'LVS Report' (including 'INV\_teacher.lvs.report.ed' and 'INV\_teacher.lvs.report'). The 'Extraction Results' pane shows a table of discrepancies:

Layout Cell / Type	Source Cell	Count	Nets	Instances	Ports
INV_teacher	INV_teacher	4	5L, 4S (+1)	2L, 1S (+1)	3L, 4S (-1)
Discrepancies					
Incorrect Nets					
Discrepancy #1					
Incorrect Ports					
Incorrect Instances					
Property Errors					

The 'Comparison Results' pane highlights 'Discrepancy #1 in INV\_teacher' with the message '\*\* missing net \*\*'. Below this, the 'Layout Netlist' and 'Source Netlist' windows are shown. The 'Layout Netlist' window displays the physical layout of the INV\_teacher cell with two transistors (M0 and M1) and their connections. The 'Source Netlist' window shows the schematic representation of the cell. Red arrows point from the text labels 'Layout netlist' and 'Source netlist' to their respective windows.

Layout netlist

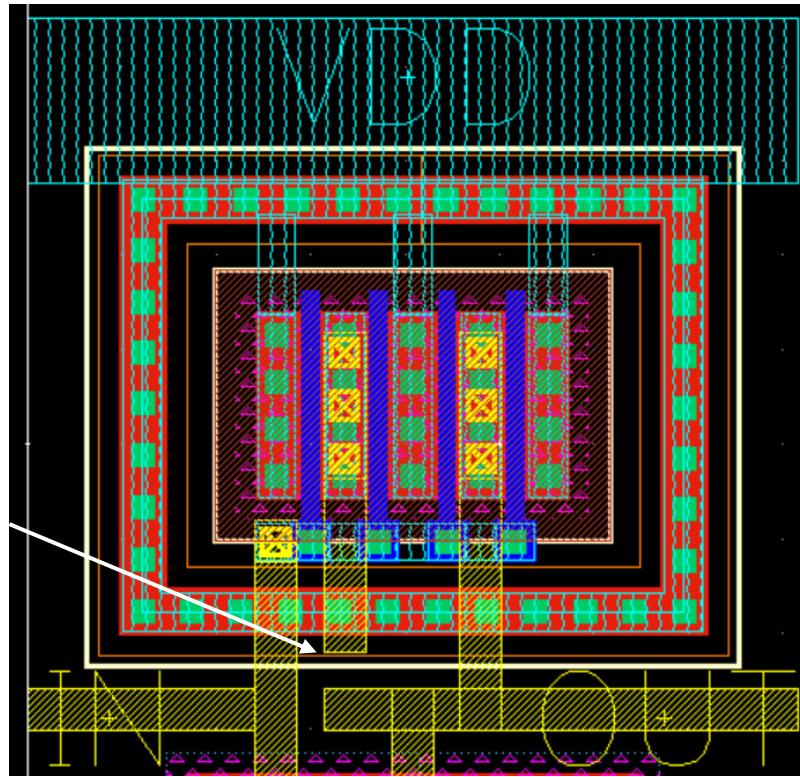
Source netlist



# Verification – LVS (10)

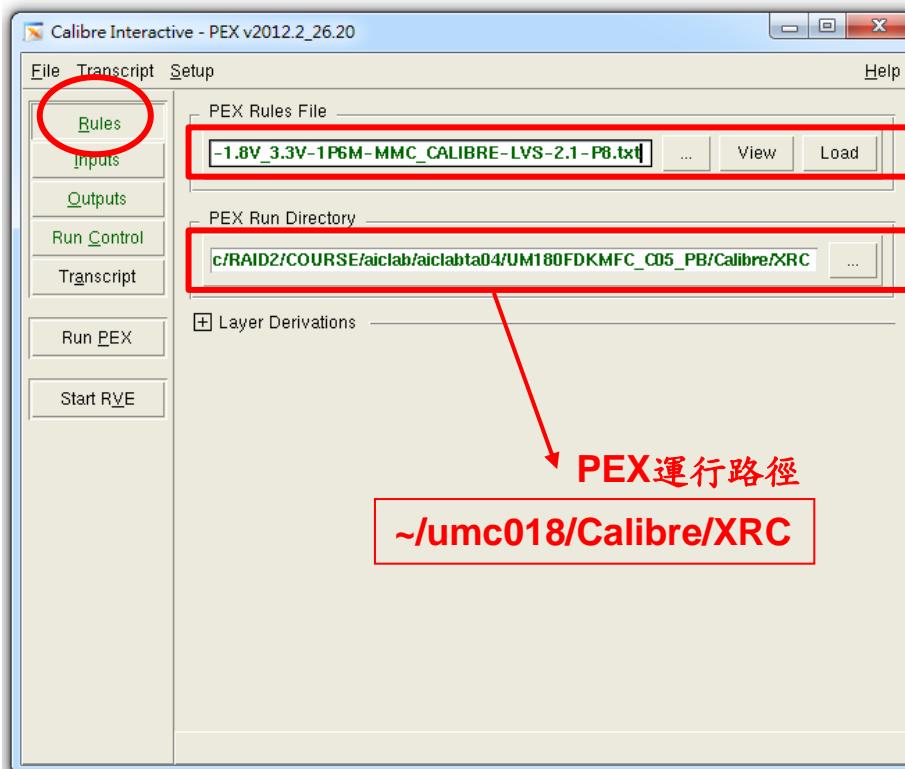
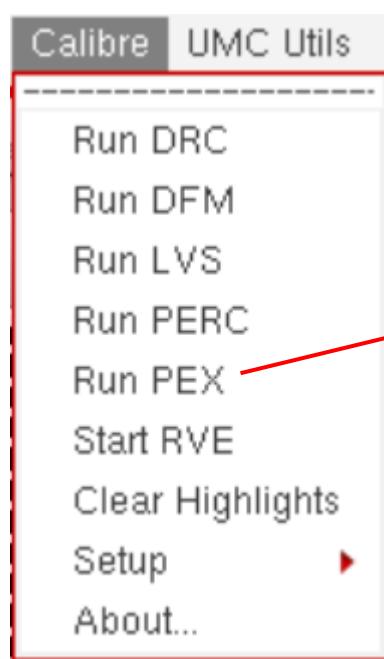
## ◆ LVS Error Example: Open Circuits (3/3)

click error的net可在  
layout viewer上看到  
error的發亮位置



# Verification – PEX (1)

## ◆ Calibre → Run PEX

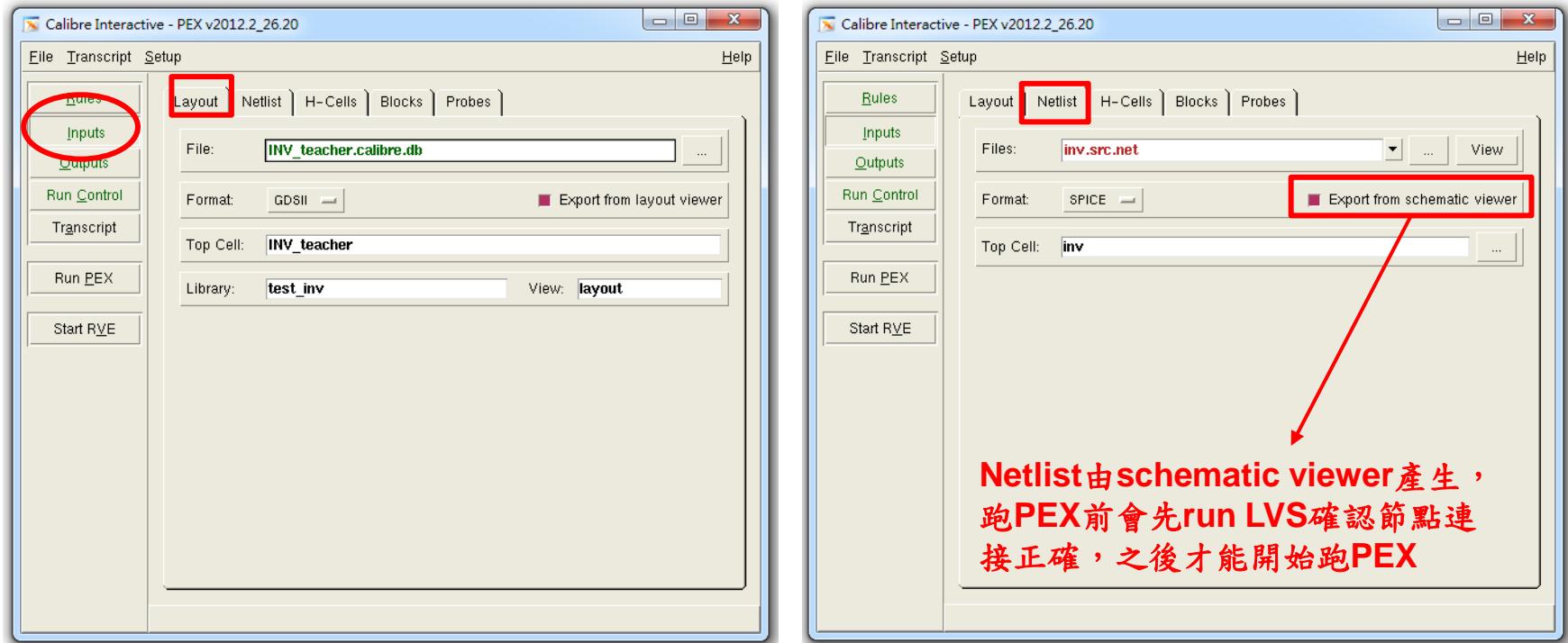


Rule檔案路徑:

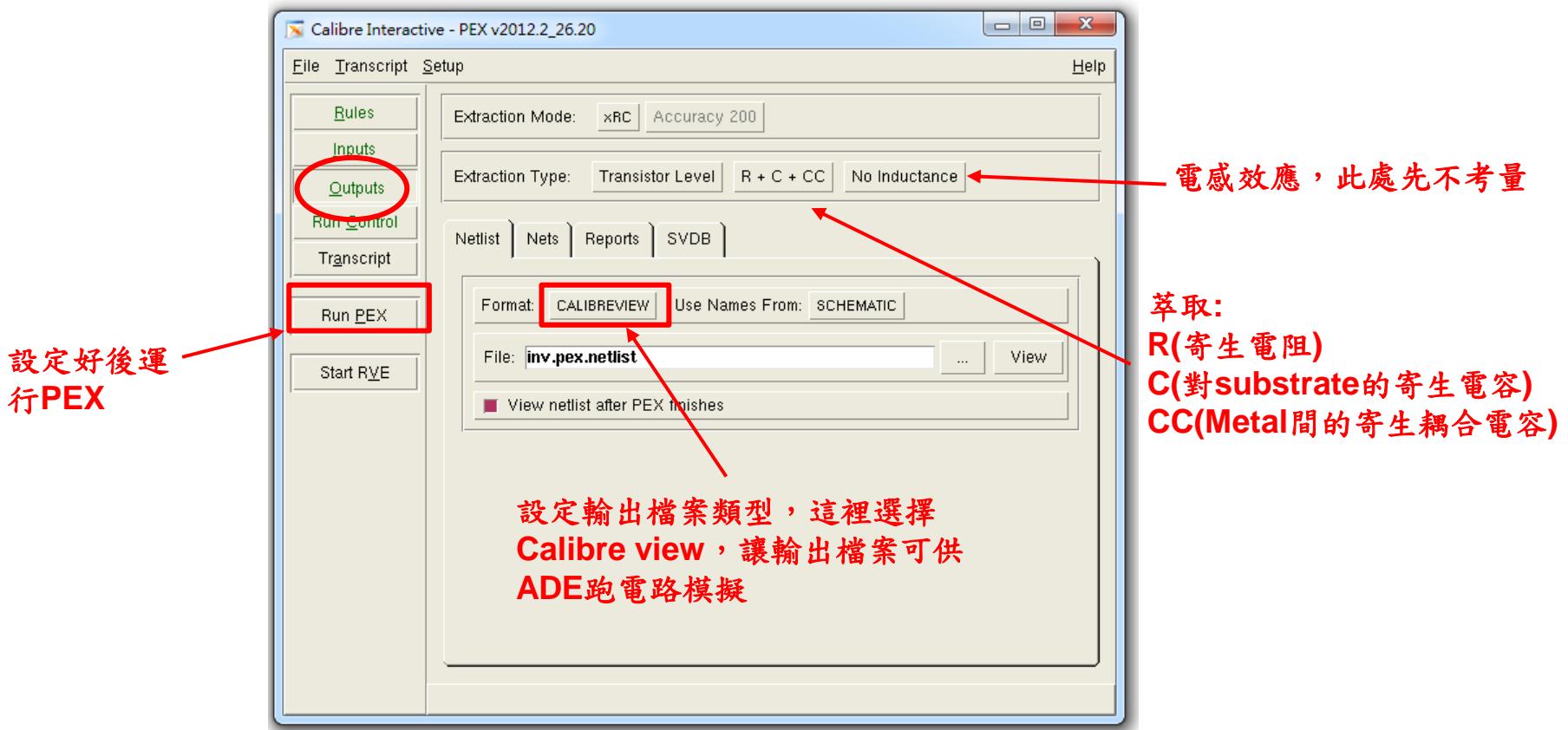
~/umc018/Calibre/XRC/G-DF-MIXED\_MODE\_RFCMOS18-1.8V\_3.3V-1P6M-MMC\_CALIBRE-LVS-2.1-P8.txt



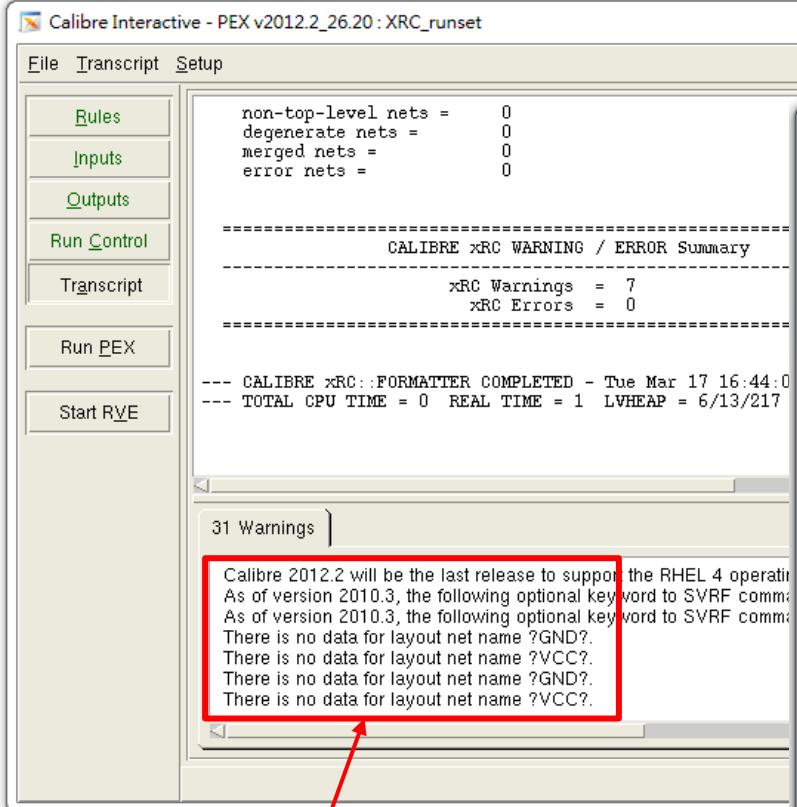
# Verification – PEX (2)



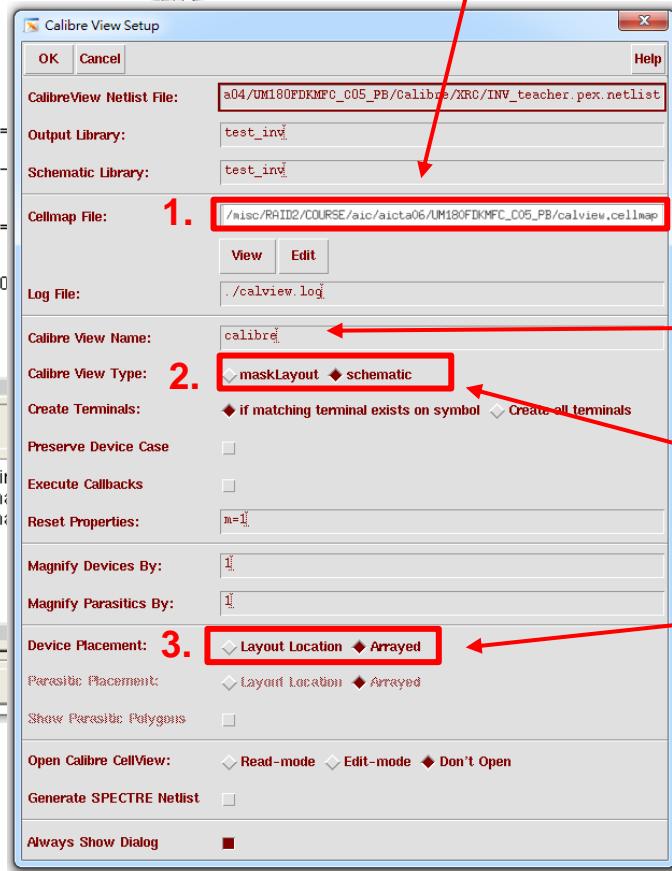
# Verification – PEX (3)



# Verification – PEX (4)



cellmap 檔，用來產生calibre view，在以下路徑：  
~/umc018/calview.cellmap (請根據實際文件存放位置設定路徑，否則PEX會無法成功進行)



此處沒有顯示LVS錯誤，若有會顯示在此

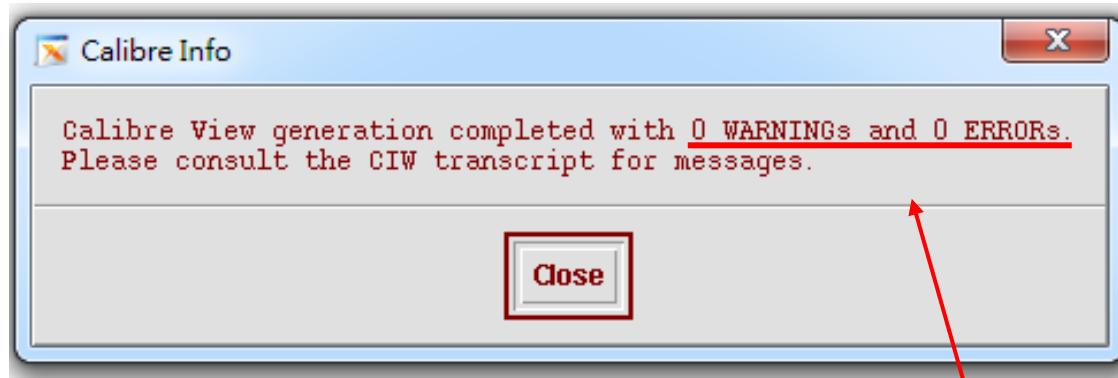
calibre view的檔名

更改calibre view的  
顯示類型為  
schematic view

將寄生元件採array方式  
排列



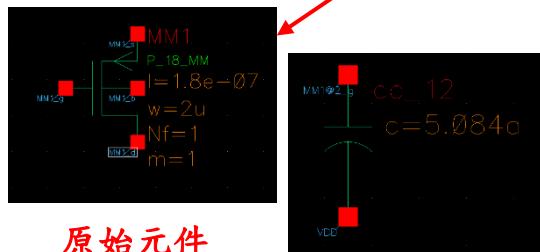
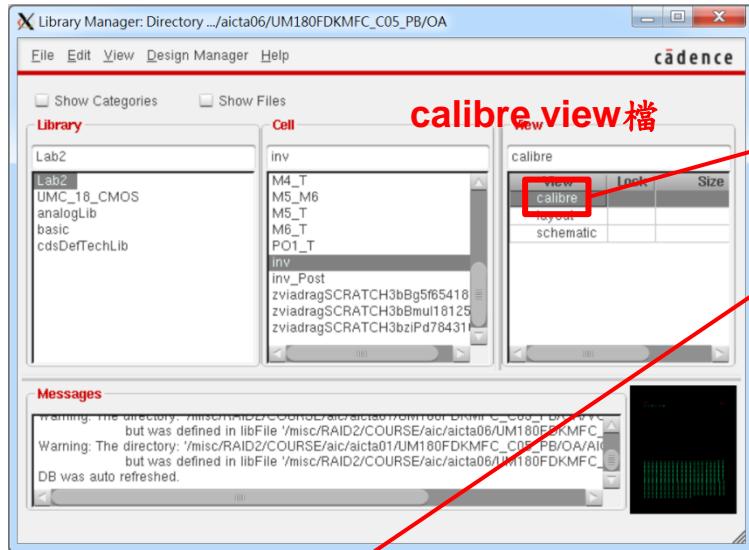
# Verification – PEX (5)



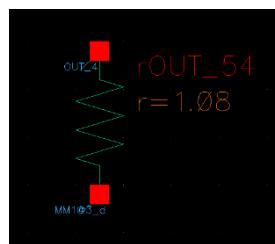
0個warning和0個error，不能有任何error  
才是成功輸出



# Verification – PEX (6)

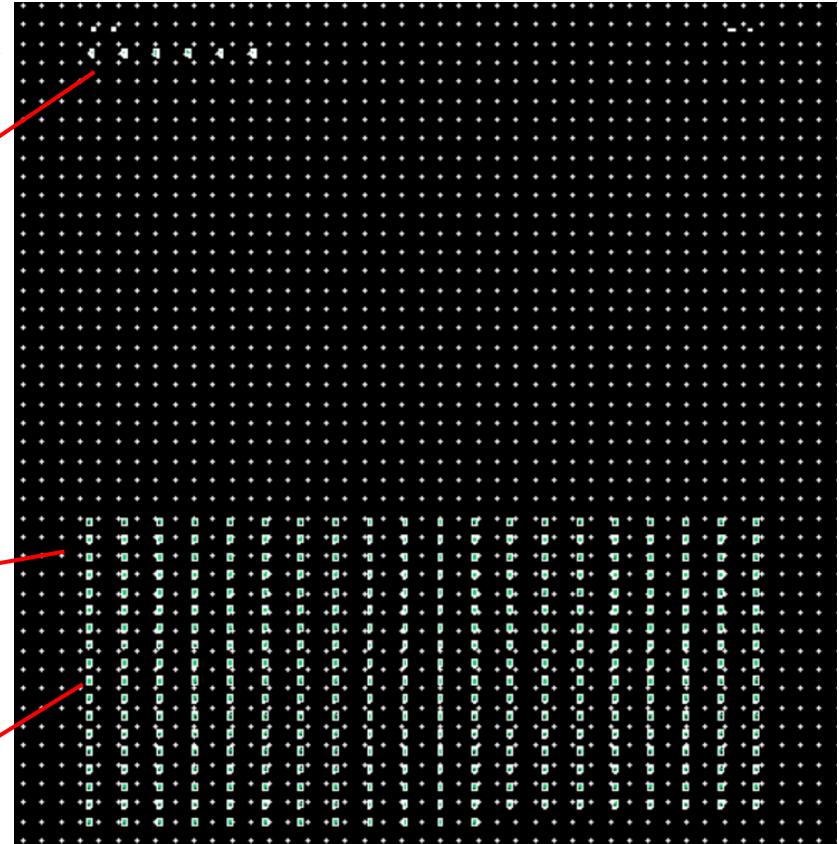


原始元件



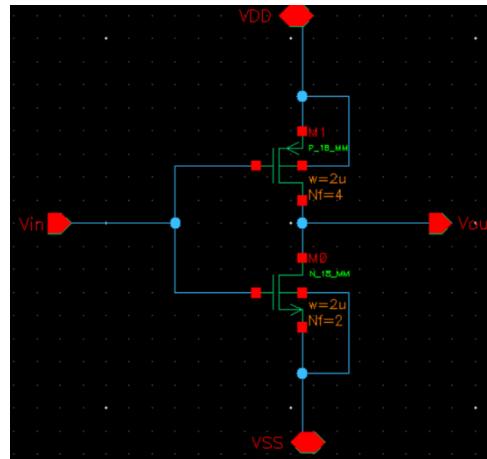
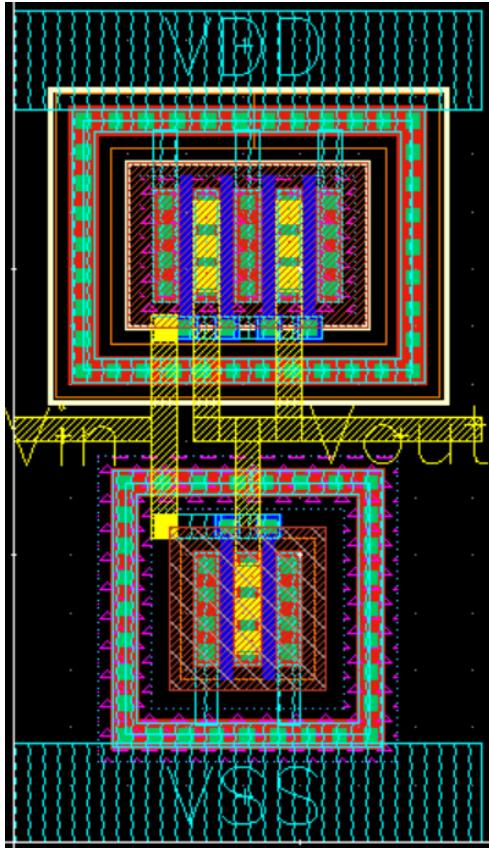
寄生電容

寄生電阻

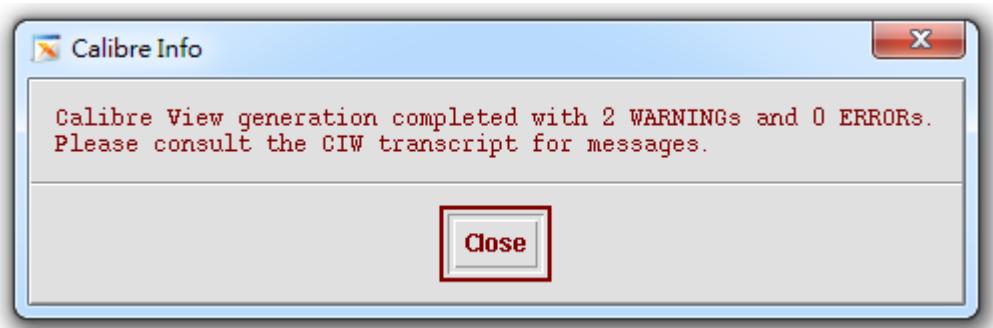


# Verification – PEX (7)

- ◆ PEX Error Example: 大小寫問題
- ◆ 若pin命名含有小寫時, LVS沒有錯誤, 但PEX萃取時會出現warning



輸入pin是"Vin"，輸出pin是"Vout"，都含有小寫



run PEX後跳出視窗，有2個warning



# Verification – PEX (8)

## ◆ 跑完PEX後，查詢warning和error

```
xterm
linux01 [aiclab/aiclabta04]# cd UM180FDKMF_C05_PB
linux01 [aiclabta04/UM180FDKMF_C05_PB]# ls
0.18um_techfile.tf
4.01Z_NO_IND_0D.density
4.14Z_NO_IND_P01.density
4.1M.density
4.20F_NO_IND_M1.density

linux01 [aiclabta04/UM180FDKMF_C05_PB]# ls
0.18um_techfile.tf      DRC_runset
4.01Z_NO_IND_0D.density  INV_teacher.calibre.db
4.14Z_NO_IND_P01.density INV_teacher.drc.results
4.1M.density            INV_teacher.drc.summary
4.20F_NO_IND_M1.density INV_teacher.erc.results
4.20S_M1.density        INV_teacher.erc.summary
4.22F_NO_IND_M2.density INV_teacher.lvs.report
4.22S_M2.density        INV_teacher.lvs.report_ext
4.24F_NO_IND_M3.density INV_teacher.sp
4.24G_NO_IND_M3.density INV_teacher.src.net
4.26F_NO_IND_M4.density Lab_inv
4.26G_NO_IND_M4.density Models
4.28F_NO_IND_M5.density PIP0.LOG
4.28G_NO_IND_M5.density PIP0.LOG_INV_teacher
4.31E_NO_IND_M6.density UMC_18_CMOS
4.31F_NO_IND_M6.density _G-DF-MIXED_MODE_RFCH0S18-1.8V_3.3V-1P6M-MMC_CALIBRE-LVS-2.1-P8.txt_
Calibre                 _G-DF-Mixed_Mode_RFCH0S18-1.8V_3.3V-1P6M-MMC-Calibre-DRC-2.11_P2_
linux01 [aiclabta04/UM180FDKMF_C05_PB]# vim calview.log
```

用文字編輯器打開calview.log檔，此檔存在跑virtuoso&的資料夾下

CIW會列出回報

```
ciwb - Log : /misc/RAID/COURSE/aiclab/aiclabta04/CDS.log
File Tools Options Help 1
// log_port port:" ./calview.log"
NOTE: Creating CalibreView for cell INV_teacher ...
WARNING: Not creating terminal VIN in (INV_teacher.calibre) since matching terminal was not found on
WARNING: Not creating terminal VOUT in (INV_teacher.calibre) since matching terminal was not found on
Portection: "INV_teacher.calibre"
Warning: Pin "MINUS" on instance "VIN_57" floating input/output.
Warning: Floating net "VIN" at (12.0125, -6.8250).
Warning: Terminal "IN" in view symbol not found in "INV_teacher.calibre".
Warning: Terminal "Vout" in view symbol not found in "INV_teacher.calibre".
Warning: Terminal "Vin" in view symbol not found in "INV_teacher.calibre".
Warning: Terminal "vin" in view schematic not found in "INV_teacher.calibre".
Calibre View generation completed with 0 WARNINGS and 0 ERRORS.
Please consult the CIW transcript for messages.
```

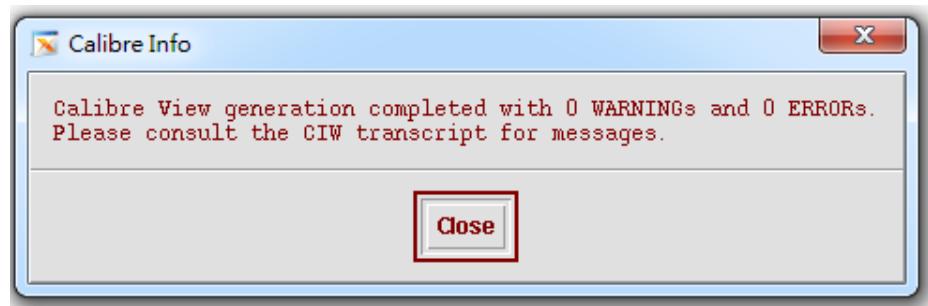
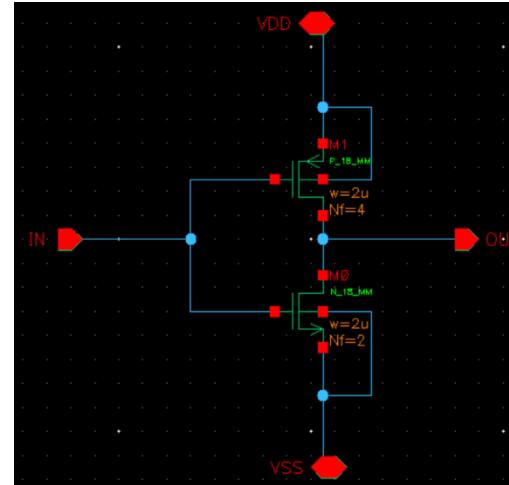
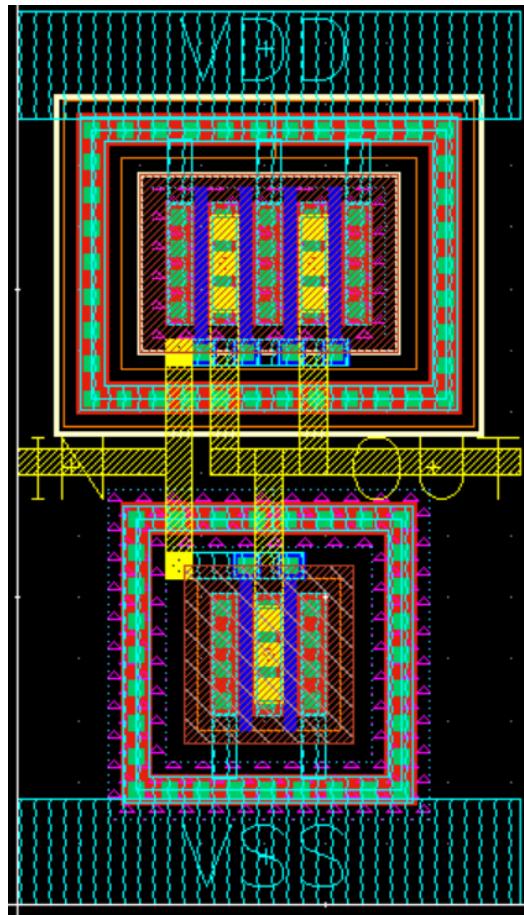
```
xterm
NOTE: Creating CalibreView for cell INV_teacher ...
WARNING: Not creating terminal VIN in (INV_teacher.calibre) since matching terminal
was not found on symbol.
WARNING: Not creating terminal VOUT in (INV_teacher.calibre) since matching termina
l was not found on symbol.
The "N_18_MM" device contains the following un-matched parametr(s):
("Ipe")
The "P_18_MM" device contains the following un-matched parametr(s):
("Ipe")
Calibre View generation completed with 2 WARNINGS and 0 ERRORS.
Please consult the CIW transcript for messages.
```

此處也會列出warning和error，這段說明找不到VIN與VOUT，這是由於PEX只會認大寫的Pin名稱



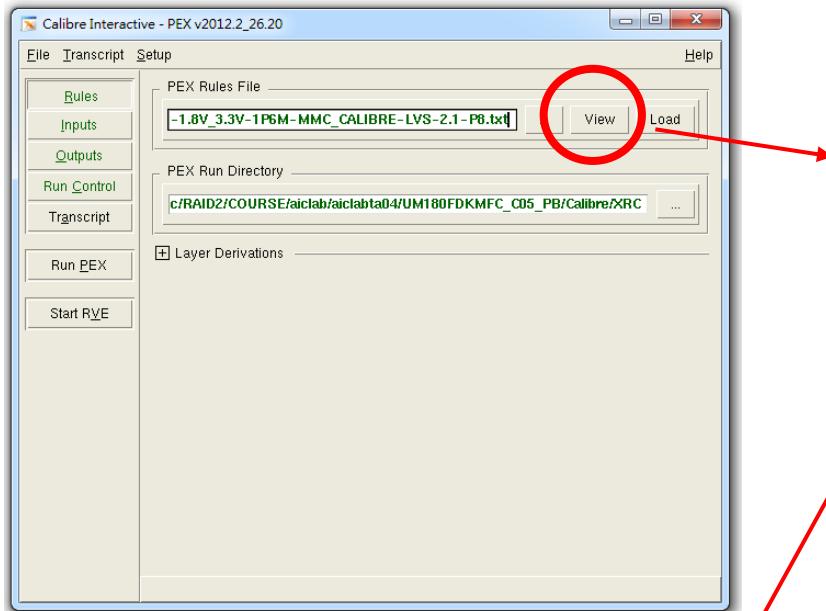
# Verification – PEX (9)

- ◆ 兩種改善方式，一種是把Pin名稱全改成大寫，如先前範例



# Verification – PEX (10)

- ◆ 另一種是在PEX的rule檔內，修改幾個選項



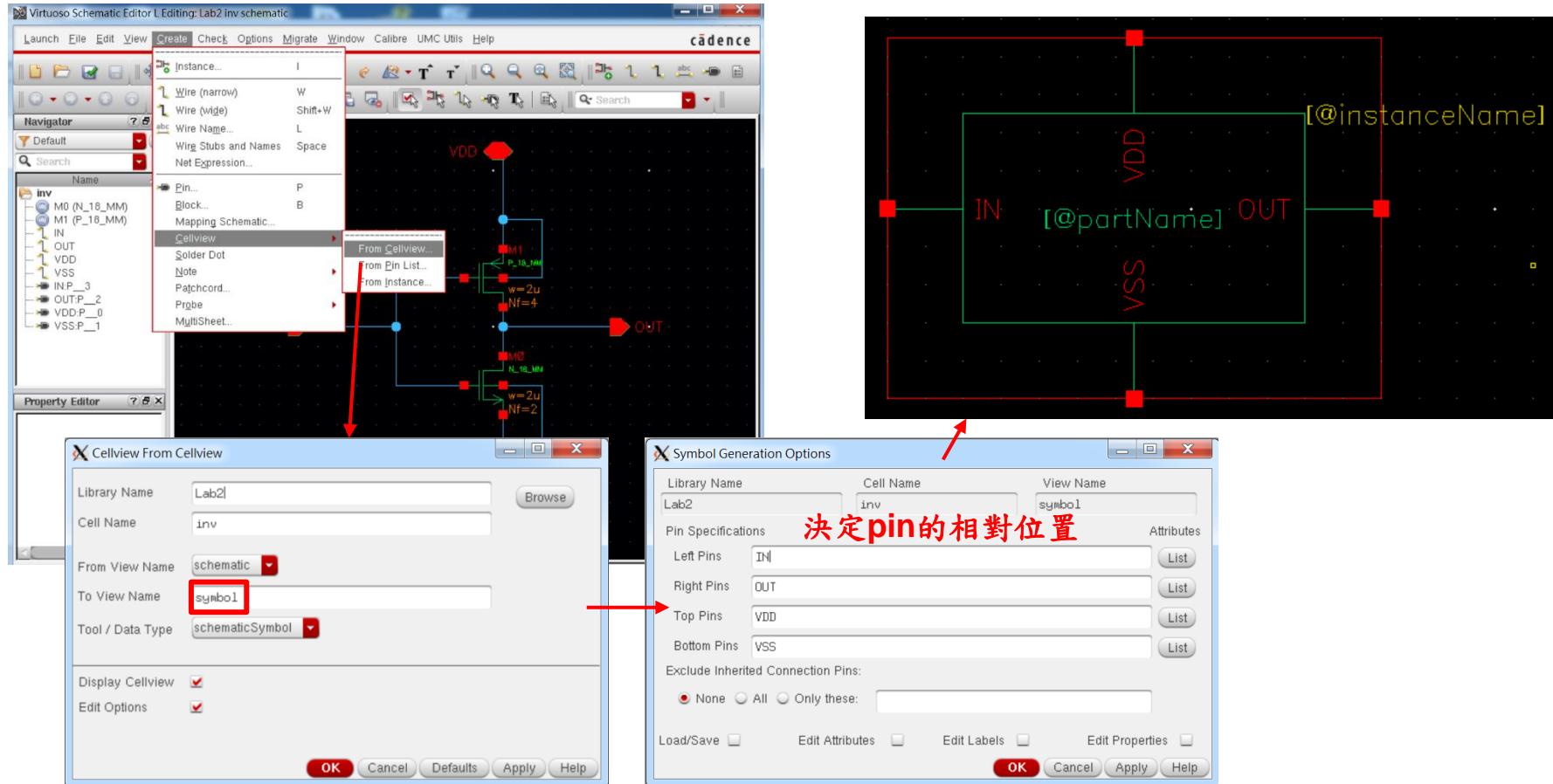
```
//////  
// LVS Setup Options  
//////  
LVS SPICE REPPLICATE DEVICES YES  
LVS ALL CAPACITOR PINS SWAPPABLE NO  
#IFDEF LIB  
    LVS IGNORE PORTS YES  
#ELSE  
    LVS IGNORE PORTS NO  
#ENDIF  
  
LVS RECOGNIZE GATES NONE //CALIBRE tool default is ALL  
LVS REDUCE SPLIT GATES YES  
LVS CHECK PORT NAMES YES //CALIBRE tool default is NO  
LVS COMPARE CASE YES  
LAYOUT CASE YES // If customers want to use the CASE sensitive for Layo  
SOURCE CASE YES // If customers want to use the CASE sensitive for sou  
  
LVS REPORT OPTION A B C D E  
LVS REPORT MAXIMUM 1000  
LVS REDUCE PARALLEL BIPOLAR YES  
LVS REDUCE PARALLEL CAPACITORS YES  
LVS REDUCE C (MIMCAPM_RF) PARALLEL NO  
  
LVS REDUCE PARALLEL DIODES YES  
LVS REDUCE PARALLEL MOS YES  
LVS REDUCE PARALLEL RESISTORS YES  
LVS REDUCE SERIES CAPACITORS YES  
LVS REDUCE SERIES RESISTORS YES  
LVS REPORT ON SUPPLY ERROR NO
```

預設是NO，改成YES可讓PEX自動認出小寫



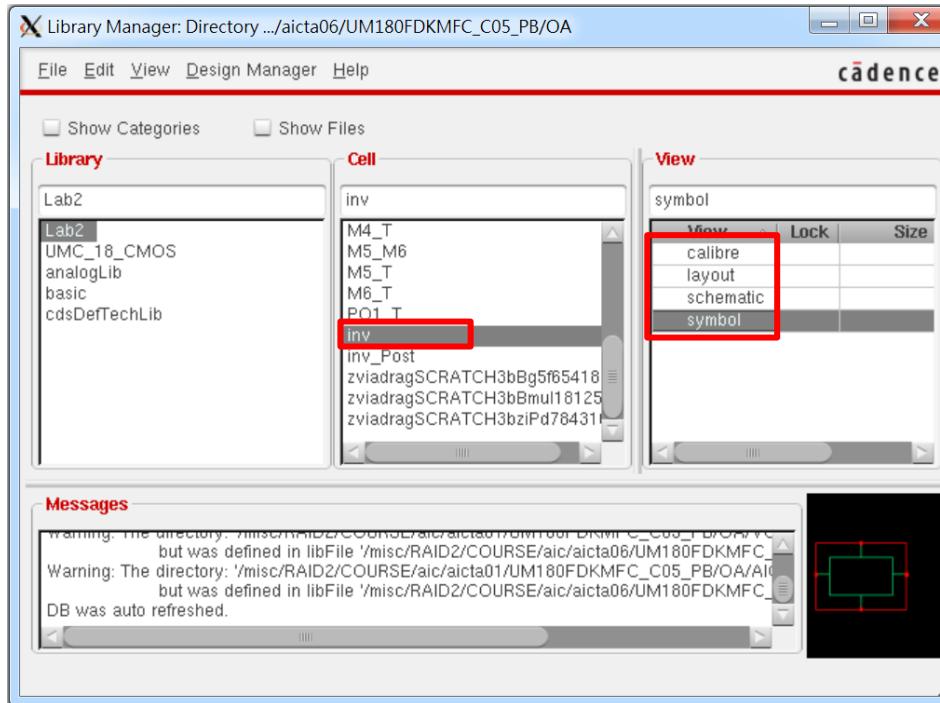
# Post-layout Simulation (1)

## ◆ 利用先前的schematic電路圖建立一個symbol



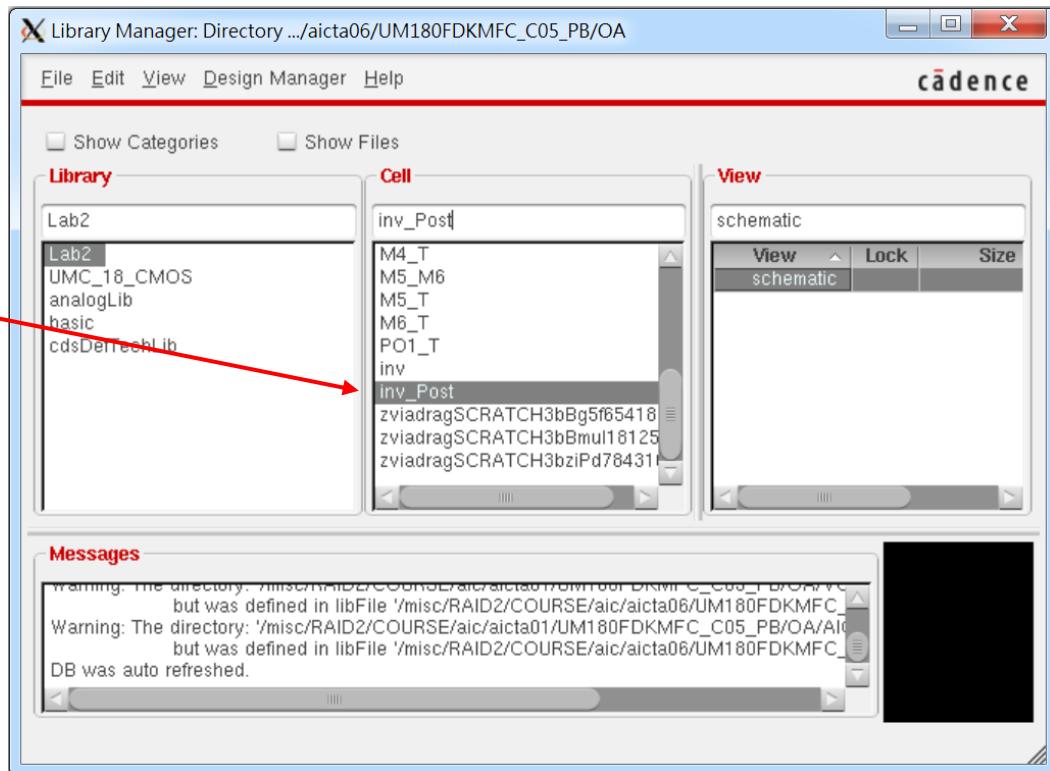
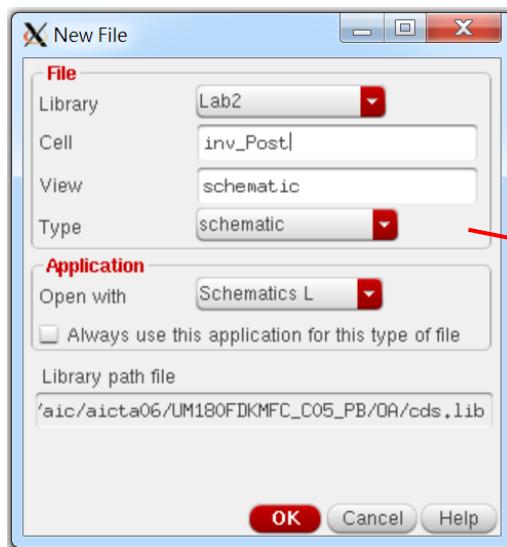
# Post-layout Simulation (2)

- ◆ 此時cell內會有layout、schematic、calibre、symbol等檔案



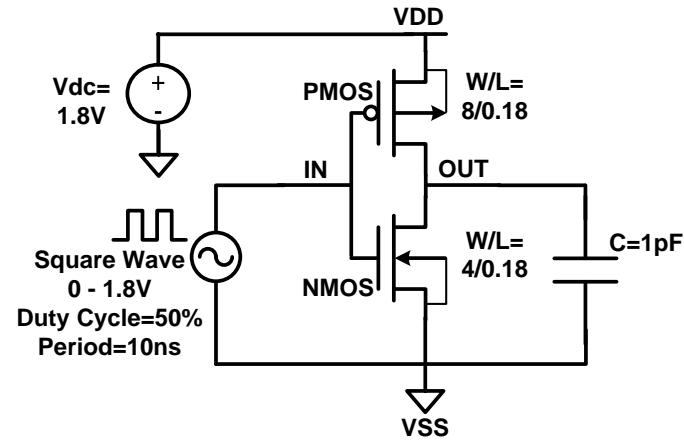
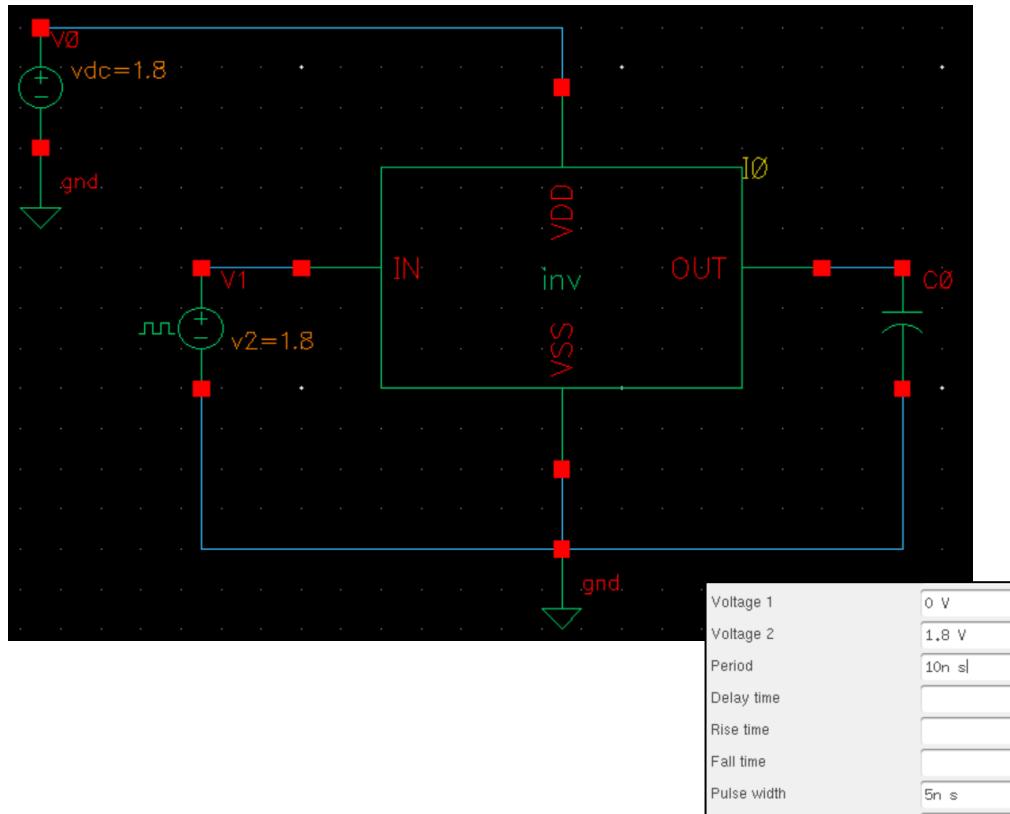
# Post-layout Simulation (3)

- ◆ 接下來在同一個library內，建立第二個Cell，名稱自取，別跟第一個cell一樣，type選擇Schematic，準備作Post-simulation



# Post-layout Simulation (4)

- ◆ 在第二個cell的Schematic內，加入第一個cell的symbol (快捷鍵”i”), 並將相關的輸入源、電源、接地等連接好，準備在ADE分析電路



analoglib

vdc: DC voltage source

gnd: ground

vpulse: square wave voltage source

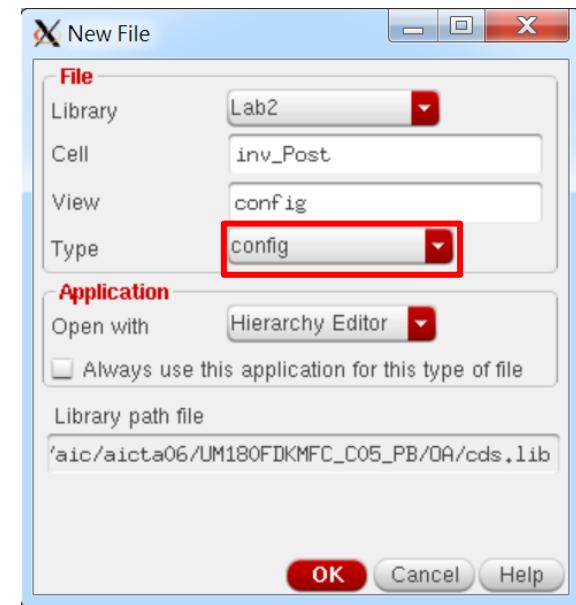
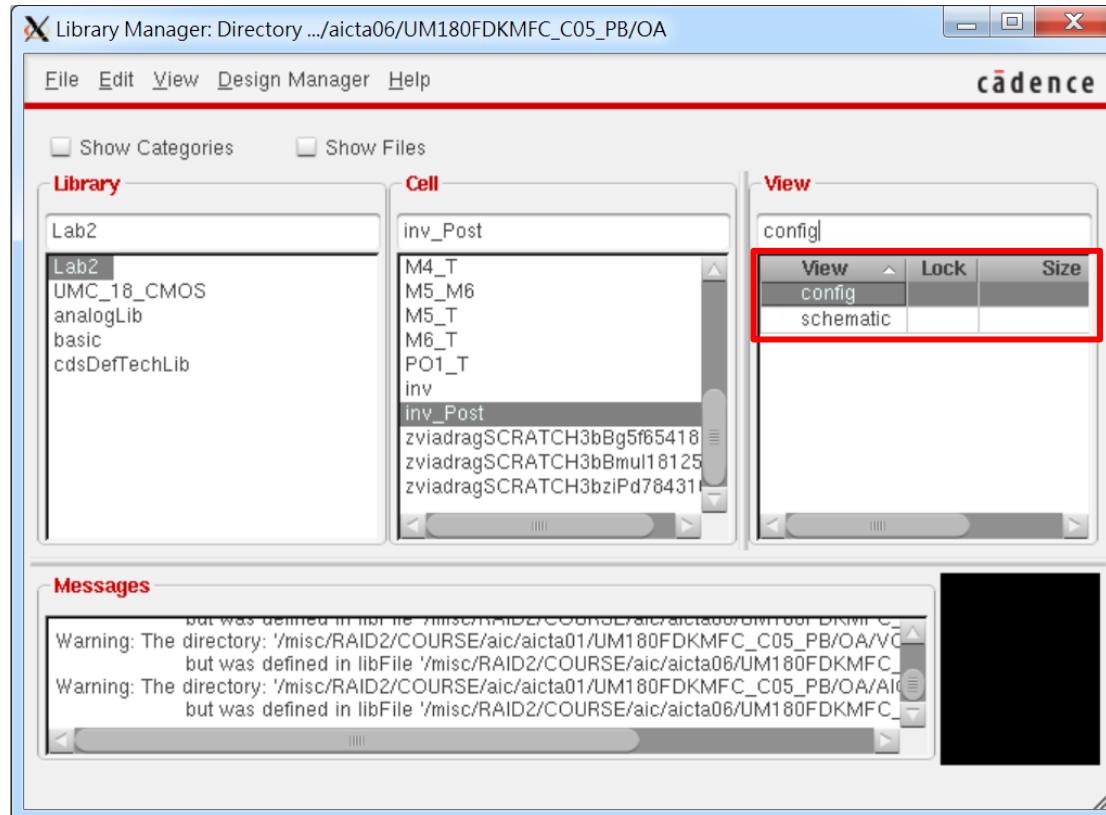
cap: capacitor

設定輸入理想方波



# Post-layout Simulation (5)

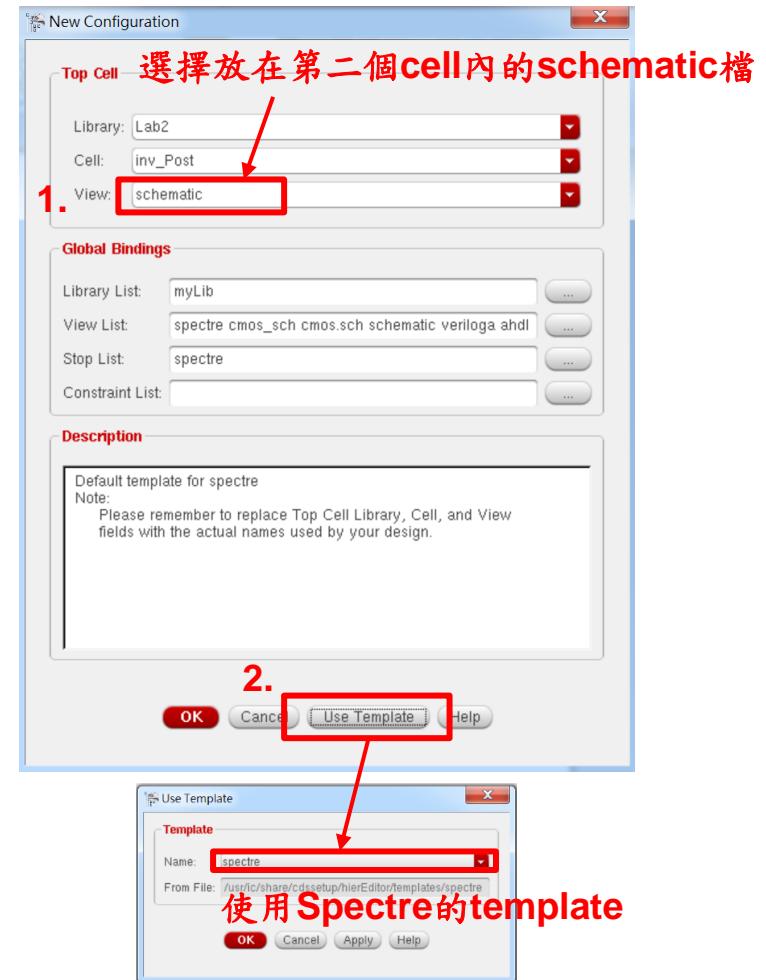
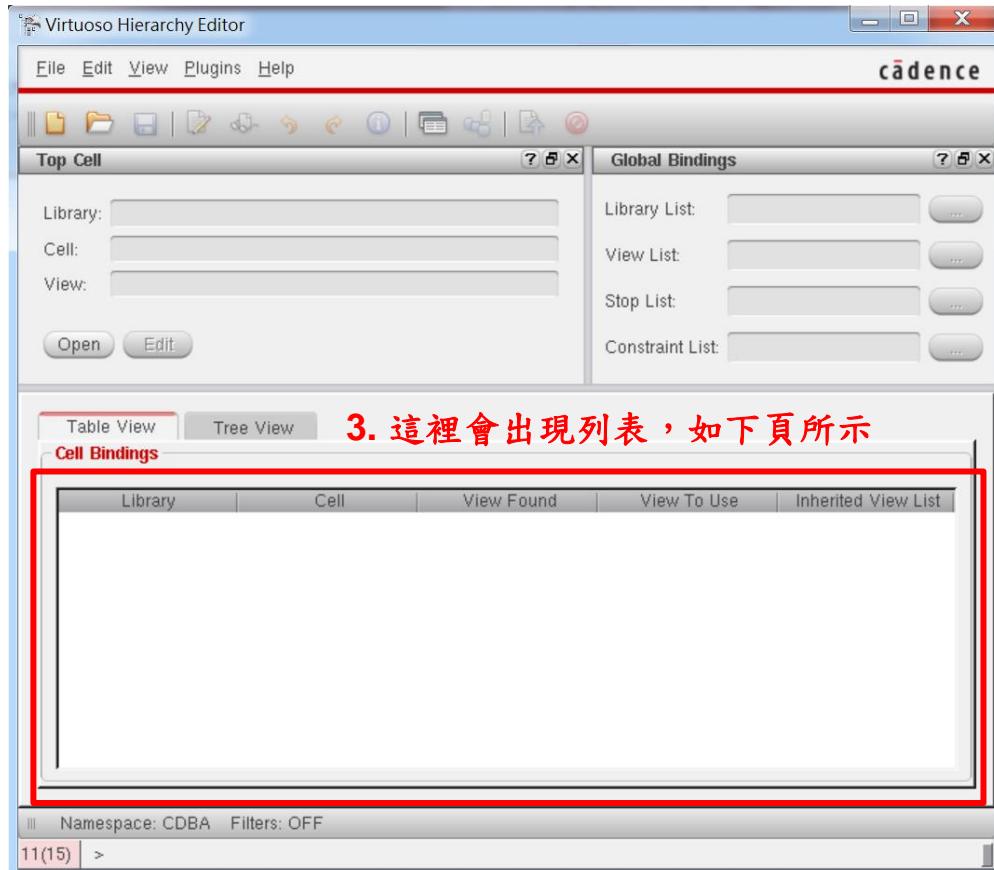
- ◆ File → New → Cell View
- ◆ 在第二個Cell內，建立config檔，type選擇config



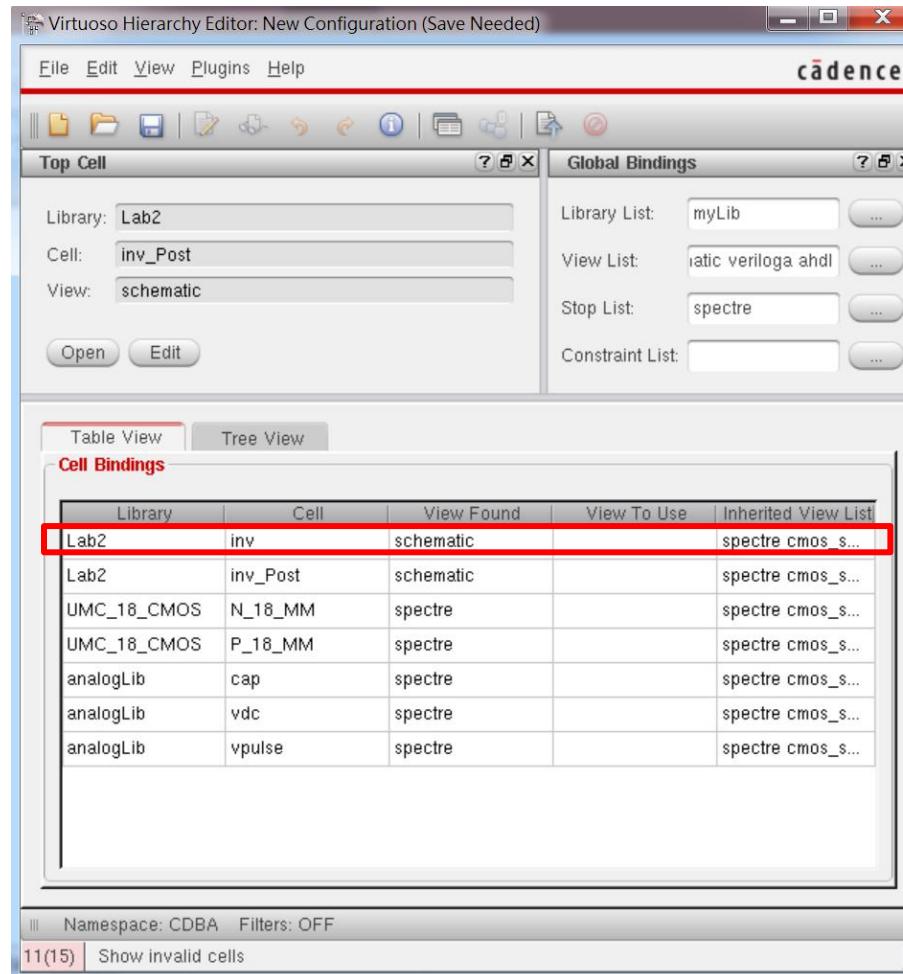
按OK後出現下頁設定視窗



# Post-layout Simulation (6)



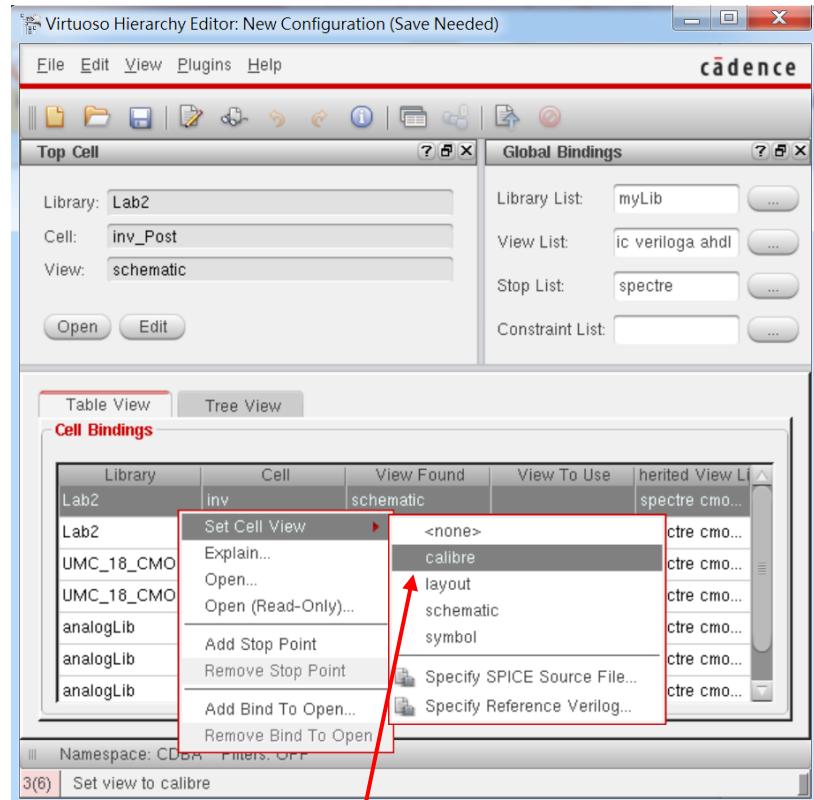
# Post-layout Simulation (7)



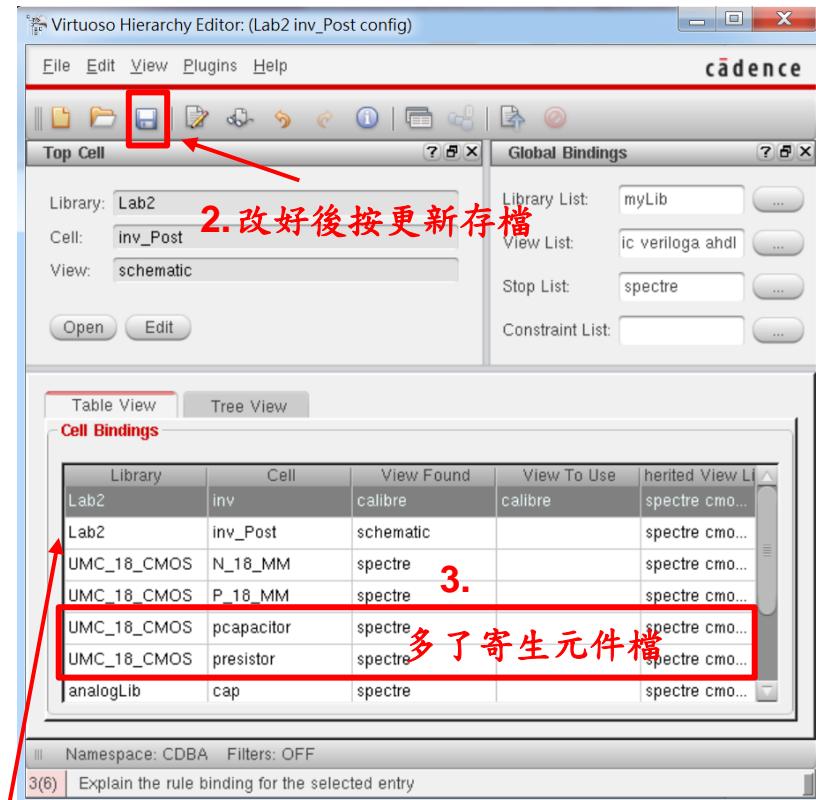
第一個Cell設定為  
Schematic檔，  
可以進行Pre-Simulation



# Post-layout Simulation (8)



1. 第一個Cell處點右鍵，選擇calibre view檔

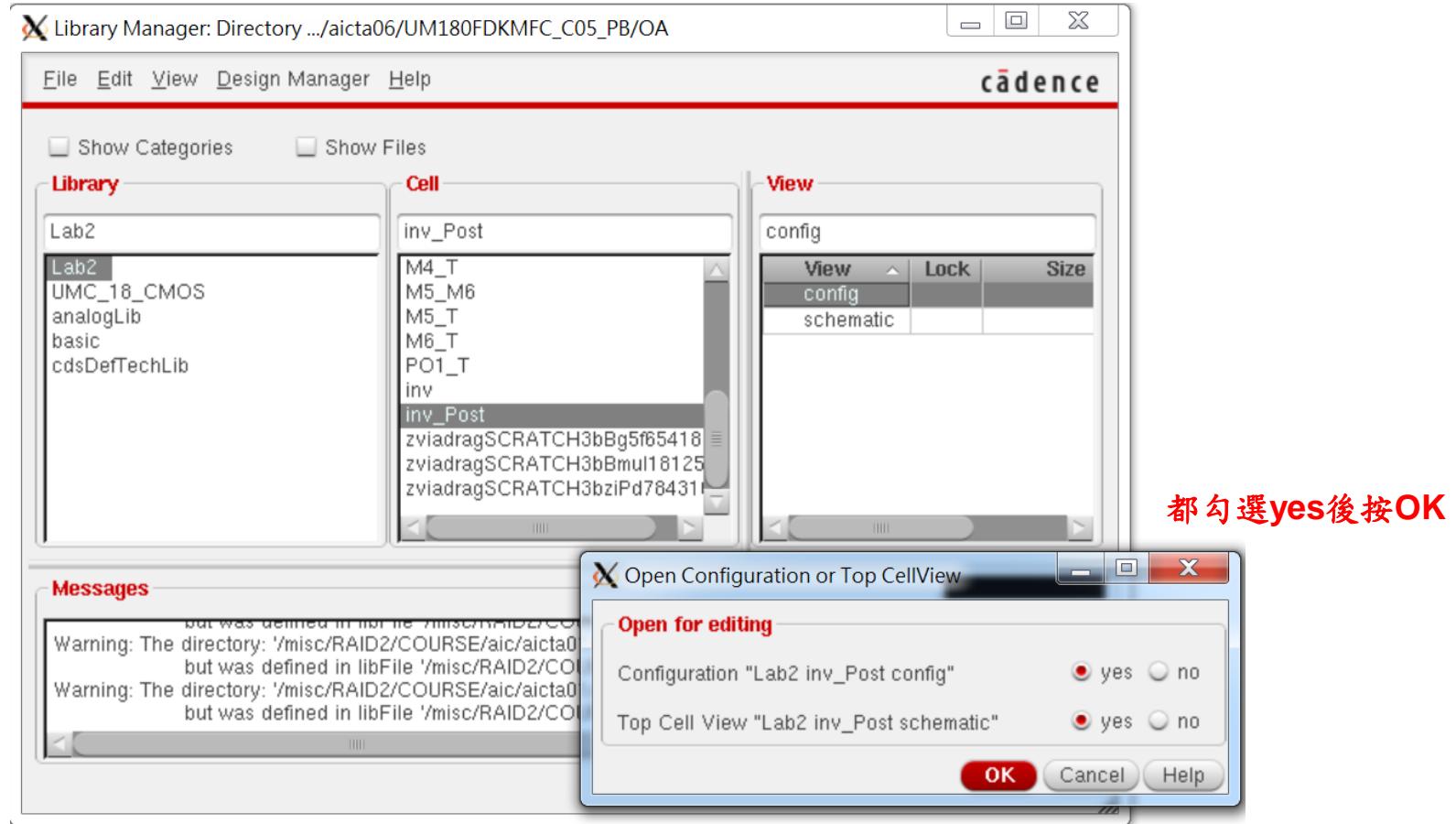


第一個Cell變更為calibre檔，可以進行Post-Simulation



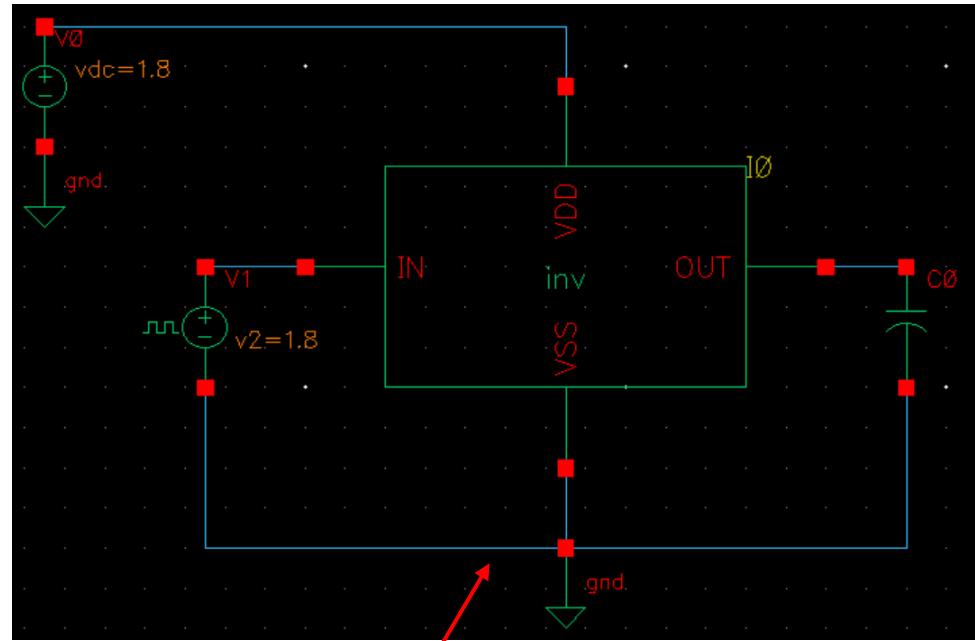
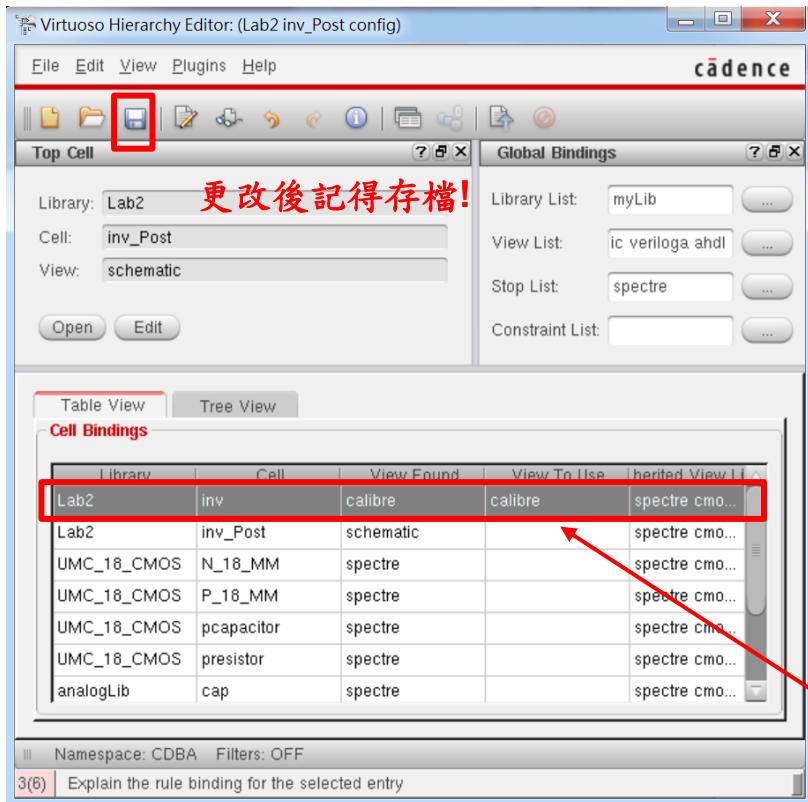
# Post-layout Simulation (9)

- ◆ 上頁存好檔後關掉，再開啟config檔，此時會跳出下列訊息視窗



# Post-layout Simulation (10)

◆ 承上頁，會跳出下列訊息視窗

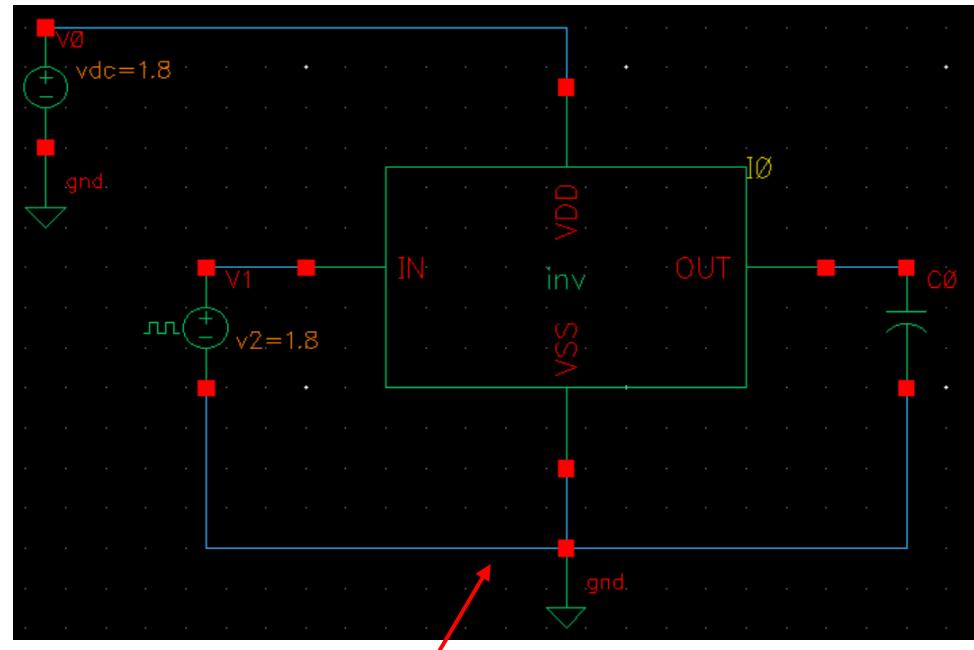
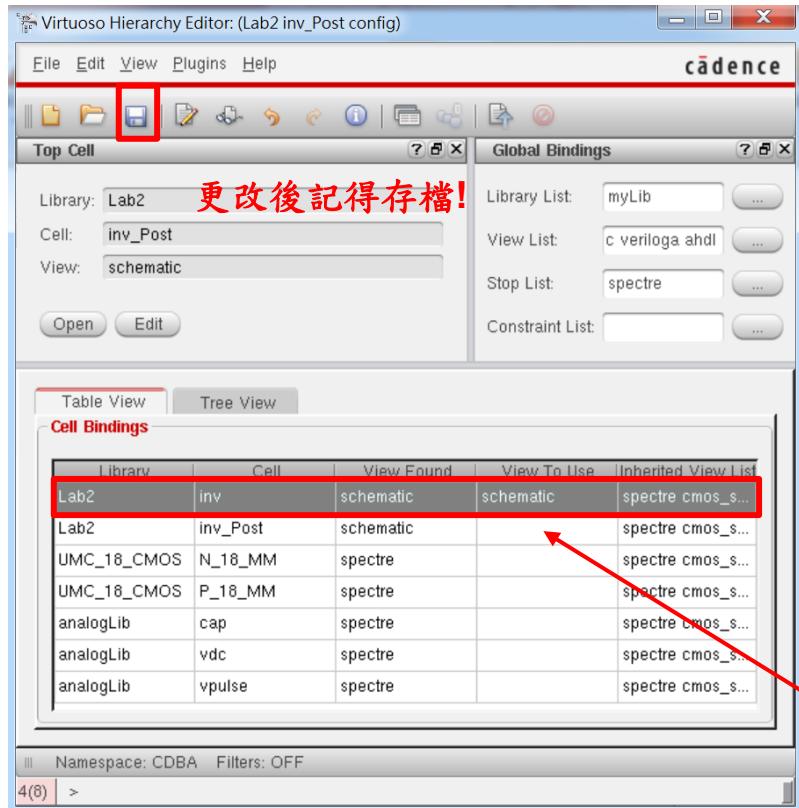


選擇calibre檔案且存檔，此時右邊的schematic view可以跑Post-layout Simulation



# Post-layout Simulation (11)

◆ 承上頁，改變輸入檔為schematic檔

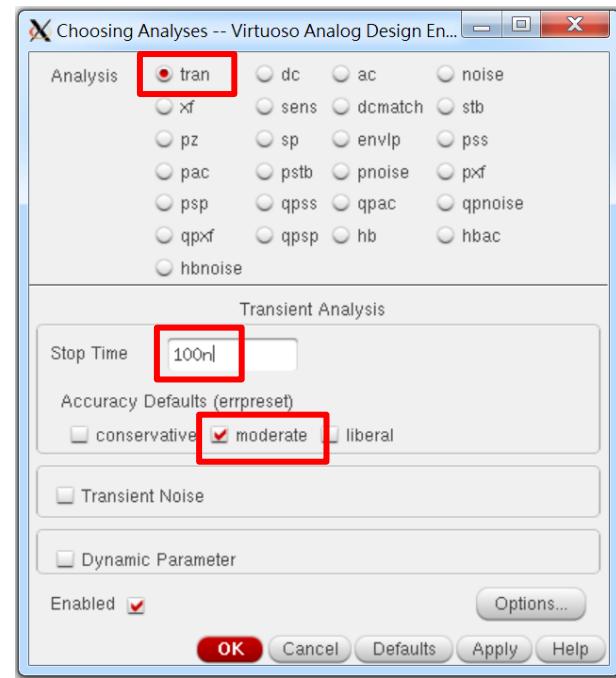
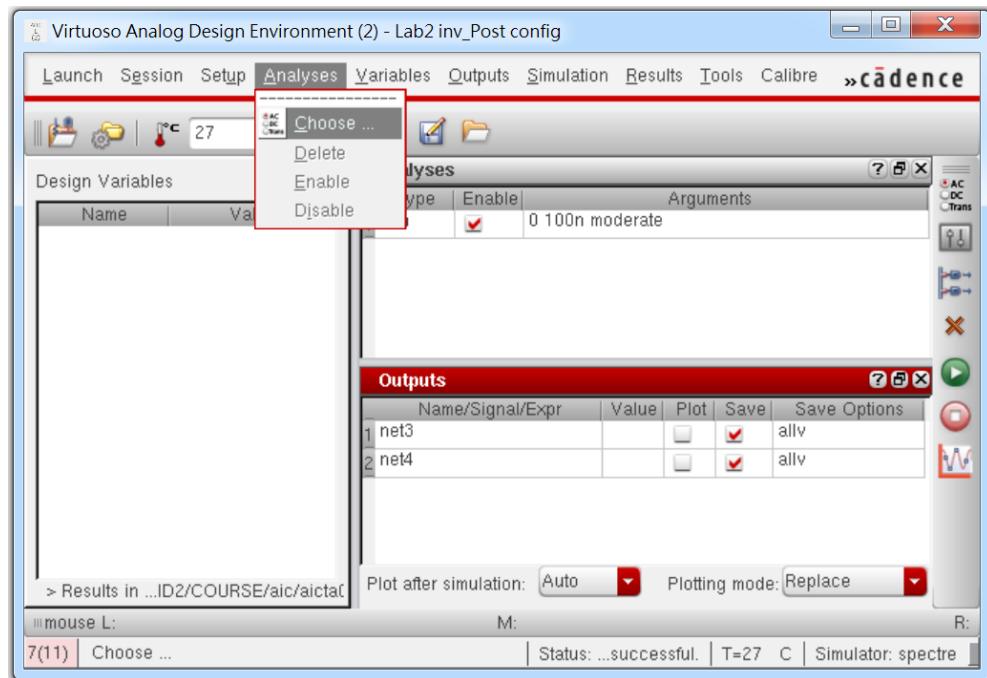


按右鍵選擇schematic檔後存檔，此時右邊的schematic view可以跑Pre-layout Simulation



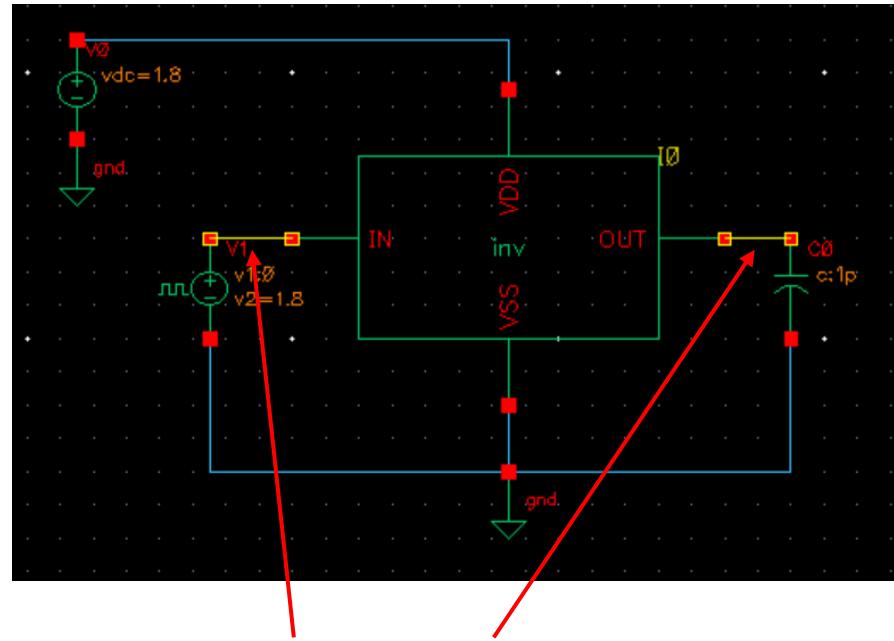
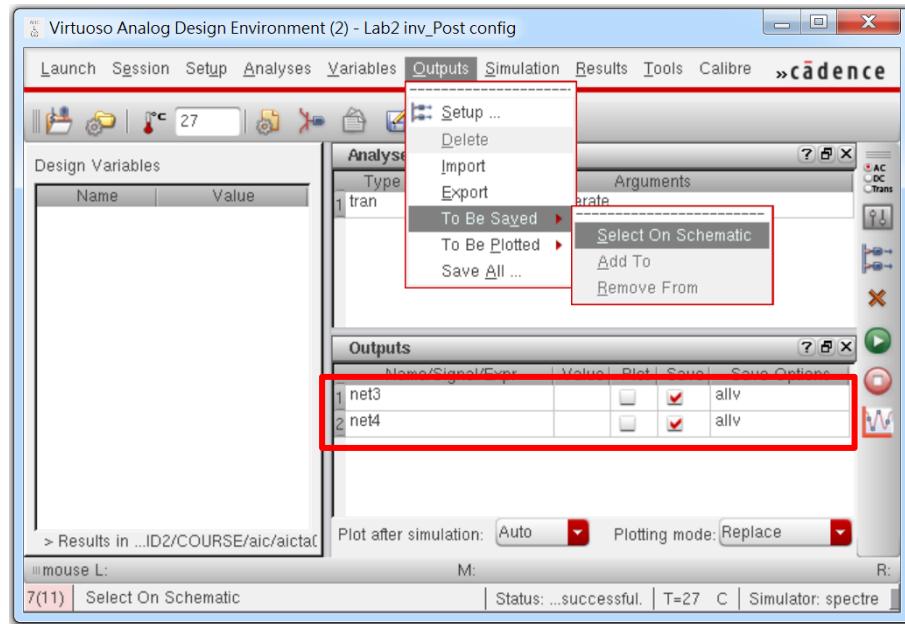
# Post-layout Simulation (12)

- ◆ Tool → Analog Environment
- ◆ 打開ADE, 做transient分析, 時間設定100ns



# Post-layout Simulation (13)

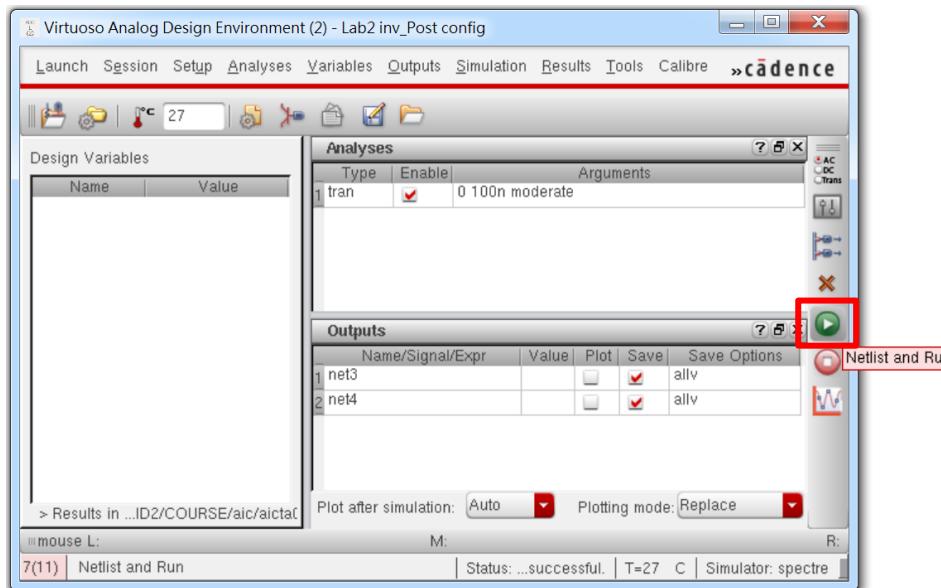
- ◆ Output → To Be Saved → Select On Schematic
- ◆ 點選IN和OUT兩個節點的wire來觀察輸入輸出的電壓訊號



在schematic上點選Wire觀察電壓



# Post-layout Simulation (14)



The screenshot shows the Cadence Spectre command-line interface. The title bar reads 'c:/misc/RAID2/COURSE/aic/aicta06/simulation/inv\_Post/spectre/config/pf/spectre.out' and the window title is 'cadence'. The main area displays the simulation transcript, which includes parameters like relref = sigglobal, cmin = 0 pF, gmin = 1 pS, maxrstd = 0 Ohm, mos\_method = s, and mos\_vres = 50 mV. It then lists numerous 'tran' analysis steps with their time, step size, and percentage completion. At the bottom of the transcript, it says 'Number of accepted tran steps = 478.', 'Initial condition solution time = 0 s.', 'Intrinsic tran analysis time = 30 ms.', and 'Total time required for tran analysis 'tran' was 30 ms.' Below the transcript, there is a message about writing operating point information to rawfile, model parameter values, instance parameter values, output parameter values, netlist parameters, primitives, and subcircuits. The status bar at the bottom indicates '12 HelpAction'.

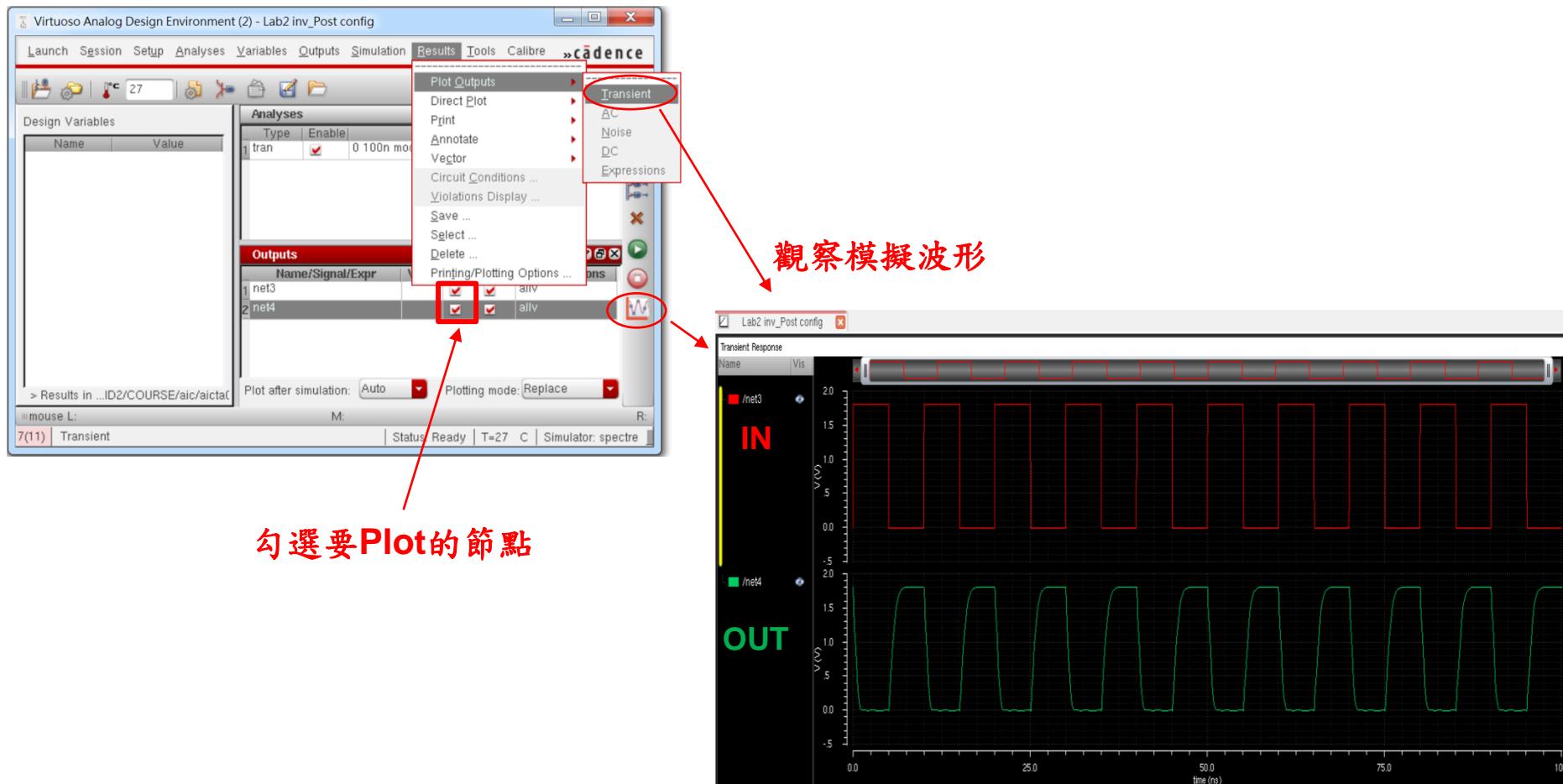
```
relref = sigglobal
cmin = 0 pF
gmin = 1 pS
maxrstd = 0 Ohm
mos_method = s
mos_vres = 50 mV

tran: time = 2,649 ns (2.65 %), step = 528.8 ps (529 m%)
tran: time = 7,859 ns (7.86 %), step = 376.3 ps (376 m%)
tran: time = 13,03 ns (13 %), step = 737.2 ps (737 m%)
tran: time = 17,87 ns (17.9 %), step = 376.2 ps (376 m%)
tran: time = 22,63 ns (22.6 %), step = 534.2 ps (534 m%)
tran: time = 27,69 ns (27.7 %), step = 333.3 ps (333 m%)
tran: time = 32,74 ns (32.7 %), step = 589.6 ps (590 m%)
tran: time = 37,86 ns (37.9 %), step = 374.6 ps (375 m%)
tran: time = 43,03 ns (43 %), step = 736.6 ps (737 m%)
tran: time = 47,87 ns (47.9 %), step = 376.2 ps (376 m%)
tran: time = 52,63 ns (52.6 %), step = 534.2 ps (534 m%)
tran: time = 57,69 ns (57.7 %), step = 333.3 ps (333 m%)
tran: time = 62,74 ns (62.7 %), step = 589.6 ps (590 m%)
tran: time = 67,86 ns (67.9 %), step = 374.6 ps (375 m%)
tran: time = 73,03 ns (73 %), step = 736.6 ps (737 m%)
tran: time = 77,87 ns (77.9 %), step = 376.2 ps (376 m%)
tran: time = 82,63 ns (82.6 %), step = 534.2 ps (534 m%)
tran: time = 87,69 ns (87.7 %), step = 333.3 ps (333 m%)
tran: time = 92,74 ns (92.7 %), step = 589.6 ps (590 m%)
tran: time = 97,86 ns (97.9 %), step = 374.6 ps (375 m%)
Number of accepted tran steps = 478.
Initial condition solution time = 0 s.
Intrinsic tran analysis time = 30 ms.
Total time required for tran analysis 'tran' was 30 ms.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```



# Post-layout Simulation (15)



# Post-layout Simulation (16)



# ADE Markers Bindkey

## ◆ Markers in Virtuoso Analog Design Environment (IC6.1.5)

Key	Function
m	Point marker
v	Vertical marker
h	Horizontal marker
a/b	Points A/B marker
Shift-d	delta's amongst selected markers
d	create 2nd marker and delta

➤ Shift-d:

Select 2 or more of the markers and then press Shift-d to get delta markers between them.

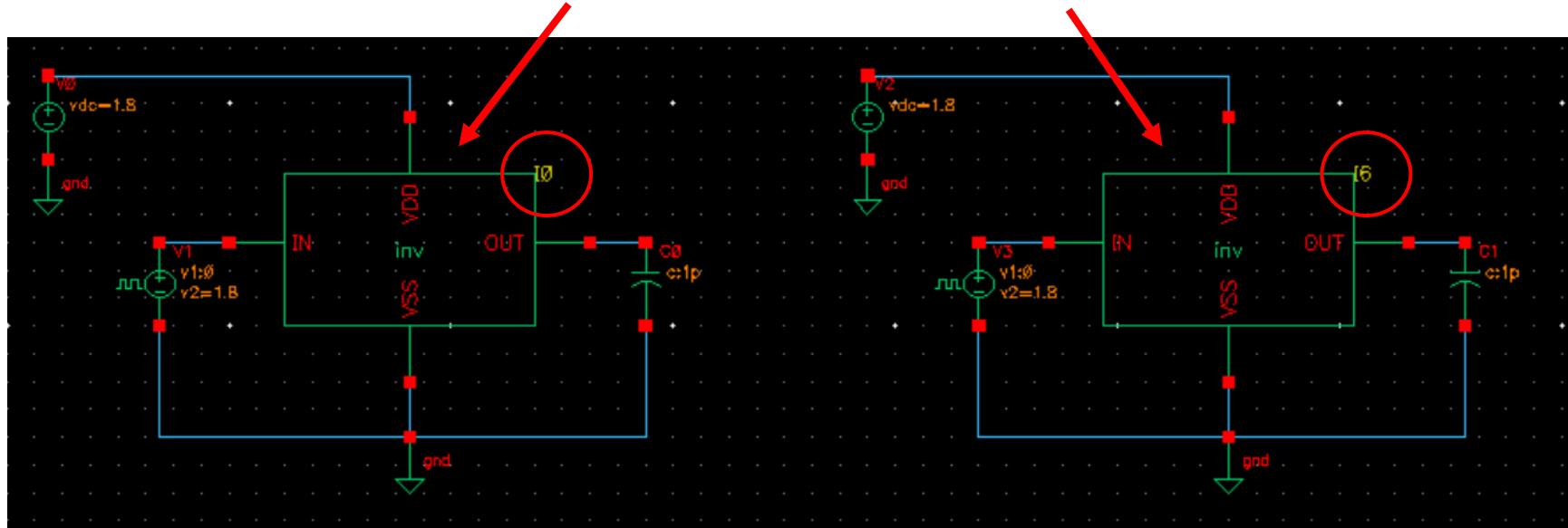
➤ Bindkey d:

Select a point, and then wherever press the d key, a 2nd marker and the delta between them will perform.

# Post-layout Simulation (17)

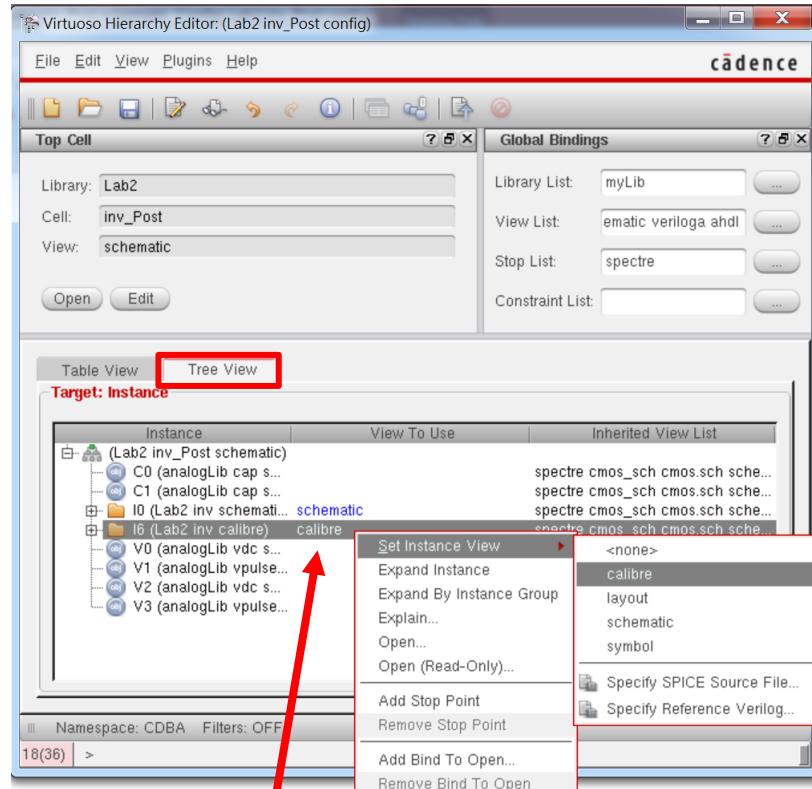
- ◆ 以下示範在ADE同時觀察Pre-Sim和Post-Sim的電路模擬結果

在schematic視窗內複製電路，電路名會不一樣，左邊是i0，右邊是i6

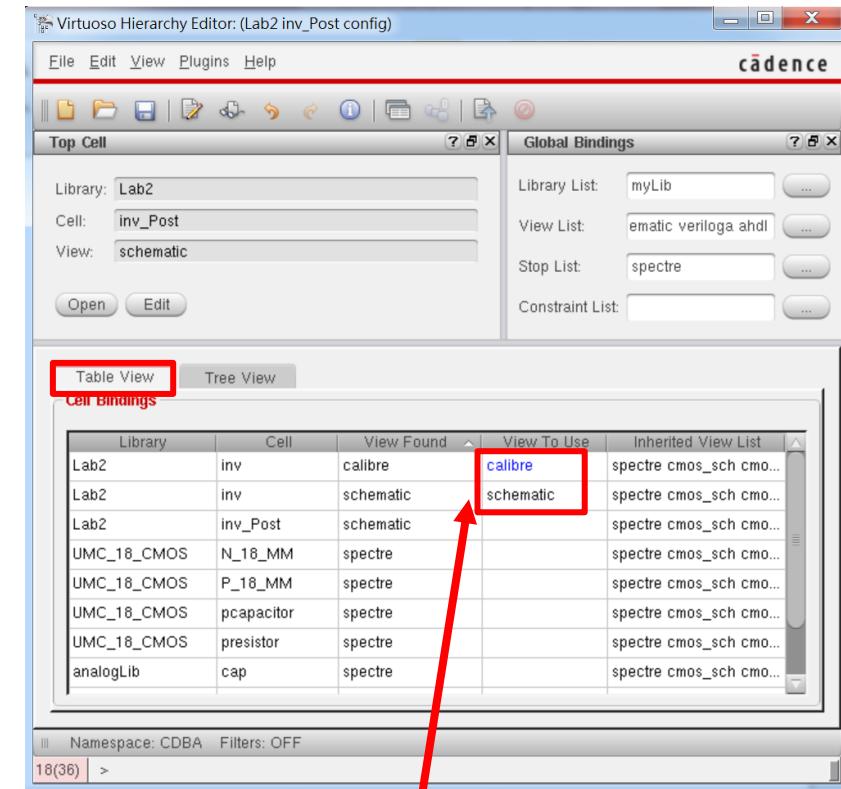


# Post-layout Simulation (18)

## ◆ 承續前頁



打開Config，在Tree View內把i6物件(滑鼠右鍵)設定成Calibre

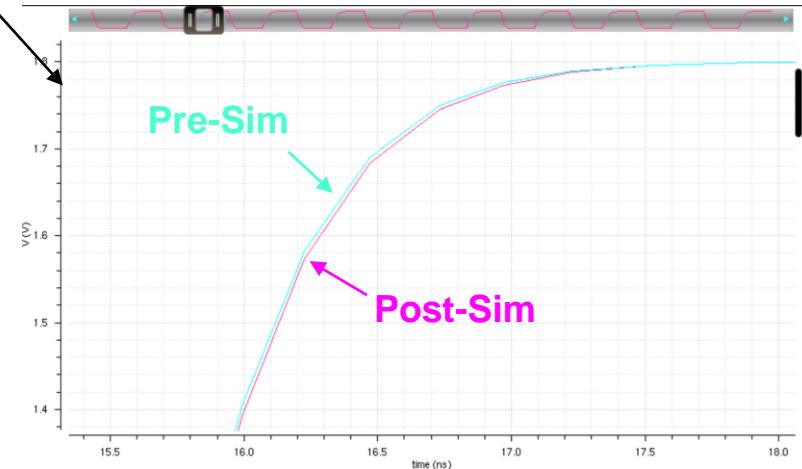
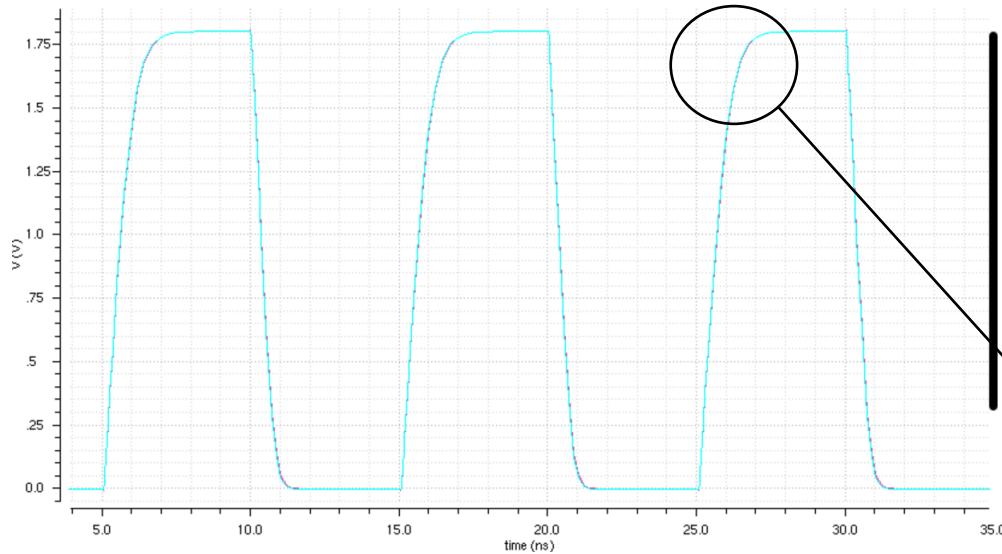


存檔後回到Table View，會出現兩種View



# Post-layout Simulation (19)

◆ 承續前頁，觀察波形



# Post-layout Simulation (20)

## ◆ 觀察節點電容值

打開PEX，點選Start RVE

```
// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.  
//  
// Mentor Graphics software executing under x86-64 Linux  
//  
// Running on Linux linux05 2.6.32-573.e16.x86_64 #1 SMP Thu Jul 23 15  
// 64 bit virtual addressing enabled  
// Running calibre/pkgs/icv/pvt/calibre.alt -nowait -rve -pex /misc/RA  
Process ID: 24873  
//  
Starting time: Tue Mar 14 15:54:54 2017  
//  
Running on 1 CPU  
//  
// Graphical User-Interface startup.... Complete.  
//  
// calibreadb license acquired.  
// RVE authorized.  
  
28 Warnings |  
  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2008.3, the following SVRF command is deprecated: PEX TEMPERATL  
As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRA'  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI  
As of version 2008.3, the following SVRF command is deprecated: PEX TEMPERATL  
As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRA'  
As of version 2009.1, the following SVRF command should not be used : PEX VIA RI
```

觀察節點電容值

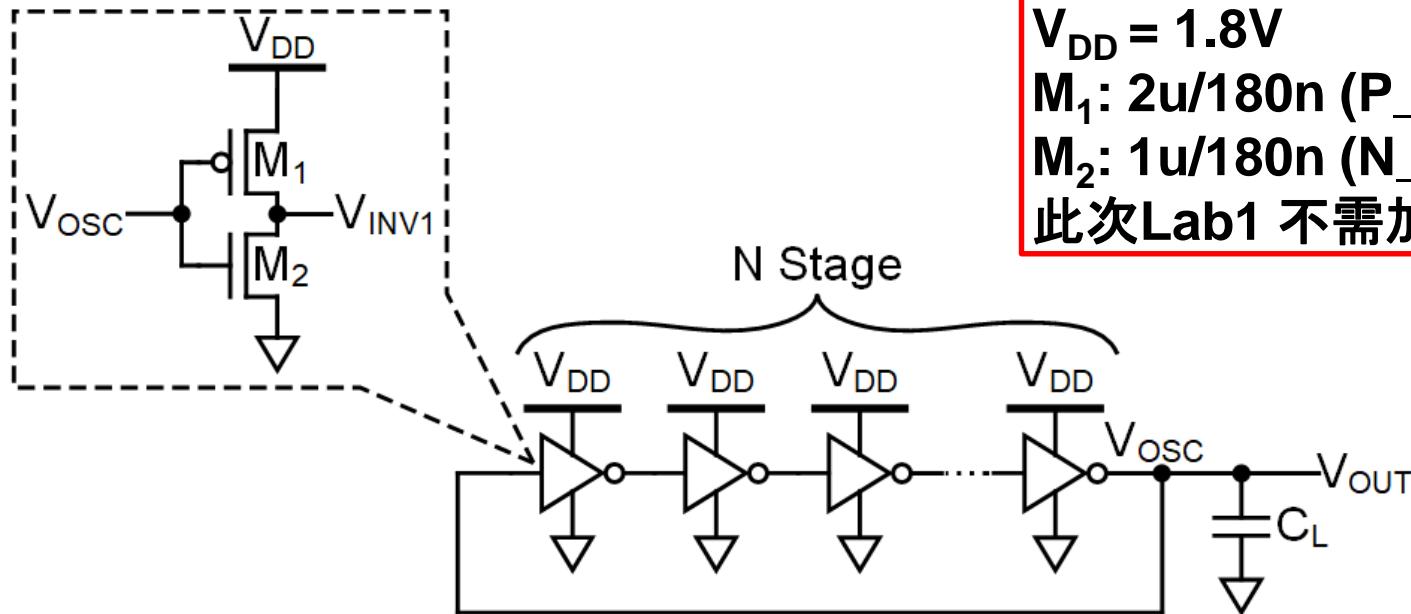
No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	IN	IN	34	8.18701E-16	2.3528E-15	3.05398E-15
2	OUT	OUT	37	2.07692E-16	3.36234E-15	3.57003E-15
3	VSS	VSS	44	7.65706E-16	1.45378E-15	2.21949E-15
4	VDD	VDD	52	7.50086E-16	2.52390E-15	3.27476E-15

C: 對地的寄生電容值  
CC: metal間寄生耦合電容值



# Lab 1

## ◆ 完成19級 Ring Oscillator的Post-Layout Simulation



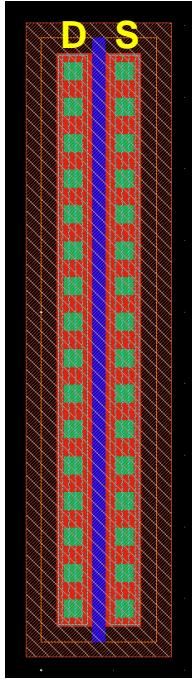
$$f_{osc} = \frac{1}{2 \cdot (t_{Delay1} + t_{Delay2} + \dots + t_{DelayN})}$$

Pre-simulation及Post-simulation結果誤差請小於2.5%內  
備註: Schematic及Layout請使用相同的finger number/ multiplier

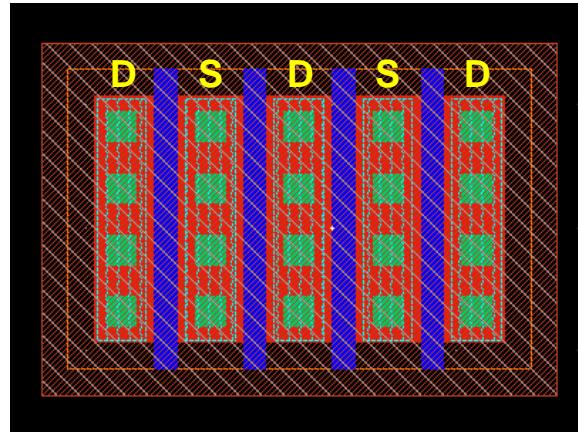


# Finger Number

## ◆ Single Finger / Multiple Fingers



更改Finger Number時，Finger Width會自動計算為Total Width/Finger Number



Total Width = 8um  
Finger Width = 8um  
L = 180nm  
Finger Number = 1

Total Width = 8um  
Finger Width = 2um  
L = 180nm  
Finger Number = 4

## Schematic View

CDF Parameter	Value	Display
Model Name	n_18_mm	off ▾
Total Width	8u M	off ▾
Finger Width	8u M	off ▾
Length	180.0n M	off ▾
Finger Number	1	off ▾
mis_flag	1	off ▾
Source Drain Metal Width	400.0n M	off ▾
AD AS PD PS Editable	<input type="checkbox"/>	off ▾
Drain diffusion area (m^2)	3.92e-12	off ▾
Source diffusion area (m^2)	3.92e-12	off ▾
Drain diffusion periphery	16.98u M	off ▾
Source diffusion periphery	16.98u M	off ▾
Multiplexer	1	off ▾

更改Multiplier時，上面的數值皆不會更動，要自行計算Total Width

## Layout View

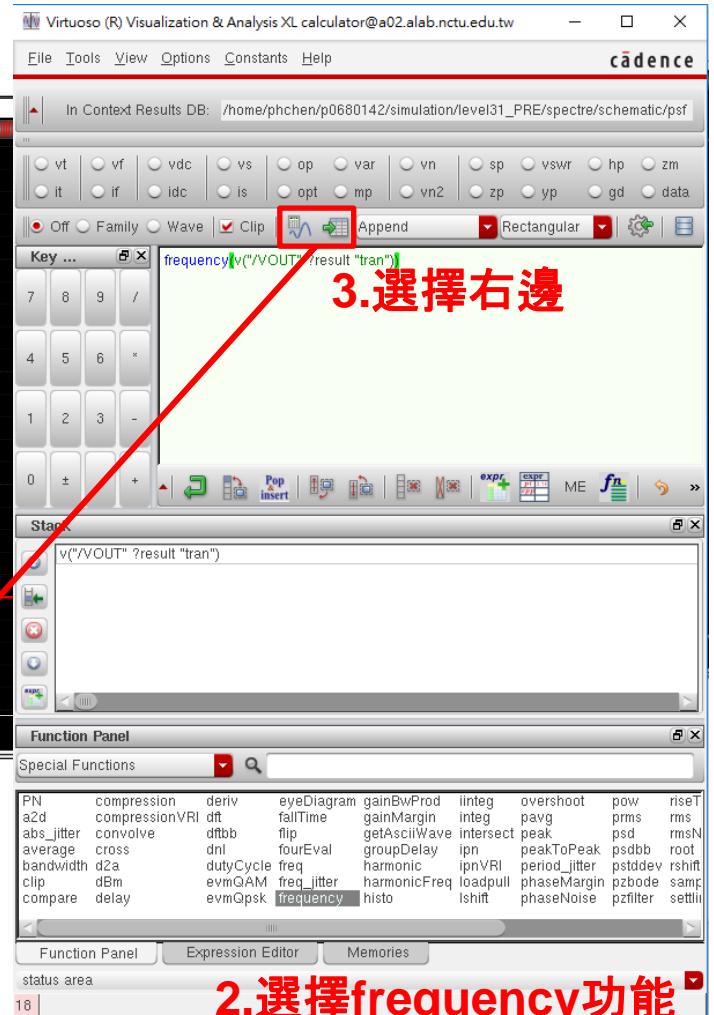
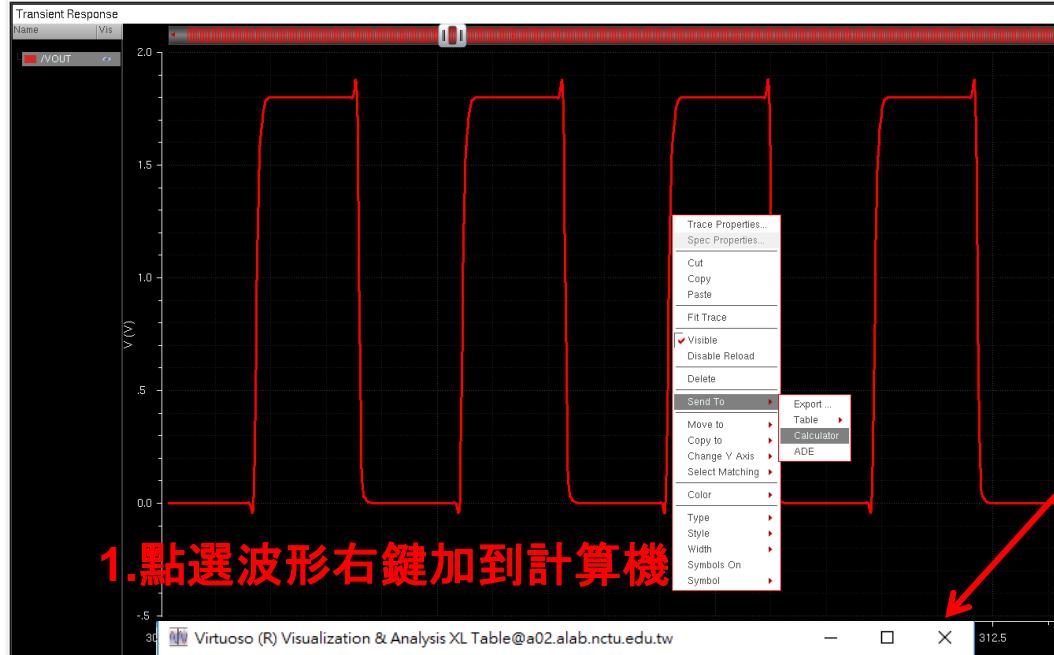
Parameters	
Model Name	n_18_mm
Total Width	8u M
Finger Width	8u M
Length	180.0n M
Finger Number	1

設定Layout所需的Finger Number



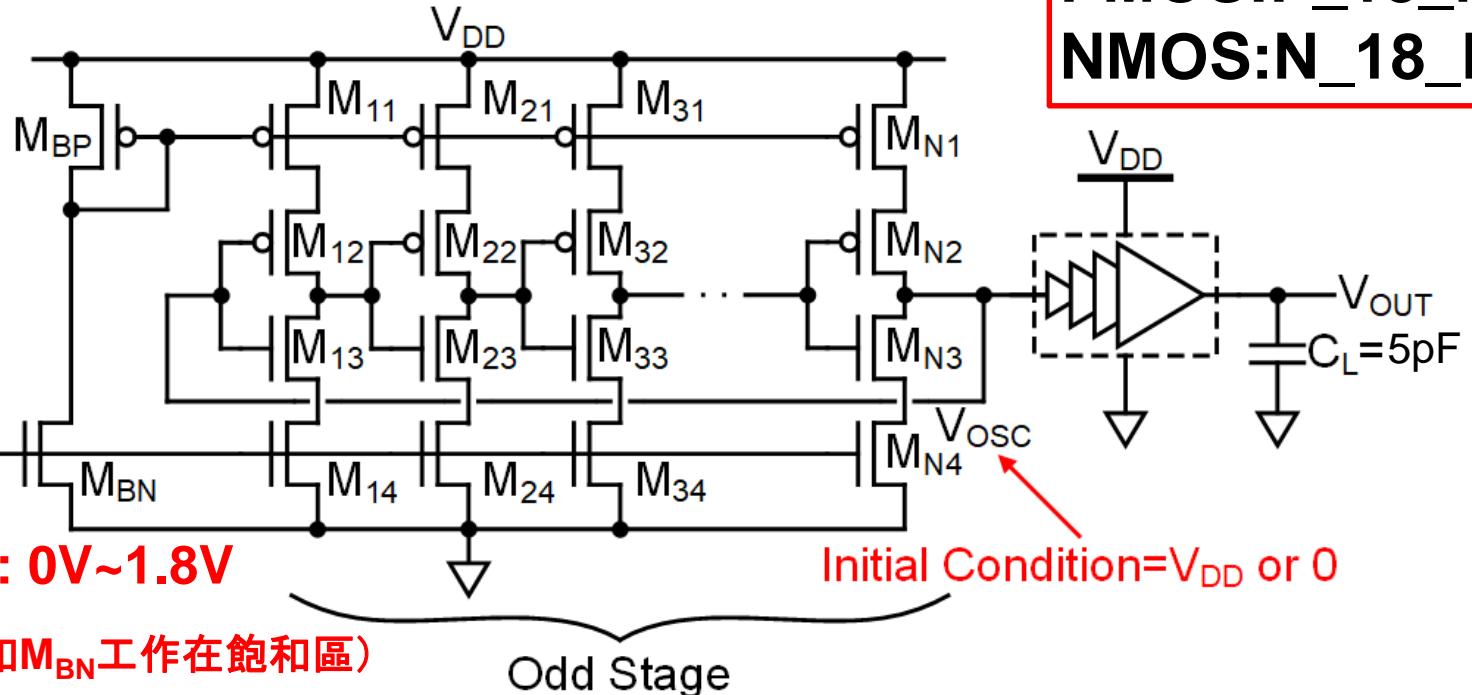
# Lab 1

## ◆ Waveform Measurement:



# Homework 1

## ◆ Voltage Control Oscillator (VCO) :

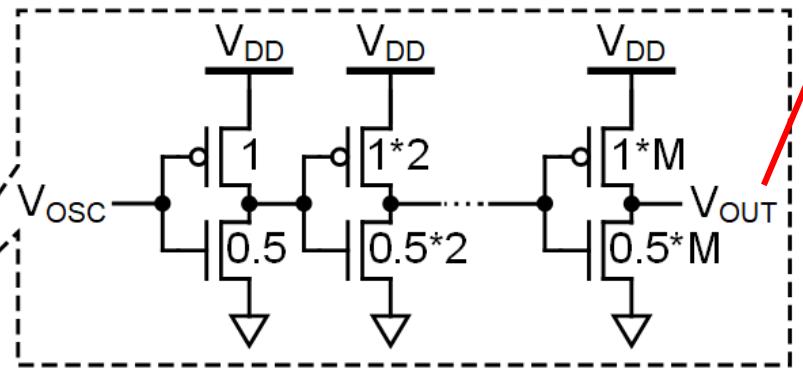
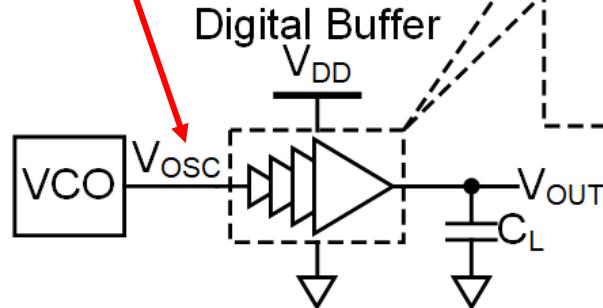
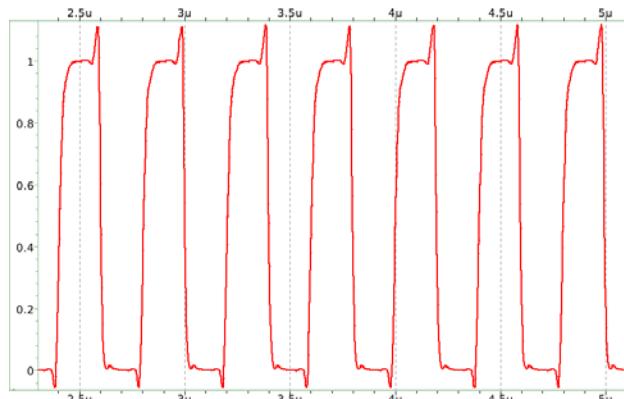


- All bodies of NMOS connected to ground and all PMOS bodies connected to  $V_{DD}$ .
- Initial condition is required to start oscillation of VCO.



# Homework 1

## ◆ Output Buffer:



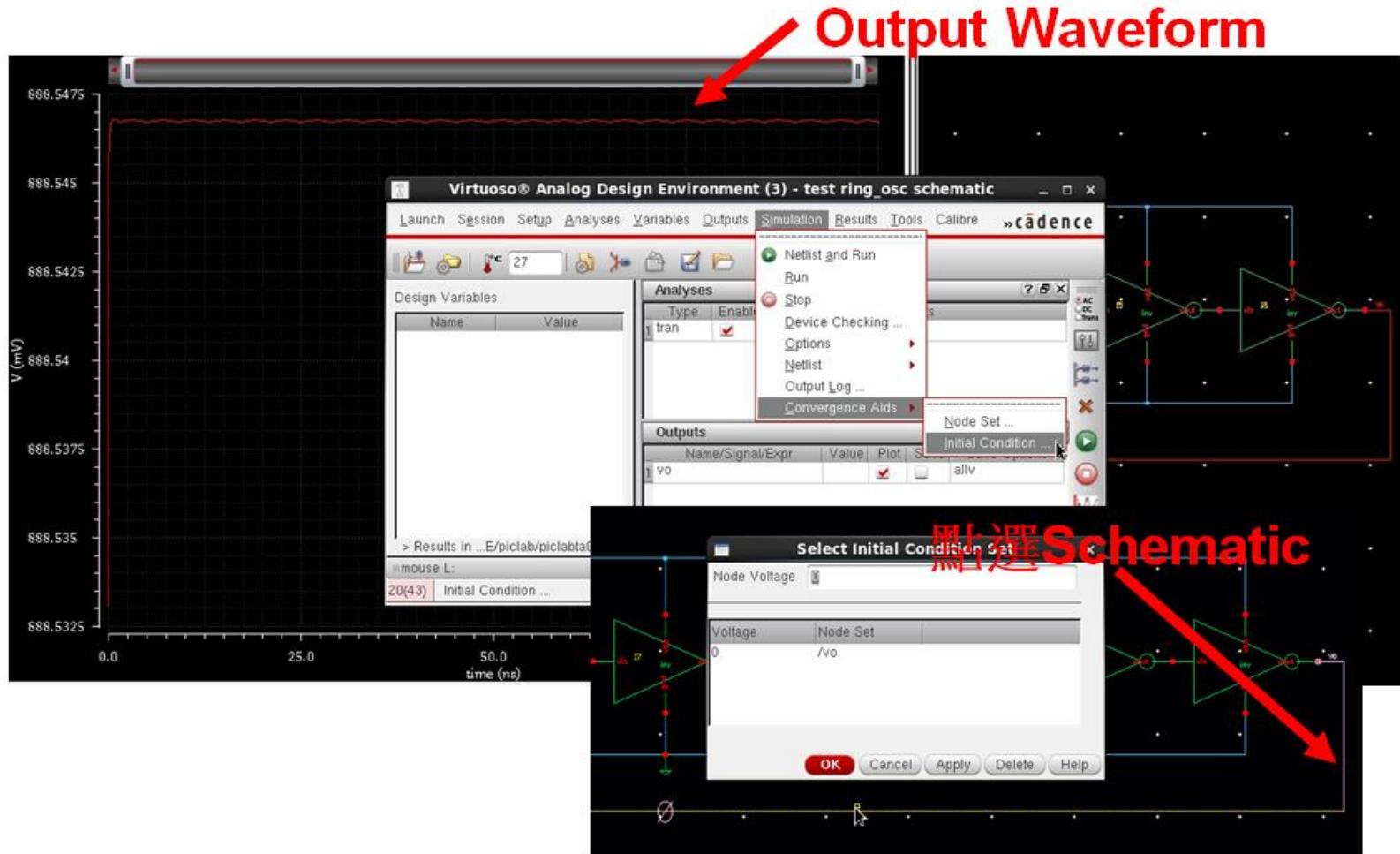
M: Finger Number  
每級以 $1/2/4\dots$ 的倍數增加

➤ Buffer stage is used to avoid long rise time and fall time.



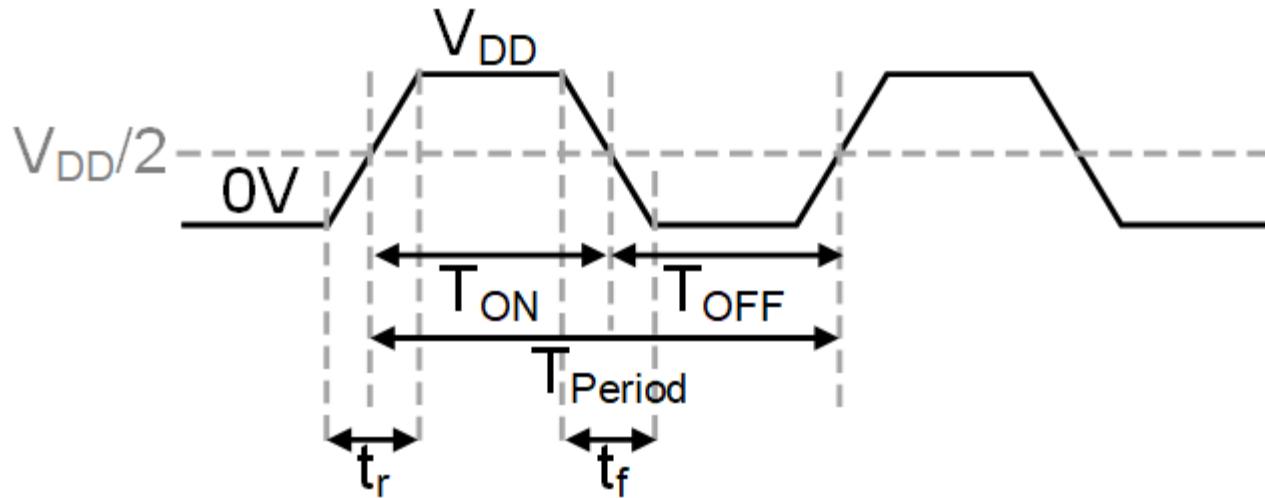
# Homework 1

## ◆ Initial Condition Setting:



# Homework 1

## ◆ Output Waveform:



**Oscillation frequency ( $f_{osc}$ ) =  $1/T_{period}$**

**Duty-cycle =  $T_{ON}/T_{Period}$**

**Rise time ( $t_r$ ) =  $t(10\% * V_{DD}) - t(90\% * V_{DD})$**

**Fall time ( $t_f$ ) =  $t(90\% * V_{DD}) - t(10\% * V_{DD})$**

# Homework 1

## ◆ Specification:

( $f_{min} < 0.5\text{MHz}$ 、 $f_{max} > 2.5\text{MHz}$ )

Parameter	Target	Pre-layout Simulation	Post-layout Simulation	Error Calculation
Supply Voltage ( $V_{DD}$ )	1.8V			
Oscillation Range ( $f_{min} \sim f_{max}$ )	0.5MHz @ $V_{CTRL}$			
	2.5MHz @ $V_{CTRL}$			
Rising Time ( $t_F$ )	<0.5ns @0.5MHz			
	<0.5ns @2.5MHz			
Falling Time ( $t_R$ )	<0.5ns @0.5MHz			
	<0.5ns @2.5MHz			
Duty-cycle	47%<D<53%			
Number of Stage (N)	Any			

- $V_{CTRL}$ : 此頻率下 Pre-layout simulation 所得出的  $V_{CTRL}$
- Error:  $\frac{|f_{POST} - f_{PRE}|}{f_{PRE}} \times 100\%$



# Homework 1

---

- 繳交一份電子檔報告，請在報告中加入Layout圖，DRC，LVS結果及Result Table。
- 作業繳交時間為2023/07/31(一)晚上12點前，請將作業報告繳交至E3平台
- Schematic與Layout的Finger number/multiplier數量需相同
- 僅需在規定的 $V_{CTRL}$ 範圍內有涵蓋0.5MHz~2.5MHz，未規定須 $V_{CTRL}=0V/1.8V$ 對應0.5M/2.5MHz
- Pre-simulation及Post-simulation結果誤差包含Rising/Falling Time及頻率，皆須小於5%內，需考慮負載電容 $C_L=5pF$ 。
- Rising/Falling Time誤差的計算亦同上述公式計算，僅需將 $f_{POST}/f_{PRE}$ 改成 $Rise_{POST}/Rise_{PRE}$ 和 $Fall_{POST}/Fall_{PRE}$ 。



# DRC Error Example

## ◆ 可暫時先忽略的DRC Error List

	Check / Cell	Resu
⊕	✗ Check 4.1M	1
⊕	✗ Check 4.29NOTICE	3
⊕	✗ Check 4.14Z.NO_IND_P01	1
⊕	✗ Check 4.22F.NO_IND_M2	1
⊕	✗ Check 4.22G	1
⊕	✗ Check 4.24F.NO_IND_M3	1
⊕	✗ Check 4.24G	1
⊕	✗ Check 4.26F.NO_IND_M4	1
⊕	✗ Check 4.26G	1
⊕	✗ Check 4.28F.NO_IND_M5	1
⊕	✗ Check 4.28G	1
⊕	✗ Check 4.31E.NO_IND_M6	1
⊕	✗ Check 4.31F	1
⊕	✗ Check 4.24C	3
⊕	✗ Check 4.26C	3
⊕	✗ Check 4.28C	3
✓	Check DENSITY_PRINT_FILES	0

Note:

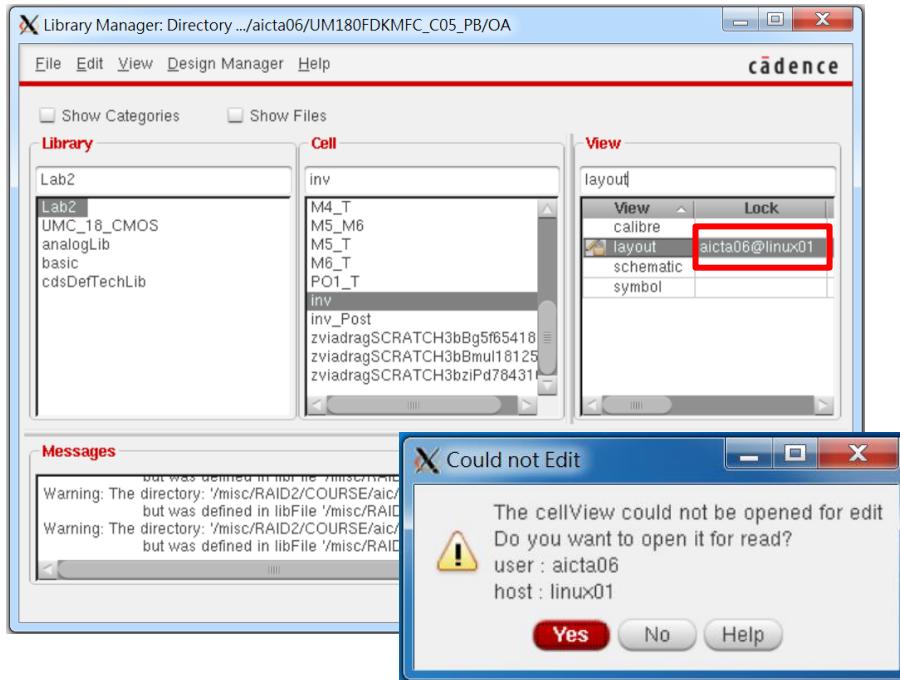
- 跑DRC時只要是跟Metal或Poly的density相關錯誤都可以先忽略



# Appendix 1

## ◆ Could not Edit

➤ 因為license不穩或不正常關閉軟體造成無法編輯檔案



刪除的.cdslock

在Cell資料夾內

檔案名稱	檔案大小	檔案類...
..	38	TAG ...
master.tag	1,462	PNG ...
thumbnail_128x128.png	48,324	OA 檔案
layout.oa	684	CDSL...
<b>layout.oa.cdslock</b>	684	17639 ...
layout.oa.cdslock.RHEL30.linux01.17639		

1. 把帶有.cdslock的lock檔案刪除，刪除後重啟virtuoso

2. 使用terminal刪除全部.cdslock

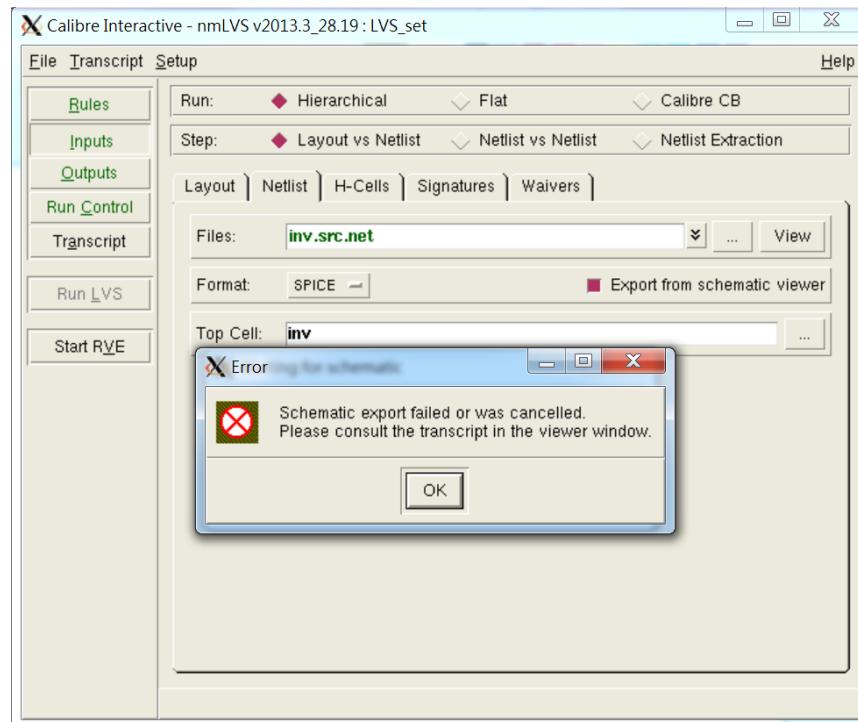
```
[@a02 ~]$ clsAdminTool  
> are .  
BEGIN: Release Edit Locks.  
[./UM180FDKMFC_C05_PB/0A/Lab4/Comparator/schematic/  
./UM180FDKMFC_C05_PB/0A/Lab4/Comparator_Pre/schematic  
./CDS.log a02.alab.nctu.edu.tw u0710769 11521 1689  
END: Release Edit Locks.  
SUMMARY: A total of 3 Edit Locks were released in t  
> quit
```



# Appendix 2

## ◆ Could not Run LVS

- 在terminal介面輸入 setenv CDS\_Netlisting\_Mode Analog，每次LVS都要輸入
- 也可在主目錄下建立.cshrc檔，寫入上列command，就不用每次輸入



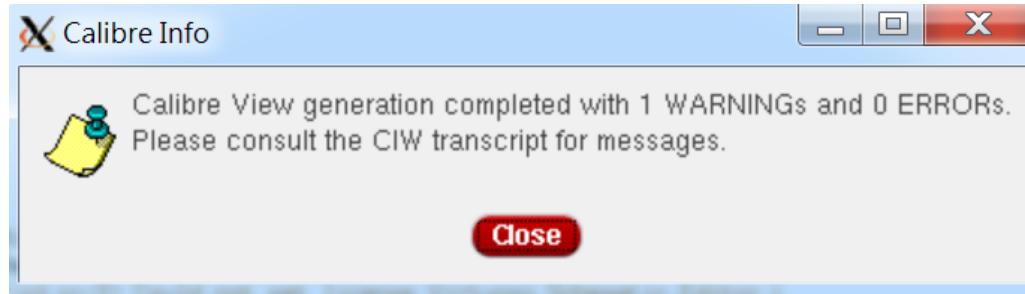
Terminal介面建立並進入.cshrc檔  
linux01 [aic/aicta06]% vim .cshrc  
.cshrc檔內輸入指令並存檔  
**setenv CDS\_Netlisting\_Mode Analog**

請注意有空格，別連著輸入!



# Appendix 3

## ◆ Get at least 1 warning after running PEX...



CIW視窗內會顯示運行訊息

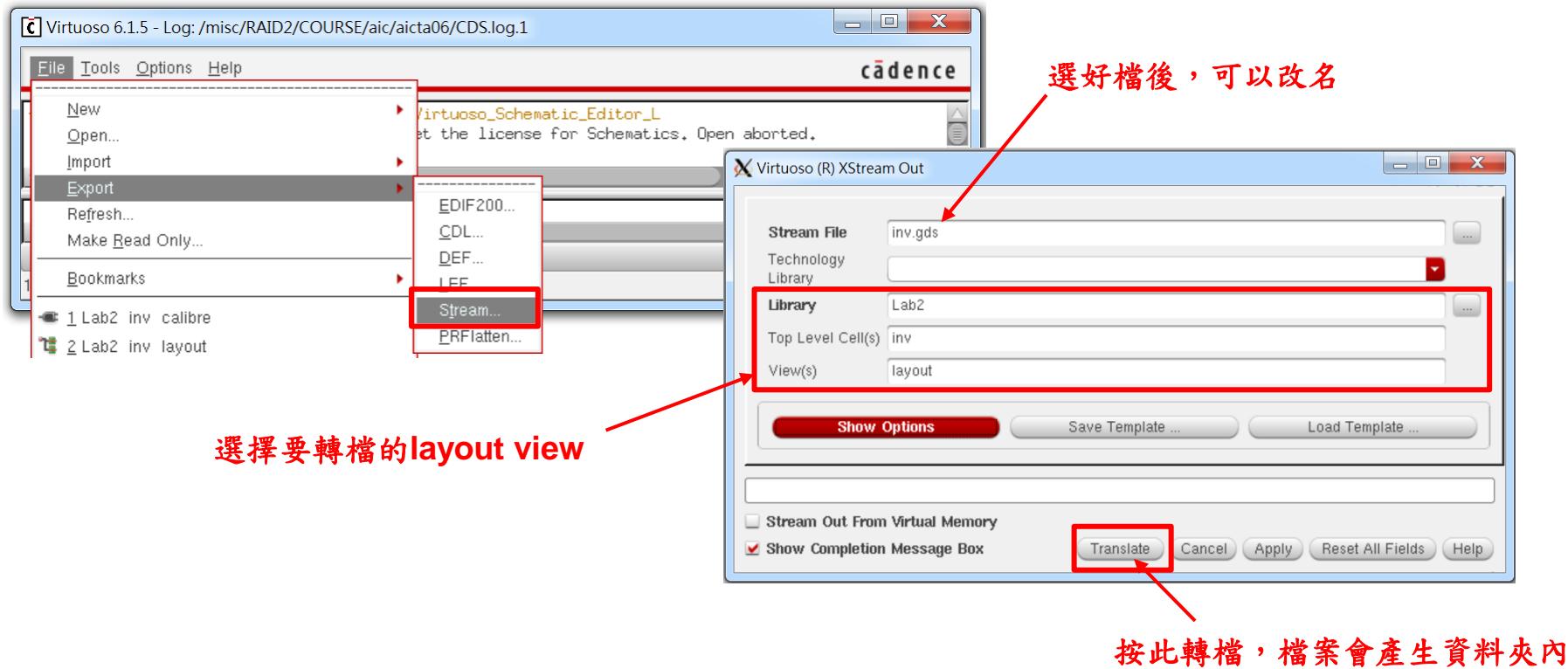
```
NOTE: Creating CalibreView for cell inv ...
Loading schematic.cxt.
*WARNING* (icLic-3) Could not get license Virtuoso Schematic Editor_L
*INFO* (icLic-25) License Virtuoso_Schematic_Editor_XL ("95115") was used to run Schematics L.
INFO (SCH-1170): Extracting "inv.calibre"
Loading lx.cxt
Loading lce.cxt
Calibre View generation completed with 1 WARNINGS and 0 ERRORS.
Please consult the CIW transcript for messages.
```

如果是License的問題，可以先不用理會



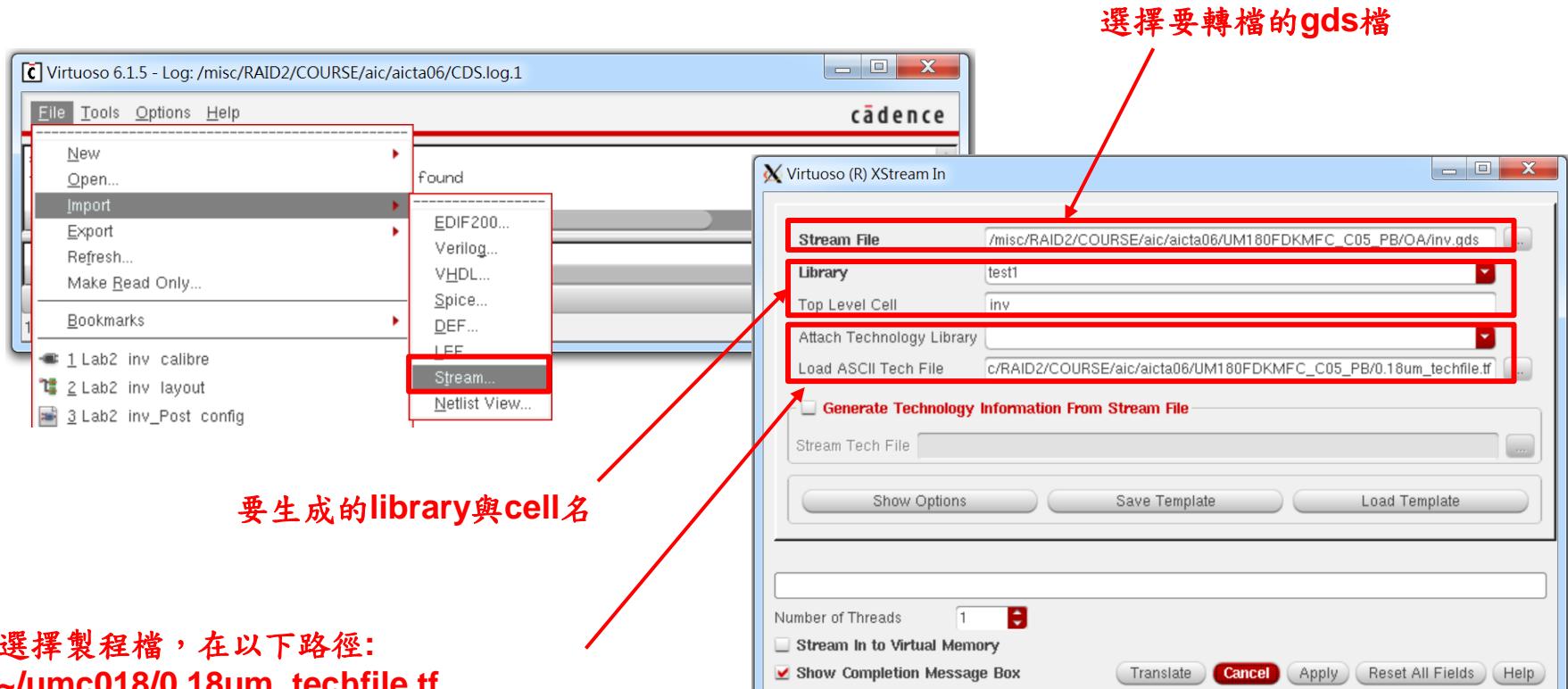
# Appendix 4

- ◆ 將layout輸出成gds檔
- ◆ File → Export → Stream out



# Appendix 5

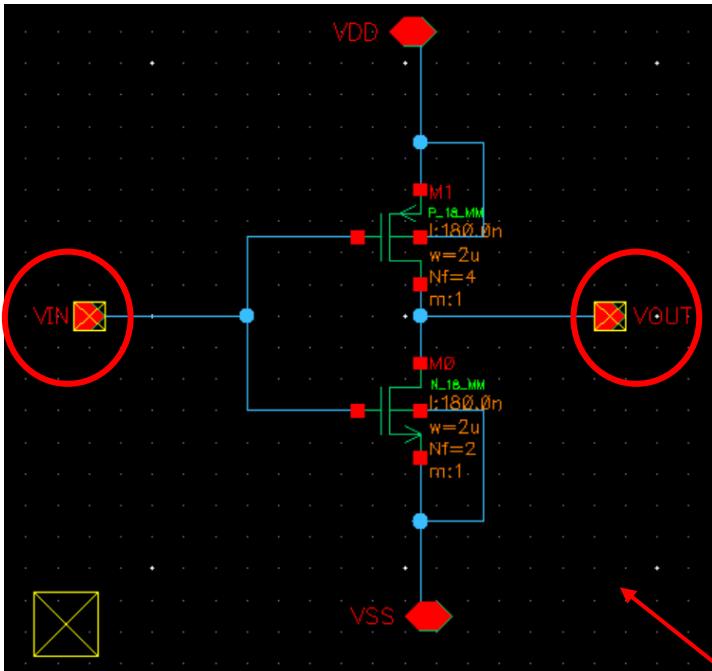
- ◆ 將gds檔輸入成layout view
- ◆ File → import → Stream in



# Appendix 6

## ◆ An error example you may face:

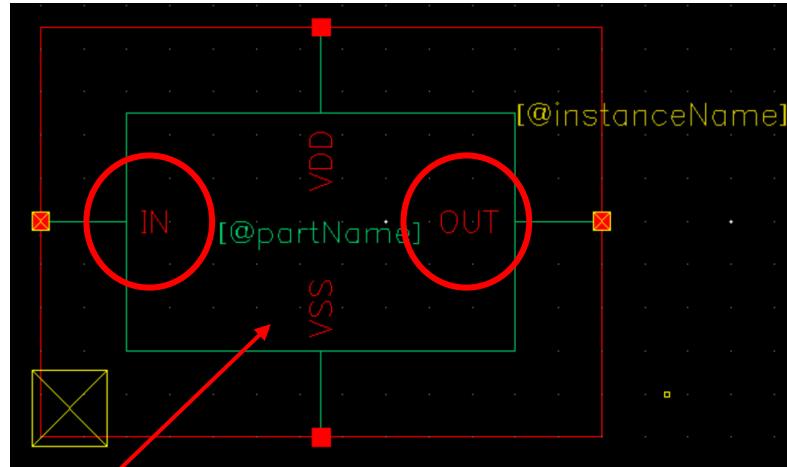
當電路圖跑出warning且出現左下矩形...



Warning訊息可以在CIW視窗確認

```
INFO (SCH-1170): Extracting "inv schematic"
Warning: Terminal "VIN" in view schematic not found in "inv symbol".
Warning: Terminal "VOUT" in view schematic not found in "inv symbol".
Warning: Terminal "IN" in view symbol not found in "inv schematic".
Warning: Terminal "OUT" in view symbol not found in "inv schematic".
INFO (SCH-1172): There were 0 errors and 4 warnings found in "Lab2 inv schematic".
INFO (SCH-1181): "Lab2 inv schematic" saved.
```

可以發現此錯誤跟symbol命名有關



Schematic的節點要與symbol的一致，請重新命名

