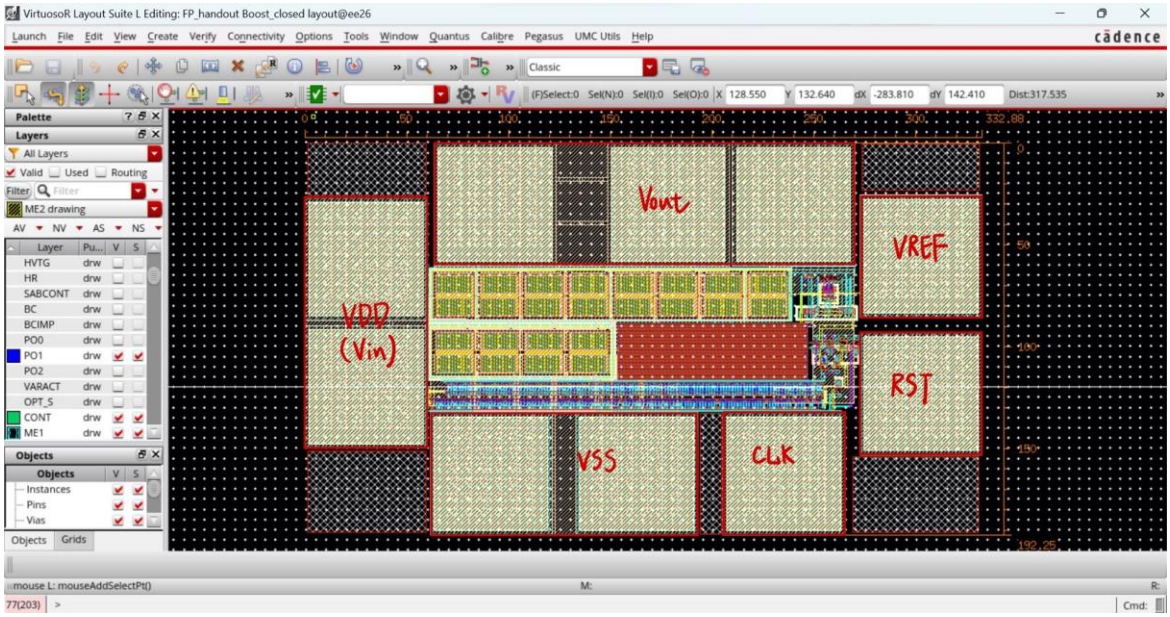
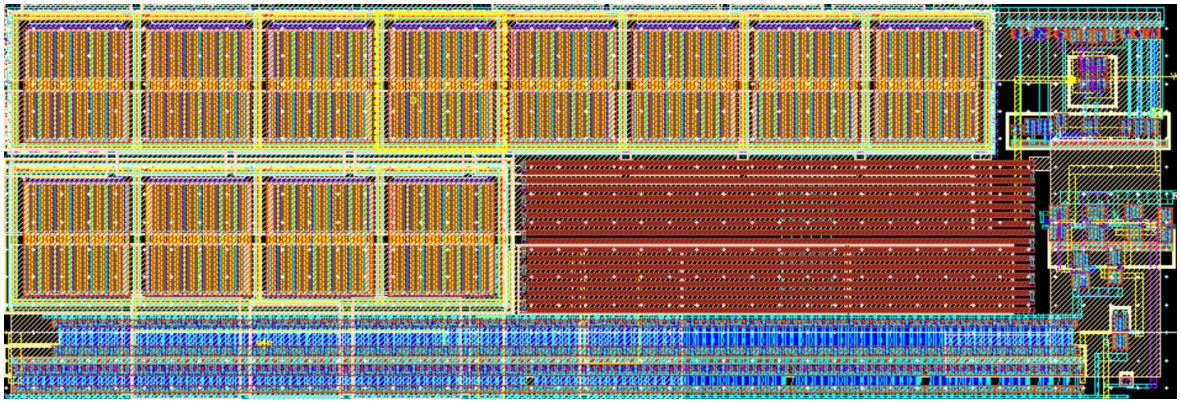
PMIC　FINAL_PROJECT _report

110511277 蔡東宏

1. Layout

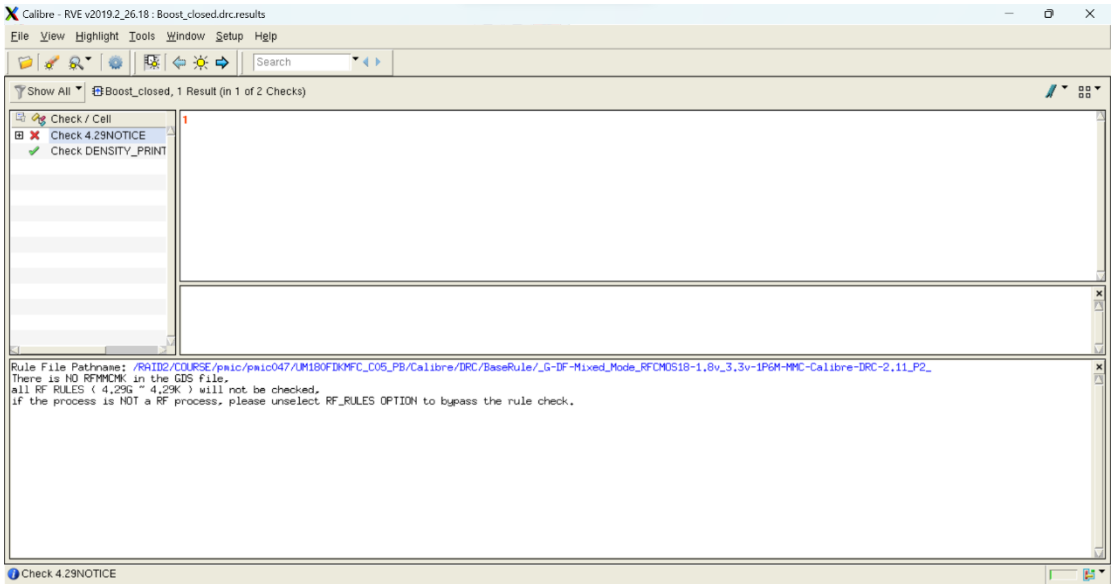


(放大)

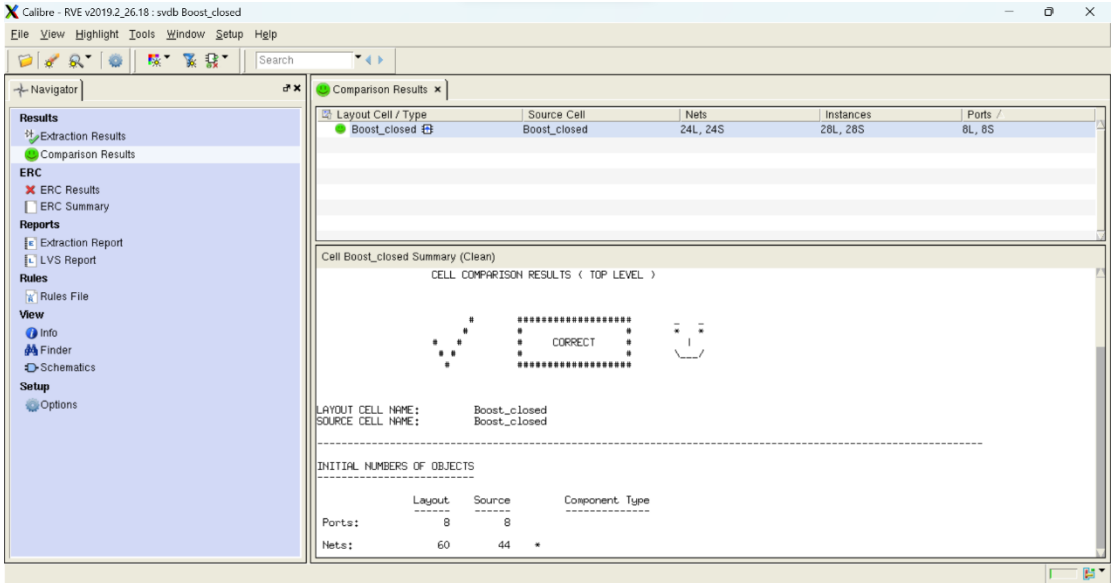


一顆 Power mos 的 w 是 20um，finger 是 25 根，而我的 pmos 放了 8 顆，nmos 放了 4 顆，所以我 power pmos 的 total width 是 4mm，而 power nmos 的 total width 是 2mm。

2. DRC


Calibre - RVE v2019.2_26.18 : Boost_closed.drc.results
File View Highlight Tools Window Setup Help
Search
Show All
Boost_closed, 1 Result (in 1 of 2 Checks)
Check / Cell
Check 4.29NOTICE
Check DENSITY_PRINT
1
Rule File Pathname: /RAID2/COURSE/pmic/pmic047/UM180FDKMFC_C05_PB/Calibre/DRC/BaseRule/_G-DF-Mixed_Mode_RFCMOS18-1.8v_3.3v-1P6M-MMC-Calibre-DRC-2.11_P2_
There is NO RFMMCMK in the GDS file.
all RF RULES (4.29G ~ 4.29K) will not be checked.
if the process is NOT a RF process, please unselect RF_RULES OPTION to bypass the rule check.
Check 4.29NOTICE

3. LVS


Calibre - RVE v2019.2_26.18 : svdb Boost_closed
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
Boost_closed
Boost_closed
24L, 24S
28L, 28S
8L, 8S
Cell Boost_closed Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Boost_closed
SOURCE CELL NAME: Boost_closed
INITIAL NUMBERS OF OBJECTS
Layout
Source
Component Type
Ports: 8 8
Nets: 60 44 *

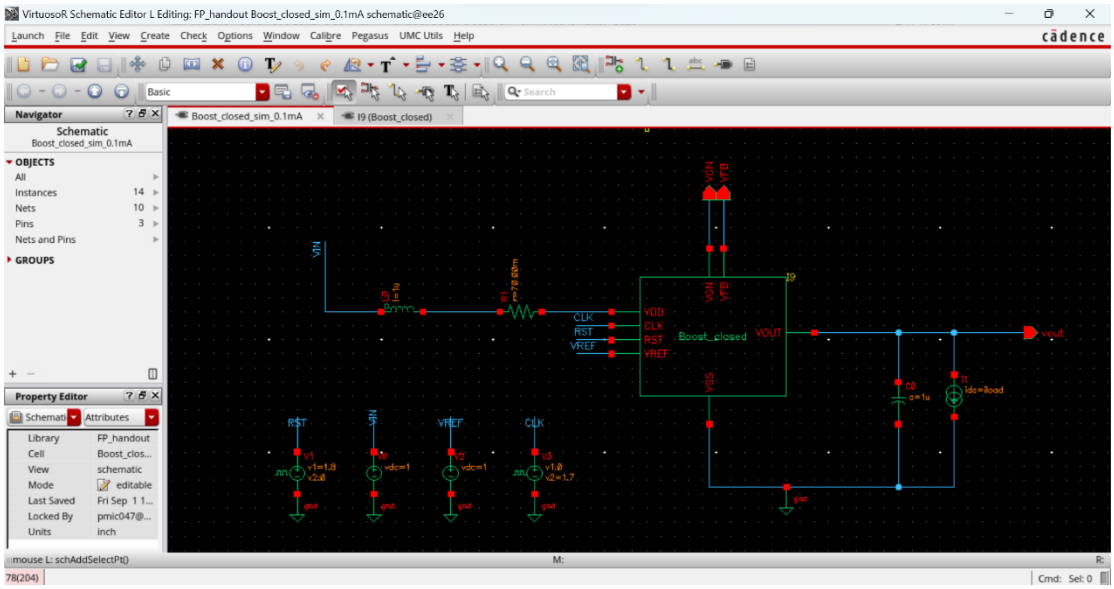
4. Result table

我將 power pmos 的 w 從 12mm 改成 4mm，power nmos 的 w 從 6mm 改成 2mm，所以我的 pre-sim 效率跟上機的時候不一樣。

◆ Final Project

Design Specification		
Input Voltage (V_{IN})	1.0V	
Switching Frequency (F_{SW})	1 MHz	
Output Voltage (V_{OUT})	1.8V	
Output Loading (I_L)	0.1mA/1mA/5mA	
Efficiency (η) @0.1mA	Pre-layout Simulation	Post-layout Simulation
	54.23%	51.98% Δη < 2.5% Δη = 2.25%
Efficiency (η) @1mA	Pre-layout Simulation	Post-layout Simulation
	69.28%	67.37% Δη < 2.5% Δη = 1.91%
Efficiency (η) @5mA	Pre-layout Simulation	Post-layout Simulation
	71.01%	69.21% Δη < 2.5% Δη = 1.8%
Chip Area(um*um)	332.88 × 192.25 = 63996.18	
FOM (%/um²)	0.00294643 (請填寫Post-layout Simulation結果)	

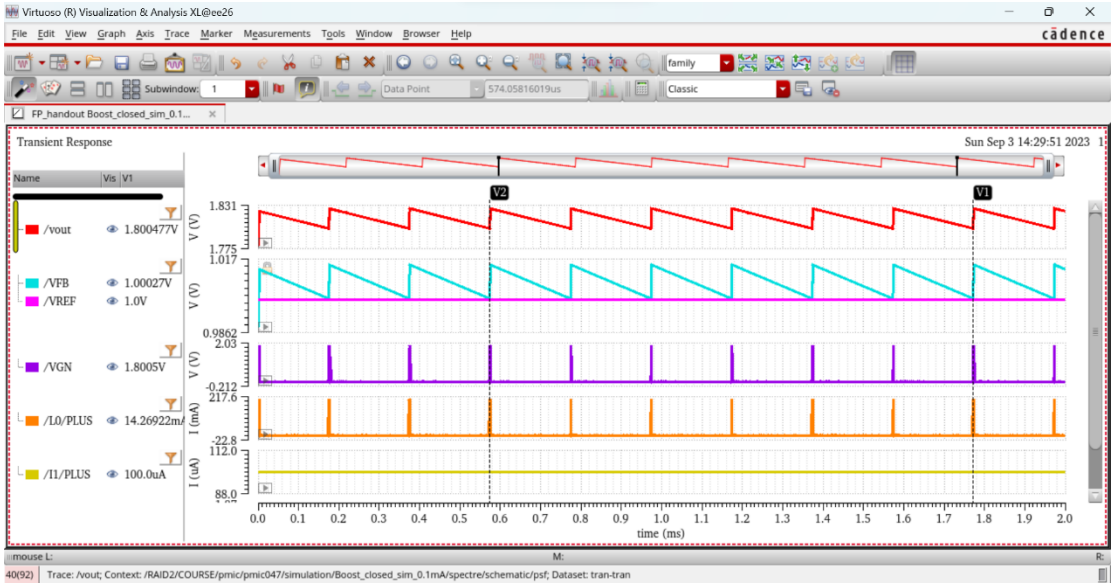
Testbench:



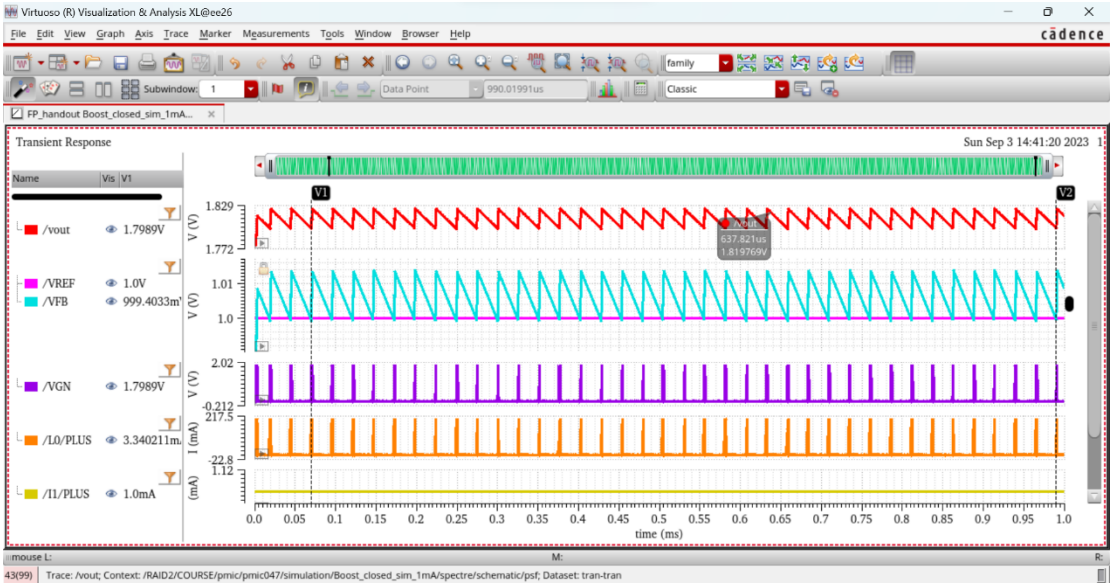
5. 波型

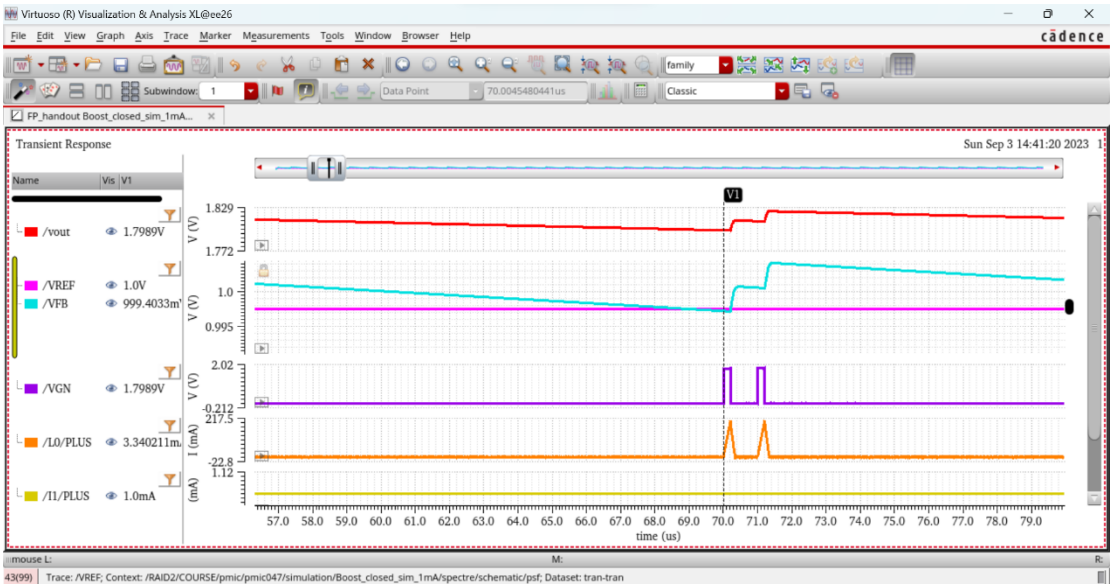
Pre-layout simulation:

0.1mA: Efficiency=54.23%

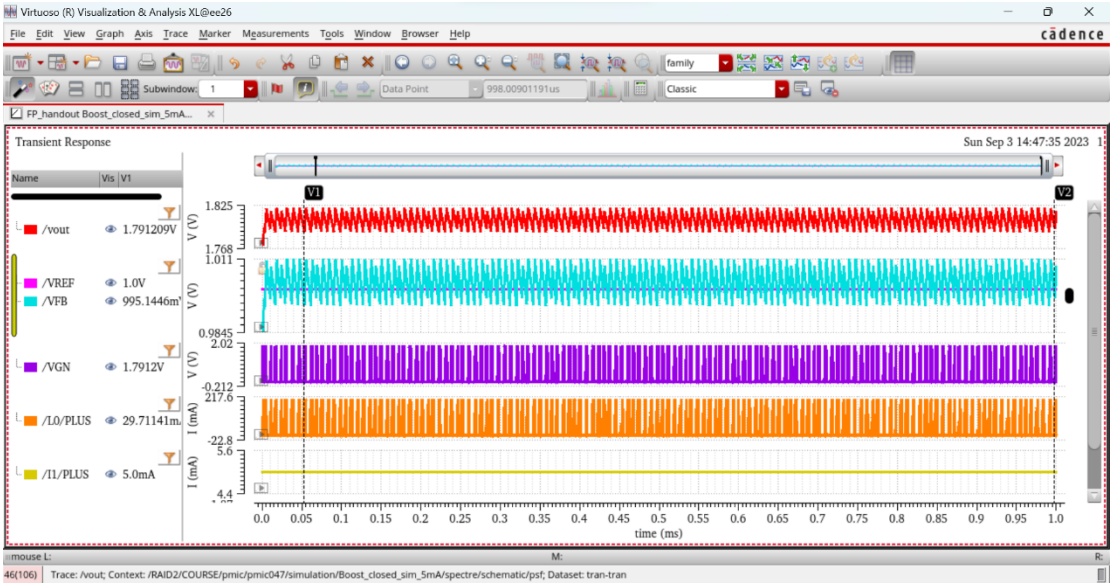


1mA: Efficiency=69.28%



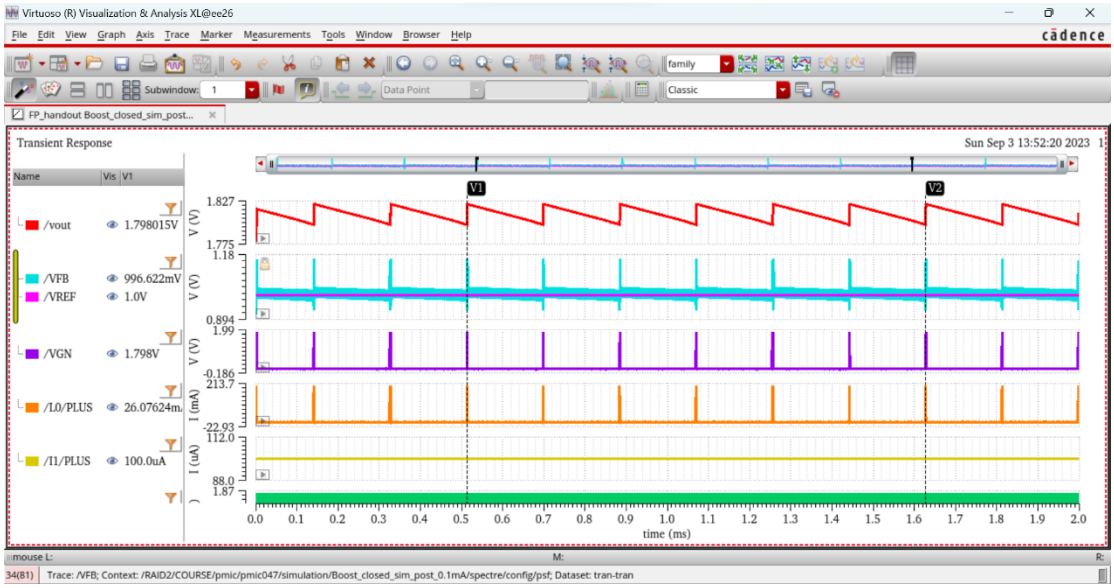


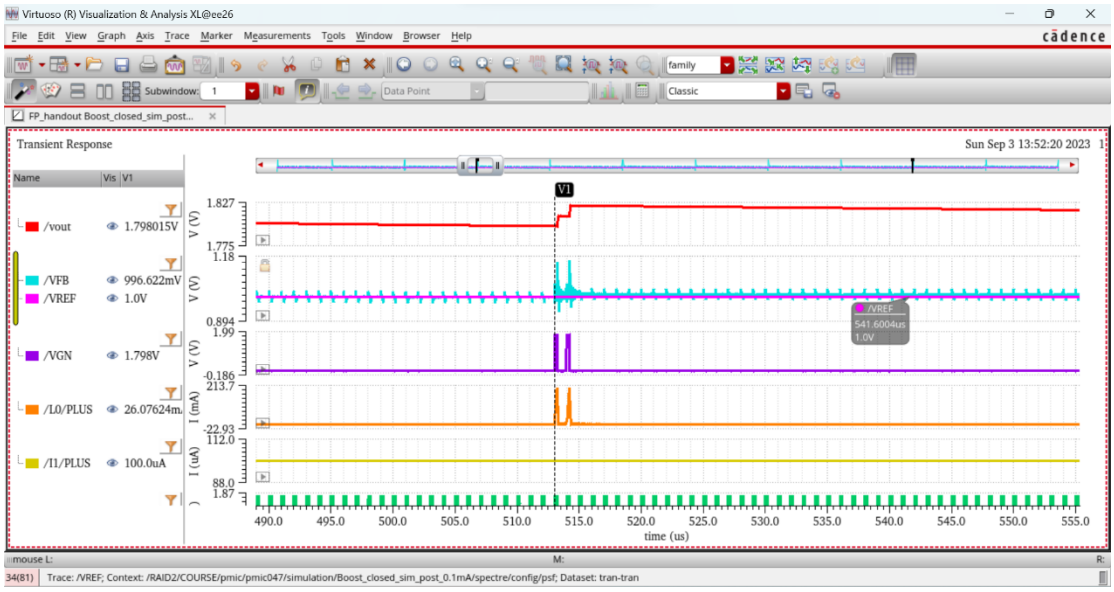
5mA: Efficiency=71.01%



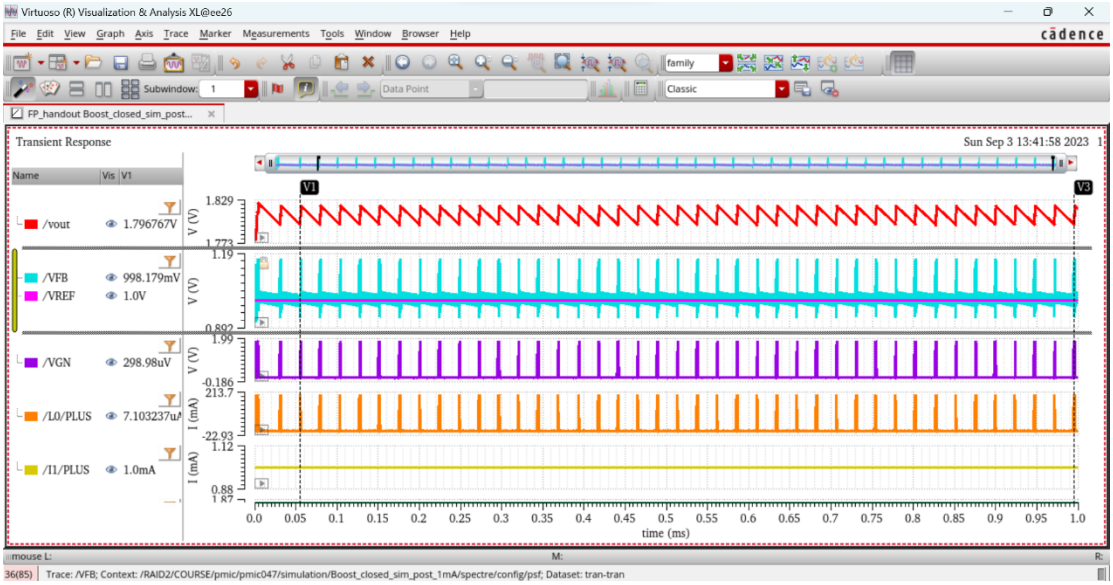
Post-layout simulation:

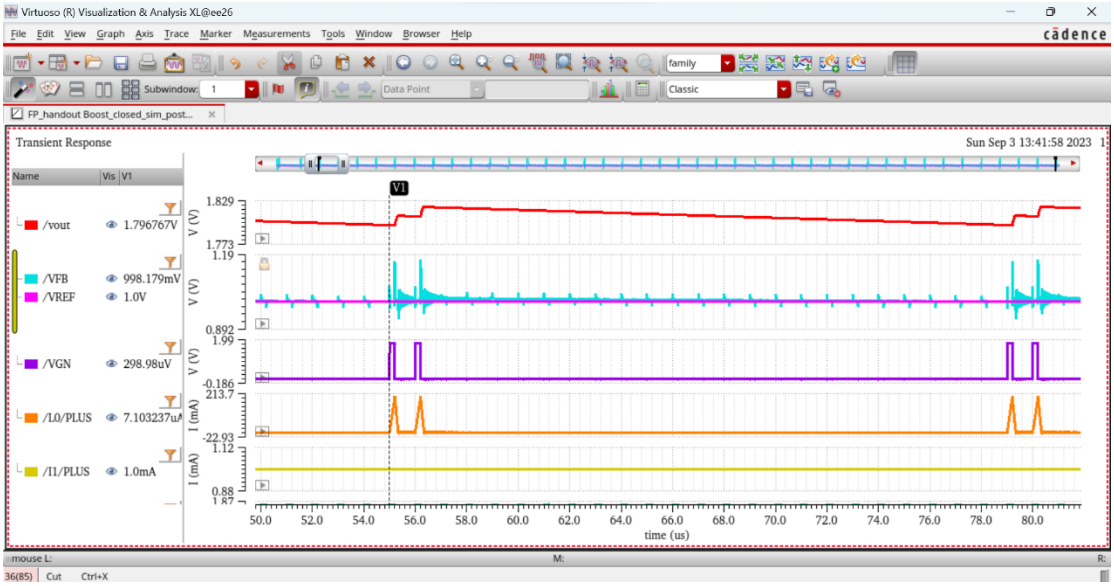
0.1mA: Efficiency=51.98%



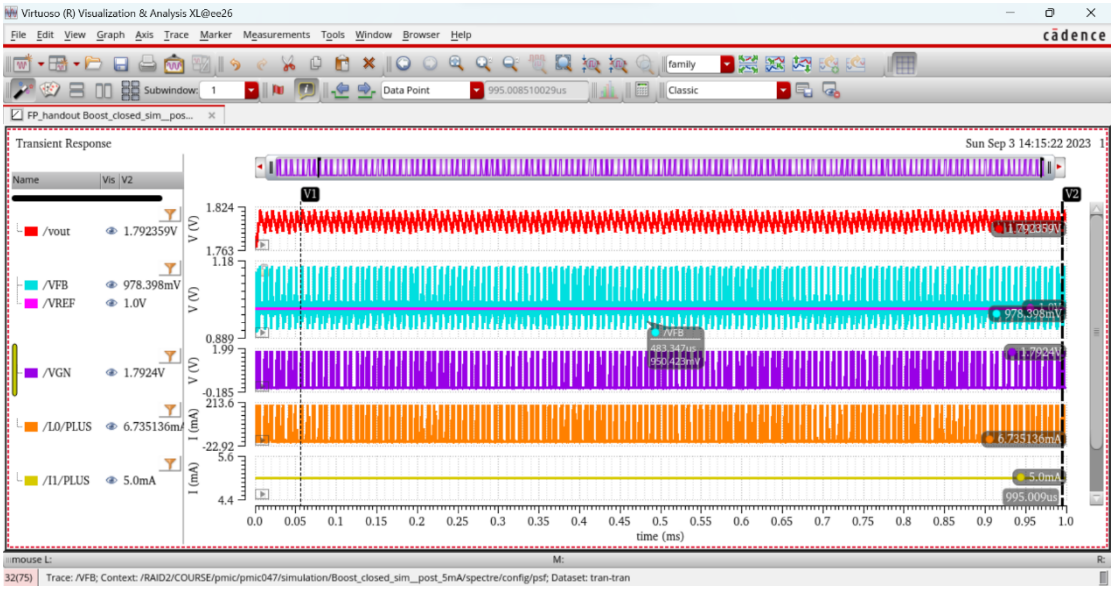


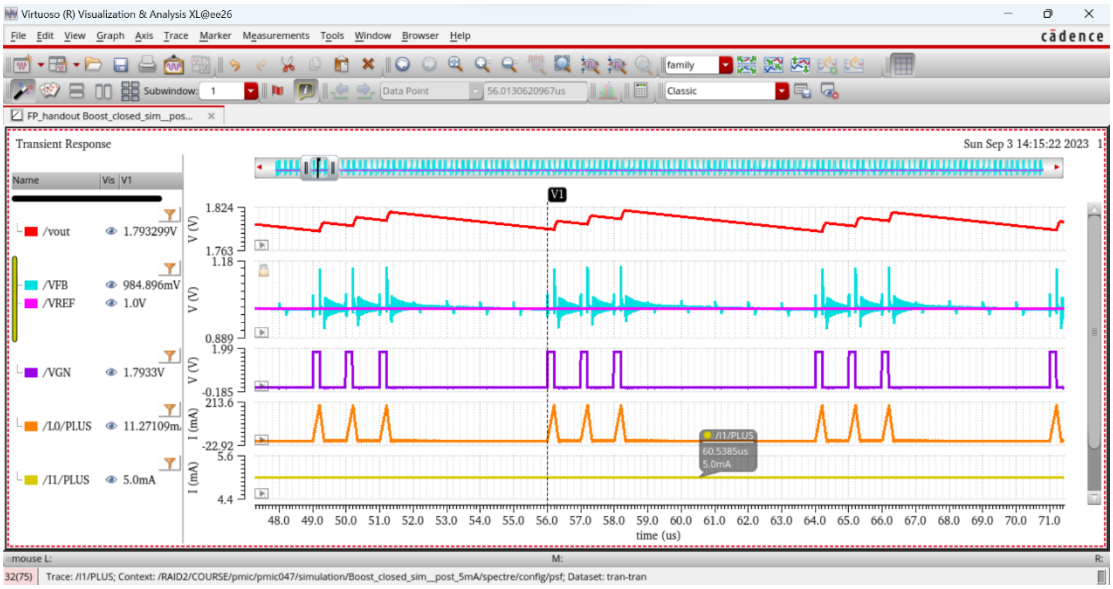
1mA: Efficiency=67.37%



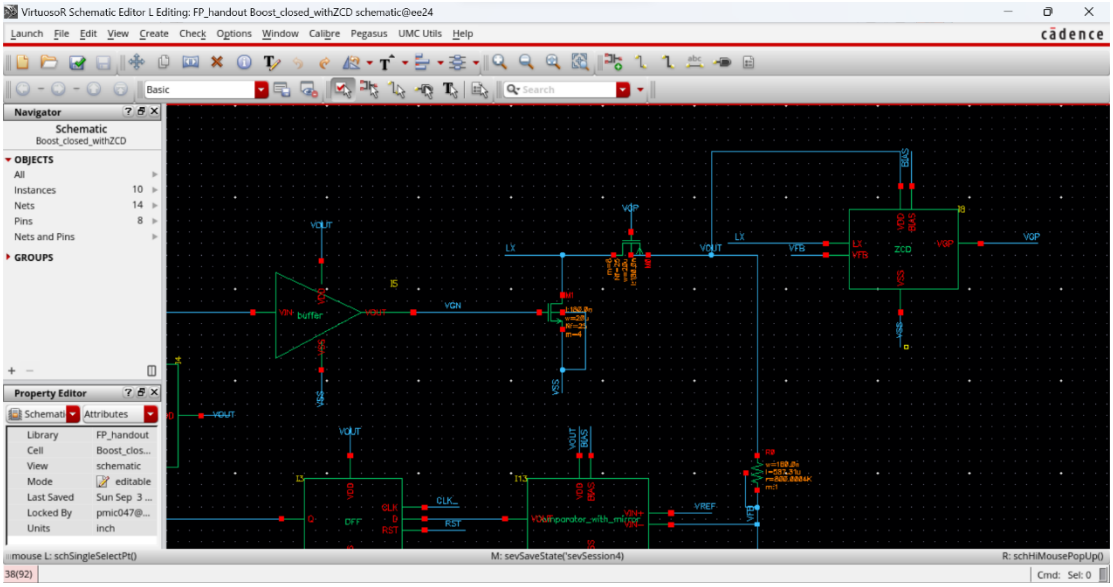


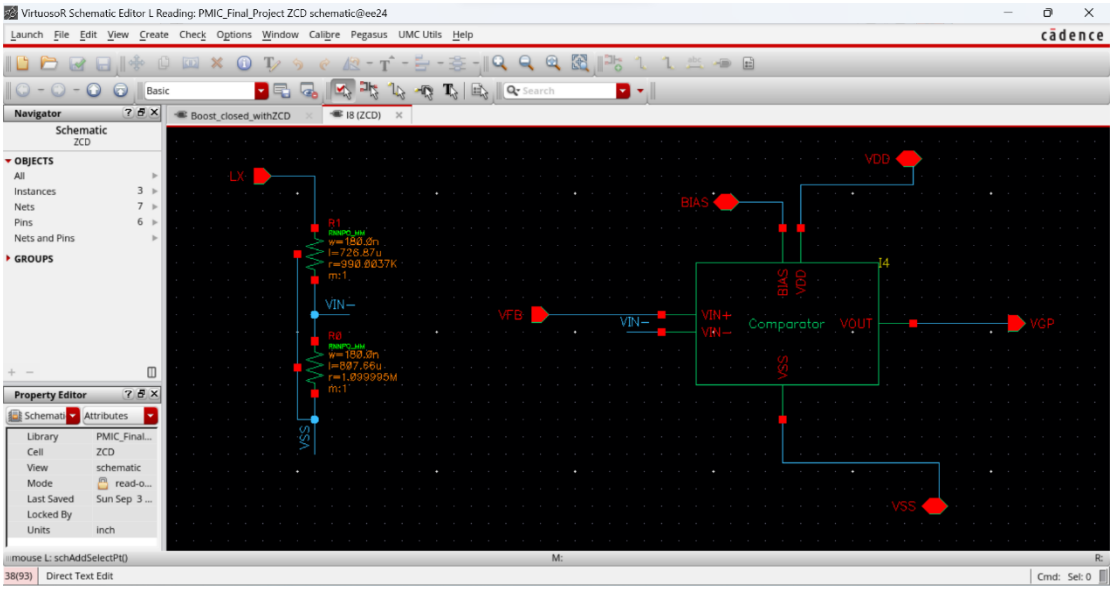
5mA: Efficiency=69.21%





7. Bonus(ZCD):





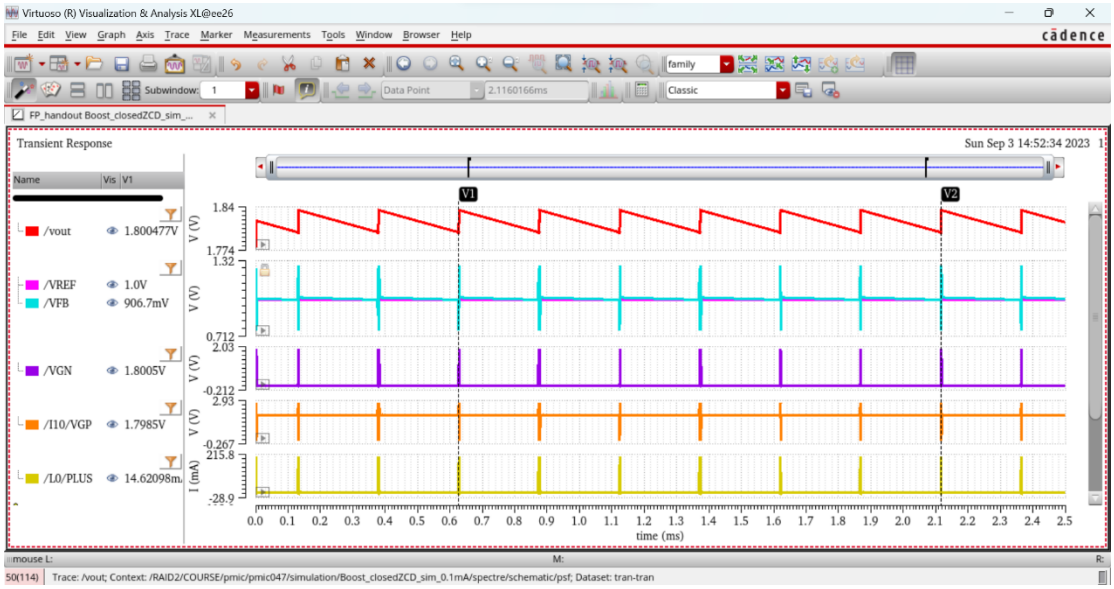
設計想法: ZCD 是為了避免電感電流出現負的情況以導致效率降低，當電感電流小於 0 時，電流流經 pmos 的方向會從 VOUT 流向 LX，此時 VOUT 會大於 LX，此時需把 pmos 關掉。為了增加效率，我在 VOUT 快要大於 LX 時，提早讓 pmos 關掉(給 VGP 高電位即可關掉 pmos)。因為 VFB 是 VOUT 的分壓(大約為 0.556 倍)，所以我將 LX 進行分壓，需分壓小於 0.556 倍，並將他跟 VFB 比較，若大於 VFB，則 VGP 給高電位讓 pmos 關掉，並且調整 LX 點的分壓可以改變 pmos 關閉的時間。而為了讓清載的效率也能提升，需盡可能的讓 ZCD 的邏輯電路越簡單越好以減少消耗，所以我將 ZCD 中 comp 的 current mirror 與迴路中 comp 的 current mirror 共用，以減少 power loss。

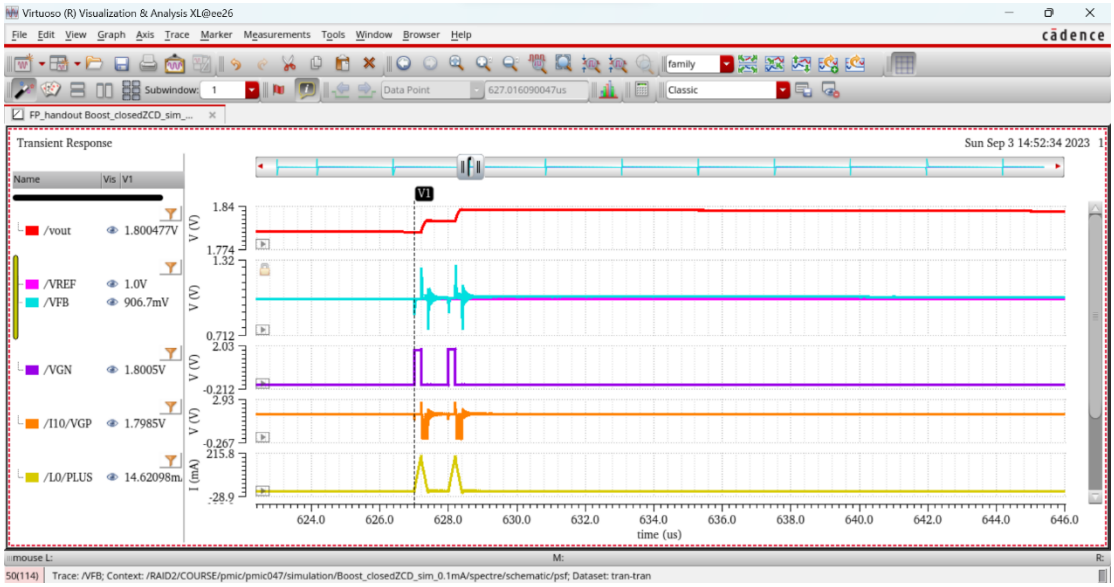
Result:

	without ZCD	with ZCD	相差
Efficiency(0.1mA)	54.23%	60.86%	6.63%
Efficiency(1mA)	69.28%	80.25%	10.97%
Efficiency(5mA)	71.01%	82.72%	11.71%

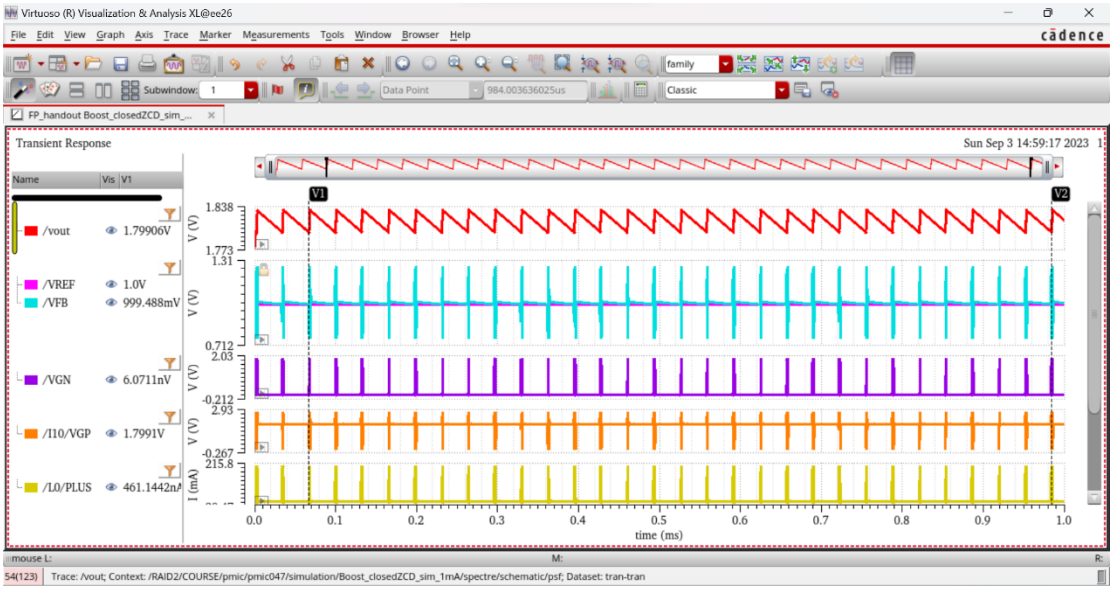
波型(ZCD):

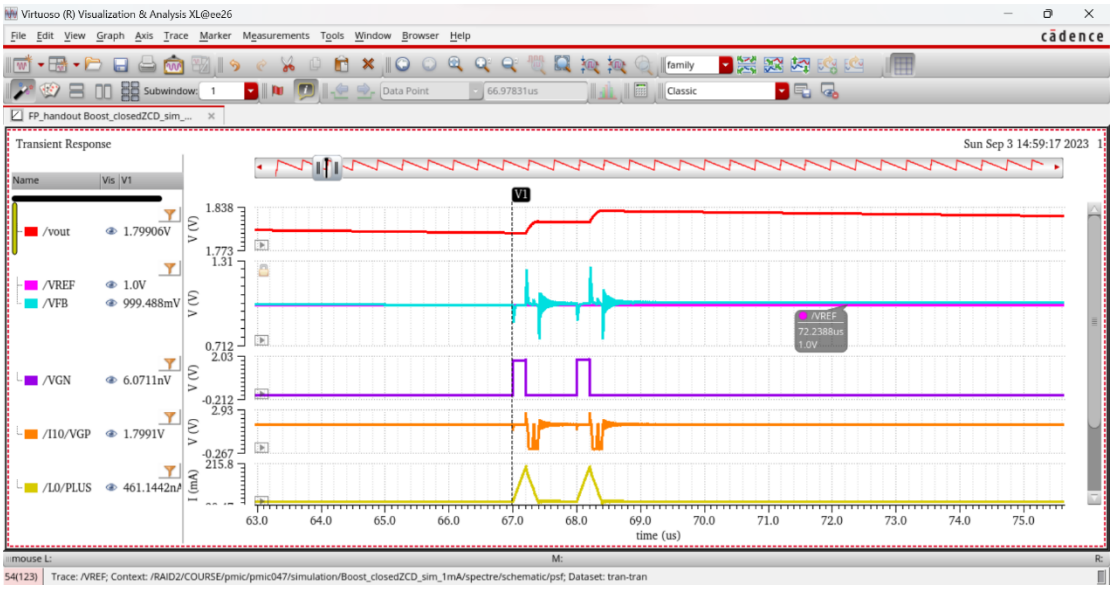
0.1mA: Efficiency=60.86%





1mA: Efficiency=80.25%





5mA: Efficiency=82.72%