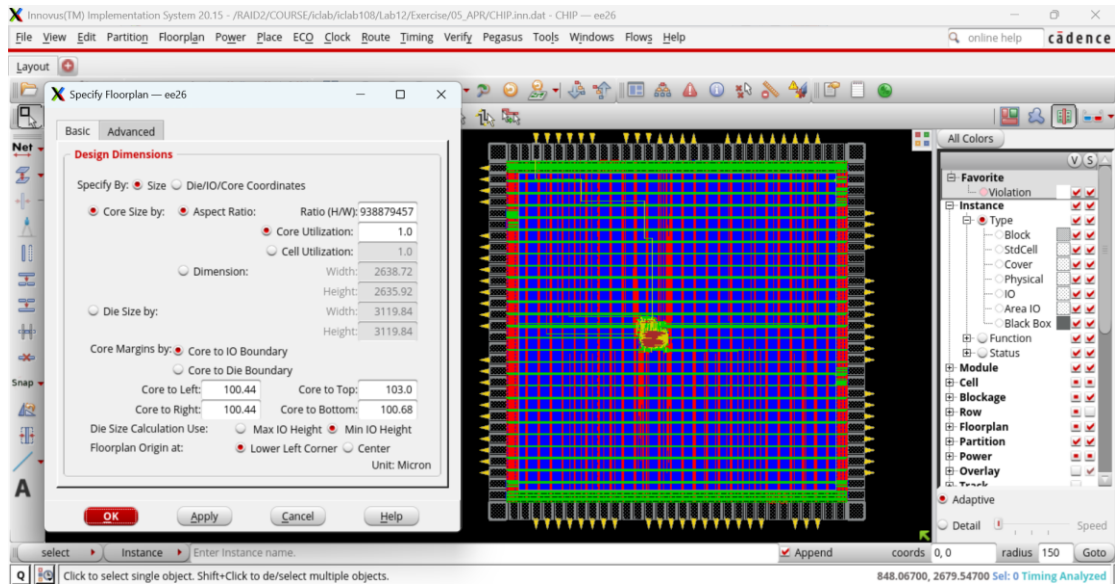


# ICLAB Lab12 Report

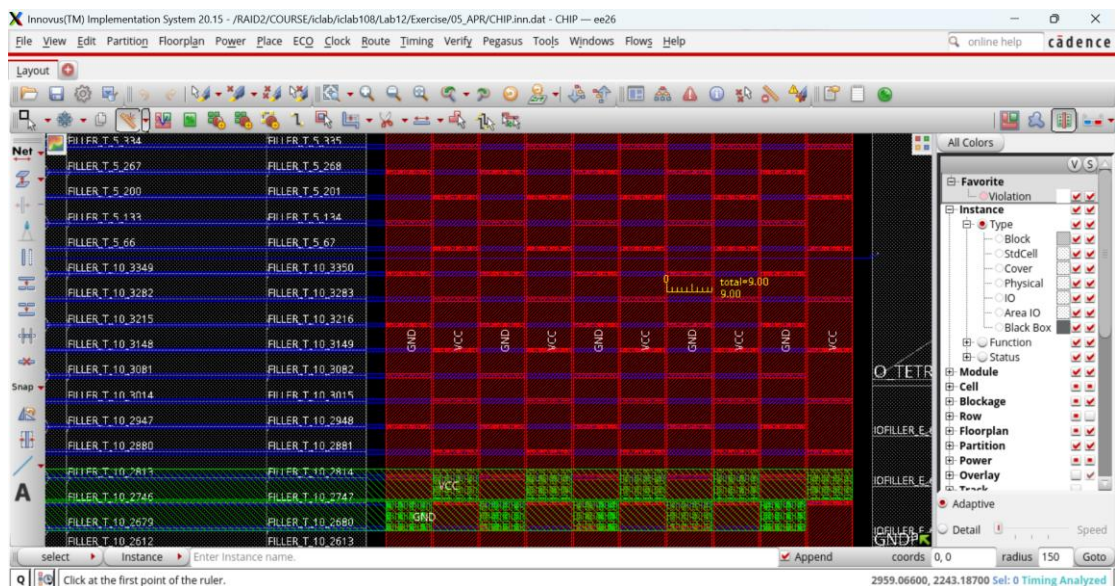
帳號 : iclab108

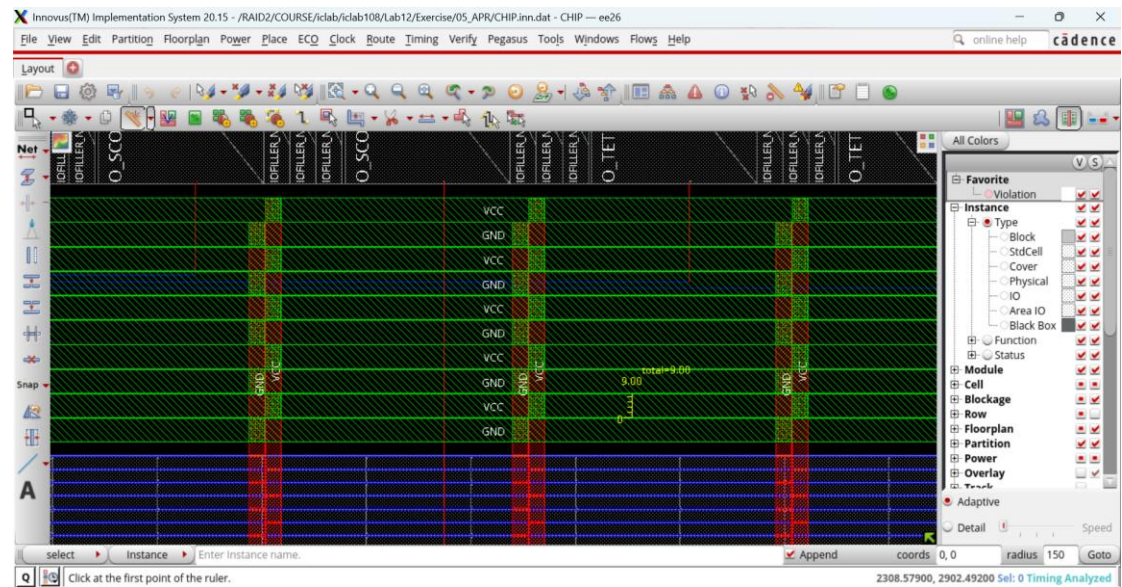
110511277 蔡東宏

## 1. Core to IO boundary:

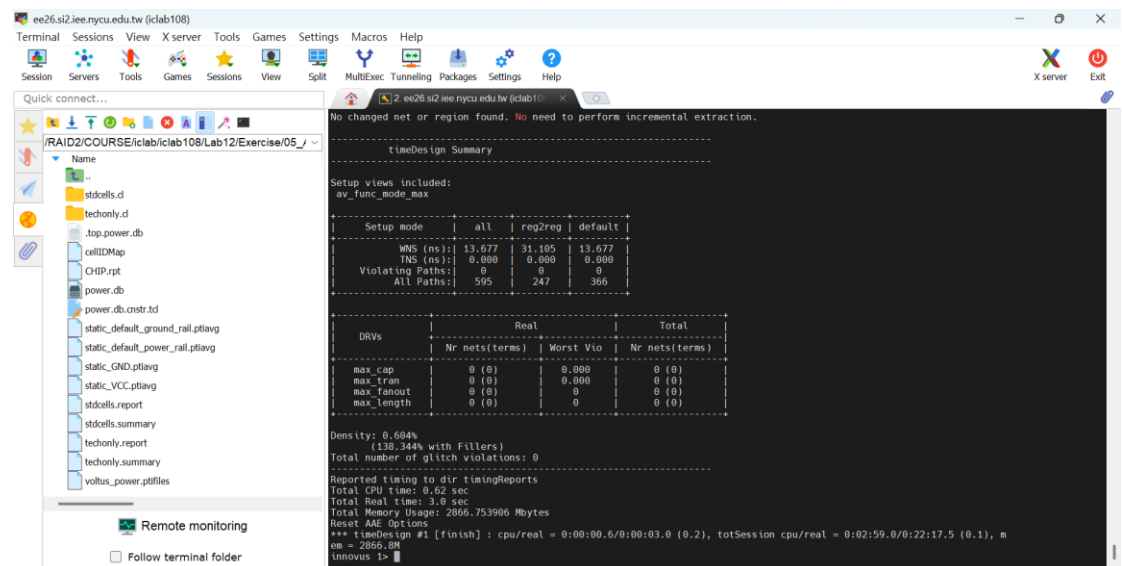


## 2. Core Ring:

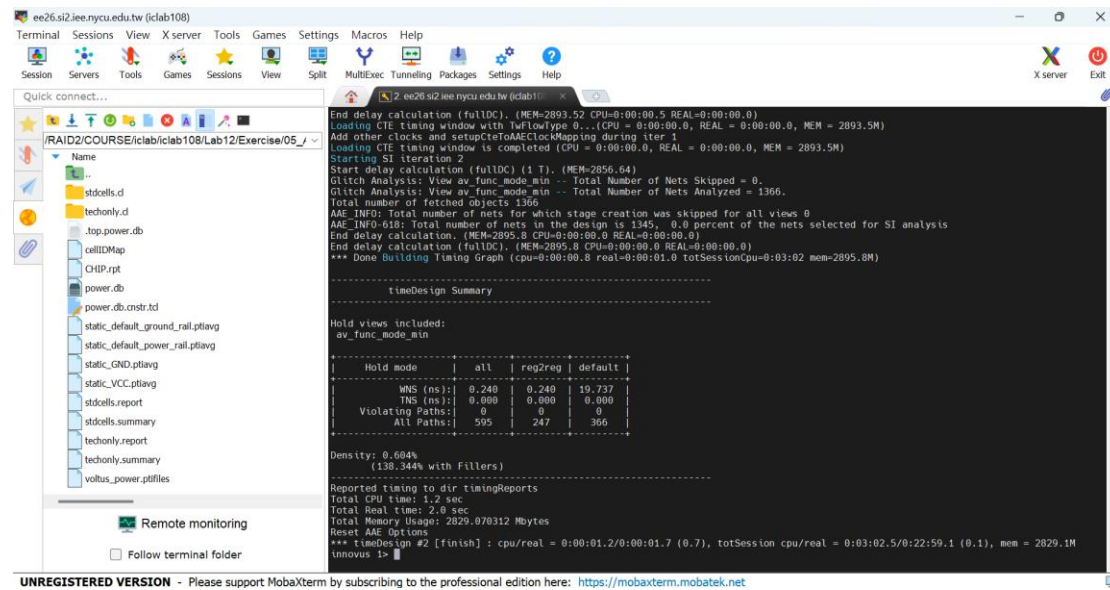




### 3. Post-Route setup time analysis:



#### 4. Post-Route hold time analysis:



```
End delay calculation (fullDC). (MEM=2893.52 CPU=0:00:00.5 REAL=0:00:00.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2893.5M)
Add other clocks and setupCteToAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2893.5M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2856.64)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Total number of fetched objects 1366
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 1366.
Total number of nets in the design is 1345, 0.0 percent of the nets selected for SI analysis
AEC_INFO-618: Total number of nets in the design is 1345, 0.0 percent of the nets selected for SI analysis
End delay calculation (fullDC). (MEM=2895.8 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2895.8 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.8 real=0:00:01.0 totSessionCpu=0:03:02 mem=2895.8M)

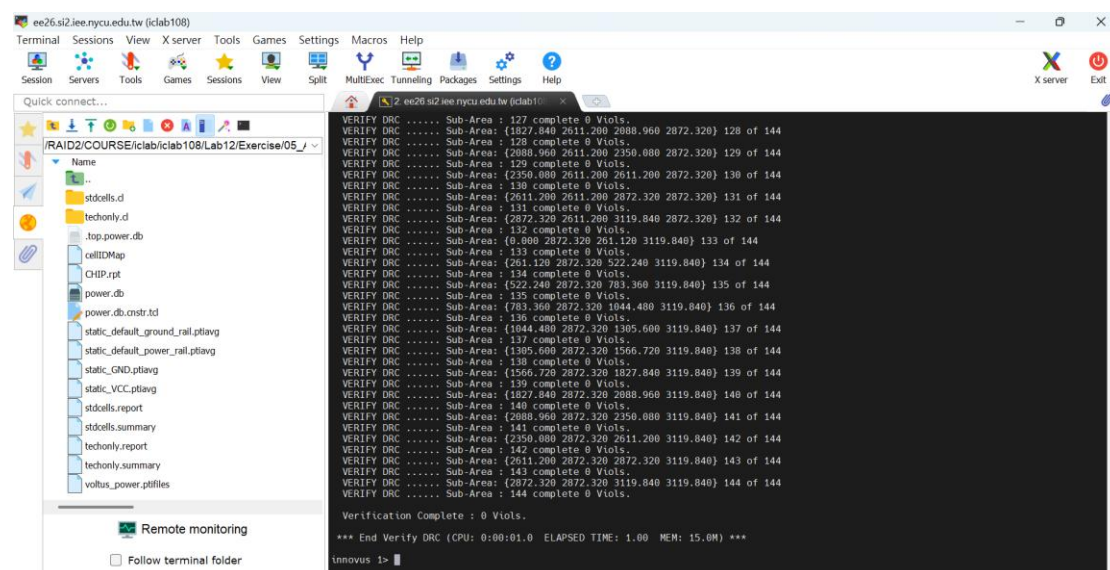
-----
timeDesign Summary
-----
Hold views included:
av_func_mode_min

| Hold mode | all | reg2reg | default |
|-----|-----|-----|-----|
| WNS (ns): | 0.240 | 0.240 | 19.737 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 595 | 247 | 366 |
|-----|-----|-----|-----|

Density: 0.684%
(138.344% with Fillers)

Reported timing to dir timingReports
Total CPU time: 1.2 sec
Total Real time: 2.0 sec
Total Memory Usage: 2829.070312 Mbytes
Reset AEC options
*** timeDesign #2 [finish] : cpu/real = 0:00:01.2/0:00:01.7 (0.7), totSession cpu/real = 0:03:02.5/0:22:59.1 (0.1), mem = 2829.1M
innovus i>
```

#### 5. DRC result :



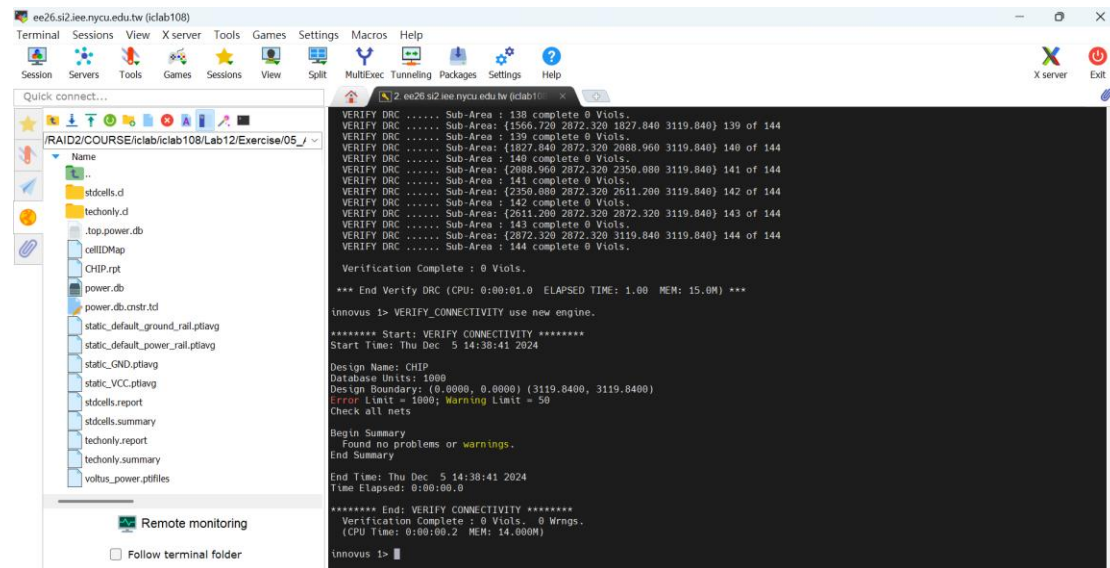
```
VERIFY DRC ..... Sub-Area : 127 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2611.200 2088.960 2872.320} 128 of 144
VERIFY DRC ..... Sub-Area : 128 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2611.200 2350.080 2872.320} 129 of 144
VERIFY DRC ..... Sub-Area : 129 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2611.200 2611.200 2872.320} 130 of 144
VERIFY DRC ..... Sub-Area : 130 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2611.200 2872.320 2872.320} 131 of 144
VERIFY DRC ..... Sub-Area : 131 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2611.200 3119.840 2872.320} 132 of 144
VERIFY DRC ..... Sub-Area : 132 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {0.000 2872.320 261.120 3119.840} 133 of 144
VERIFY DRC ..... Sub-Area : 133 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {261.120 2872.320 522.240 3119.840} 134 of 144
VERIFY DRC ..... Sub-Area : 134 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {522.240 2872.320 783.360 3119.840} 135 of 144
VERIFY DRC ..... Sub-Area : 135 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {783.360 2872.320 1044.480 3119.840} 136 of 144
VERIFY DRC ..... Sub-Area : 136 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1044.480 2872.320 1305.600 3119.840} 137 of 144
VERIFY DRC ..... Sub-Area : 137 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1305.600 2872.320 1566.720 3119.840} 138 of 144
VERIFY DRC ..... Sub-Area : 138 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1566.720 2872.320 1827.840 3119.840} 139 of 144
VERIFY DRC ..... Sub-Area : 139 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2872.320 2088.960 3119.840} 140 of 144
VERIFY DRC ..... Sub-Area : 140 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2872.320 2350.080 3119.840} 141 of 144
VERIFY DRC ..... Sub-Area : 141 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2872.320 2611.200 3119.840} 142 of 144
VERIFY DRC ..... Sub-Area : 142 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2872.320 2872.320 3119.840} 143 of 144
VERIFY DRC ..... Sub-Area : 143 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2872.320 3119.840 3119.840} 144 of 144
VERIFY DRC ..... Sub-Area : 144 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.0 ELAPSED TIME: 1.00 MEM: 15.0M) ***
innovus i>
```



## 6. LVS result :



The screenshot shows a terminal window with the title "ee26.siz.lee.nycu.edu.tw (iclab108)". The left sidebar displays a file tree under the path "/RAID2/COURSE/iclab/iclab108/Lab12/Exercise/05\_". The main terminal area shows the output of a Design Rule Check (DRC) and a connectivity check. The DRC results show 138 complete violations and 0 warnings. The connectivity check shows 0 violations and 0 warnings. The terminal output is as follows:

```
VERIFY DRC ..... Sub-Area : 138 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1566.720 2872.320 1827.840 3119.840} 139 of 144
VERIFY DRC ..... Sub-Area : 139 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2872.320 2088.960 3119.840} 140 of 144
VERIFY DRC ..... Sub-Area : 140 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2872.320 2350.080 3119.840} 141 of 144
VERIFY DRC ..... Sub-Area : 141 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2872.320 2611.200 3119.840} 142 of 144
VERIFY DRC ..... Sub-Area : 142 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2872.320 2872.320 3119.840} 143 of 144
VERIFY DRC ..... Sub-Area : 143 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2872.320 3119.840 3119.840} 144 of 144
VERIFY DRC ..... Sub-Area : 144 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.0 ELAPSED TIME: 1.00 MEM: 15.0M) ***

innovus i> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 5 14:38:41 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3119.8400, 3119.8400)
Error Limit = 1000; Warning Limit = 50
Check all nets

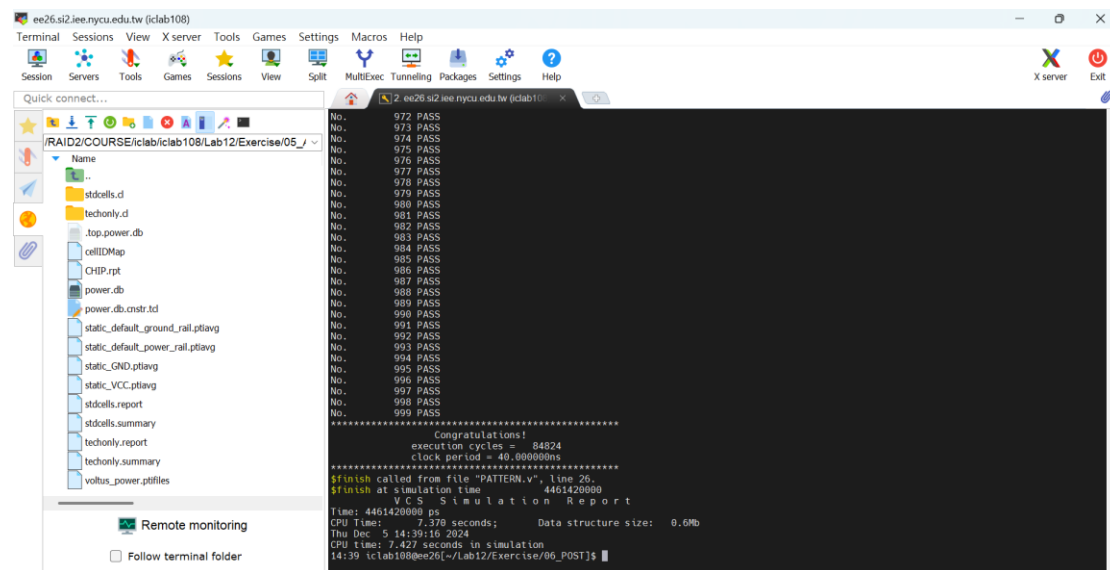
Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu Dec 5 14:38:41 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.2 MEM: 14.000M)

innovus i>
```

## 7. Post Layout simulation results :

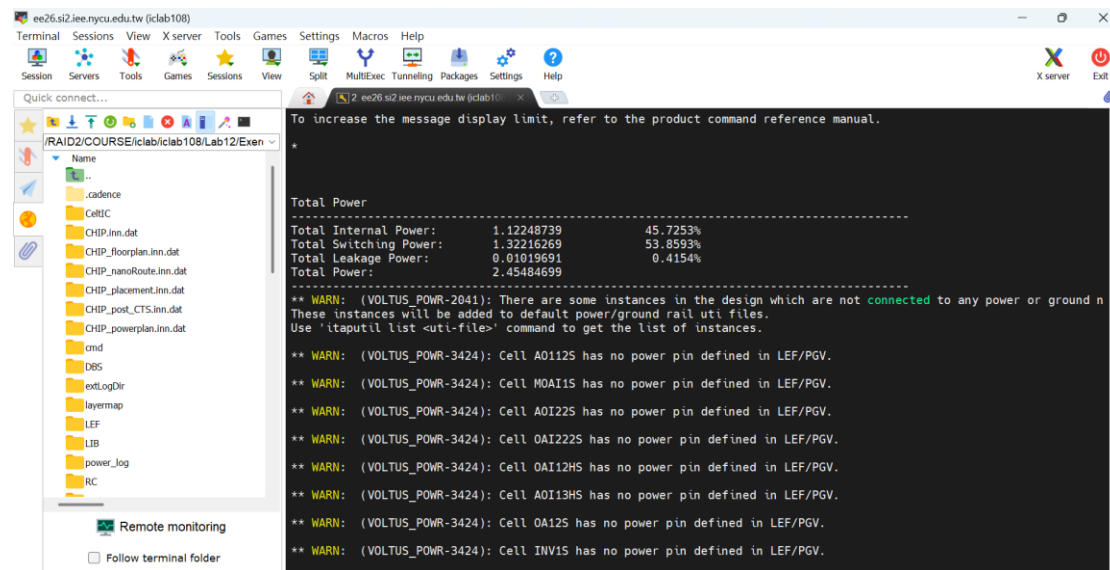


The screenshot shows a terminal window with the title "ee26.siz.lee.nycu.edu.tw (iclab108)". The left sidebar displays a file tree under the path "/RAID2/COURSE/iclab/iclab108/Lab12/Exercise/05\_". The main terminal area shows the output of a Post Layout simulation. The simulation results show 972 PASS, 973 PASS, 974 PASS, 975 PASS, 976 PASS, 977 PASS, 978 PASS, 979 PASS, 980 PASS, 981 PASS, 982 PASS, 983 PASS, 984 PASS, 985 PASS, 986 PASS, 987 PASS, 988 PASS, 989 PASS, 990 PASS, 991 PASS, 992 PASS, 993 PASS, 994 PASS, 995 PASS, 996 PASS, 997 PASS, 998 PASS, and 999 PASS. The simulation time is 4461420000 ps. The terminal output is as follows:

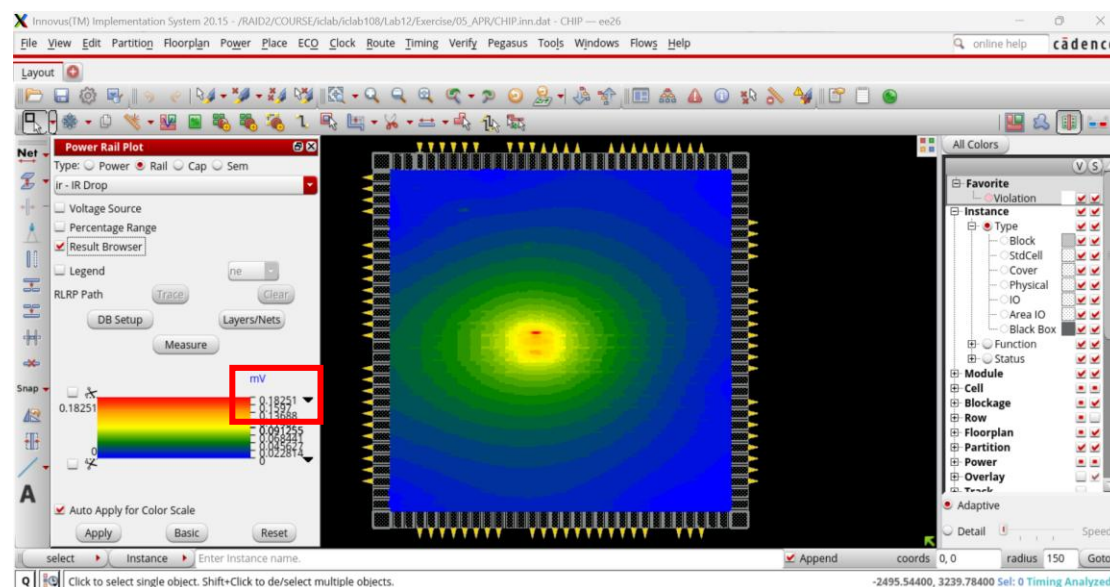
```
No. 972 PASS
No. 973 PASS
No. 974 PASS
No. 975 PASS
No. 976 PASS
No. 977 PASS
No. 978 PASS
No. 979 PASS
No. 980 PASS
No. 981 PASS
No. 982 PASS
No. 983 PASS
No. 984 PASS
No. 985 PASS
No. 986 PASS
No. 987 PASS
No. 988 PASS
No. 989 PASS
No. 990 PASS
No. 991 PASS
No. 992 PASS
No. 993 PASS
No. 994 PASS
No. 995 PASS
No. 996 PASS
No. 997 PASS
No. 998 PASS
No. 999 PASS

*****
Congratulations!
execution cycles = 84824
clock period = 40.000000ns
*****
$finish called from file "PATTERN.v", line 26.
$finish at simulation time 4461420000
V C S S i m u l a t i o n R e p o r t
Time: 4461420000 ps
CPU Time: 7.378 seconds; Data structure size: 0.0Mb
Thu Dec 5 14:39:16 2024
CPU time: 7.427 seconds in simulation
14:39 iclab108@ee26[~/Lab12/Exercise/06_POST]$
```

## 8. Power result :



## 9. IR Drop results :



在一條金屬導線上，若寄生電阻太大，將導致 IR drop 的現象，如果未能有效的減少 IR drop，會造成電源供應不足，影響晶片效能。因此我使用了 8 組 core power pad 以及使用更粗的電源線 stripe 去減少 IR drop。