ECE 385
Spring 2021
Experiment 1

Introductory Experiment

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Introduction

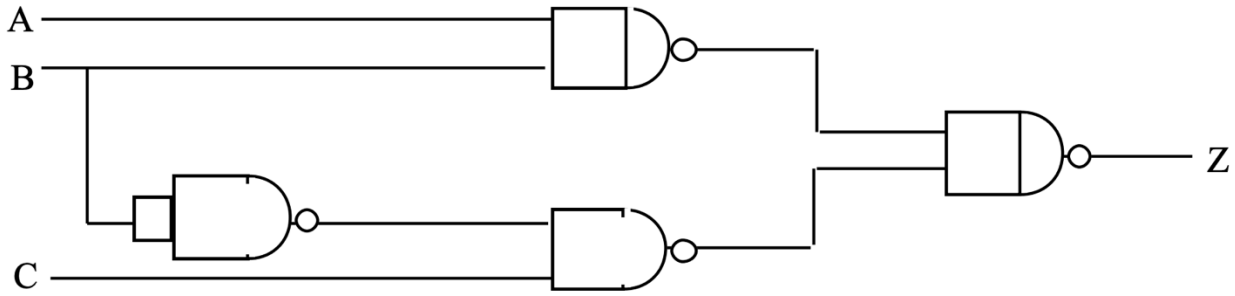
In lab 1, we study and observe how propagation delay of TTL will cause a static-1 hazard which is the possibility of producing a 0 glitch (pulse) when the steady state of the output should be a logic 1. Then we redesign the circuit and solve the static-1 hazard.

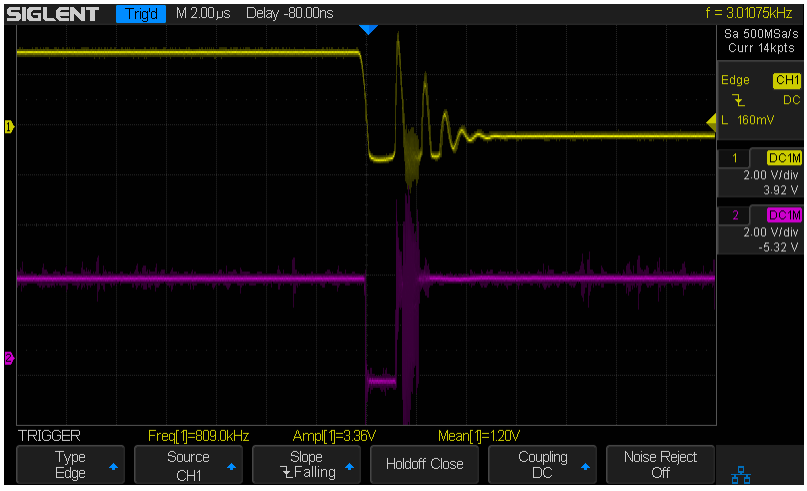
Purpose of the circuit

The purpose of the circuit is to show that the propagation delay of the gates will cause the static hazard which will momentarily generate the incorrect output of the circuit.

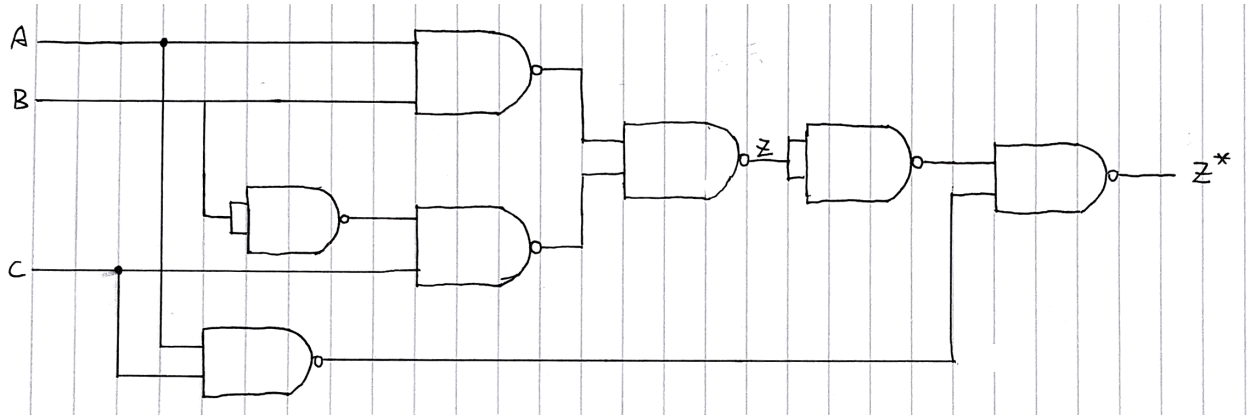
Written Description of Circuit

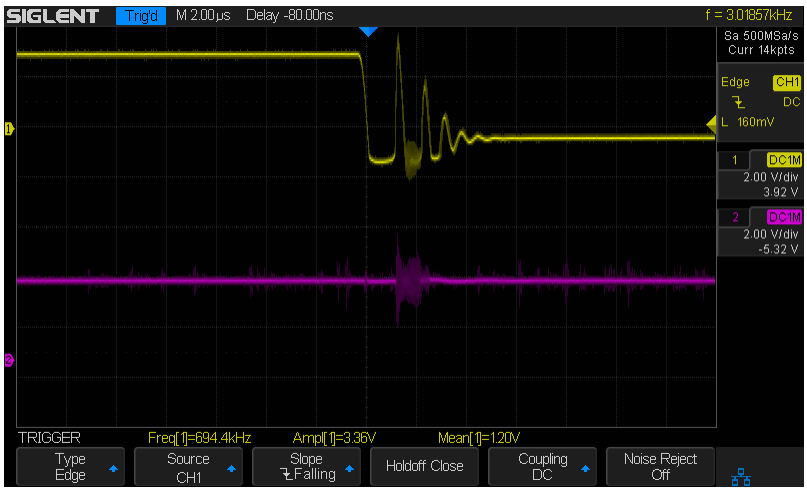
2-to-1 Mux using only NAND gates (with Static Hazard)
Boolean Expression: $Z = AB + \bar{B}C$





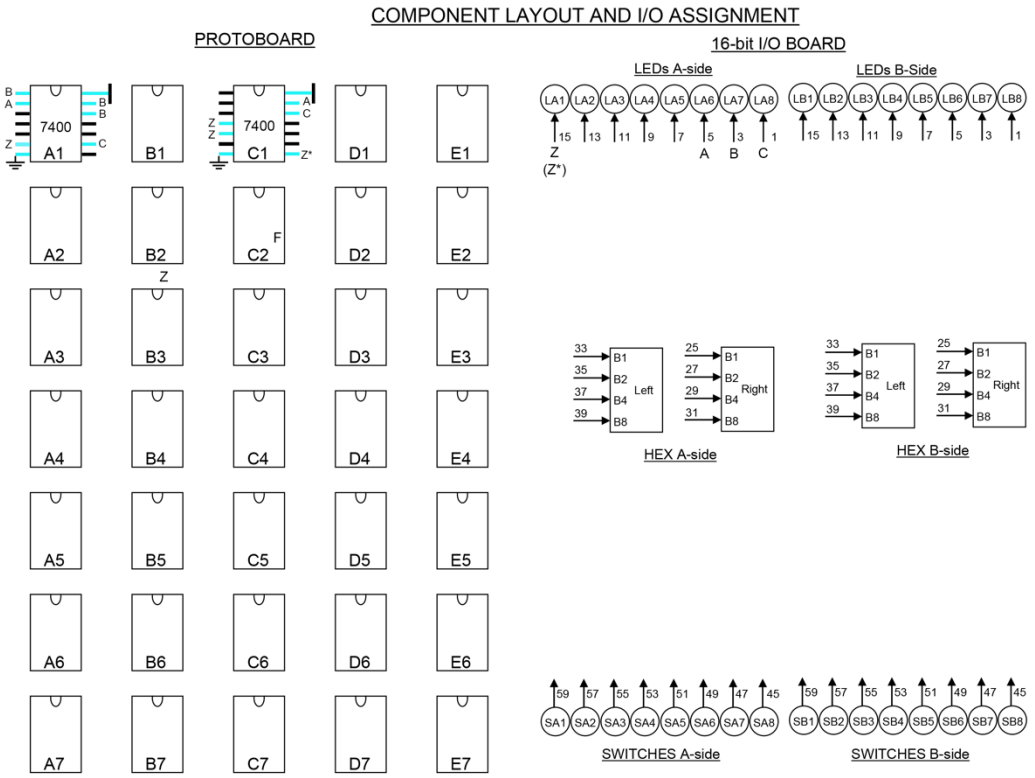
2-to-1 Mux using only NAND gates (eliminate Static Hazard)
Boolean Expression: $Z = AB + \bar{B}C + AC$





Component Layout and I/O Assignment

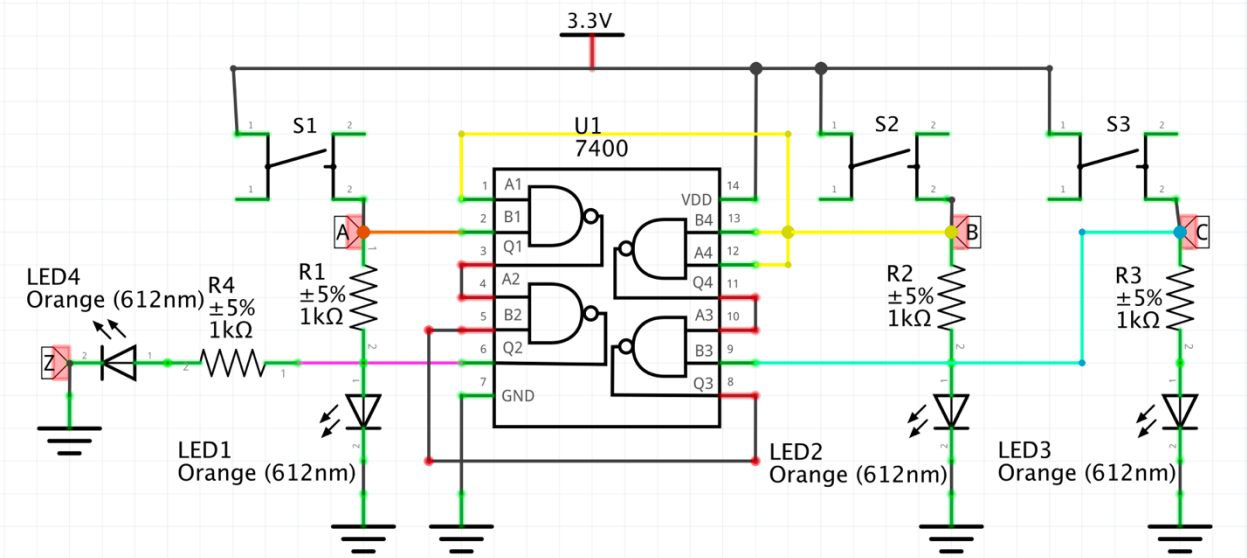
A : Input A	Input signal of Multiplexer
B : Input B	Select signal of Multiplexer
C : Input C	Input signal of Multiplexer
Z : Output Z	Output signal of Multiplexer (Part A)
Z*: Output Z*	Output signal of Multiplexer (Part B – Eliminate static-1 hazards)



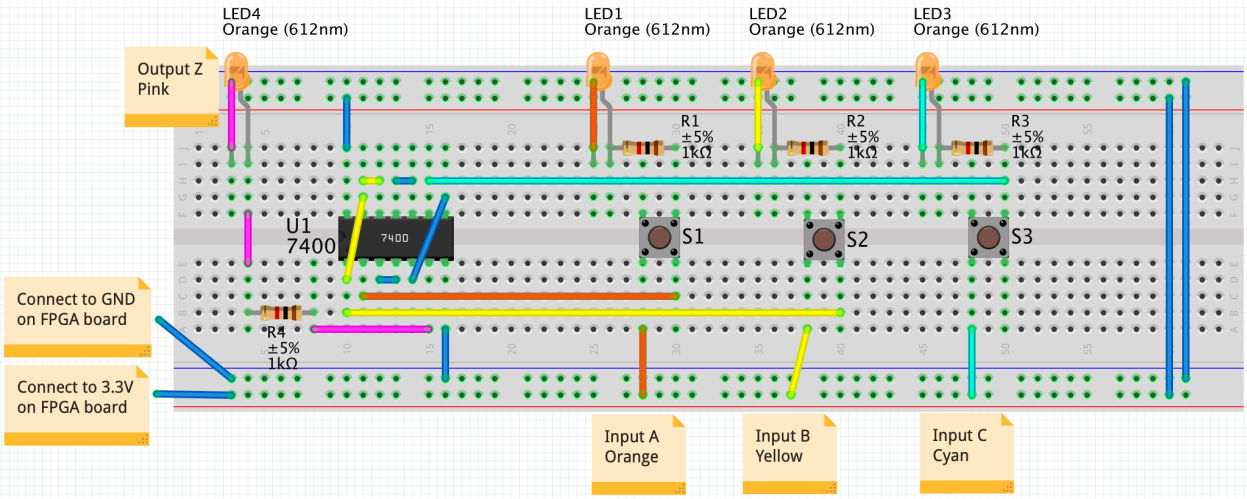
Circuit Diagrams

Part A

Schematic View

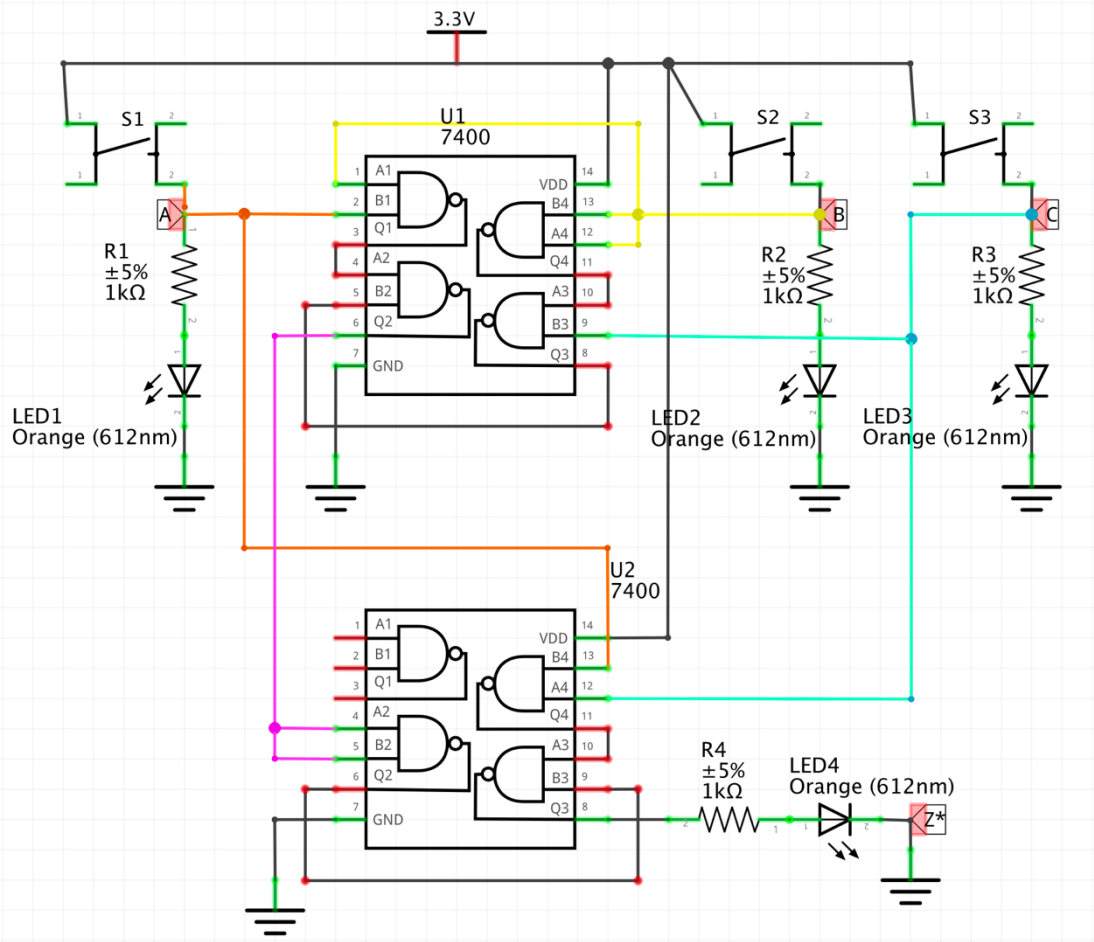


Breadboard View

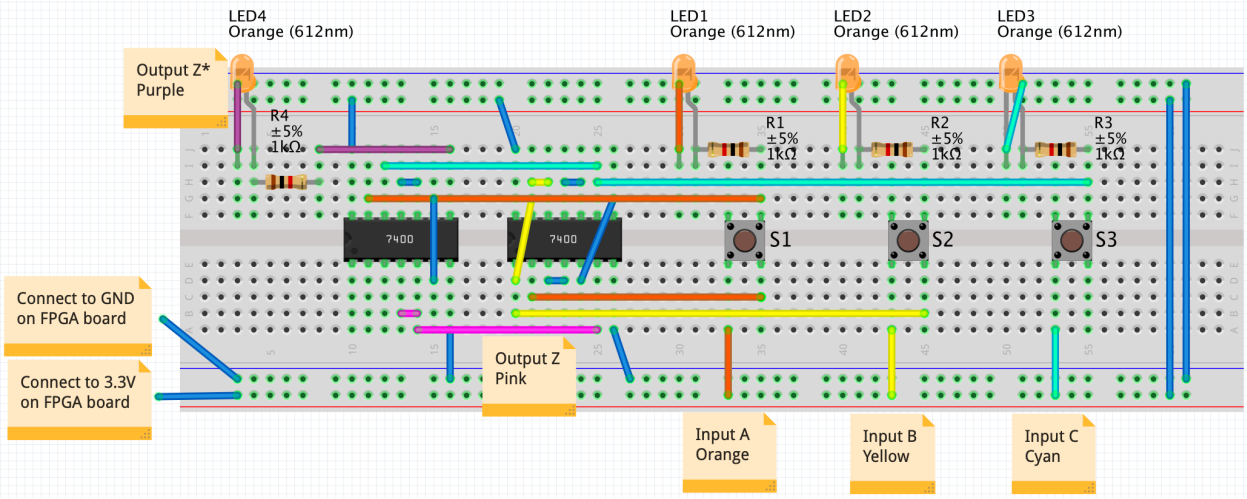


Part B

Schematic View



Breadboard View



Truth Tables and K-maps

Part A

Truth Table

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

K-Map

Z		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

Part B

Truth Table

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

K-Map

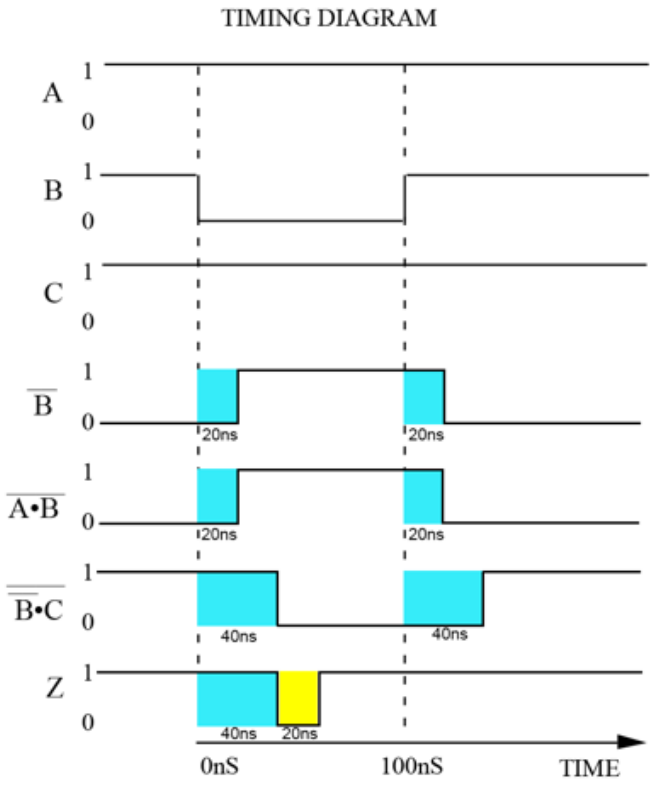
Z		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

The truth tables are same for part A and part B because both of them represents the steady state output of a 2-to-1 Multiplexer.

According to ECE 120, these two circuits should have the same results since they are the same implementation of the same circuit. However, the propagation delay of the NAND gate is not considered in that situation. Therefore, the oscilloscope of part A shows a static-1 hazard of the circuit. In order to fix this issue, we add an extra group of terms (AC) to the boolean expression of Z. In the oscilloscope of part B, the glitch is eliminated because we add the extra term AC. Thus, it successfully eliminates the static-1 hazard.

Post-Lab Questions

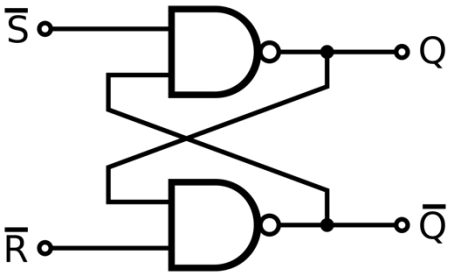
1. Assume the propagation delay of a 7400 has maximum delay time (20ns)
   The shaded regions indicate the delay of the 7400 chip



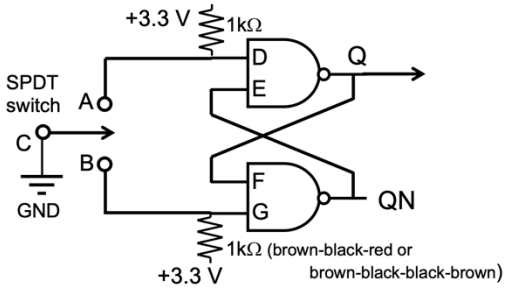
According to the time diagram, it takes 60ns to stabilize on the falling edge of B when we assume the 7400 chip has maximum delay time (20ns). It takes 0ns to stabilize on the rising edge of B because when B changes from 0 to 1, $\overline{AB}$ and $\overline{\bar{B}C}$ will have the combinations 10, 00, 01, and these combinations will always produce a 1 from a NAND gate. Therefore, there aren't any potential glitches in the output Z except the falling edge of B.

2.

SR Latch



Debouncer Circuit



Truth Table of SR Latch

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	No change	

The debouncer circuit uses a SR latch to solve the contact bounce issue. The input D in the debouncer circuit is equivalent to the input $\overline{S}$ in SR latch. The input G in the debouncer circuit is equivalent to the input $\overline{R}$ in SR latch.
When C (SPDT switch) is in position A, the input D is connected to ground (logic 0), and the input G is pulled to a logic 1 by the pull-up resistor. Therefore, the output Q has a stable logic 1 output (switch closed). When C (SPDT switch) is in position B, the input G is connected to ground (logic 0), and the input D is pulled to a logic 1 by the pull-up resistor. Therefore, the output Q has a logic 0 (switch open).
Since the inputs of the debouncer circuit (A and B) are connected with its own pull-up resistors, the logic values of input A and input B are always 1 when C (SPDT switch) is not connected to either point A or B. The debounce circuit will maintain its current output until either input D or input G is changed (SPDT switch is connected to either point A or point B). Therefore, the circuit eliminates the contact bounce issue.

General Guide Questions

GG.6

Larger noise immunity will have more tolerance with the input. When the input is unstable, a stable output (logic 1 or logic 0) can be still produced. The last inverter observes because as signal goes through many inverters, the noises add up, and the total noise increases. Therefore, it makes more obvious to observe.

The noise immunity for the inverter for a logic "1" can be calculated by using the middle value of the nominal "1" range minus the minimum value of "1" which is $3.5V - 1.35V = 2.15V$.

The noise immunity for the inverter for a logic “0” can be calculated by using the maximum value of “0” minus the middle value of the nominal “0” range which is $1.15V - 0.35V = 0.8V$.

GG.31

When we are connecting several parallel LEDs in series with a single resistor, we can control the total current goes through all the LEDs. However, we cannot control the current through each LED. Therefore, this may cause the situation that some of the LEDs may be very bright, and some of the LEDs may be dim. Therefore, it is not helpful for us to test or debug the circuit.

Conclusion

In conclusion, static hazards are going to appear commonly in circuits because of the propagation delay of the chips. Therefore, it is very important to take care of them while designing the circuits, such as adding an extra term into the boolean expression. In addition, debounce switches are also crucial for designing a circuit because it can ensure the signals to be stable whenever we change the logic values.

The lab is simple, and everything works fine, but there may be one issues that the propagation delay of the gate is so small that the glitch is hard to be observed. Therefore, we may have to use some alternative methods such as adding more gates or a capacitor to manually increase the delay.