ព្រះរាជាណាចក្រកម្ពុជា

ជាតិ សាសនា ព្រះមហាក្សត្រ

Assignment of Computer Architecture

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- **ANSWER**

1. DRAM and SRAM are two different types of computer memory. SRAM is faster but more expensive than DRAM. DRAM is slower but cheaper than SRAM. Most computers use a combination of both types of memory to optimize performance. Also, the difference between DRAM and SRAM is that SRAM uses six transistors while DRAM only uses one. This makes SRAM much faster than DRAM, but it also means that SRAM requires more power which makes it more expensive. While SRAM is the better choice if you need a fast memory chip, DRAM might be a better choice if you are willing to sacrifice some speed for lower power consumption and cost.
2. The main advantages of DRAM are its simple design and low cost in comparison to alternative types of memory. The main disadvantages of DRAM are its high volatility and high-power consumption relative to other options.
3. ROM is not volatile memory. It stores the data permanently. The applications are
    - ROM is used in embedded systems or any systems where the programming does not need to change.
    - ROM is used in many appliances, toys, automobiles uses chips to maintain information when the power is shut off.
    - ROMs are also used extensively in calculators and peripheral devices such as laser printers, which store their fonts.
4. Explain the concept of a memory hierarchy:
    a. Registers:
        - Speed: Fastest 1ns - 2ns
        - Cost: Most expensive
        - Use: Stores the most critical data for the CPU to use right away.

    b. Level 1 Cache (L1 Cache):
        - Speed: Very fast 3ns - 10ns
        - Cost: Expensive
        - Use: Holds frequently used data to speed up processing.

    c. Level 2 Cache (L2 Cache):
        - Speed: Fast 25ns - 50ns
        - Cost: Less expensive than L1
        - Use: Stores data not in L1 but still needed quickly.

d. Main Memory (RAM):
   - Speed: Moderate 30ns - 90ns
   - Cost: Cheaper than cache
   - Use: Holds data and programs currently in use.

e. Hard Drive:
   - Speed: Slow 5ms – 20ms
   - Cost: Affordable
   - Use: Long-term storage of files and programs.

f. Optical Disk (e.g., CD/DVD):
   - Speed: Slower 100ms – 5sec
   - Cost: Cheap
   - Use: Archival storage, not used frequently.

g. Magnetic Tape:
   - Speed: Slowest 10sec – 3min
   - Cost: Cheapest
   - Use: Storing large amounts of data for a long time, usually offline.

5. The L1 cache is faster than the L2 cache and the L1 cache is smaller than the L2 cache. Because it is fast enough to keep up with the CPU's speed, fits on the limited space of the CPU chip, remains cost-effective, and provides quick access to essential data, maintaining overall efficiency.

6. A page fault occurs when a program tries to access memory that isn't currently in RAM, prompting the operating system to load the required memory from disk into RAM. While essential for efficient memory management and enabling virtual memory, excessive page faults can degrade system performance, a condition known as thrashing.

7. The difference between virtual memory address and physical memory address is:

   - Virtual addresses are used by the CPU during a program's execution, while physical addresses refer to actual hardware memory locations. In more detail, a virtual address is a memory address that is generated by the CPU during a program's execution. On the other hand, a physical address is a location in the actual hardware memory, such as RAM.

➢ The virtual memory is typically larger than physical memory because:

- Address Space: Virtual memory has a much larger address space (up to 16 exabytes on a 64-bit system) compared to the limited size of physical RAM (usually GB to TB).
- Process Isolation: Each process gets its own virtual address space, requiring more addresses than the shared physical memory.
- Swapping and Paging: Virtual memory uses disk storage to extend beyond the actual physical memory.
- Future-Proofing: Larger virtual address spaces accommodate growing hardware capabilities and complex applications.

8. A TLB (Translation Lookaside Buffer) is a hardware cache that is used in computer systems to improve the efficiency of virtual memory management. It stores recently accessed virtual-to-physical address translations, eliminating the need to access the page table for every memory access. TLBs are typically implemented in the memory management unit (MMU) of a processor. The TLB improves the Effective Access Time (EAT) of memory operations by reducing the time required for address translation. Without a TLB, every memory access would require accessing the page table, resulting in additional memory accesses and increased latency. By caching frequently used translations in the TLB, subsequent memory accesses that require the same translation can be performed much faster, reducing the overall memory access time.

9. The pros and cons of paging are:

➢ Pros:

⇔ No Fragmentation:

- Avoids memory gaps by using fixed-size pages.
- Simplifies memory allocation.

⇔ Efficient Use:

- Only loads necessary pages, saving memory.
- Allows more virtual memory than physical memory.

⇔ Process Isolation:

- Each process has its own memory space, improving security.
- Prevents processes from accessing each other's memory.

⇔ Simplifies Management:

- Fixed-size pages make memory management easier.
- Uniform handling of pages by the operating system.

⇔ Supports Virtual Memory:

- Enables running larger applications.
- Swaps inactive pages to disk, freeing up RAM.

➢ Cons:

⇔ Overhead:

- Address translation adds extra time.
- Page tables consume memory.

⇔ Page Faults:

- Fetching pages from disk slows down performance.
- Frequent page faults can lead to thrashing.

⇔ Fixed Page Size:

- Can waste memory if pages don't fit perfectly.
- Choosing the right page size is difficult.

⇔ Complexity:

- Requires advanced hardware and software support.
- Managing large page tables is complicated.

In summary paging overhead includes the extra time and memory required for address translation, maintaining page tables, and handling page faults.

10. The advantages and disadvantages of Virtual memory are:

➢ The advantaged of Virtual memory

Virtual memory offers several advantages that improve the overall performance and efficiency of computer systems. Some of the key benefits are described below:

- Memory management
- Efficient use of primary memory

- Increased capacity
- Program isolation
- Flexible memory allocation

➢ The disadvantages of Virtual memory

While virtual memory offers numerous benefits, it also has some drawbacks and potential issues that can negatively impact system performance. Some of the key disadvantages and problems associated with virtual memory usage are:

- Performance overhead
- Page faults and increased latency
- Thrashing
- Increased hardware requirements
- Complex management

EXERCISE:

I.

a) There are 2^{16} blocks of main memory.

b) The format of a memory address as seen by the cache, that is have 11 tag, 5 blocks and 4 word.

c) The memory reference $0DB63_{16}$ map is in the 22 cache.

II.

a) There are 2^{18} blocks in main memory.

b) The format of a memory address as seen by the cache, that is have 11 tag, and 7 word.

c) The memory reference $01D872_{16}$ map is anywhere of the cache.

III.

a) Direct mapped
word = $2^5 = 5\ bits$
block = 64 KB/32 = 11 bits
tag = 24-11-5=8

b) Associative
block = 5blocks
tag = 24-5 = 19bits

c) 4-way set associative
tag = 24-5-3 = 16
set = $2^5/2^2 = 2^3$=3
word = 5

IV.

a) Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes

4K = 212 blocks
8 word each = 23 bits
=>main memory = block x words each = 212 x 23 = 215 words
We have 15 bits in address
Cache contain = 23 blocks = 3 bits
Each block has 23 word = 3 bits
Tag = 15 – 3 – 3 = 9 bits

b) Compute the hit ratio

Loops 4 times from location 0 to 67
Block 0 = 0 to 7
Block 1 = 8 to 15
Block 2 = 16 to 23
Block 3 = 24 to 31
Block 4 = 32 to 39
Block 5 = 40 to 47
Block 6 = 48 to 55
Block 7 = 56 to 63
Block 8 = 64 to 67

Block 0: 4 misses, 28 hits
Block 1: 1 miss, 31 hits
Block 2: 1 miss, 31 hits
Block 3: 1 miss, 31 hits
Block 4: 1 miss, 31 hits
Block 5: 1 miss, 31 hits
Block 6: 1 miss, 31 hits
Block 7: 1 miss, 31 hits
Block 8: 4 misses, 12 hits
Total miss = 15
Total hit = 257
Hit ratio = 257/ (15 + 257) = 94.49%

c) Effective access time

EAT= (Hit Ratio × Hit Time) + (Miss Ratio × Miss Time)
Miss Ratio = 1 - Hit Ratio = 1 - 0.875 = 0.125
EAT=(0.875×22ns) + (0.125×322ns) = 59.5ns

V.

a) TLB hit, cache hit

Time = TLB hit + cache hit = 5 + 12 = 17 ns, possible

b) TLB miss, page table hit, cache hit

Time = TLB miss + page table hit + cache hit = 5 + 25 + 12 = 42ns, possible

c) TLB miss, page table hit, cache miss

Time = 5 + 25 + 12 = 42ns, possible

d) TLB miss, page table miss, cache hit

It is impossible, we get a table miss we cannot go cache.

e) TLB miss, page table miss

First, we can access the disk and update the memory and restore the instruction
Time = TLB miss + page table miss + disk access + TLB access + page table access
= 5ns + 25ns + 200ms + 5ns + 12ns = 200.015ms

VI.

a) Require for each virtual address:
_ The max of address space is
➢ 16MB = $2^{20} \times 2^4 = 2^{24}$ = 24 bits
Therefore: There are 24 bits are required for each virtual address.

b) Require for each physical address:
➢ Physical address = 2MB = 2^{21} = 21 bits
Therefore: There are 21 bits are required for each physical address.

c) The maximum number of entries in a page table:
➢ Max number of entries page = $\frac{2^{24}}{2^{10}} = 2^{14}$ = 14 bits

Therefore: 14 bits is the maximum number of entries in a page table.

d) Physical address will the virtual address 1524_{10} translate:
_ Virtual page 1 → Page frame 2

➢Page 0 = 0 → 10^{23}
➢Page 1 = 1024 → 2047

e) Virtual address will translate to physical address 1024_{10}

_ Virtual address → Physical address 1024_{10}

➢ Virtual page 0 → Page frame 1