ESE501 Project 1 Phase 1 Report

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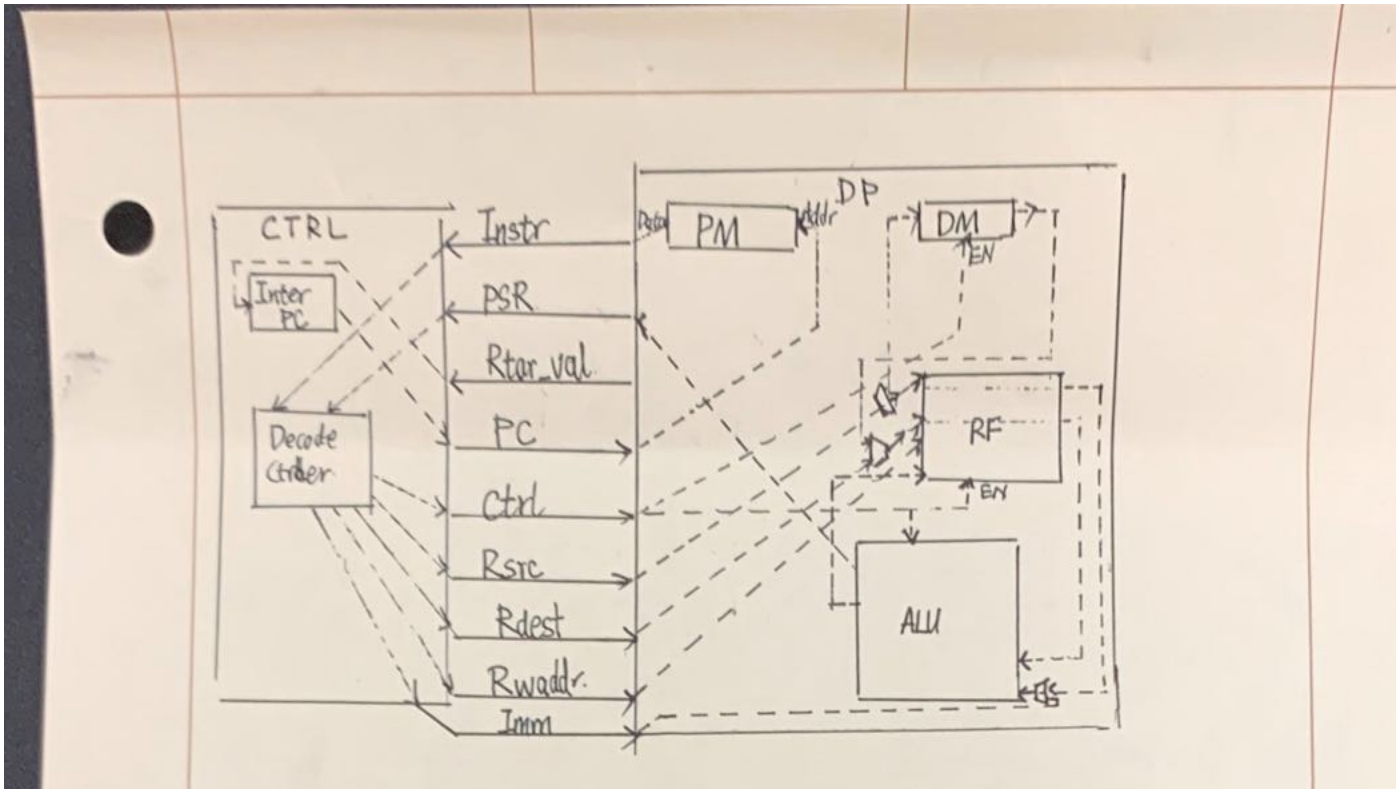
Objectives:

In this project, we are asked to design a processor that can deal with some basic 16-bit instructions by writing 6 simple modules.

In phase 1, we are not required to design pipelines and do any clock manipulations. Thus, we are just asked to connect all 6 modules and test their functionality.

Diagram:



Control Signals

Operation	Signals from CTRL to Datapath. (In

	decimal)
ADD	1
ADDI	*2
SUB	3
SUBI	*4
CMP	5
CMPI*	*6
AND	7
ANDI	*8
OR	9
ORI	*10
XOR	11
XORI	*12
MOV	13
MOVI	*14
LSH	15
LSHI	*16
ASH	17
ASHI	*18
LUI	19

LOAD	20
STOR	21
Bcond EQ	22
Bcond NE	23
Bcond GE	24
Bcond CS	25
Bcond CC	26
Bcond GT	27
Bcond LE	28
Bcond LT	29
Jcond EQ	30
Jcond NE	31
Jcond GE	32
Jcond CS	33
Jcond CC	34
Jcond GT	35
Jcond LE	36
Jcond LT	37
JAL	38
NOP	39

(Some of the control signals may not be used in ALU, but we will pass every signal to Datapath)

Summary:

Since this is the very first step in our project1, we designed some complicated branches to deal with different instructions and tried to make each branch as clear and as separate as possible so that we may save some time in the future in expanding the current project to a pipelined one.