USB-KW41Z Sniffer/Development Board
User's Guide

1. Introduction

This guide describes the hardware for the USB-KW41Z sniffer/development board. The USB-KW41Z sniffer/development board is a small, low-power, and cost-effective evaluation and development board for application prototyping and demonstration of the KW41Z/31Z/21Z (KW41Z) family of devices. These evaluation boards offer easy-to-use mass-storage-device mode flash programmer, a virtual serial port, and standard programming and run-control capabilities.

The KW41Z is an ultra low-power, highly integrated single-chip device that enables Bluetooth Low Energy (BLE), Generic FSK (at 250, 500 and 1000 kbps) or IEEE Standard 802.15.4 with Thread support for portable, extremely low-power embedded systems.

The KW41Z integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, up to 512 KB Flash and up to 128 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications

2. Overview and Description

The USB-KW41Z development board is an evaluation environment supporting NXP's KW41Z/31Z/21Z (KW41Z)

Contents

Wireless MCUs. The KW41Z integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range (supporting a range of FSK/GFSK and O-QPSK modulations) and an ARM Cortex-M0+ MCU into a single package.

NXP supports the KW41Z with tools and software that include hardware evaluation and development boards, software development IDE, applications, drivers, custom PHY usable with IEEE Std. 802.15.4 compatible MAC, BLE Link Layer, and enables the usage of the Bluetooth Low Energy protocol in the MBAN frequency range for proprietary applications. The USB-KW41Z development board consists of the KW41Z device with a 32 MHz reference oscillator crystal, RF circuitry (including antenna).

The board is a standalone PCB and supports application development with NXP's Bluetooth Low Energy, Generic FSK and IEEE Std. 802.15.4 protocol stacks including Thread.

3.1   Board features

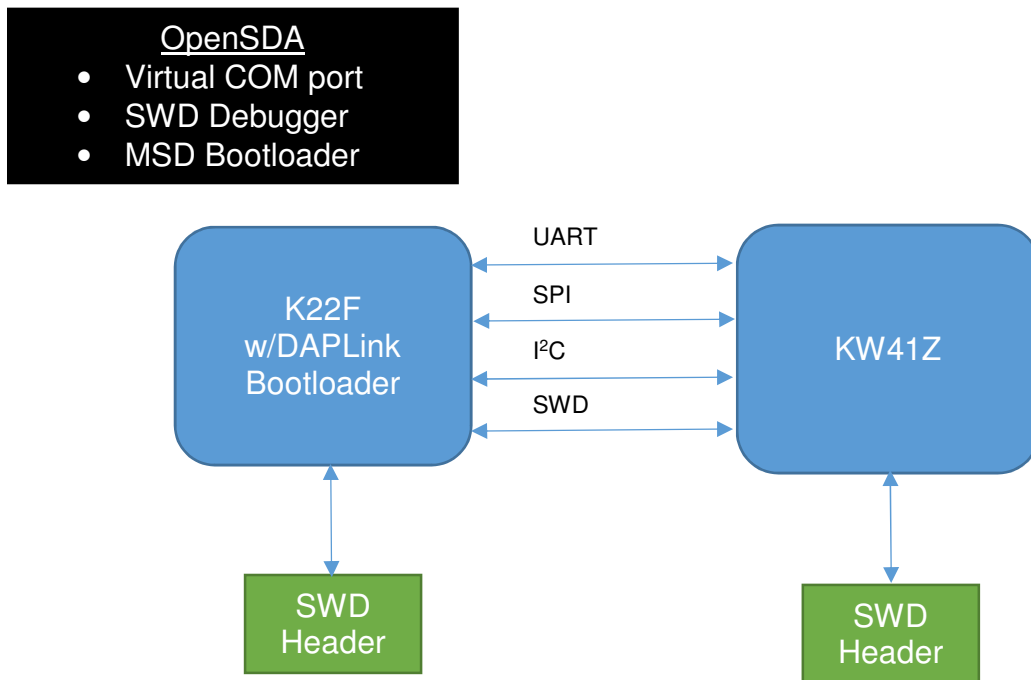A high level block diagram of the USB-KW41Z board features is in the following figure:

Figure 1: USB-KW41Z block diagram

2.1.1 USB-KW41Z board

The USB-KW41Z sniffer/development board is primarily targeted as a BLE or 802.15.4 sniffer. It also has the capability to act as a limited function development platform for KW41Z/31Z/21Z, or as a two

MCU development platform for Kinetis connectivity solutions. Figure 2 shows the USB-KW41Z development board.
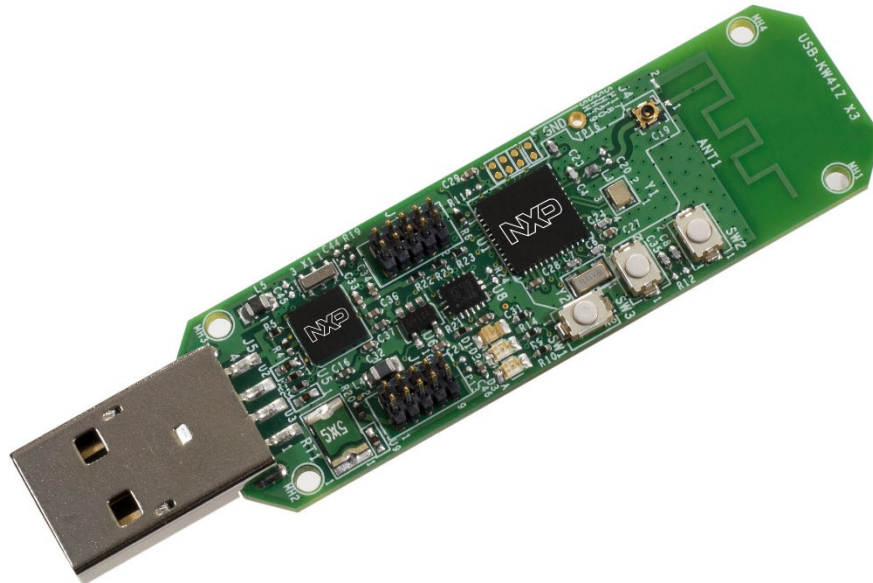
Figure 2: USB-KW41Z Freedom development board.

The USB-KW41Z development board has these features:
- NXP's ultra-low-power KW41Z Wireless MCU supporting BLE, Generic FSK, and IEEE Std. 802.15.4 (Thread) platforms
- IEEE Std. 802.15.4, 2006-compliant transceiver supporting 250 kbps O-QPSK data in 5.0 MHz channels, and full spread-spectrum encoding and decoding
- Fully compliant Bluetooth v4.2 Low Energy (BLE)
- Reference design area with small-footprint, low-cost RF node:
    — Single-ended input/output port
    — Low count of external components
    — Programmable output power from -30 dBm to +3.5 dBm at the SMA connector, no harmonic trap, with DC/DC Bypass and Buck modes of operation
    — Receiver sensitivity is -100 dBm, typical (@1 % PER for 20-byte payload packet) for 802.15.4 applications, at the SMA connector
    — Receiver sensitivity is -95 dBm (for BLE applications).
- Integrated PCB meander antenna
- 32 MHz reference oscillator
- 32 kHz reference oscillator
- 2.4 GHz frequency operation (ISM and MBAN)
- Integrated Open-Standard Serial and Debug Adapter (OpenSDA)
- Cortex 10-pin (0.05″) SWD debug port for target MCU
- Cortex 10-pin (0.05″) JTAG port for OpenSDA updates
- Two red LED indicators
- One green LED power indicator
- One push-button switches

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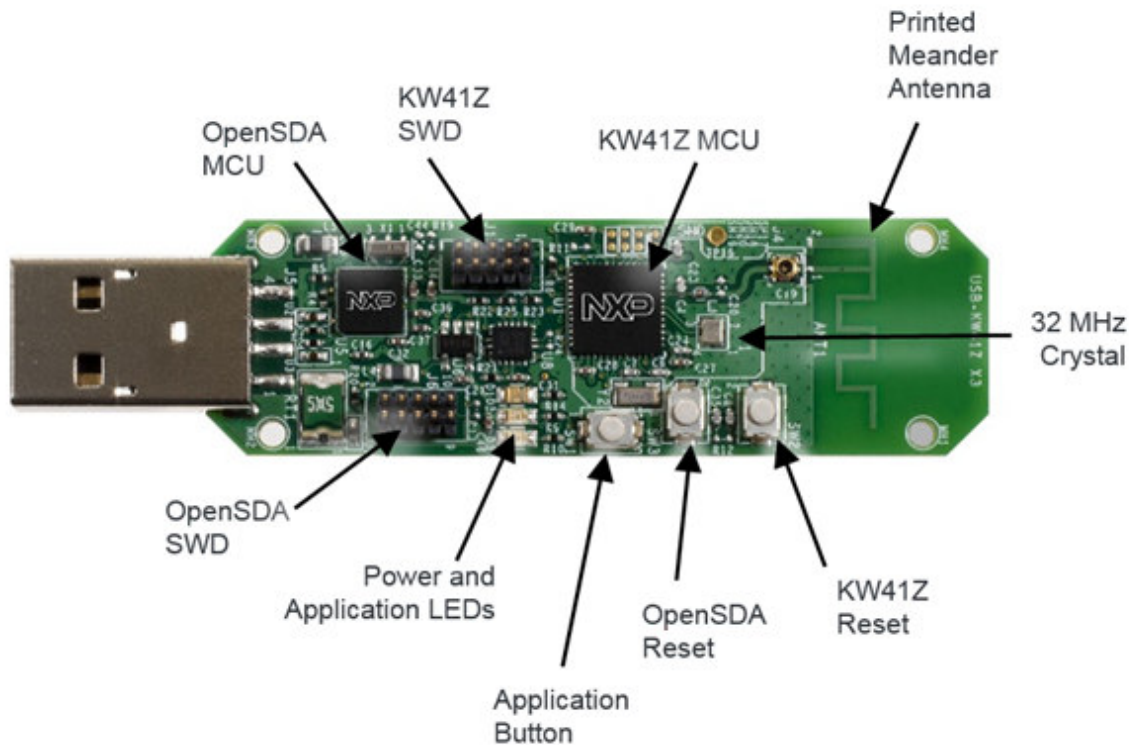This figure shows the main board features for the USB-KW41Z board:

Figure 3: USB-KW41Z component placement.

3.2   Serial and Debug Adapter

The USB-KW41Z development board includes an OpenSDA v3.2 circuit, which is based on a NXP Kinetis K22F family MCU with 512 KB of embedded flash and an integrated USB controller. It acts as a bridge for the serial and debug communications between a USB host and an embedded target processor such as the KW41Z, as shown in Figure 3. The K22F on the USB-KW41Z comes preloaded with sniffer firmware that can be used in conjunction with the sniffer firmware loaded on the KW41Z and the Kinetis Protocol Analyzer Adapter PC software in order to sniff wireless networks. This default K22F firmware also includes the DAPLink bootloader, which can be activated by holding down SW2 while plugging in the USB-KW41Z. This will bring up a DAPLINKBOOT drive on the host PC, and different OpenSDA apps can be drag-and-dropped into that drive to reprogram the K22F. The OpenSDA circuit block diagram is presented in the following diagram.
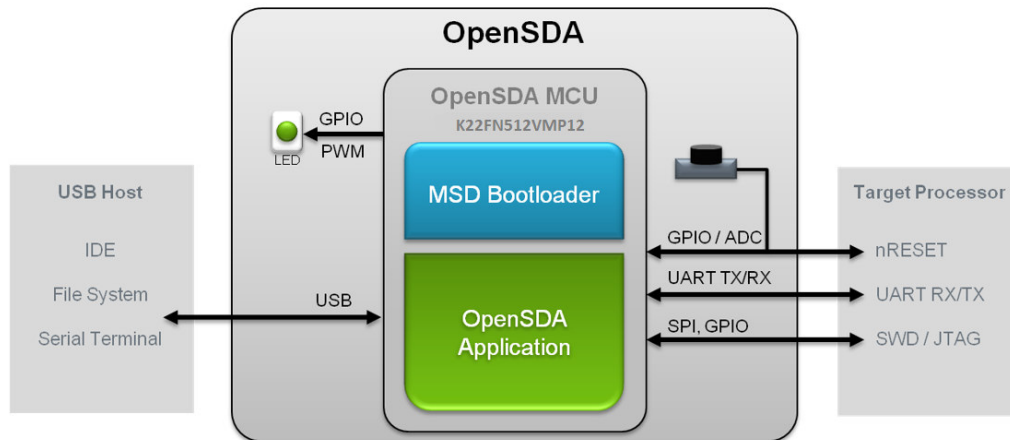
Figure 4: OpenSDAv3.2 high-level block diagram.

The JLink OpenSDA application (provided by Segger) is one such OpenSDA application that can be loaded onto the OpenSDA 3.2 circuit using the bootloader. This application provides a MSD flash programming interface, a virtual serial port interface, and a J-Link debug protocol interface. For more information on the OpenSDAv3.2 software, see mbed.org, https://github.com/mbedmicro/DAPLink, and https://www.segger.com/opensda.html.

The default sniffer application can be reprogrammed into the K22F using the OpenSDA bootloader as well. It can be found in the Connectivity Software package at \tools\wireless\binaries\sniffer_usbkw41z_k22f_0x8000.bin

NOTE: If an external debug probe is used to reprogram the K22F as part of a Connectivity Software example, this will erase the DAPLink bootloader. This then means the JLink OpenSDA app will no longer be supported by this circuit since that firmware assumes the bootloader is present on the K22F. The sniffer application can be still be ran however by programming in the \tools\wireless\binaries\sniffer_usbkw41z_k22f.bin firmware with an external debug probe.

3.2.1 Virtual serial port

A serial port connection is available between the OpenSDAv3.2 MCU and pins PTC6 and PTC7 of the KW41Z. This is used by the JLink OpenSDA application to provide a virtual COM port.
NOTE
To enable the Virtual COM, Debug, and MSD features, Segger J-Link drivers must be installed. Download the drivers at https://www.segger.com/downloads/jlink.

3. Functional description

4.1.1 RF performance and considerations

The USB-KW41Z RF circuit provides an RF interface for users to begin application development. A minimum matching network to the MCU antenna pin is provided through C4 and L3. Additional matching components, C47 & L6, are provided to match the printed meander antenna to the 50 ohm controlled line.

An optional MMCX connector is located at J4. This is can be bypassed by populating a 10 pF capacitor at C19. The following figure 6 shows the RF circuit in detail:
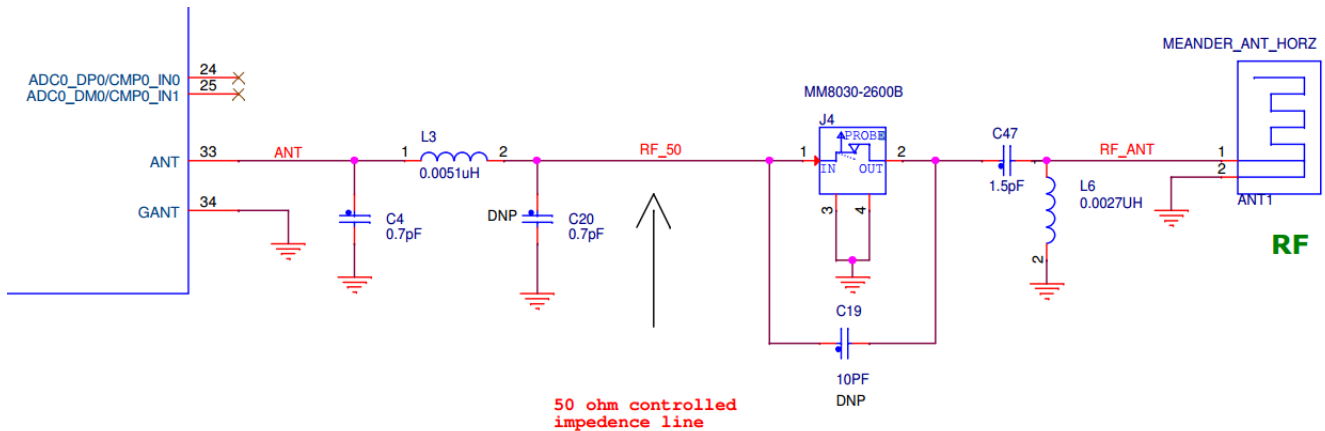
Figure 5: USB-KW41Z RF circuit.

4.1.2 Clocks

The USB-KW41Z board provides two clocks. A 32 MHz clock for clocking the MCU and Radio, and 32.768 kHz clock to provide an accurate low power time base.
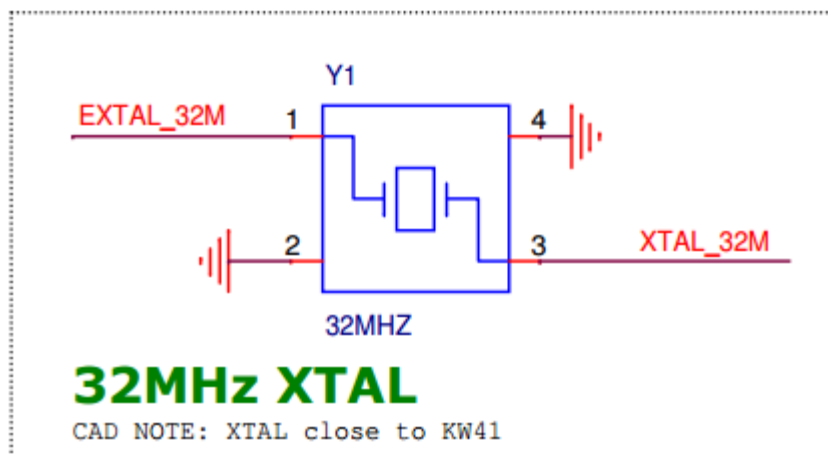
Figure 6: USB-KW41Z 32 MHz reference oscillator circuit.

- 32 MHz Reference Oscillator

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- o Figure above shows the 32 MHz external crystal Y1, which is an IEEE std. 802.15.4 compliant crystal. The IEEE Std. 802.15.4 requires the frequency to be accurate to less than ±40 ppm
- o Internal load capacitors provide the bulk of the crystal load capacitance. At 25 °C, the frequency must be accurate to ±10 ppm (or less) to enable temperature variation
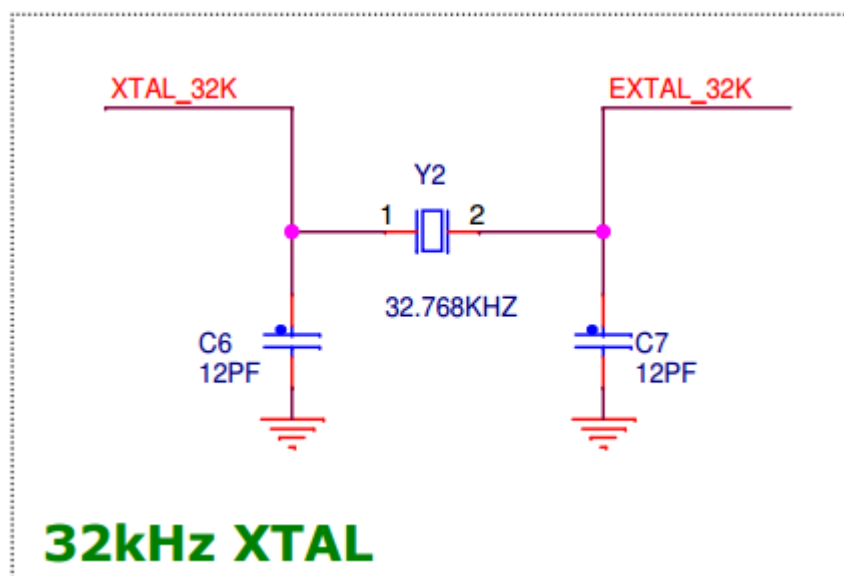- o To measure the 32 MHz oscillator frequency, program the CLKOUT (PTB0) signal to provide buffered output clock signal

Figure 7: USB-KW41Z 32.786 kHz oscillator circuit.

- • 32.768 kHz Crystal Oscillator (for accurate low-power time base)
  - o A secondary 32.768 kHz crystal Y2 is provided (see Figure above)
  - o Load capacitors C6 & C7 provide the entire crystal load capacitance

4.1.3 Power management

The USB-KW41Z is powered through the USB connector (J5). This is fed to the VREGIN of the K22F, which in turn provides a 3.3V supply to the board components. See figures below for power scheme.

Figure 8: USB-KW41Z USB connector

Figure 9: USB-KW41Z VREGIN and VOUT33 power scheme

4.1.4 Inter-processor communication

The USB-KW41Z development board provides several methods of inter-processor communication between the K22F and KW41Z MCUs. The following table shows the processor interconnects in more detail:

Interconnect Type	Signal Name	K22F Function [Pin]	KW41Z Function [Pin]
UART	UART_TXD	LPUART0_RX[PTC3]	LPUART0_TX[PTC7]
	UART_RXD	LPUART0_TX[PTC4]	LPUART0_RX[PTC6]
	UART_CTS	LPUART0_RTS[PTC1]	LPUART0_CTS[PTC4]
	UART_RTS	LPUART0_CTS[PTC2]	LPUART0_RTS[PTC5]
SPI	SPI_SS	SPI0_PCS0[PTD0]	SPI1_PCS0[PTA19]

	SPI_CLK	SPI0_SCK[PTD1]	SPI1_SCK[PTA18]
	SPI_SIN	SPI0_SOUT[PTD2]	SPI1_SIN[PTA17]
	SPI_SOUT	SPI0_SIN[PTD3]	SPI1_SOUT[PTA16]
I2C	PTC2_KW41_I2C1_SCL	I2C1_SCL[PTC10]	I2C1_SCL[PTC2]
	PTC3_KW41_I2C1_SDA	I2C1_SDA[PTC11]	I2C1_SDA[PTC3]
BSM	BSM_FRAME	SPI1_PCS0[PTD4]	BSM_FRAM[PTC17]
	BSM_SCK	SPI1_SCK[PTD5]	BSM_CLK[PTC19]
	BSM_DATA	SPI1_SIN[PTD7]	BSM_DATA[PTC18]
GPIO	PTB0_KW41Z	GPIOB0[PTB0]	GPIOB0[PTB0]
	PTB1_KW41Z	GPIOB1[PTB1]	GPIOB1[PTB1]
	PTB2_KW41Z	GPIOB2[PTB2]	GPIOB2[PTB2]
RESET	RST_TGTMCU_b	GPIOB3[PTB3]	RESET_b[PTA2]

4.1.4.1 LEDs

Two red LEDs are populated for the user to program. Both LEDs are connected to GPIO on the KW41Z MCU. See figure below of connection details.
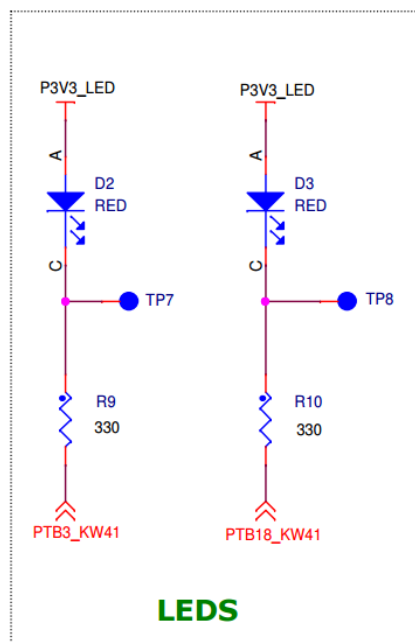
Figure 10: USB-KW41Z user LEDs

4.1.4.2 Push button

A single user push button is provide to interact with the KW41Z. It is connected to PTB2 on the KW41Z. Figure below shows details.
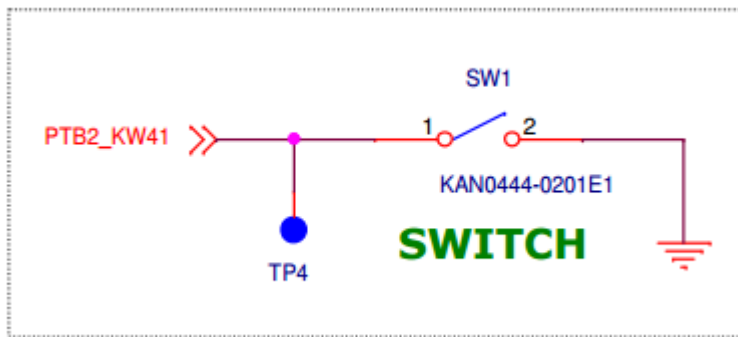
Figure 11: USB-KW41Z user push button

4. References

The following references are available on www.nxp.com/USB-KW41Z:

- USB-KW41Z Design Package

5. Revision history

Rev.	Date	Substantive change(s)
0	10/2016	Initial revision.
1	01/2017	Updated OpenSDA serial and debug chapter (chapter 2.3).

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