VHDL Assignment 3 Report

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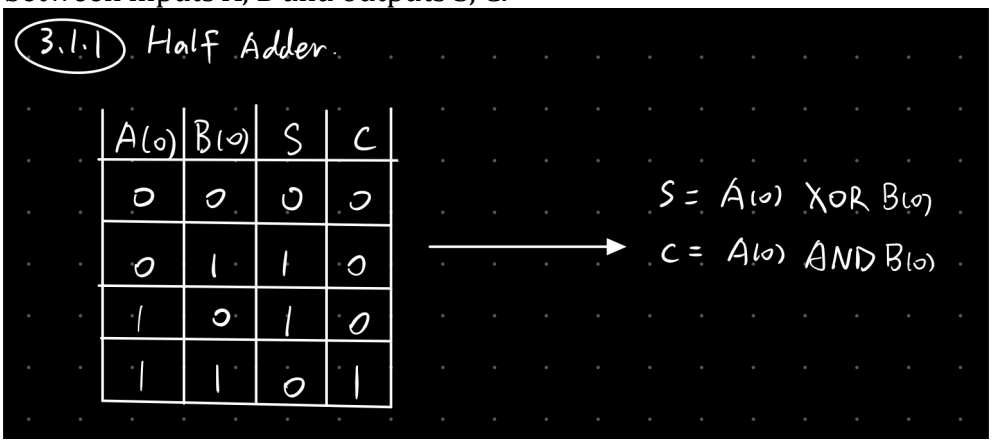
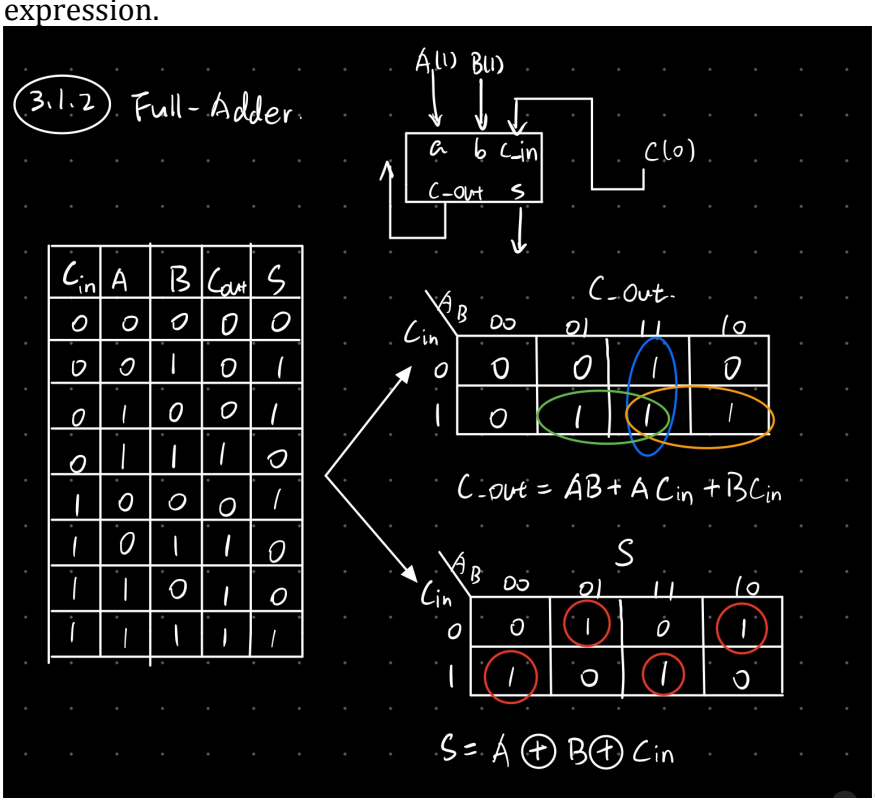
1. Briefly explain your VHDL code implementation of all circuits.
   - Half Adder: Use the truth table below we can obtain the relationship between inputs A, B and outputs S, C.

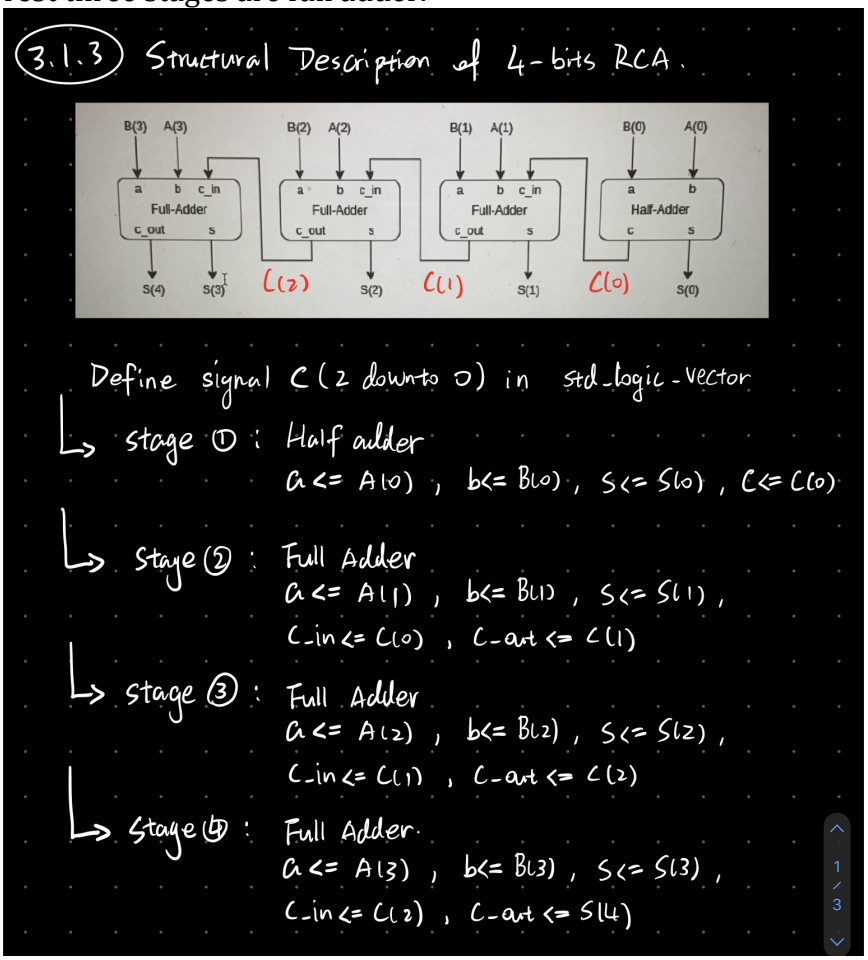


   - Full Adder: First we draw the truth table of inputs (A, B, C_in) and outputs (C_out, S), then we use k-map to obtain the simplified SOP expression.



   - Structural description of 4-bits RCA: The 4-bits RCA was divided into 4 stages as shown in the photo below. The first stage is a half adder and the

rest three stages are full adder.



- Behavioral description of the 4-bits RCA: For the behavioral description, the arithmetic operator "+" was used. In order to use "+" operator, we must first define the two input signals std_logic_vector a and b to be unsigned vector. Secondly, because inputs A and B are 4 bits vectors and output S is 5 bits vectors, an extra bit of 0 is added in front of a and b so that they now have the same number of bits with s.
- Structural Description of a BCD Adder in VHDL: In a one bit BCD adder, the inputs signals are A(3 downto 0) and B(3 downto 0), the output signals are C and S(3 downto 0). Where C is the carry, c=0 when (A+B) is less than or equal to 9, and c=1 when (A+B) is greater than9. Three intermediate signals were defined, (Z) represent the sum of A and B after the 4 bits RCA, (carry) represent the carry in the 4 bits RCA, (carry2) represents the carry in the 2 bits RCA. The circuit is shown below:

One digit BCD adder.

↳ Inputs : A, B : std_logic_vector (3 downto 0)

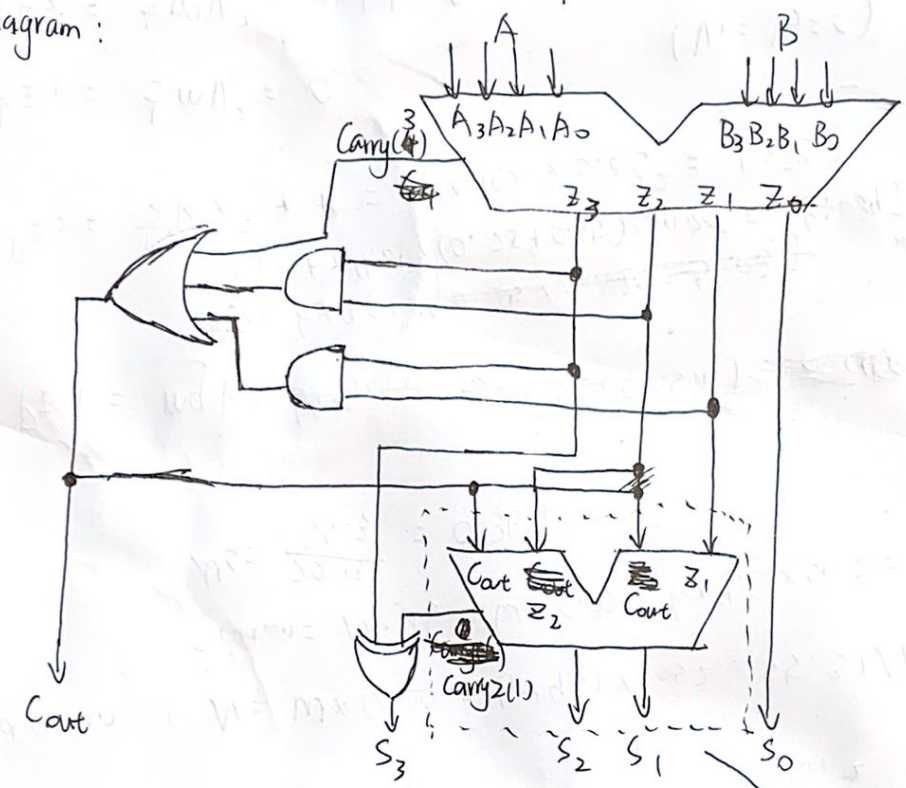
outputs : S : std_logic_vector (3 down to 0)

C : std_logic ⟹ C is the Carry, used to check for overflow

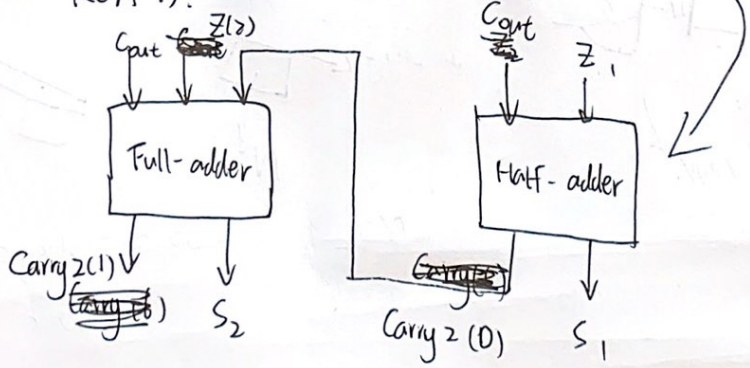
↳ C = 0 when A+B ≤ 9

C = 1 when A+B > 9.

Circuit diagram :

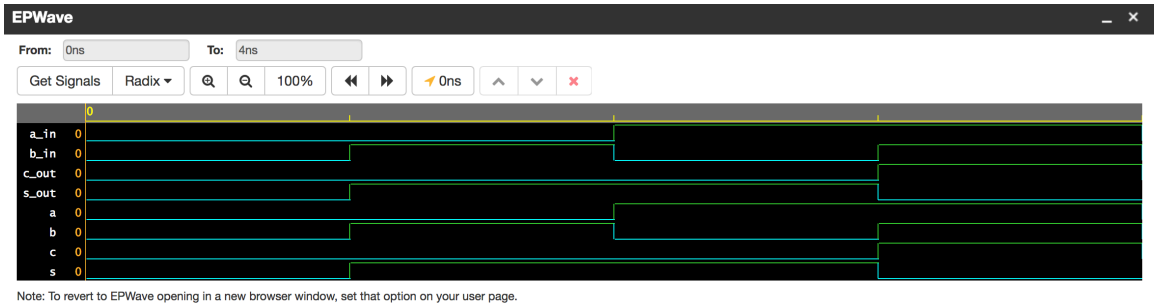


Where the 2-bits RCA is :

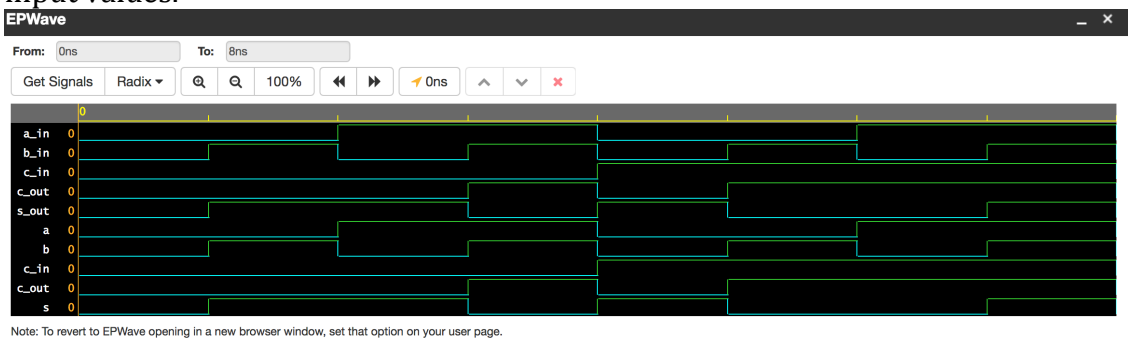


- Behavioral Description of a BCD Adder in VHDL : In the behavioral description, the input signals are A (3 downto 0), B (3 downto 0), and the output signals are S(3 downto 0) and C. Where c represent the carry, c=0 when (A+B) is less than or equal to 9, and c=1 when (A+B) is greater than 9. An intermediate signal z (4 downto 0) was defined, z represent the binary sum of (A+B), and since z has one more bits than A and B, so Z can handle the overflow. Another intermediate signal p (4 downto 0) was defined, where (P = Z+6), we use P instead of Z to represent (A+B) when (A+B) is greater than 9. Now in this case, the output s <= z(3 downto 0) when (c=0), else p(3 downto 0) when (c=1).

2. Show representative simulation plots of the half-adder circuit for all possible input values.

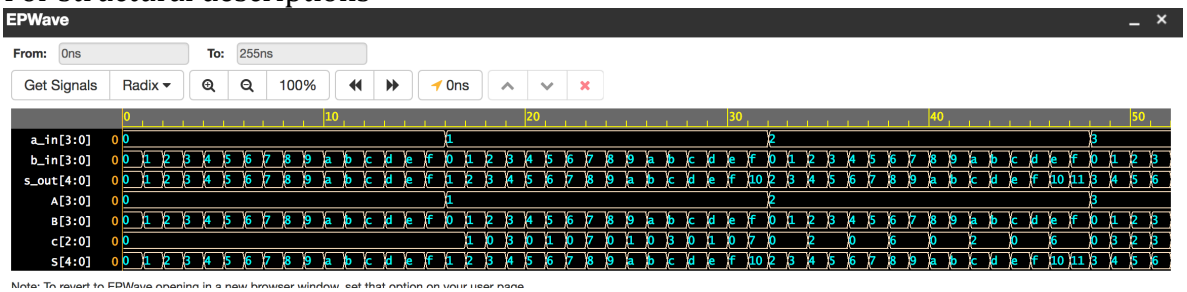


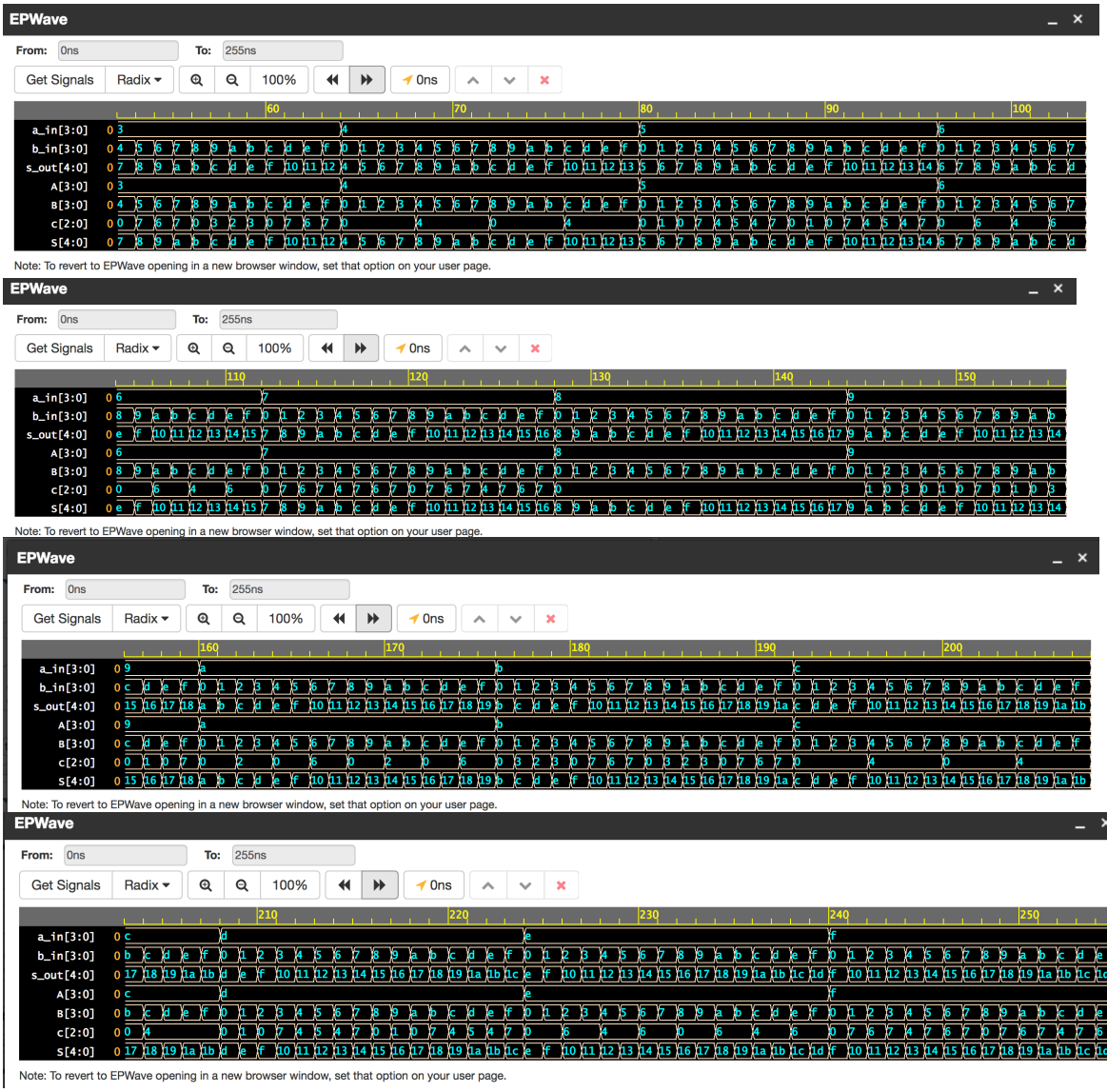
3. Show representative simulation plots of the full-adder circuit for all possible input values.



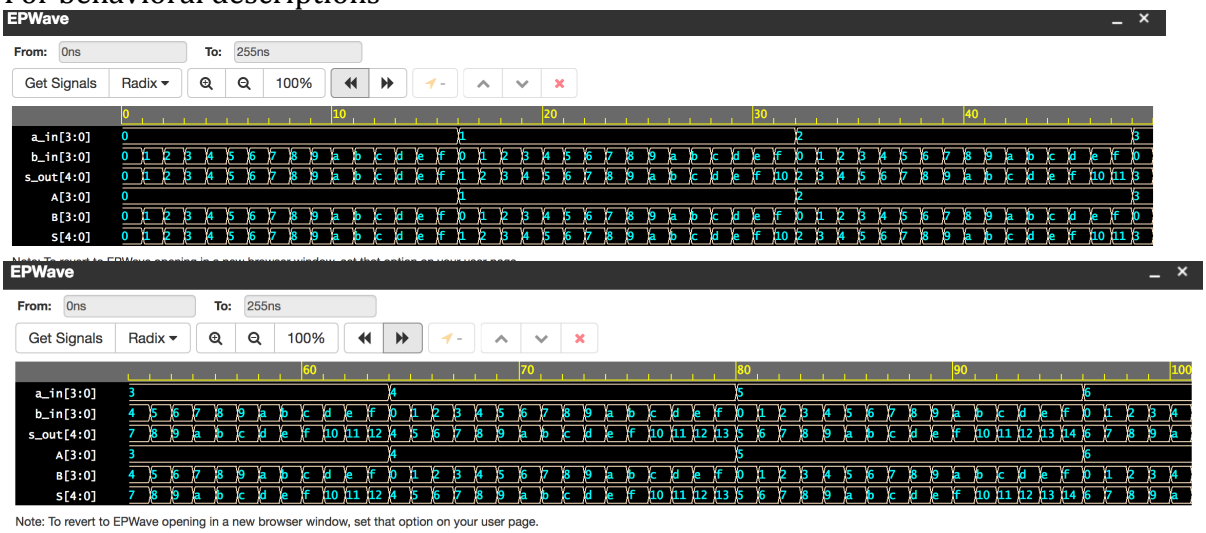
4. Show representative simulation plots of both behavioral and structural descriptions of the 4-bit RCA for all possible input values.

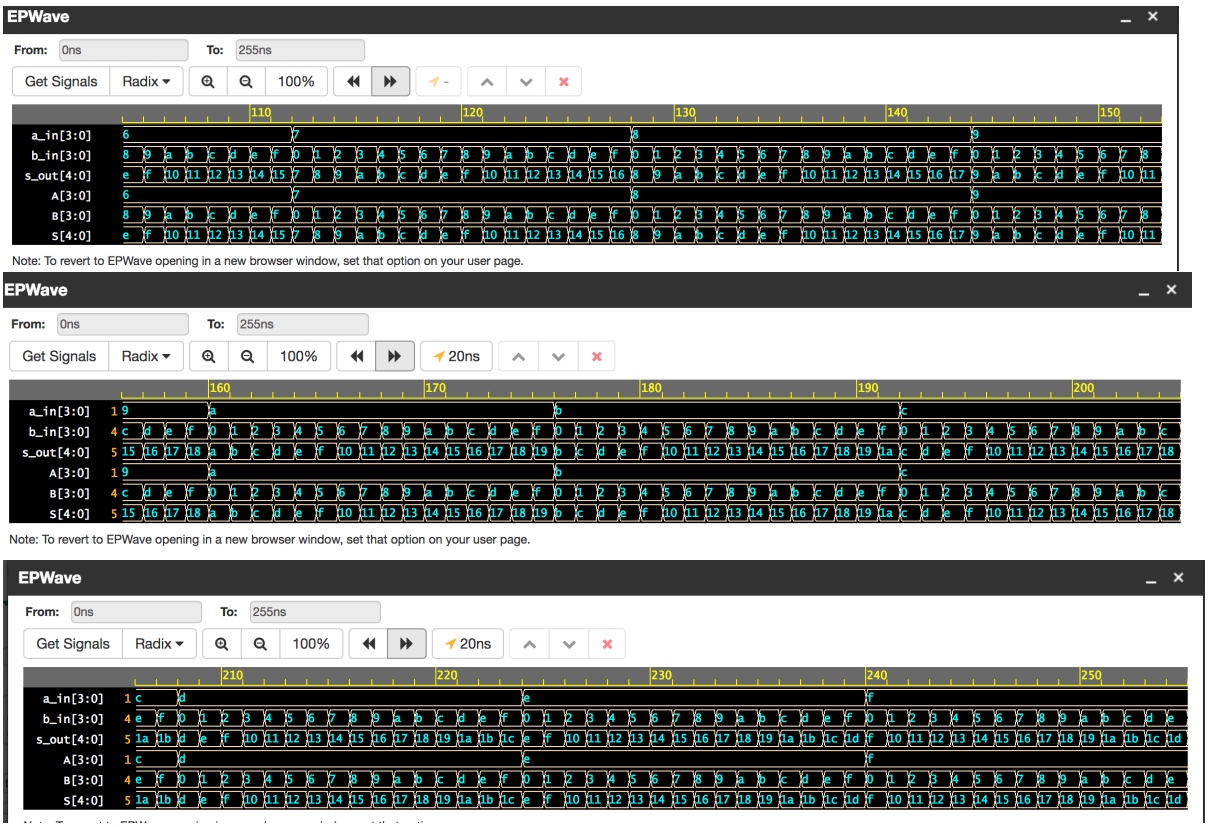
- For structural descriptions





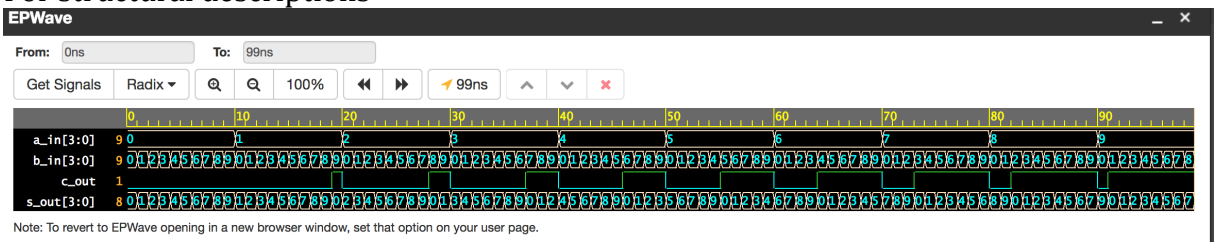
➢ For behavioral descriptions



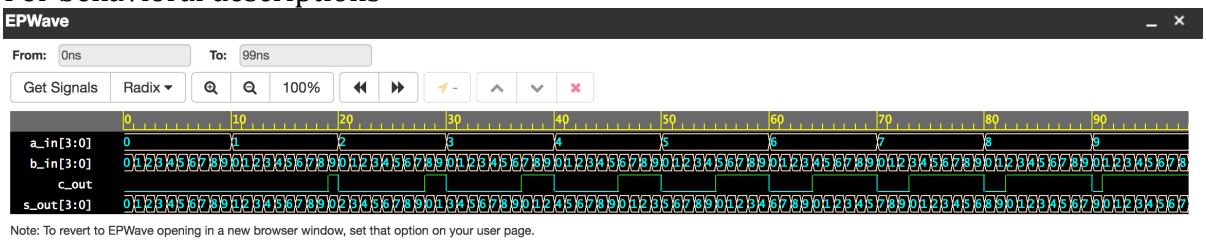


5. Show representative simulation plots of both behavioral and structural descriptions of the one-digit BCD adder circuit for all possible input values.

- For structural descriptions



- For behavioral descriptions



6. Timing analysis of one digit BCD adder

- According to the Timing analysis log file, the delay of the critical paths(from A(3) to S(3)) for both structural description and behavioral description for BCD adder is 15.000ns. (as shown in the two diagrams below)
- Assuming that an additional delay of 10 ns can be added to the critical path due to wiring, and we want a 5ns positive slack, so 10ns + 5ns =15ns, which means we want a 15ns slack displayed in the Timing analysis log file. So the command should be :

set_max_delay -from [get_ports A[*]] -to [get_ports S[*]] 20

set_max_delay -from [get_ports B[*]] -to [get_ports S[*]] 15

Log Share

```
# Info:                  CTE Path Report
# Info: Critical path #1, (path slack = 15.000):, Logic Levels = 3
# Info: SOURCE CLOCK: name: <not found>  Path is min/max delay constrained
# Info: NAME               GATE       DELAY    ARRIVAL DIR  FANOUT LEVEL
# Info: A(3)             (port)                 0.000   dn
# Info: A(3)             (net)        0.000                 1     0
# Info: A_ibuf(3)/I      IBUF                   0.000   dn
# Info: A_ibuf(3)/O      IBUF         1.298     1.298   dn
# Info: A_int(3)         (net)        0.354                 4     1
# Info: ix47514z39522/I3 LUT5                   1.652   dn
# Info: ix47514z39522/O  LUT5         0.124     1.776   up
# Info: nx47514z1        (net)        0.333                 1     2
# Info: S_obuf(3)/I      OBUF                   2.109   up
# Info: S_obuf(3)/O      OBUF         2.891     5.000   up
# Info: S(3)             (net)        0.000                 0     3
# Info: S(3)             (port)                 5.000   up
# Info:                 Minmax delay constraint:     20.000
# Info:                 Source clock delay:       -    0.000
# Info:                 Dest clock delay:         +    0.000
# Info:                                          -----------
# Info:                 Edge separation:             20.000
# Info:                 Setup constraint:         -    0.000
# Info:                                          -----------
# Info:                 Data required time:          20.000
# Info:                 Data arrival time:        -    5.000   ( 86.26% cell delay, 13.74% net delay )
# Info:                                          -----------
# Info:                 Slack:                       15.000
# Info: End CTE Analysis ..... CPU Time Used: 0 sec.
```


```
Info: -- CTE report timing..
Info:                  CTE Path Report
Info: Critical path #1, (path slack = 15.000):, Logic Levels = 3
Info: SOURCE CLOCK: name: <not found>  Path is min/max delay constrained
Info: NAME               GATE       DELAY    ARRIVAL DIR  FANOUT LEVEL
Info: A(3)             (port)                 0.000   dn
Info: A(3)             (net)        0.000                 1     0
Info: A_ibuf(3)/I      IBUF                   0.000   dn
Info: A_ibuf(3)/O      IBUF         1.298     1.298   dn
Info: A_int(3)         (net)        0.354                 4     1
Info: ix47514z39522/I3 LUT5                   1.652   dn
Info: ix47514z39522/O  LUT5         0.124     1.776   up
Info: nx47514z1        (net)        0.333                 1     2
Info: S_obuf(3)/I      OBUF                   2.109   up
Info: S_obuf(3)/O      OBUF         2.891     5.000   up
Info: S(3)             (net)        0.000                 0     3
Info: S(3)             (port)                 5.000   up
Info:                 Minmax delay constraint:     20.000
Info:                 Source clock delay:       -    0.000
Info:                 Dest clock delay:         +    0.000
Info:                                          -----------
Info:                 Edge separation:             20.000
Info:                 Setup constraint:         -    0.000
Info:                                          -----------
Info:                 Data required time:          20.000
Info:                 Data arrival time:        -    5.000   ( 86.26% cell delay, 13.74% net delay )
Info:                                          -----------
Info:                 Slack:                       15.000
Info: End CTE Analysis ..... CPU Time Used: 0 sec.
```


7.

	RCA		One-digit BCD adder	
	Structural	Behavioral	Structural	Behavioral
Logic Utilization (in LUTs)	Used: 6 Avail: 63400	Used: 6 Avail: 63400	Used: 8 Avail: 63400	Used: 8 Avail: 63400
Total pins	Used: 13 Avail: 210	Used: 13 Avail: 210	Used: 13 Avail: 210	Used: 13 Avail: 210