VHDL Assignment 5 Report

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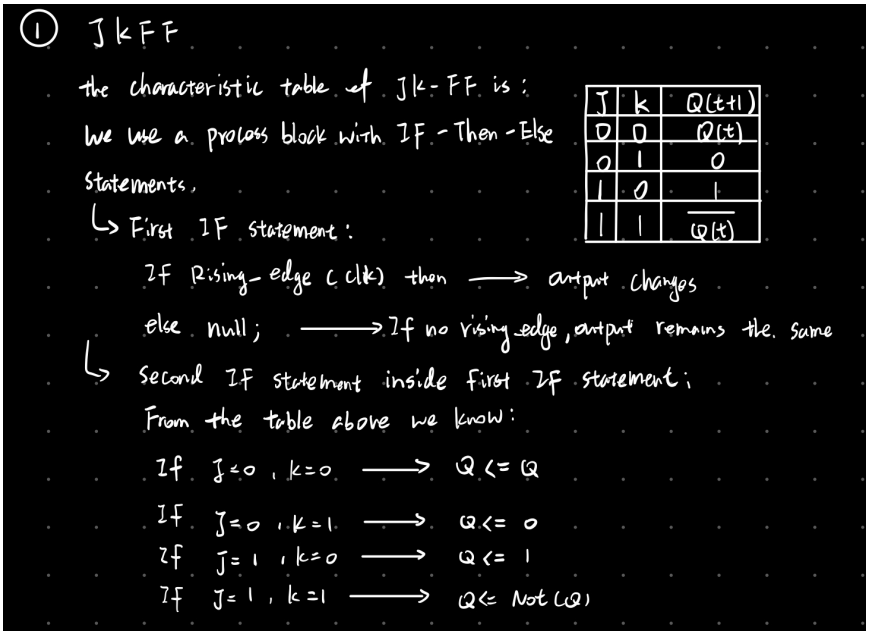
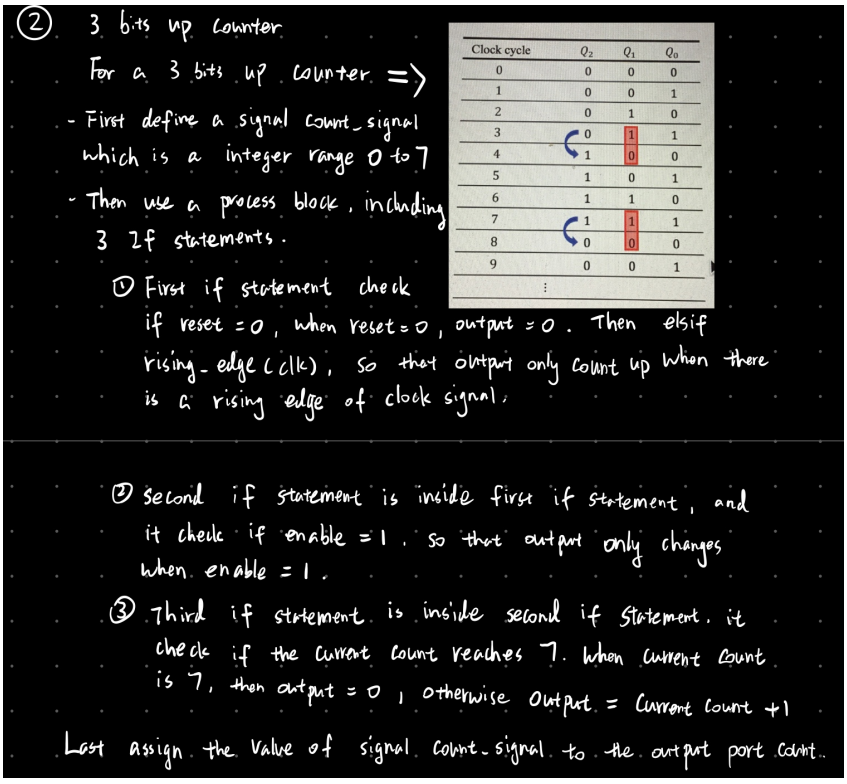
1. Briefly explain your VHDL code implementation of all circuits.
   - For the JKFF



   - For the counter



- For the clock divider

③ clock divider

Because 10Hz clock frequency means clock period is 0.1 s, so if we want to assert an enable signal every 1 second, we need clock divider of N=10, which include a 4 bits 9 -> 0 down counter.

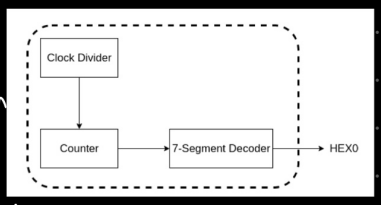
First define a signal represent the output value of the down counter Then implement the 9 -> 0 down counter, which is similar to the up counter above, differences are when reset = 0, count = 9 and if current count = 0, then next count = 9.

At last, the output of the clock divider is the NOR of the output bits of down counter.

- For the 3-bit Up-Counter that Counts in Increments of 1 Second

④ Wrapper

As the circuit shown, this wrapper circuit is the combination of previous circuits.



First define the intermediate signals:

For clock divider:
- signal en_out → output of clock divider
- down_counter → output of the down counter

For counter:
- signal count (2 downto 0) → output of the counter
- signal four_bit_count (3 downto 0) → used to change count to a 4 bits std_logic_vector.

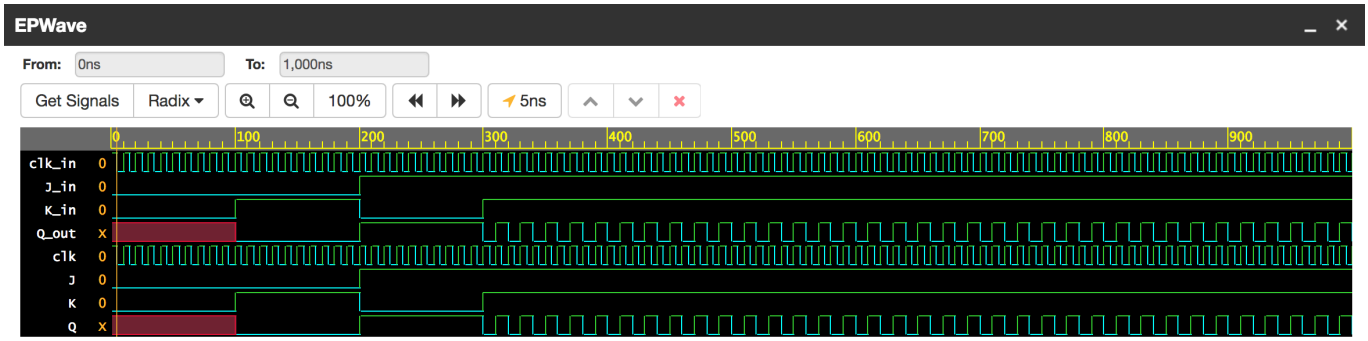
Implementation of circuit:

① First implement the clock divider
Same steps as above

② Then take the output en_out of the clock divider as the enable input of the counter, and implement counter

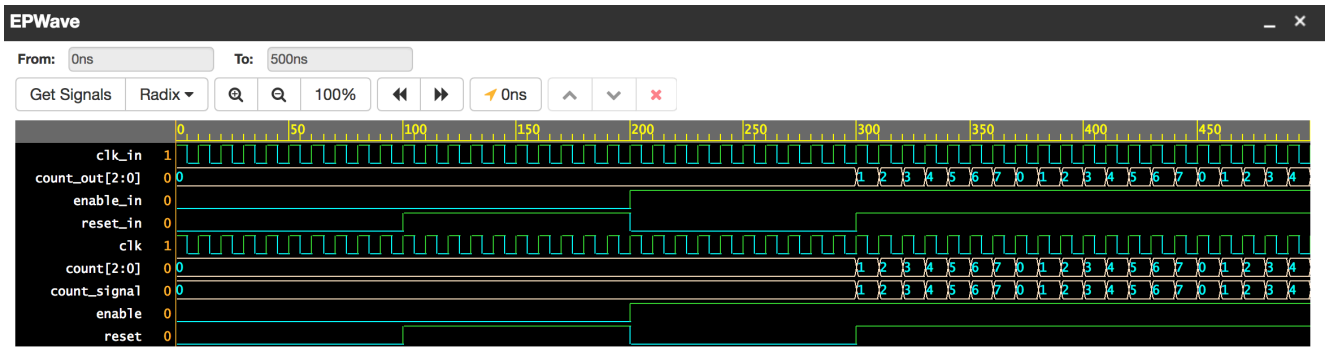
③ Because output of counter is 3 bits, but input to 7-segment decoder is 4 bits, so we add a "0" in front of the output of counter. Then we can implement 7-segment decoder.

2. Provide waveforms for each of the individual circuits (each section) and for the 3-bit up-counter.
   - For the JKFF

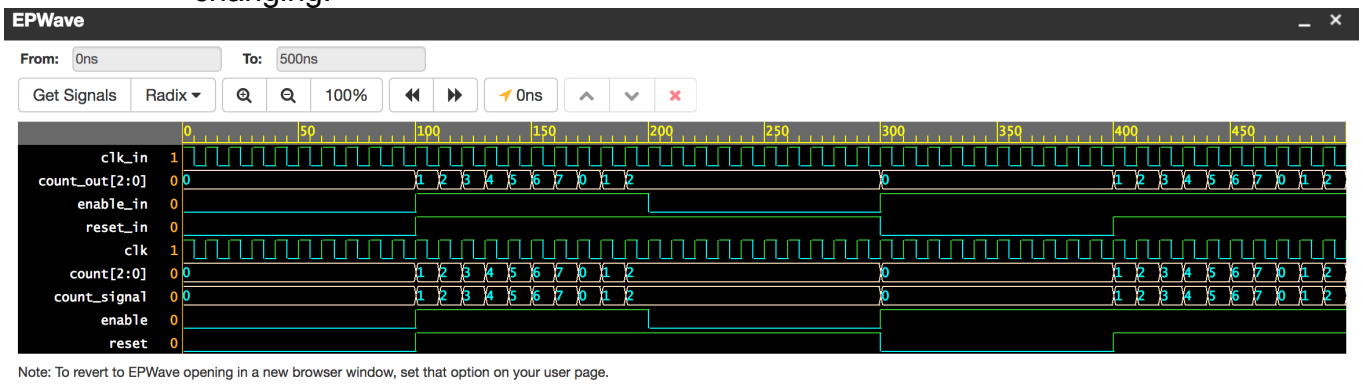


In the diagram, the output Q between t=0 and t=100 ns is unknown, this is because at this time J=0 and K=0, so Q(t+1) = Q(t), Q will maintain it's previous value. However in this case, we have no previous value of Q, so Q is unknown between t=0 and t=100 ns.

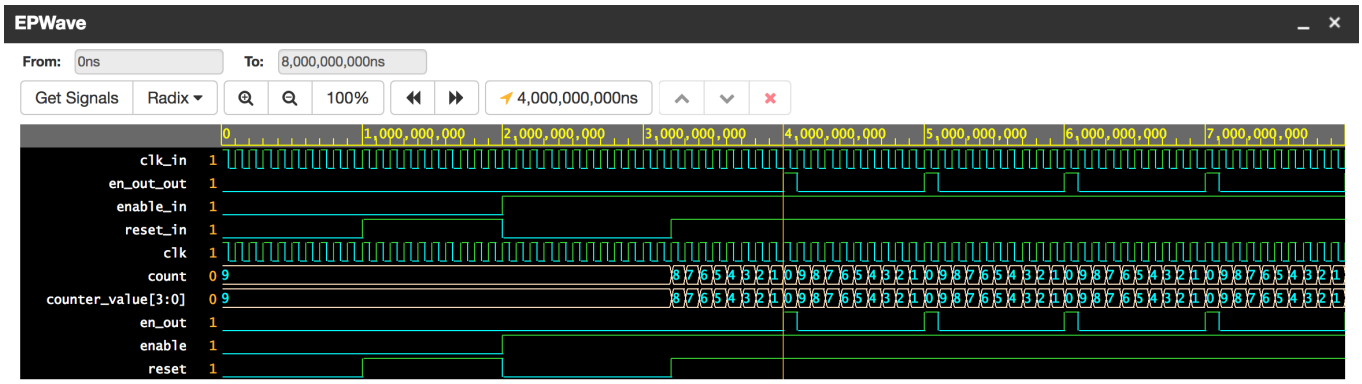
   - For the counter



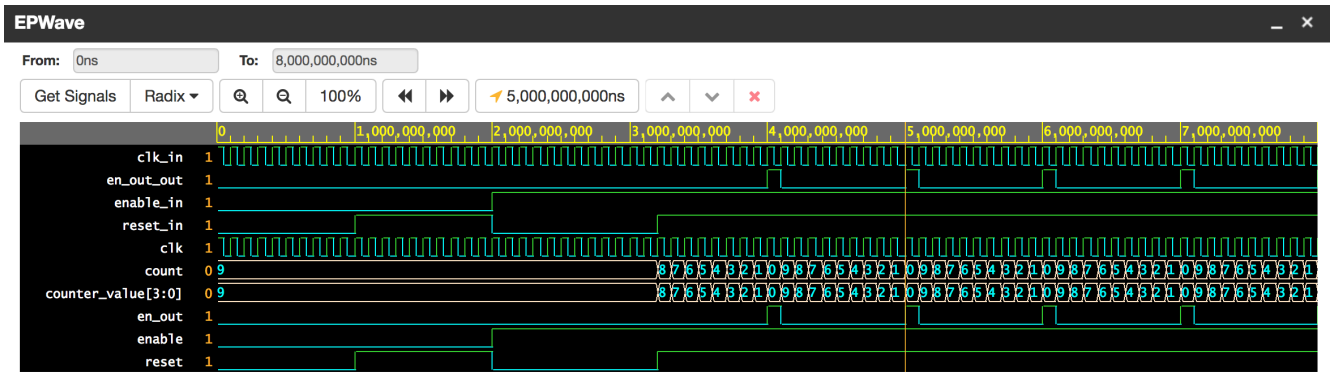
The below EPwave diagram is for testing the enable signal, I added a part with enable=0 during the counting to see if the output stops changing.



   - For the clock divider



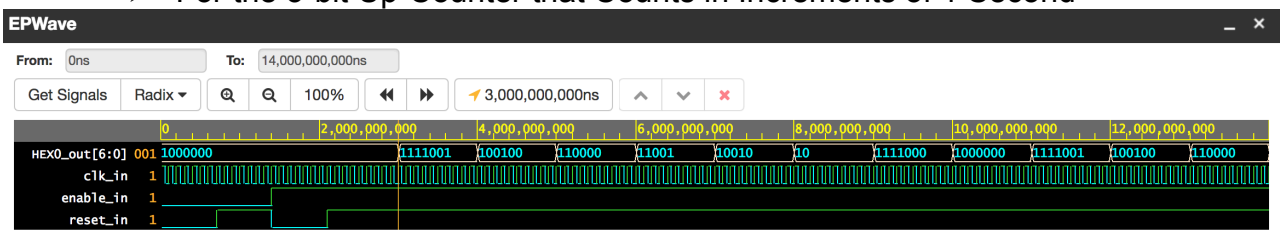
Note: To revert to EPWave opening in a new browser window, set that option on your user page.



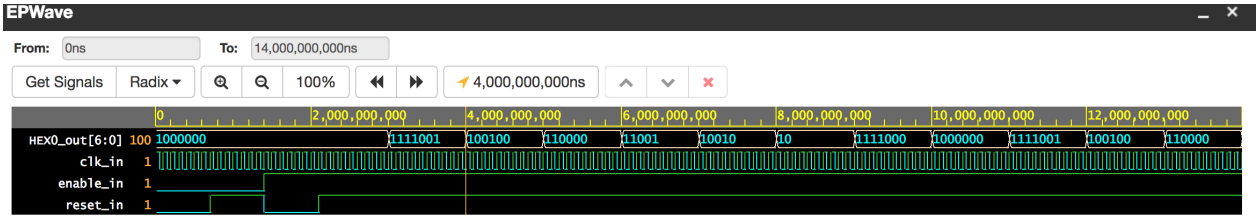
Note: To revert to EPWave opening in a new browser window, set that option on your user page.

The above two diagrams show the time interval between two en_out=1 signal is 1 second.

- For the 3-bit Up-Counter that Counts in Increments of 1 Second

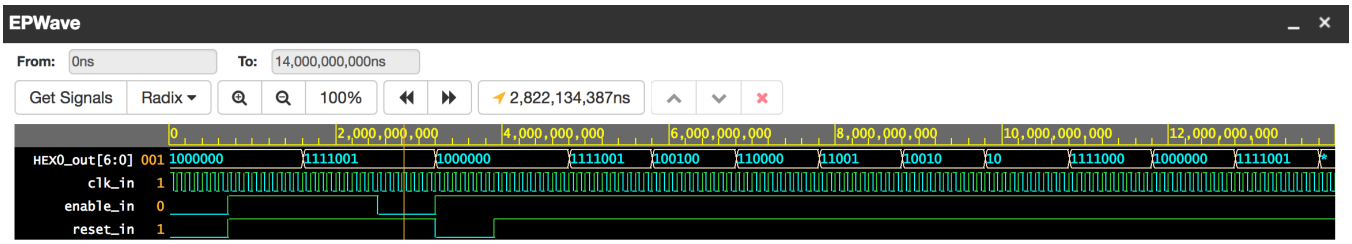


Note: To revert to EPWave opening in a new browser window, set that option on your user page.



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

The above two EPwaves show that the counter increments every 1 second, and counts from 0 to 7 and wraps around to 0. The diagram below shows that when enable=0, reset=1, the output stops changing and when enable=1, reset=0, the counter reset to 0.



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

3. Perform timing analysis of the 3-bit up counter and find the critical path(s) of the circuit. What is the delay of the critical path(s)?
   - Timing analysis screenshot

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# Info: -- POST-SYNTHESIS TIMING REPORTS ARE ESTIMATES AND SHOULD NOT BE RELIED ON TO MAKE QoR DECISIONS. For accurate timing information
# Info: -- Device: Xilinx - ARTIX-7 : 7A100TCSG324 : 1
# Info: -- CTE report timing..
# Info:                   CTE Path Report
# Info: Critical path #1, (path slack = 18.496):, Logic Levels = 1
# Info: SOURCE CLOCK: name: clk period: 20.000000
# Info:      Times are relative to the 1st rising edge
# Info:   DEST CLOCK: name: clk period: 20.000000
# Info:      Times are relative to the 2nd rising edge
# Info: NAME                                        GATE      DELAY    ARRIVAL DIR  FANOUT LEVEL
# Info: reg_down_counter(0)/C                      FDPE                0.000   up
# Info: reg_down_counter(0)/Q                      FDPE       0.456    0.456   up
# Info: down_counter_value(0)                      (net)      0.378                5     0
# Info: ix31013z1315/I3                            LUT4                0.834   up
# Info: ix31013z1315/O                             LUT4       0.124    0.958   dn
# Info: nx31013z1                                  (net)      0.341                3     1
# Info: modgen_counter_four_bits_count_reg_q(0)/CE FDCE                1.299   dn
# Info:                 Initial edge separation:     20.000
# Info:                 Source clock delay:      -    1.435
# Info:                 Dest clock delay:        +    1.435
# Info:                                          -----------
# Info:                 Edge separation:             20.000
# Info:                 Setup constraint:        -    0.205
# Info:                                          -----------
# Info:                 Data required time:          19.795
# Info:                 Data arrival time:       -    1.299   ( 44.65% cell delay, 55.35% net delay )
# Info:                                          -----------
# Info:                 Slack:                       18.496
# Info: End CTE Analysis ..... CPU Time Used: 0 sec.
# Info: //
```

   - The critical path is from reg_down_counter(0)/C to modgen_counter_four_bits_count_reg_q(0)/CE
   - Critical path slack =18.496, so delay = 20 -18.496 = 1.504

4. Report the number of pins and logic modules used to fit your 4-bit comparator design on the FPGA board

	3-bit up counter
Logic Utilization (in LUTs)	Used: 16 Avail: 63400
Total pins	Used: 10 Avail: 210