TEF6614

Advanced tuner on main-board IC

Rev. 3 — 11 October 2011 Product data sheet

1. General description

The TEF6614 is an AM/FM radio including Phase-Locked Loop (PLL) tuning system. The system is designed in such a way, that it can be used as a world-wide tuner covering common FM and AM bands for radio reception. All functions are controlled by the I^{2}C-bus. Besides the basic feature set it provides a good weak signal processing function and a dynamic bandwidth control at FM reception.

It includes a newly developed demodulator for data reception of Radio Data System (RDS) and Radio Broadcast Data System (RBDS) transmissions.

2. Features and benefits

- Backwards compatible with TEF6606; equal footprint, application and performance
- Fully integrated RDS/RBDS demodulator with improved performance
- RDS demodulator data output via I^{2}C-bus; 32-bit buffer for reduced read out
- RDS data available signalled by I^{2}C-bus bit (polling)
- FM tuner for Japan, Europe, US and OIRT reception
- AM tuner for Long Wave (LW), Medium Wave (MW) and Short Wave (SW) reception
- Integrated AM Radio Frequency (RF) selectivity
- Integrated PLL tuning system; controlled via I^{2}C-bus including automatic low/high side Local Oscillator (LO) injection
- Fully integrated LO
- No alignment needed
- Very easy application on the main board
- No critical RF components
- Fully integrated Intermediate Frequency (IF) filters and FM stereo decoder
- Fully integrated FM noise blanker
- Fully integrated AM audio noise blanker
- Field strength (LEVEL), multipath [Wideband AM (WAM)], noise [UltraSonic Noise (USN)] and deviation dependent stereo blend
- Field strength (LEVEL), multipath (WAM), noise (USN) and deviation dependent High-Cut Control (HCC)
- Field strength (LEVEL), multipath (WAM) and noise (USN) dependent soft mute
- Adjacent channel and deviation dependent IF bandwidth control [Precision Adjacent Channel Suppression (PACS)]
- Single power supply
- Qualified in accordance with AEC-Q100

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	on pins V_{CC1} and V_{CC2}	8	8.5	9	V
I_{CC}	supply current	into pins V_{CC1}, V_{CC2} and VREGSUP				
		FM	90	120	140	mA
		AM	100	134	150	mA
FM path						
f_{RF}	RF frequency	FM tuning range	65	-	108	MHz
$V_{i(sens)}$	input sensitivity voltage	(S+N)/N = 26 dB; including weak signal handling	-	5	-	dBμV
		for 50 % block quality RDS reception; Δf_{RDS} = 2 kHz; AF = stereo; Δf = 22.5 kHz	-	17	-	dBμV
		for 95 % block quality RDS reception; Δf_{RDS} = 2 kHz; AF = stereo; Δf = 22.5 kHz	-	20	-	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 1 mV; Δf = 22.5 kHz	55	60	-	dB
THD	total harmonic distortion	mono; Δf = 75 kHz; $V_{i(RF)}$ = 1 mV	-	0.4	0.8	%
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	50	60	-	dB
α_{cs}	channel separation	$V_{i(RF)}$ = 1 mV; data byte Fh bits CHSEP[2:0] = 100	26	40	-	dB
AM path						
f_{RF}	RF frequency	AM (LW) tuning range	144	-	288	kHz
		AM (MW) tuning range	522	-	1710	kHz
		AM (SW) tuning range	2.94	-	18.135	MHz
$V_{i(sens)}$	input sensitivity voltage	S/N = 26 dB; data byte 3h bits DEMP[1:0] = 10				
		MW	-	34	-	dBμV
		LW	-	40	-	dBμV
		SW	-	35	-	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 10 mV	50	56	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 1 mV; m = 80 %	-	0.7	1	%
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	45	55	-	dB

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6614T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

5. Block diagram

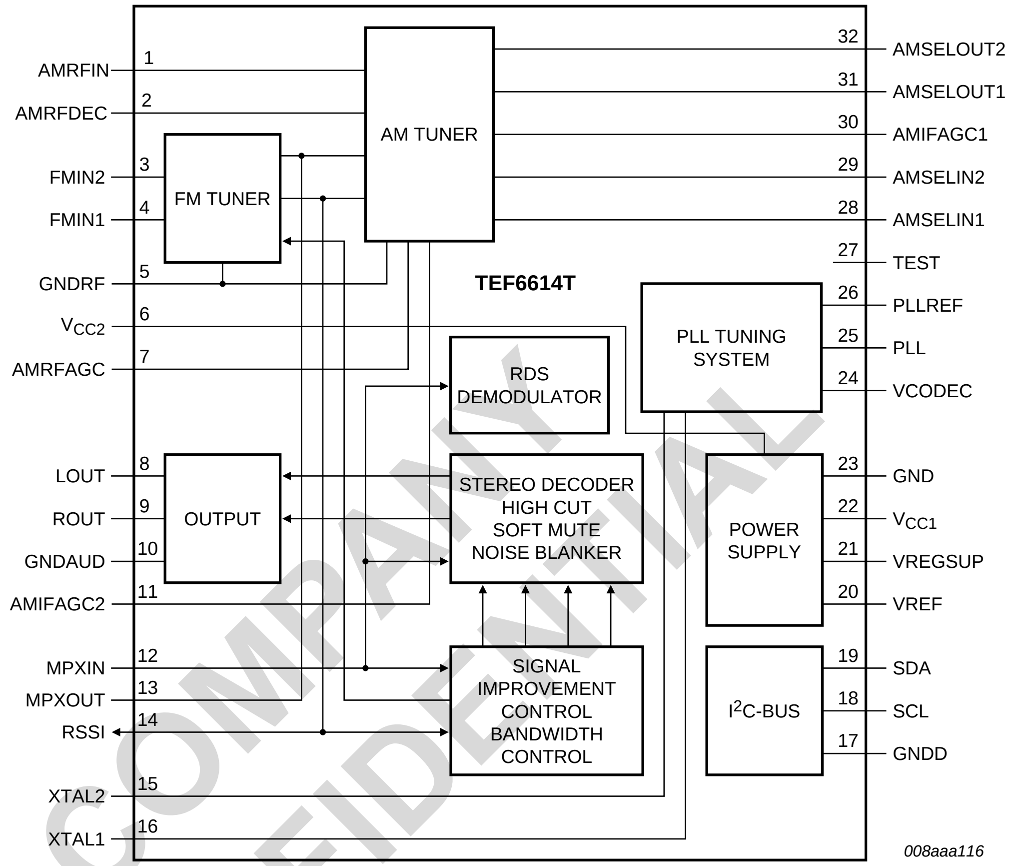


Fig 1. Block diagram of TEF6614T

6. Pinning information

6.1 Pinning

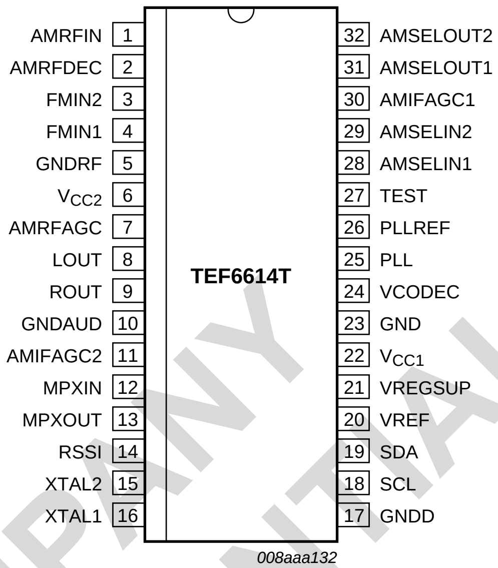


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
AMRFIN	1	AM RF single-ended input
AMRFDEC	2	AM RF decoupling
FMIN2	3	FM RF differential input 2
FMIN1	4	FM RF differential input 1
GNDRF	5	RF ground
V_{CC2}	6	supply voltage 2
AMRFAGC	7	AM RF Automatic Gain Control (AGC)
LOUT	8	audio left output
ROUT	9	audio right output
GNDAUD	10	audio ground
AMIFAGC2	11	AM IF AGC 2
MPXIN	12	FM Multiplex (MPX) and AM audio input to stereo decoder
MPXOUT	13	FM MPX and AM audio output from tuner part
RSSI	14	Received Signal Strength Indication (RSSI)
XTAL2	15	4 MHz crystal oscillator pin 2
XTAL1	16	4 MHz crystal oscillator pin 1
GNDD	17	digital ground
SCL	18	I^2C-bus clock input

Table 3. Pin description *...continued*

Symbol	Pin	Description
SDA	19	I^2C-bus data input and output
VREF	20	reference voltage decoupling
VREGSUP	21	supply voltage internal voltage regulators
V_{CC1}	22	supply voltage 1
GND	23	ground
VCODEC	24	decoupling for Voltage-Controlled Oscillator (VCO) supply voltage
PLL	25	PLL tuning voltage
PLLREF	26	PLL reference voltage
TEST	27	test pin with optional general use (open-drain output); in normal operation, the pin is left open
AMSELIN1	28	AM selectivity input 1
AMSELIN2	29	AM selectivity input 2
AMIFAGC1	30	AM IF AGC 1
AMSELOUT1	31	AM selectivity output 1
AMSELOUT2	32	AM selectivity output 2

7. Functional description

7.1 RDS demodulator

The TEF6614 includes a newly developed full-digital RDS function. Very good RDS sensitivity is achieved by optimized digital filtering and linear signal processing. The MPX signal is converted from analog to digital and then filtered for selection of the 57 kHz RDS signal and data shaping. Synchronous 57 kHz demodulation is realized by means of Costas loop phase control followed by synchronization to the bit phase for sampling of the RDS data.

The RDS demodulator data is provided by the I^2C-bus for further data processing in a microcontroller. For reduced data output rate a 32-bit buffer is included.

Availability of new group data is signalled by read bit RDAV (read data byte 0h or read data byte 5h).

To avoid loss of RDS demodulator data the I^2C-bus reading shall be done at least every 26 ms.

7.2 FM tuner

The RF input signal is mixed to a low IF with inherent image suppression. The IF signal is filtered and demodulated. The complete signal path is fully integrated.

7.3 AM tuner

The RF signal is filtered and mixed to a low IF with inherent image suppression. The IF signals are filtered and demodulated. The signal path is highly integrated.

7.4 PLL tuning system

The PLL tuning system includes a fully integrated VCO. To avoid problems with unwanted signals on image side, the receiver controls automatically high-side or low-side injection.

7.5 Signal dependent FM IF bandwidth control

The bandwidth of the FM IF filter will be controlled by an adjacent channel detector and a deviation detector to optimize the reception.

7.6 FM stereo decoder

The MPX signal from the FM tuner is translated by the stereo decoder into a left and right audio channel. Good channel separation is achieved without alignment.

7.7 Weak signal processing and noise blanker

The reception quality of the station received is measured by a combination of detectors: field strength (LEVEL), multipath (WAM) and noise (USN). The audio processing functions soft mute, HCC and stereo blend are controlled accordingly to maintain the best possible audio quality in case of poor signal conditions. Audio disturbances like e.g. ignition noise are suppressed by the noise blanker circuit, using USN detection on MPX and spike detection on the level signal.

7.8 I^2C-bus transceiver

The IC can be controlled by means of the I^2C-bus including fast mode.

8. I^2C-bus protocol

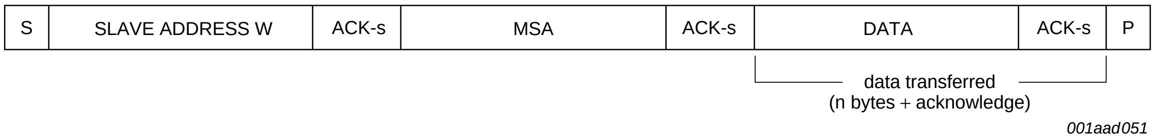


Fig 3. Write mode

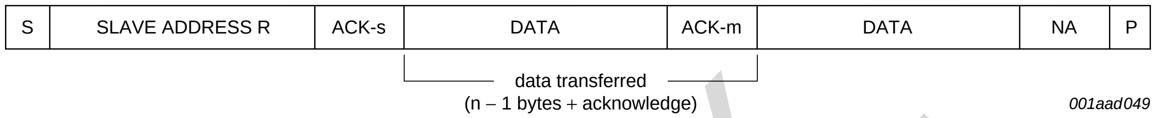


Fig 4. Read mode

Table 4. Description of I^2C-bus format

Code	Description
S	START condition
SLAVE ADDRESS W	1100 0000b
SLAVE ADDRESS R	1100 0001b
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge
MSA	mode and subaddress byte
DATA	data byte
P	STOP condition

8.1 Read mode

Table 5. Read register overview

Data byte	Name	Reference
0h	STATUS	Section 8.1.1
1h	LEVEL	Section 8.1.2
2h	USN_WAM	Section 8.1.3
3h	IFCOUNTER	Section 8.1.4
4h	ID	Section 8.1.5
5h	RDS_STATUS	Section 8.1.6
6h	RDS_DAT3	Section 8.1.7
7h	RDS_DAT2	Section 8.1.8
8h	RDS_DAT1	Section 8.1.9
9h	RDS_DAT0	Section 8.1.10
Ah	RDS_DATEE	Section 8.1.11

8.1.1 Read mode: data byte STATUS

Table 6. STATUS - data byte 0h bit allocation

7	6	5	4	3	2	1	0
QRS1	QRS0	POR	STIN	-	RDAV	TAS1	TAS0

Table 7. STATUS - data byte 0h bit description

Bit	Symbol	Description
7 and 6	QRS[1:0]	quality read status[1]
		00 = no quality data available (tuning is in progress or quality data is settling)
		01 = quality data (LEVEL, USN and WAM) available; for IF counter check the IFCS status
		10 = AF update quality data available of LEVEL, USN, WAM and IF counter
		11 = not used
5	POR	power-on reset indicator
		0 = normal operation
		1 = power on or power dip detected; I^{2}C-bus settings are lost
4	STIN	stereo indicator
		0 = no pilot detected
		1 = stereo pilot detected
3	-	not used
2	RDAV	RDS new data available
		0 = no data available
		1 = RDS new data available (via read data bytes 5h to Fh)
1 and 0	TAS[1:0]	tuning action state
		00 = tuning not active; not muted
		01 = muting in progress
		10 = tuning in progress
		11 = tuning ready and muted

[1] When PLL tuning is ready the quality detectors are reset for fastest result. In FM mode the first reliable quality result of LEVEL, USN and WAM is available from 1 ms after reset. In AM mode the first level result is available from 1 ms, gradually changing from peak LEVEL towards average LEVEL realizing the maximum attenuation of AM modulation influence from 32 ms. The quality result of an AF update tuning is stored and can be read at any time later.

8.1.2 Read mode: data byte LEVEL

Table 8. LEVEL - data byte 1h bit allocation

7	6	5	4	3	2	1	0
LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 9. LEVEL - data byte 1h bit description

Bit	Symbol	Description
7 to 0	LEV[7:0]	level detector (RSSI) output signal via fast level detector timing
		0 to 255 = 0.25 V to 4.25 V

8.1.3 Read mode: data byte USN_WAM

Table 10. USN_WAM - data byte 2h bit allocation

7	6	5	4	3	2	1	0
USN3	USN2	USN1	USN0	WAM3	WAM2	WAM1	WAM0

Table 11. USN_WAM - data byte 2h bit description

Bit	Symbol	Description
7 to 4	USN[3:0]	FM ultrasonic noise
		0 to 15 = 0 % to 100 % equivalent FM modulation at 100 kHz ultrasonic noise content (USN)
3 to 0	WAM[3:0]	FM wideband AM (multipath)
		0 to 15 = 0 % to 100 % AM modulation at 20 kHz wideband AM content (WAM)

8.1.4 Read mode: data byte IFCOUNTER

Table 12. IFCOUNTER - data byte 3h bit allocation

7	6	5	4	3	2	1	0
IFCS1	IFCS0	IFCN	IFC4	IFC3	IFC2	IFC1	IFC0

Table 13. IFCOUNTER - data byte 3h bit description

Bit	Symbol	Description
7 and 6	IFCS[1:0]	IF counter status[1]
		00 = no first counter result available
		01 = first counter result available from 2 ms count time
		10 = counter result available from 8 ms count time
		11 = counter result available from 32 ms count time
5	IFCN	IF count result negative
		0 = positive RF frequency difference
		1 = negative RF frequency difference
4 to 0	IFC[4:0]	IF counter result; see Table 14

[1] When PLL tuning is ready the IF counter and other quality detectors are reset for fastest result. The first IF counter result is available from 2 ms after reset. Further results are available from 8 ms and 32 ms after reset, reducing the influence of FM modulation on the counter result. Later counter results are available at a count time of 32 ms.

Table 14. IF counter result

IFC4	IFC3	IFC2	IFC1	IFC0	Frequency difference	
					FM	AM
0	0	0	0	0	0 kHz to 5 kHz	0 kHz to 0.5 kHz
0	0	0	0	1	5 kHz to 10 kHz	0.5 kHz to 1 kHz
0	0	0	1	0	10 kHz to 15 kHz	1 kHz to 1.5 kHz
0	0	0	1	1	15 kHz to 20 kHz	1.5 kHz to 2 kHz
0	0	1	0	0	20 kHz to 25 kHz	2 kHz to 2.5 kHz

Table 14. IF counter result *...continued*

IFC4	IFC3	IFC2	IFC1	IFC0	Frequency difference	
					FM	AM
:	:	:	:	:	:	:
1	1	1	1	0	150 kHz to 155 kHz	15 kHz to 15.5 kHz
1	1	1	1	1	> 155 kHz	> 15.5 kHz

8.1.5 Read mode: data byte ID

Table 15. ID - data byte 4h bit allocation

7	6	5	4	3	2	1	0
TINJ	IFBW2	IFBW1	IFBW0	-	ID2	ID1	ID0

Table 16. ID - data byte 4h bit description

Bit	Symbol	Description
7	TINJ	LO injection
		0 = low injection LO
		1 = high injection LO
6 to 4	IFBW[2:0]	IF bandwidth information
		000 to 111 = narrow to wide FM IF filter bandwidth
3	-	not used
2 to 0	ID[2:0]	device type identification 110 = TEF6614; read data byte 5h bit RID = 0

8.1.6 Read mode: data byte RDS_STATUS

Table 17. RDS_STATUS - data byte 5h bit allocation

7	6	5	4	3	2	1	0
RDAV	DOFL	-	-	-	-	-	RID

Table 18. RDS_STATUS - data byte 5h bit description

Bit	Symbol	Description
7	RDAV	RDS new data available (duplicate of RDAV at read data byte 0h)
		0 = no data available
		1 = RDS new data available (via read data bytes 5h to Fh)
6	DOFL	data overflow notification[1]
		0 = no data loss
		1 = previous data was not read and is replaced by new 32-bit data
5 to 1	-	not used
0	RID	RDS device type identification
		0 = demodulator; see also read data byte 4h bits ID[2:0]
		1 = not used; fixed to logic 0

[1] DOFL = 1 does not indicate a data error, available data is not corrupted and can be used without restriction.

8.1.7 Read mode: data byte RDS_DAT3

Table 19. RDS_DAT3 - data byte 6h bit allocation

7	6	5	4	3	2	1	0
DD31	DD30	DD29	DD28	DD27	DD26	DD25	DD24

Table 20. RDS_DAT3 - data byte 6h bit description

Bit	Symbol	Description
7 to 0	DD[31:24]	RDS demodulator data; first (oldest) byte of 32-bit buffered data stream

8.1.8 Read mode: data byte RDS_DAT2

Table 21. RDS_DAT2 - data byte 7h bit allocation

7	6	5	4	3	2	1	0
DD23	DD22	DD21	DD20	DD19	DD18	DD17	DD16

Table 22. RDS_DAT2 - data byte 7h bit description

Bit	Symbol	Description
7 to 0	DD[23:16]	RDS demodulator data; second byte of 32-bit buffered data stream

8.1.9 Read mode: data byte RDS_DAT1

Table 23. RDS_DAT1 - data byte 8h bit allocation

7	6	5	4	3	2	1	0
DD15	DD14	DD13	DD12	DD11	DD10	DD9	DD8

Table 24. RDS_DAT1 - data byte 8h bit description

Bit	Symbol	Description
7 to 0	DD[15:8]	RDS demodulator data; third byte of 32-bit buffered data stream

8.1.10 Read mode: data byte RDS_DAT0

Table 25. RDS_DAT0 - data byte 9h bit allocation

7	6	5	4	3	2	1	0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Table 26. RDS_DAT0 - data byte 9h bit description

Bit	Symbol	Description
7 to 0	DD[7:0]	RDS demodulator data; fourth (newest) byte of 32-bit buffered data stream

8.1.11 Read mode: data byte RDS_DATEE

Table 27. RDS_DATEE - data byte Ah bit allocation

7	6	5	4	3	2	1	0
-	-	-	-	DEE3	DEE2	DEE1	DEE0

Table 28. RDS_DATEE - data byte Ah bit description

Bit	Symbol	Description
7 to 4	-	not used
3 to 0	DEE[3:0]	RDS demodulator data error estimation
		0000 to 1111 = no error (high reception quality) to high error (no RDS)

8.2 Write mode

Table 29. Write mode subaddress overview

Subaddress	Name	Default	Reference
0h	TUNER0	0010 0110b	Section 8.2.2
1h	TUNER1	1111 1010b	Section 8.2.3
2h	TUNER2	0000 0000b	Section 8.2.4
3h	RADIO	1000 0000b	Section 8.2.5
4h	SOFTMUTE0	0000 0000b	Section 8.2.6
5h	SOFTMUTE1	0000 0000b	Section 8.2.7
6h	SOFTMUTE2_FM	0000 0000b	Section 8.2.8
6h	SOFTMUTE2_AM	0000 0000b	Section 8.2.9
7h	HIGHCUT0	0000 0000b	Section 8.2.10
8h	HIGHCUT1	0000 0000b	Section 8.2.11
9h	HIGHCUT2	0000 0000b	Section 8.2.12
Ah	STEREO0	0000 0000b	Section 8.2.13
Bh	STEREO1	0000 0000b	Section 8.2.14
Ch	STEREO2	0000 0000b	Section 8.2.15
Dh	CONTROL	0001 0100b	Section 8.2.16
Eh	LEVEL_OFFSET	0100 0000b	Section 8.2.17
Fh	AM_LNA	0000 0100b	Section 8.2.18
10h	RDS	0100 0000b	Section 8.2.19
11h	EXTRA	0000 0000b	Section 8.2.20

8.2.1 Mode and subaddress byte for write

Table 30. MSA - mode and subaddress byte bit allocation

7	6	5	4	3	2	1	0
MODE2	MODE1	MODE0	SA4	SA3	SA2	SA1	SA0

Table 31. MSA - mode and subaddress byte bit description

Bit	Symbol	Description
7 to 5	MODE[2:0]	mode; see Table 32
4 to 0	SA[4:0]	subaddress; subaddressing with SA4 = 0 can be combined with any of the eight MODE[2:0] settings; subaddressing with SA4 = 1 (data byte 10h or 11h) requires standard mode (MODE[2:0] = 000); the subaddress auto-increments for writing consecutive data bytes in a single transmission

Table 32. Tuning action modes

MODE2	MODE1	MODE0	Symbol	Description
0	0	0	standard	write without tuning action
0	0	1	preset	tune to new station with short mute time; see Figure 5
0	1	0	search	tune to new station and stay muted; see Figure 6 and Figure 7
0	1	1	AF update	tune to AF station; store AF quality and tune back to main station; see Figure 8 and Figure 9
1	0	0	AF jump	tune to AF station in minimum mute time; see Figure 10 and Figure 11
1	0	1	AF check	tune to AF station and stay muted; see Figure 12, Figure 13 and Figure 14
1	1	0	mirror test	check current image situation and select injection mode for best result; see Figure 15
1	1	1	end	end; release mute from search mode or AF check mode

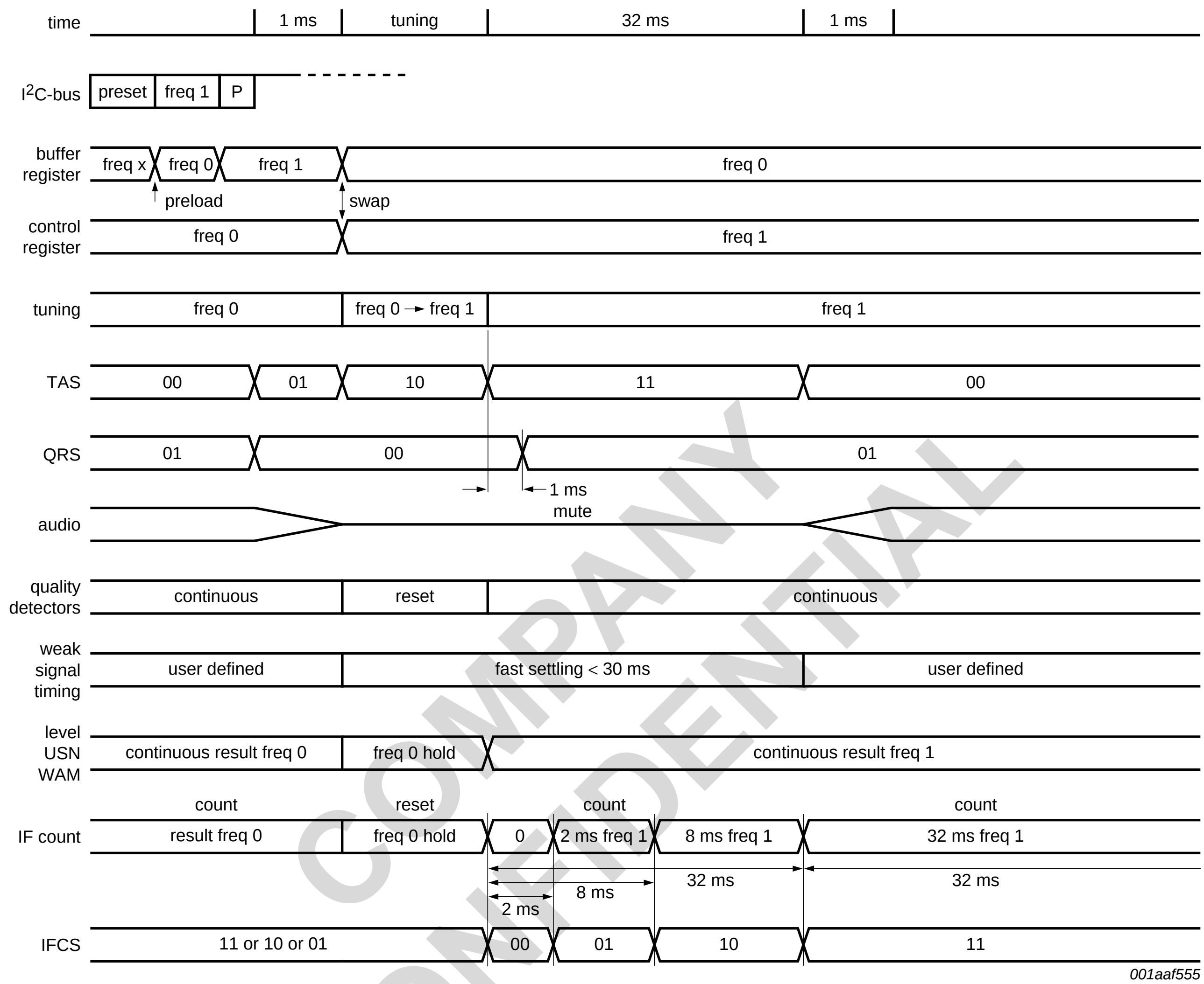


Fig 5. Preset mode

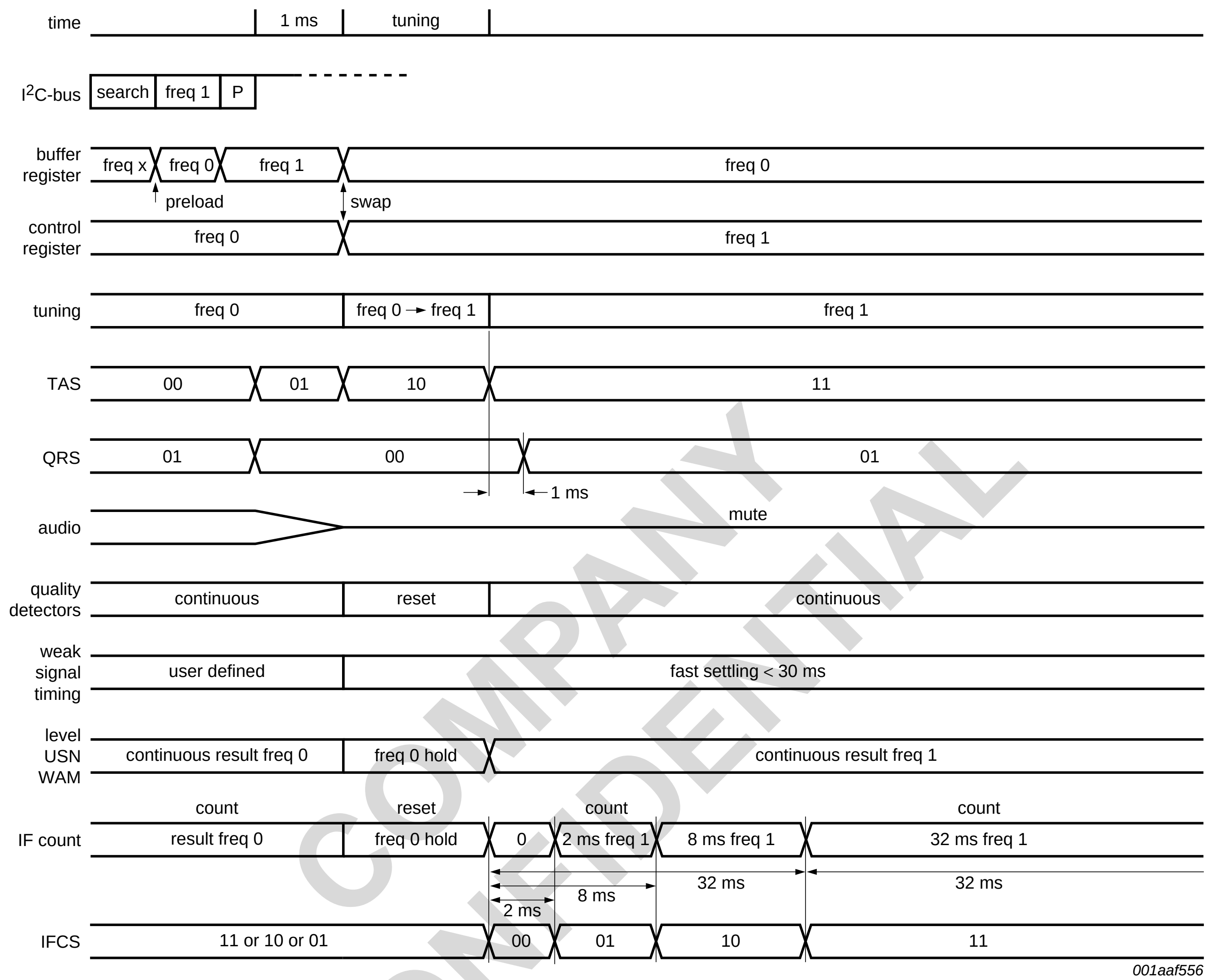


Fig 6. Search mode

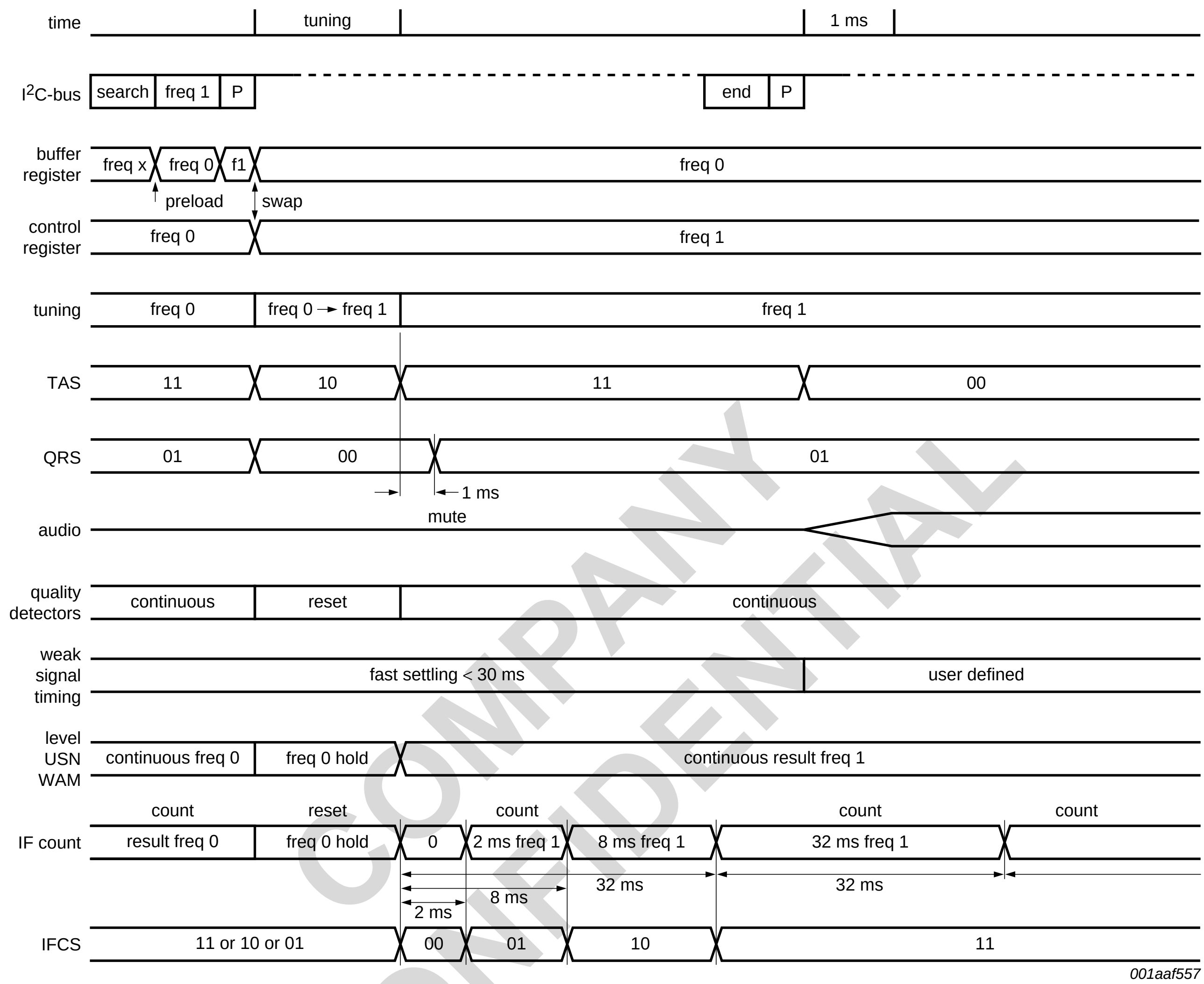


Fig 7. Search mode after search, end

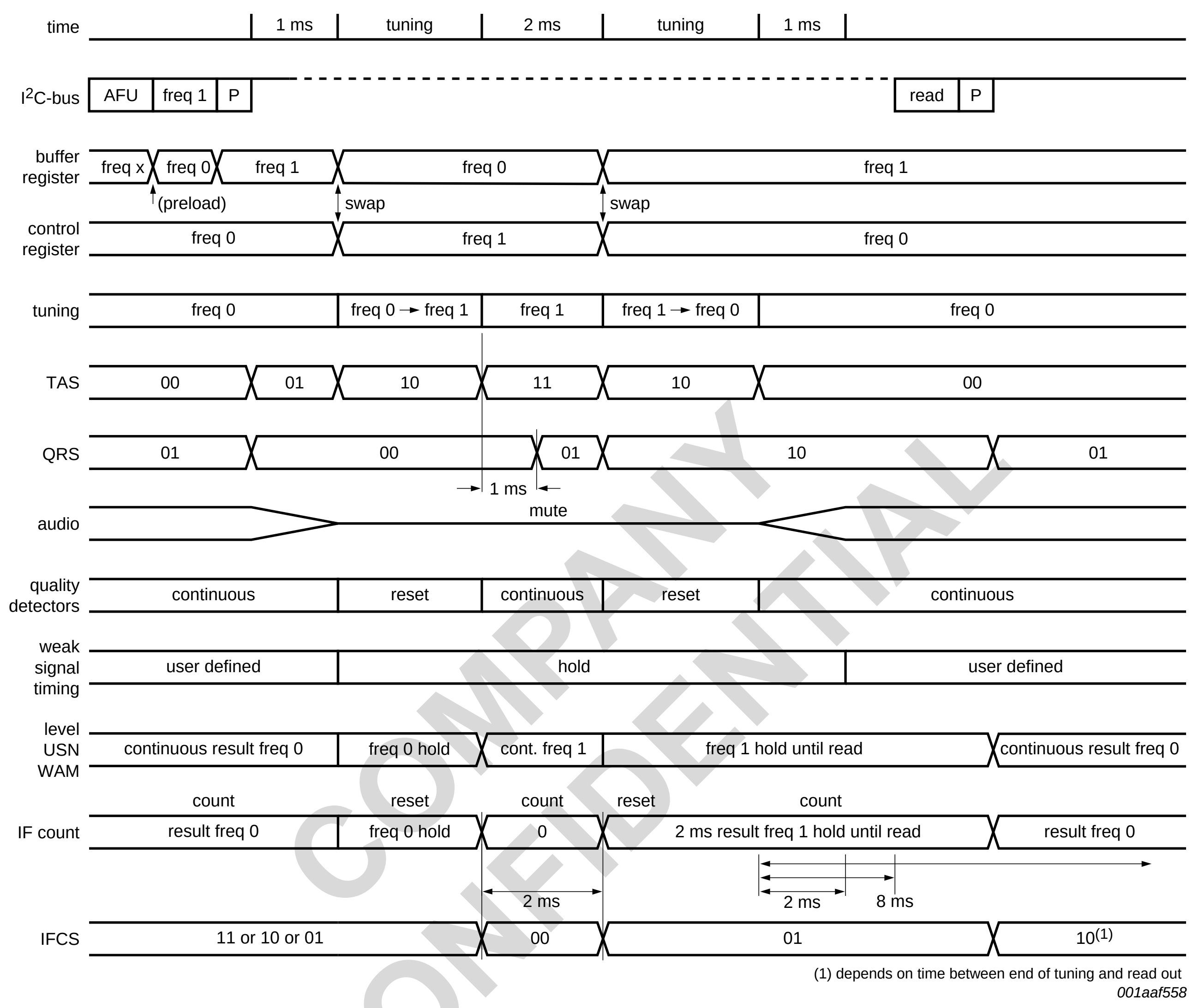


Fig 8. AF update mode

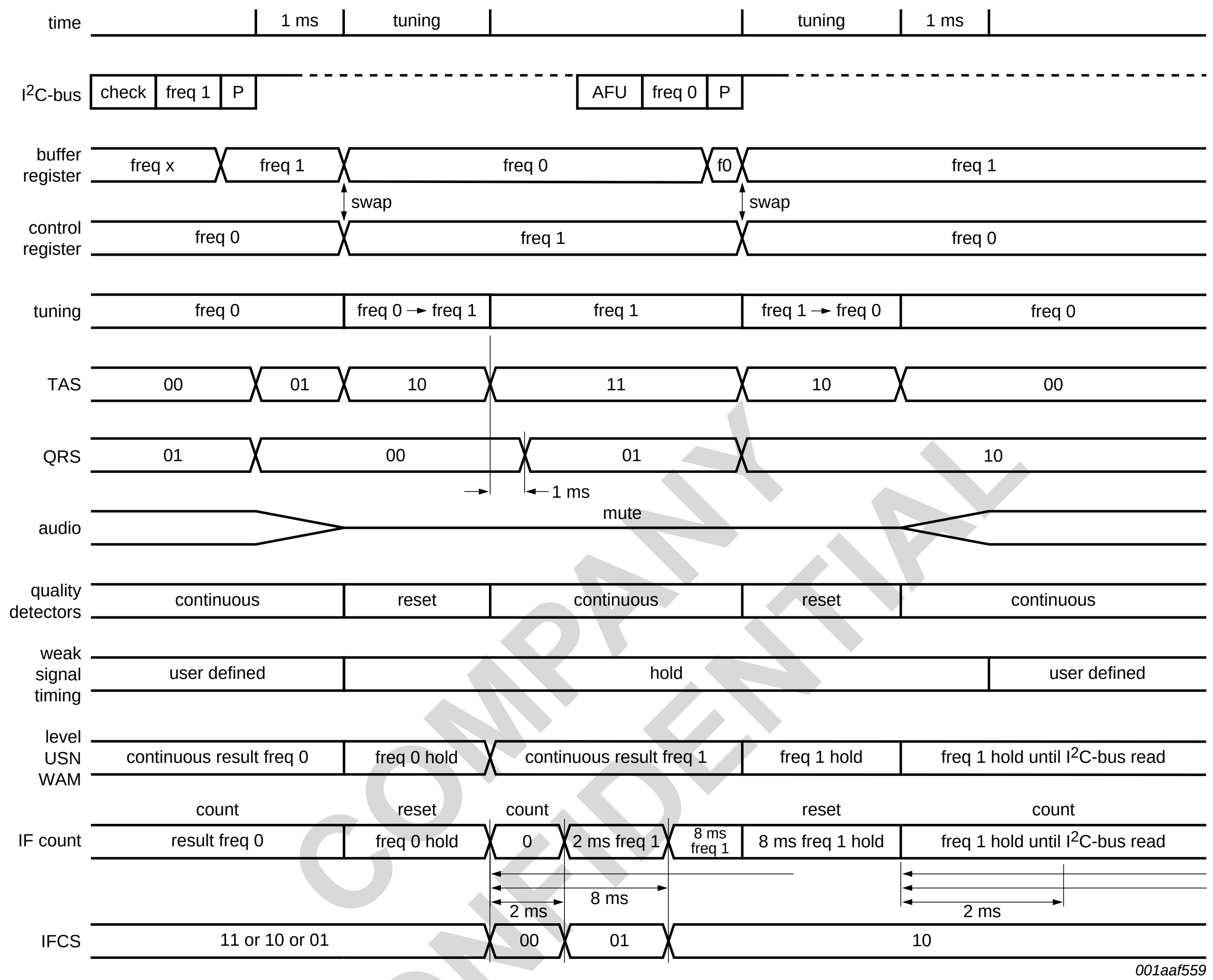


Fig 9. AF update mode after check

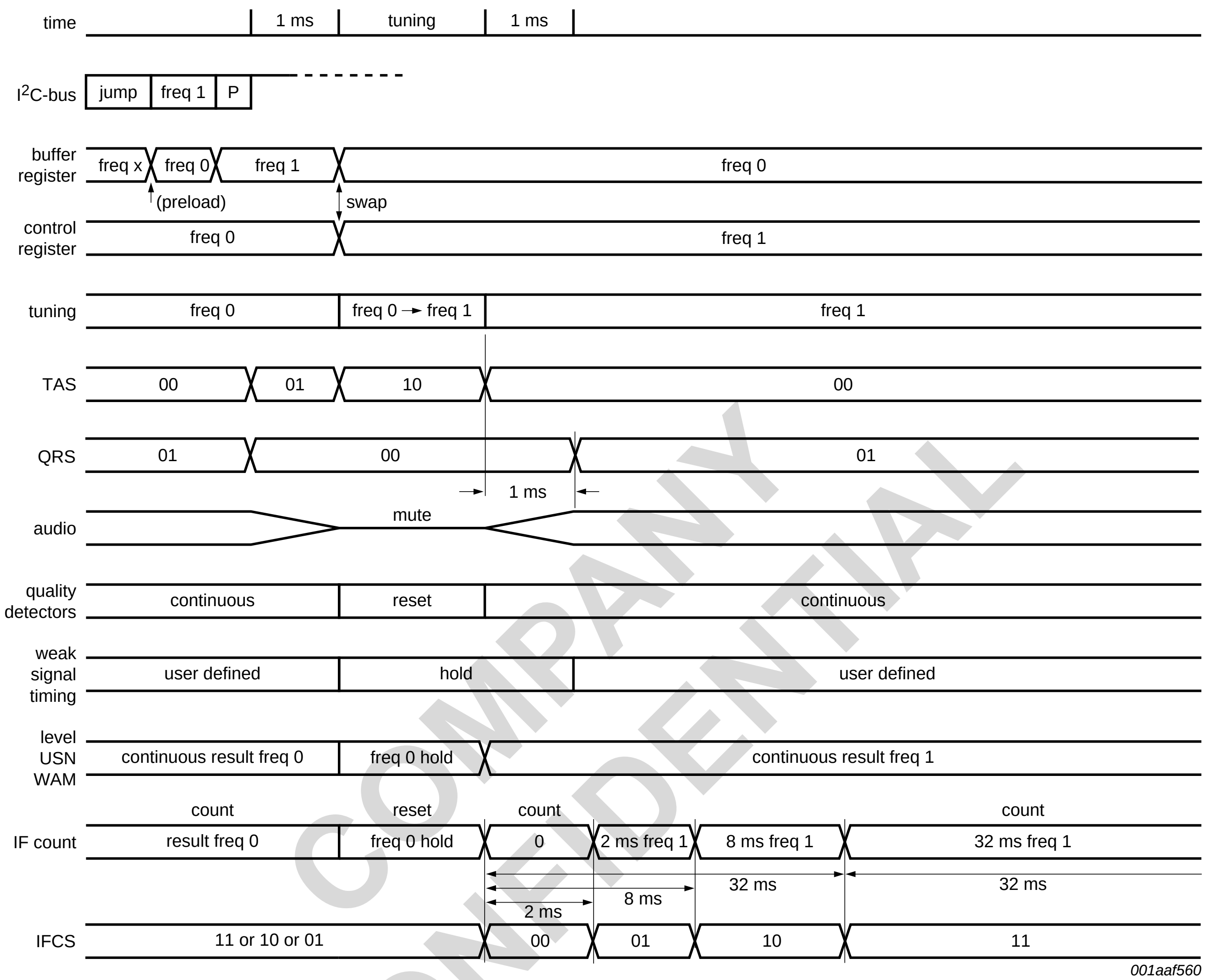


Fig 10. Jump mode

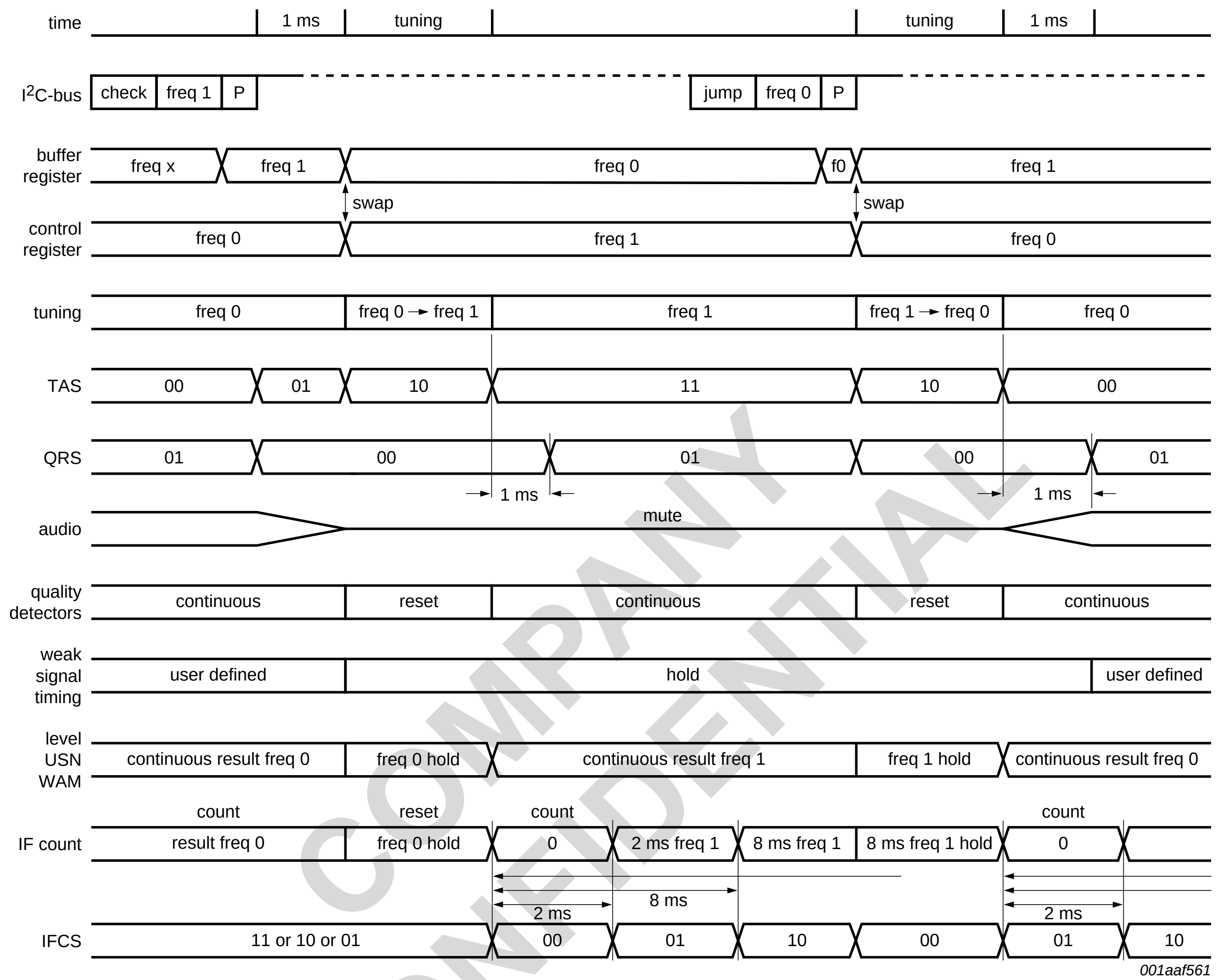


Fig 11. Jump mode after check

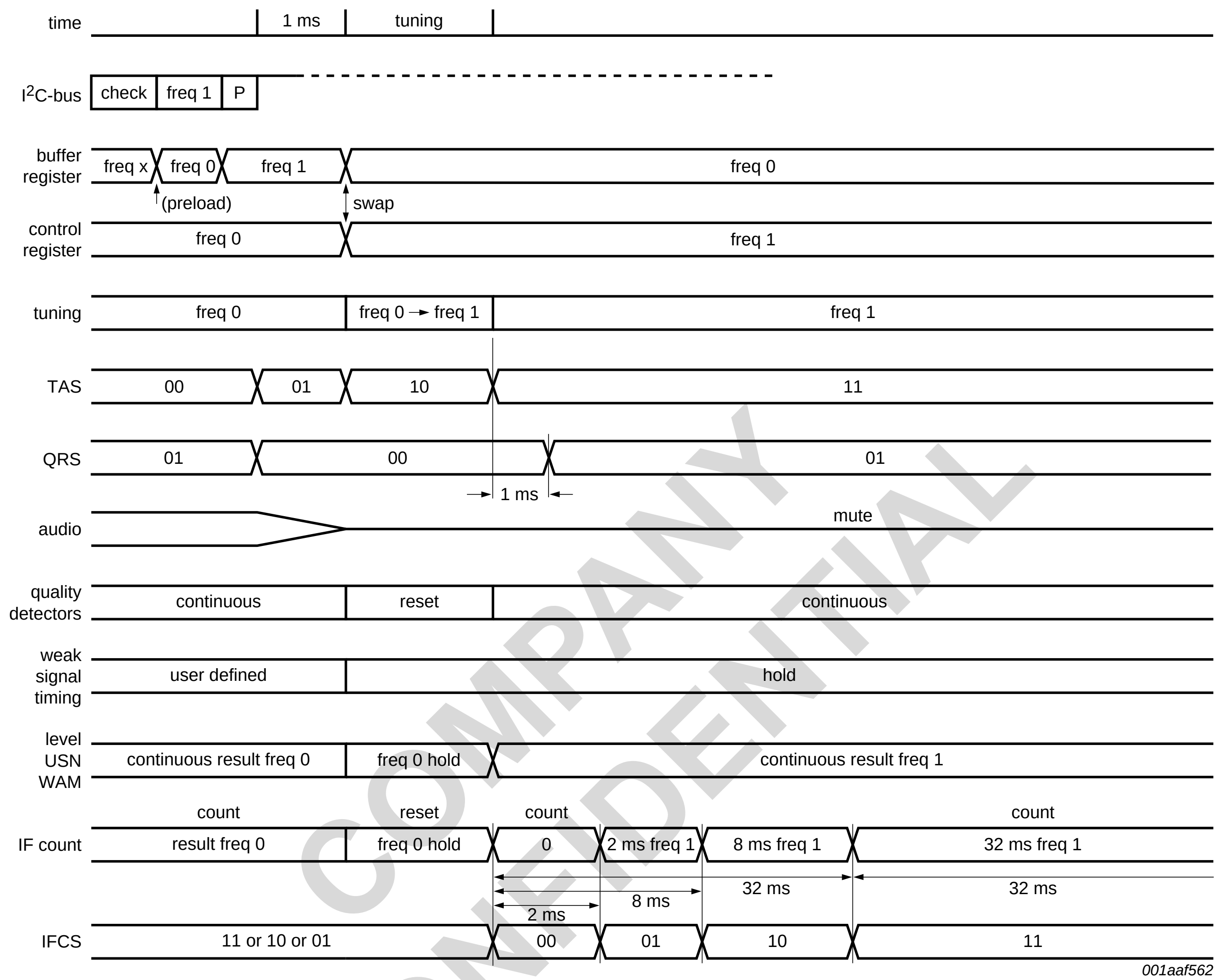


Fig 12. Check mode

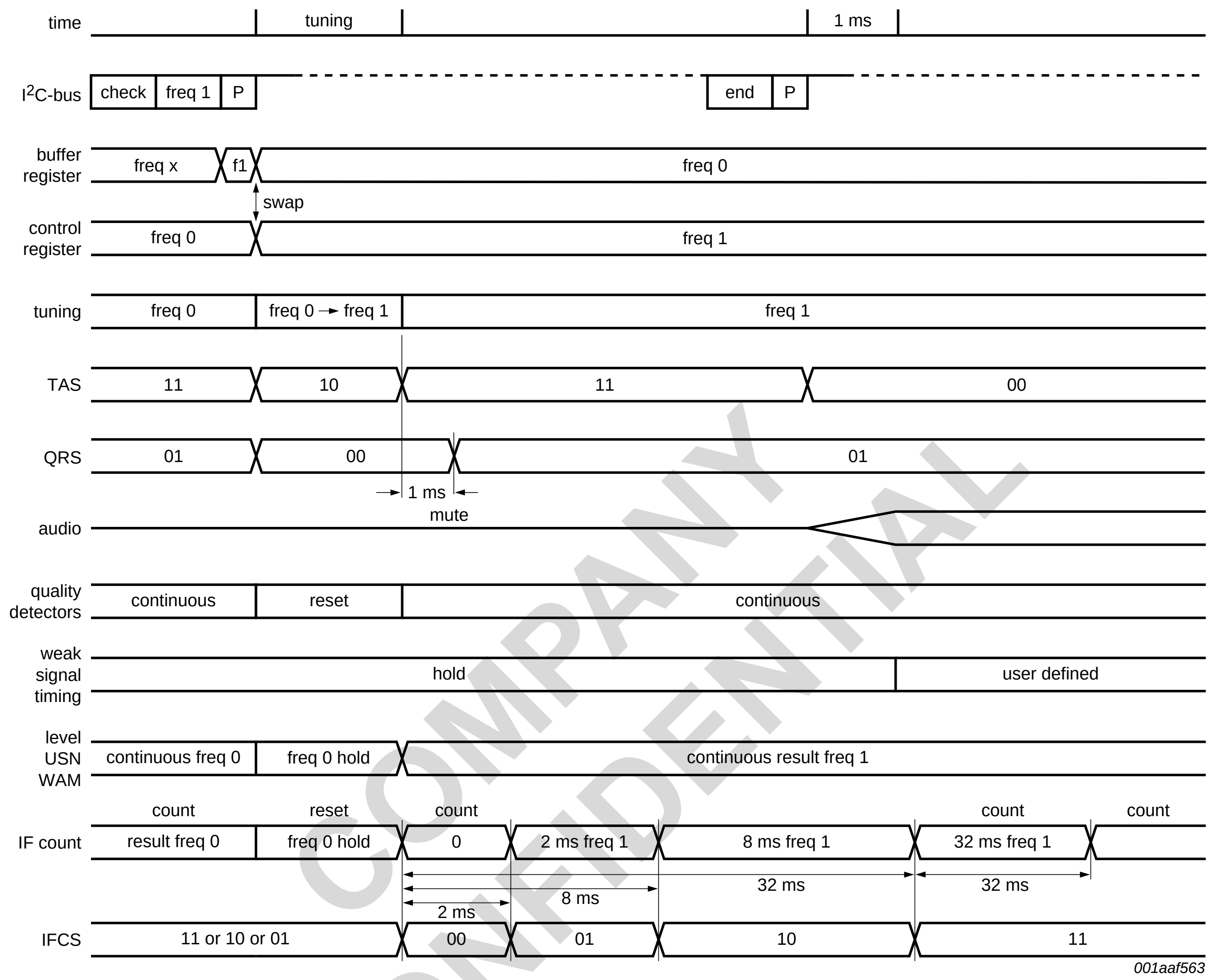


Fig 13. Check mode after check, end

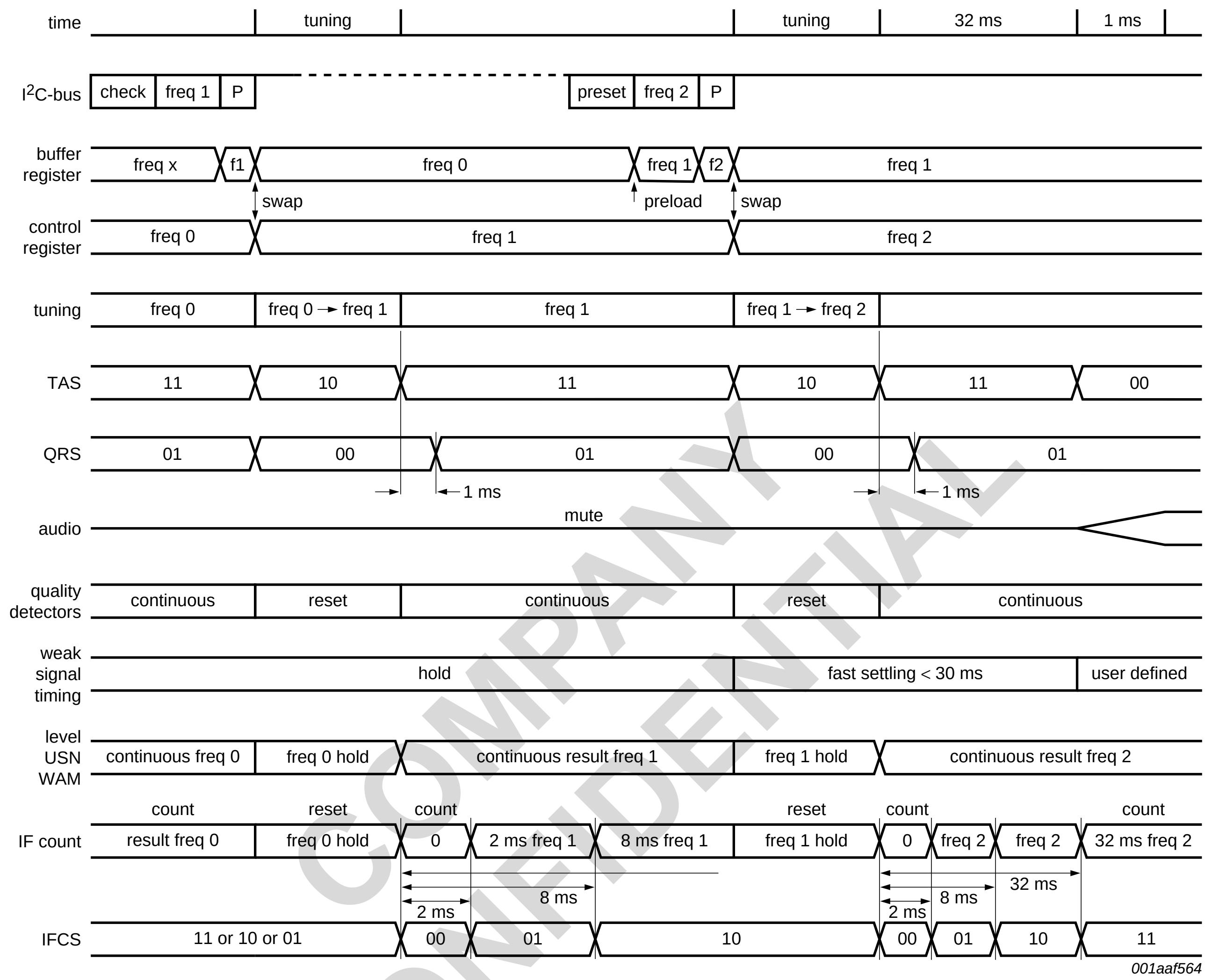


Fig 14. Check mode after check, preset

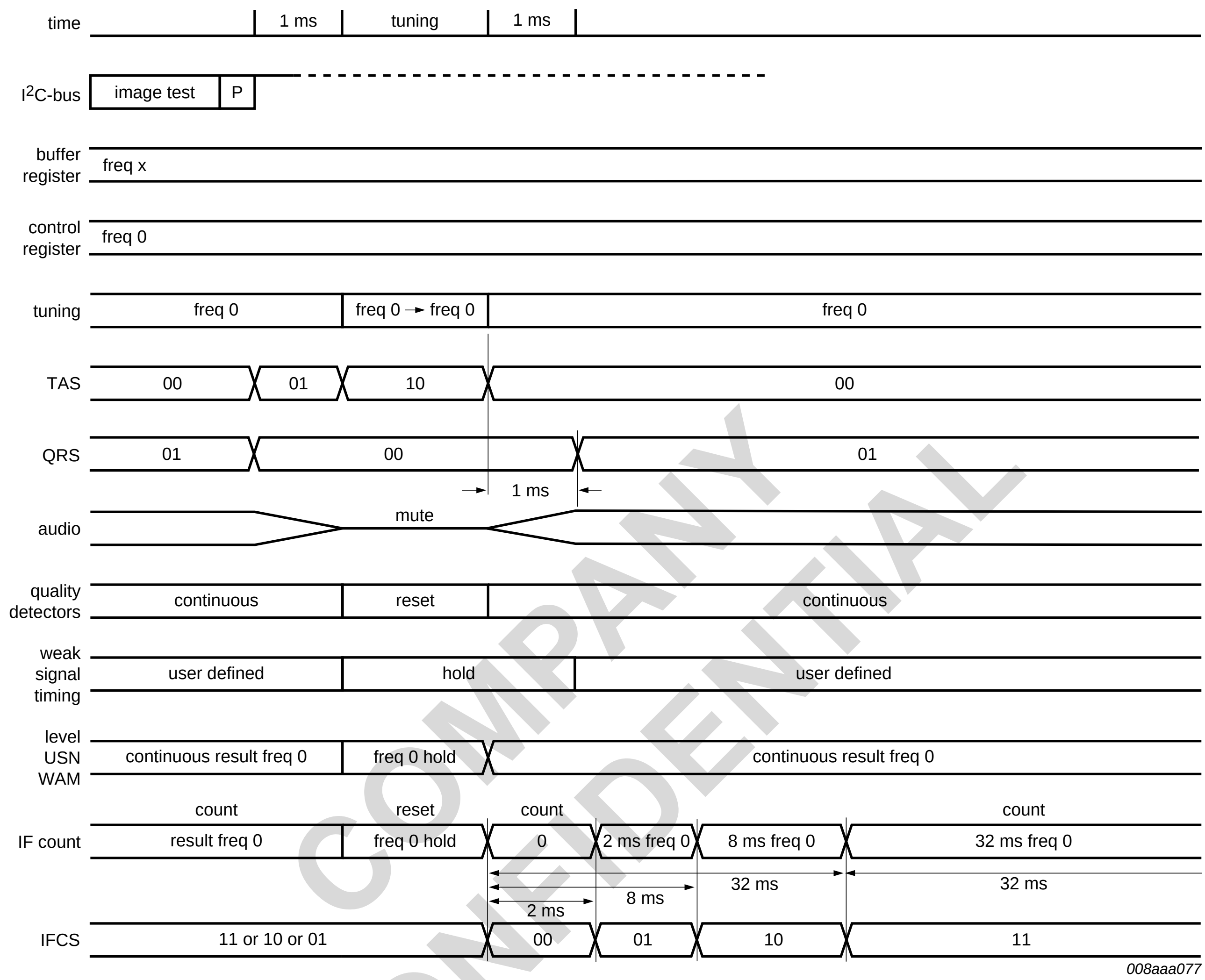


Fig 15. Image test

8.2.2 Write mode: data byte TUNER0

Table 33. TUNER0 - data byte 0h bit allocation with default setting

7	6	5	4	3	2	1	0
0	BAND1	BAND0	FREQ12	FREQ11	FREQ10	FREQ9	FREQ8
	0	1	0	0	1	1	0

Table 34. TUNER0 - data byte 0h bit description

Bit	Symbol	Description
7	-	not used, must be set to logic 0
6 and 5	BAND[1:0]	frequency band[1]
		00 = AM: LW and MW
		01 = FM: standard Europe, USA and Japan
		10 = AM: SW
		11 = FM: OIRT (eastern Europe)
4 to 0	FREQ[12:8]	upper byte of tuning frequency word[1]; see Table 37

[1] For a correct tuning result a change in the BAND or FREQ setting should always be combined with a tuning action of MODE[2:0] = 001 to 101.

8.2.3 Write mode: data byte TUNER1

Table 35. TUNER1 - data byte 1h bit allocation with default setting

7	6	5	4	3	2	1	0
FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0
1	1	1	1	1	0	1	0

Table 36. TUNER1 - data byte 1h bit description

Bit	Symbol	Description
7 to 0	FREQ[7:0]	lower byte of tuning frequency word[1]; see Table 37

[1] For a correct tuning result a change in the BAND or FREQ setting should always be combined with a tuning action of MODE[2:0] = 001 to 101.

Table 37. Tuning frequency

BAND	FREQ[12:0] value	Reception frequency	Frequency correlation	Step
AM: LW and MW	144 to 1720	144 kHz to 1720 kHz	FREQ[12:0] = f_{RF} [kHz]	1 kHz
FM: standard Europe, USA and Japan	1520 to 2160	76 MHz to 108 MHz	FREQ[12:0] = f_{RF} [MHz] $\times$ 20	50 kHz
AM: SW	588 to 3627	2940 kHz to 18135 kHz	FREQ[12:0] = f_{RF} [kHz] $\times$ 5	5 kHz
FM: OIRT (eastern Europe)	6500 to 7400	65 MHz to 74 MHz	FREQ[12:0] = f_{RF} [MHz] $\times$ 100	10 kHz

8.2.4 Write mode: data byte TUNER2

Table 38. TUNER2 - data byte 2h bit allocation with default setting

7	6	5	4	3	2	1	0
RFAGC1	RFAGC0	INJ1	INJ0	0	FMBW2	FMBW1	FMBW0
0	0	0	0		0	0	0

Table 39. TUNER2 - data byte 2h bit description

Bit	Symbol	Description
7 and 6	RFAGC[1:0]	AM RF AGC sensitivity control
		00 = AGC threshold not reduced
		01 = AGC threshold reduced by 2 dB
		10 = AGC threshold reduced by 4 dB
		11 = AGC threshold reduced by 6 dB
		FM RF AGC sensitivity control
		00 = AGC threshold not reduced
		01 = AGC threshold reduced by 2 dB
		10 = AGC threshold reduced by 4 dB
		11 = AGC threshold reduced by 6 dB
5 and 4	INJ[1:0]	injection[1]
		00 = automatic injection
		01 = high injection LO
		10 = low injection LO
		11 = undefined, do not use
3	-	not used, must be set to logic 0
2 to 0	FMBW[2:0]	FM bandwidth control
		000 = dynamic mode (optimum bandwidth is selected depending on reception conditions)
		001 to 111 = narrow to wide FM IF filter bandwidth

[1] For a correct tuning result a change in the INJ setting should always be combined with MODE[2:0] = 110 or a tuning action of MODE[2:0] = 001 to 101.

8.2.5 Write mode: data byte RADIO

Table 40. RADIO - data byte 3h bit allocation with default setting

7	6	5	4	3	2	1	0
NBS1	NBS0	LOCUT	MONO	DEMP1	DEMP0	0	OUTA
1	0	0	0	0	0		0

Table 41. RADIO - data byte 3h bit description

Bit	Symbol	Description
7 and 6	NBS[1:0]	AM and FM noise blanker sensitivity control
		00 = AM and FM noise blanker off
		01 = low AM and FM noise blanker sensitivity
		10 = medium AM and FM noise blanker sensitivity
		11 = high AM and FM noise blanker sensitivity
5	LOCUT	control of audio high-pass filter
		0 = no limitation (–3 dB at 7 Hz)
		1 = high-pass function (–3 dB at 100 Hz)
4	MONO	mono/stereo switch
		0 = FM stereo enabled
		1 = FM stereo disabled (forced mono)
3 and 2	DEMP[1:0]	de-emphasis setting
		00 = 50 μs de-emphasis
		01 = 75 μs de-emphasis
		10 = 103 μs low-pass
		11 = not used
1	-	not used, must be set to logic 0
0	OUTA	audio output gain
		0 = low audio gain at LOUT and ROUT
		1 = high audio gain at LOUT and ROUT

8.2.6 Write mode: data byte SOFTMUTE0

Table 42. SOFTMUTE0 - data byte 4h bit allocation with default setting

7	6	5	4	3	2	1	0
0	0	0	MAT2	MAT1	MAT0	MRT1	MRT0
			0	0	0	0	0

Table 43. SOFTMUTE0 - data byte 4h bit description

Bit	Symbol	Description
7 to 5	-	not used, must be set to logic 0
4 to 2	MAT[2:0]	soft mute slow attack time; see Table 44
1 and 0	MRT[1:0]	soft mute slow recovery time
		00 = 2 times attack time
		01 = 4 times attack time
		10 = 8 times attack time
		11 = 16 times attack time

Table 44. Soft mute attack time

MAT2	MAT1	MAT0	Soft mute attack time
0	0	0	60 ms
0	0	1	125 ms
0	1	0	250 ms
0	1	1	0.5 s
1	0	0	1 s
1	0	1	2 s
1	1	0	4 s
1	1	1	8 s

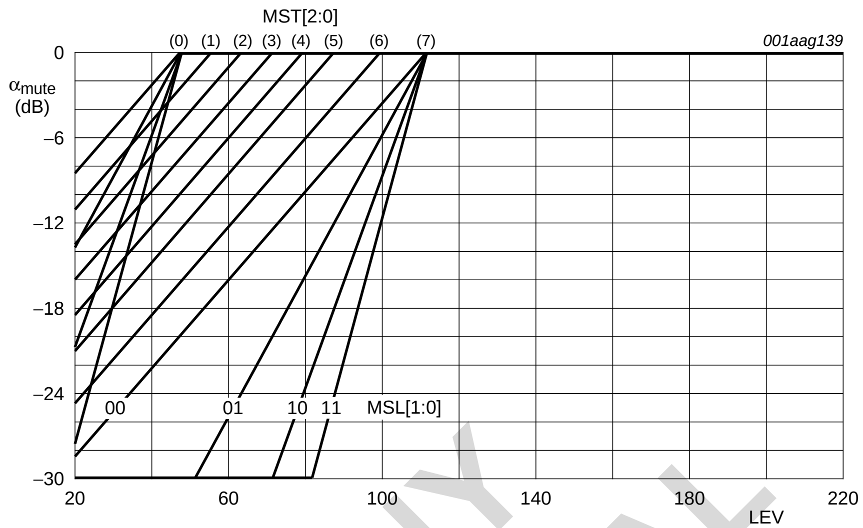
8.2.7 Write mode: data byte SOFTMUTE1

Table 45. SOFTMUTE1 - data byte 5h bit allocation with default setting

7	6	5	4	3	2	1	0
MFOL	MSOL	0	MST2	MST1	MST0	MSL1	MSL0
0	0		0	0	0	0	0

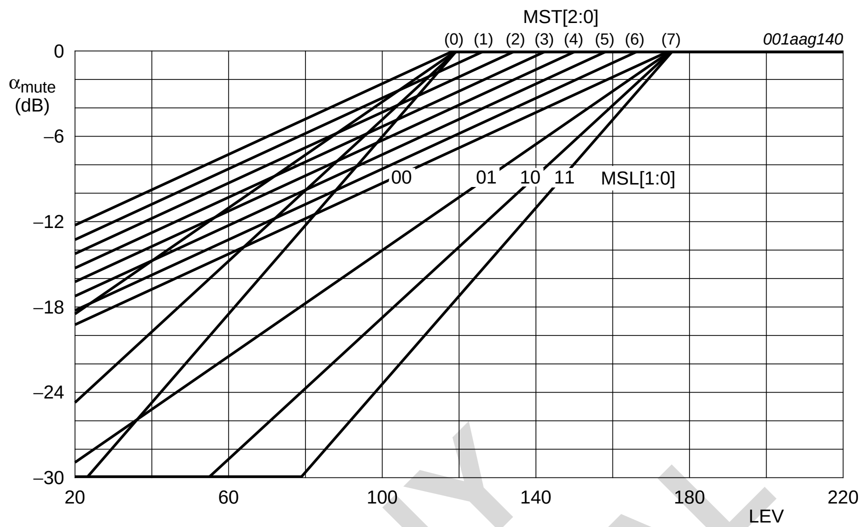
Table 46. SOFTMUTE1 - data byte 5h bit description

Bit	Symbol	Description
7	MFOL	soft mute fast on level
		0 = no fast control on level
		1 = fast control on level active
6	MSOL	soft mute slow on level
		0 = no slow control on level
		1 = slow control on level active
5	-	not used, must be set to logic 0
4 to 2	MST[2:0]	soft mute start on level
		000 to 111 = high threshold to low threshold of weak signal soft mute control; see Figure 16 and Figure 17
1 and 0	MSL[1:0]	soft mute slope on level
		00 to 11 = low steepness to high steepness of slope of weak signal soft mute control; see Figure 16 and Figure 17



(0) MST[2:0] = 000
(1) MST[2:0] = 001
(2) MST[2:0] = 010
(3) MST[2:0] = 011
(4) MST[2:0] = 100
(5) MST[2:0] = 101
(6) MST[2:0] = 110
(7) MST[2:0] = 111

Fig 16. FM soft mute controlled by level information



(0) MST[2:0] = 000

(1) MST[2:0] = 001

(2) MST[2:0] = 010

(3) MST[2:0] = 011

(4) MST[2:0] = 100

(5) MST[2:0] = 101

(6) MST[2:0] = 110

(7) MST[2:0] = 111

Fig 17. AM soft mute controlled by level information

8.2.8 Write mode: data byte SOFTMUTE2_FM

Table 47. SOFTMUTE2_FM - data byte 6h bit allocation with default setting

7	6	5	4	3	2	1	0
MFON	MSON	MNS1	MNS0	MFOM	MSOM	MMS1	MMS0
0	0	0	0	0	0	0	0

Table 48. SOFTMUTE2_FM - data byte 6h bit description

Bit	Symbol	Description
7	MFON	soft mute fast on noise (USN)
		0 = no fast control on noise (USN)
		1 = fast control on noise (USN) active
6	MSON	soft mute slow on noise (USN)
		0 = no slow control on noise (USN)
		1 = slow control on noise (USN) active
5 and 4	MNS[1:0]	sensitivity of soft mute on noise (USN)
		00 to 11 = weak to strong soft mute control by FM noise (USN); see Figure 18

Table 48. SOFTMUTE2_FM - data byte 6h bit description *...continued*

Bit	Symbol	Description
3	MFOM	soft mute fast on multipath (WAM)
		0 = no fast control on multipath (WAM)
		1 = fast control on multipath (WAM) active
2	MSOM	soft mute slow on multipath (WAM)
		0 = no slow control on multipath (WAM)
		1 = slow control on multipath (WAM) active
1 and 0	MMS[1:0]	sensitivity of soft mute on multipath (WAM)
		00 to 11 = weak to strong soft mute control by FM multipath (WAM); see Figure 19

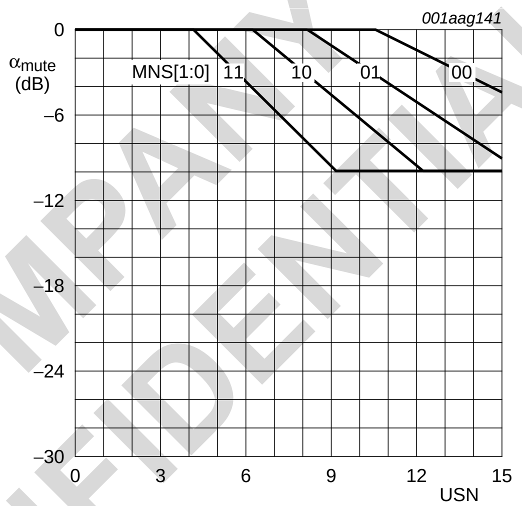


Fig 18. Soft mute controlled by USN information

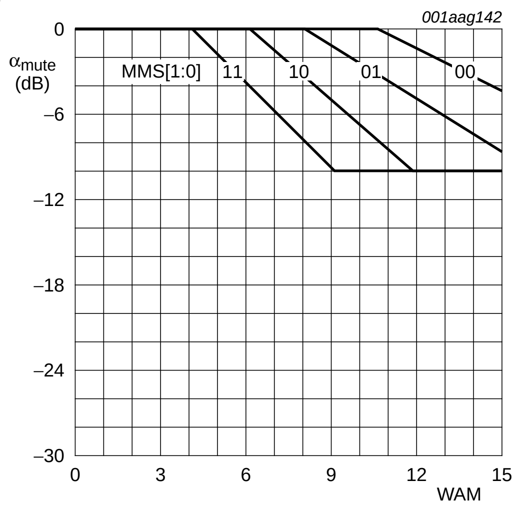


Fig 19. Soft mute controlled by WAM information

8.2.9 Write mode: data byte SOFTMUTE2_AM

Table 49. SOFTMUTE2_AM - data byte 6h bit allocation with default setting

7	6	5	4	3	2	1	0
0	0	0	MLIM4	MLIM3	MLIM2	MLIM1	MLIM0
			0	0	0	0	0

Table 50. SOFTMUTE2_AM - data byte 6h bit description

Bit	Symbol	Description
7 to 5	-	not used, must be set to logic 0
4 to 0	MLIM[4:0]	soft mute limit
		0 0000 to 1 1110 = soft mute control limited at 0 dB to 30 dB; the soft mute control can be limited to the point at which natural soft mute starts

8.2.10 Write mode: data byte HIGHCUT0

Table 51. HIGHCUT0 - data byte 7h bit allocation with default setting

7	6	5	4	3	2	1	0
HMOD1	HMOD0	HLIM	HAT2	HAT1	HAT0	HRT1	HRT0
0	0	0	0	0	0	0	0

Table 52. HIGHCUT0 - data byte 7h bit description

Bit	Symbol	Description
7 and 6	HMOD[1:0]	high-cut on modulation; see Figure 20
		00 = no modulation control
		01 = high-cut (50 μs to 103 μs) for < 30 % modulation
		10 = high-cut (50 μs to 103 μs) for < 50 % modulation
		11 = high-cut (50 μs to 165 μs) for < 50 % modulation
5	HLIM	limitation of high-cut control on level, noise (USN) and multipath (WAM)
		0 = high-cut limit at 165 μs, −10 dB at 10 kHz (for 50 μs de-emphasis)
		1 = high-cut limit at 103 μs, −6 dB at 10 kHz (for 50 μs de-emphasis)
4 to 2	HAT[2:0]	high-cut slow attack time; see Table 53
1 and 0	HRT[1:0]	high-cut slow recovery time
		00 = 2 times attack time
		01 = 4 times attack time
		10 = 8 times attack time
		11 = 16 times attack time

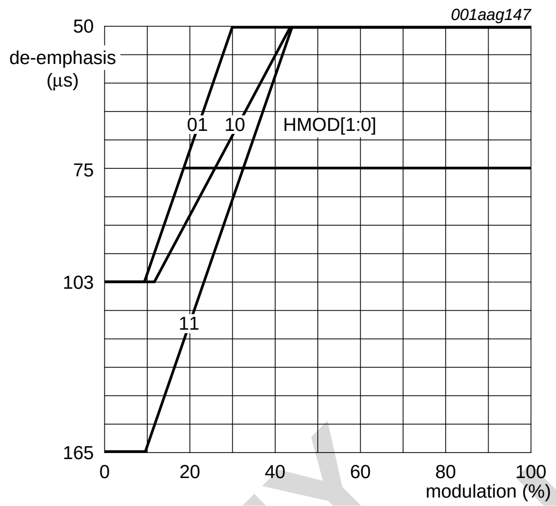


Fig 20. High-cut controlled by modulation

Table 53. High-cut attack time

HAT2	HAT1	HAT0	High-cut attack time
0	0	0	60 ms
0	0	1	125 ms
0	1	0	250 ms
0	1	1	0.5 s
1	0	0	1 s
1	0	1	2 s
1	1	0	4 s
1	1	1	8 s

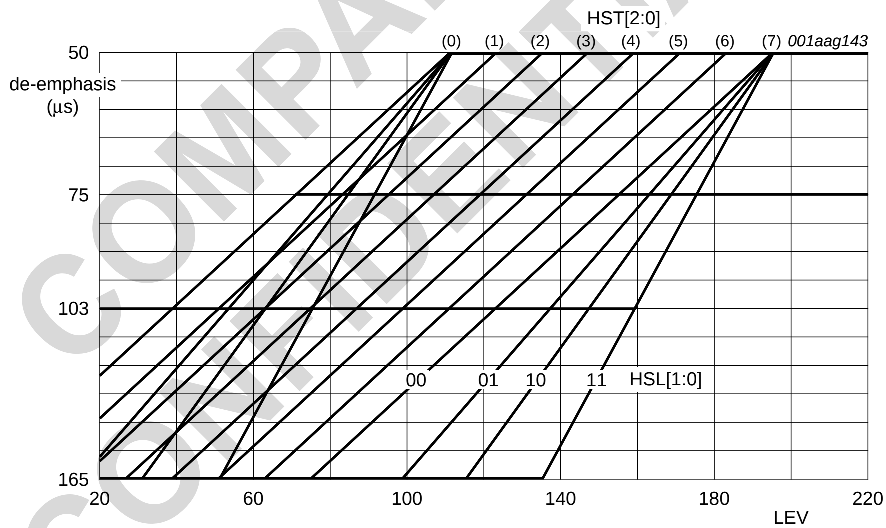
8.2.11 Write mode: data byte HIGHCUT1

Table 54. HIGHCUT1 - data byte 8h bit allocation with default setting

7	6	5	4	3	2	1	0
HFOL	HSOL	0	HST2	HST1	HST0	HSL1	HSL0
0	0		0	0	0	0	0

Table 55. HIGHCUT1 - data byte 8h bit description

Bit	Symbol	Description
7	HFOL	high-cut fast on level
		0 = no fast control on level
		1 = fast control on level active
6	HSOL	high-cut slow on level
		0 = no slow control on level
		1 = slow control on level active
5	-	not used, must be set to logic 0
4 to 2	HST[2:0]	high-cut start on level
		000 to 111 = high threshold to low threshold of weak signal high-cut control; see Figure 21 and Figure 22
1 and 0	HSL[1:0]	high-cut slope on level
		00 to 11 = low steepness to high steepness of slope of weak signal high-cut control; see Figure 21 and Figure 22



(0) HST[2:0] = 000

(1) HST[2:0] = 001

(2) HST[2:0] = 010

(3) HST[2:0] = 011

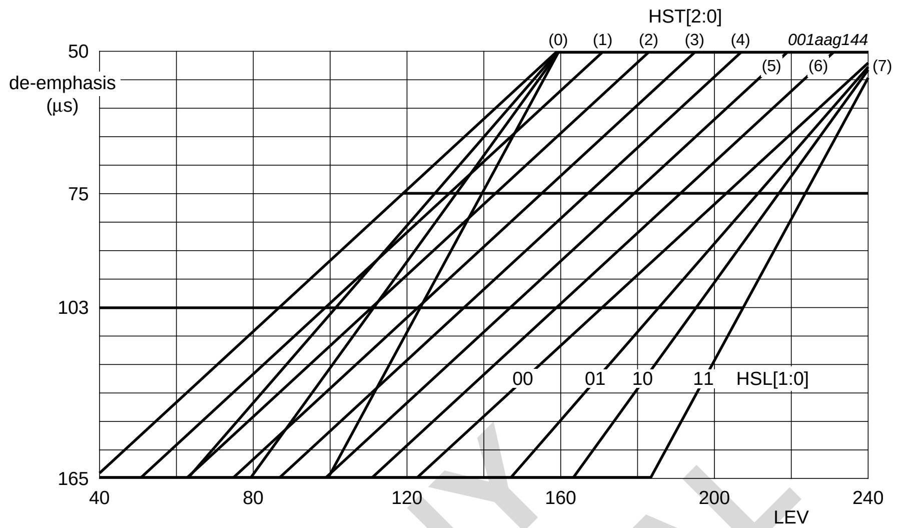
(4) HST[2:0] = 100

(5) HST[2:0] = 101

(6) HST[2:0] = 110

(7) HST[2:0] = 111

Fig 21. FM high-cut controlled by level information



(0) HST[2:0] = 000
(1) HST[2:0] = 001
(2) HST[2:0] = 010
(3) HST[2:0] = 011
(4) HST[2:0] = 100
(5) HST[2:0] = 101
(6) HST[2:0] = 110
(7) HST[2:0] = 111

Fig 22. AM high-cut controlled by level information

8.2.12 Write mode: data byte HIGHCUT2

Table 56. HIGHCUT2 - data byte 9h bit allocation with default setting

7	6	5	4	3	2	1	0
HFON	HSON	HNS1	HNS0	HFOM	HSOM	HMS1	HMS0
0	0	0	0	0	0	0	0

Table 57. HIGHCUT2 - data byte 9h bit description

Bit	Symbol	Description
7	HFON	high-cut fast on noise (USN)
		0 = no fast control on noise (USN)
		1 = fast control on noise (USN) active
6	HSON	high-cut slow on noise (USN)
		0 = no slow control on noise (USN)
		1 = slow control on noise (USN) active
5 and 4	HNS[1:0]	sensitivity of high-cut on noise (USN)
		00 to 11 = weak to strong high-cut control by FM noise (USN); see Figure 23

Table 57. HIGHCUT2 - data byte 9h bit description *...continued*

Bit	Symbol	Description
3	HFOM	high-cut fast on multipath (WAM)
		0 = no fast control on multipath (WAM)
		1 = fast control on multipath (WAM) active
2	HSOM	high-cut slow on multipath (WAM)
		0 = no slow control on multipath (WAM)
		1 = slow control on multipath (WAM) active
1 and 0	HMS[1:0]	sensitivity of high-cut on multipath (WAM)
		00 to 11 = weak to strong high-cut control by FM multipath (WAM); see Figure 24

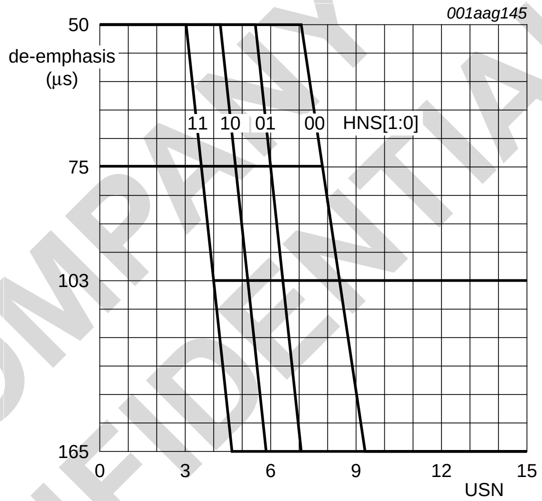


Fig 23. High-cut controlled by USN information

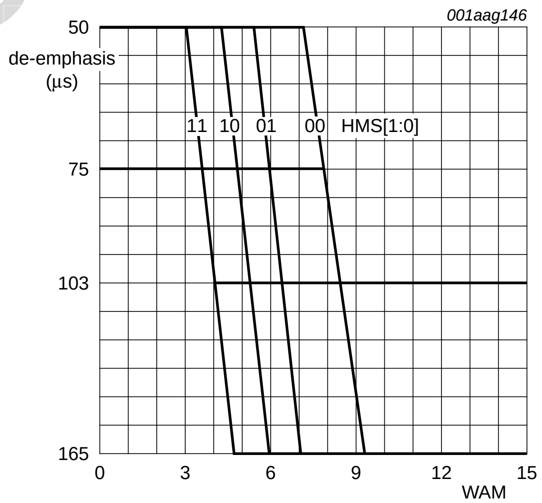


Fig 24. High-cut controlled by WAM information

8.2.13 Write mode: data byte STEREO0

Table 58. STEREO0 - data byte Ah bit allocation with default setting

7	6	5	4	3	2	1	0
SMOD1	SMOD0	0	SAT2	SAT1	SAT0	SRT1	SRT0
0	0		0	0	0	0	0

Table 59. STEREO0 - data byte Ah bit description

Bit	Symbol	Description
7 and 6	SMOD[1:0]	stereo blend on modulation; see Figure 25
		00 = no modulation control
		01 = stereo blend (stereo to mono) for < 30 % modulation
		10 = stereo blend (stereo to 6 dB channel separation) for < 30 % modulation
		11 = stereo blend (stereo to mono) for < 15 % modulation
5	-	not used, must be set to logic 0
4 to 2	SAT[2:0]	stereo blend slow attack time; see Table 60
1 and 0	SRT[1:0]	stereo blend slow recovery time
		00 = 2 times attack time
		01 = 4 times attack time
		10 = 8 times attack time
		11 = 16 times attack time

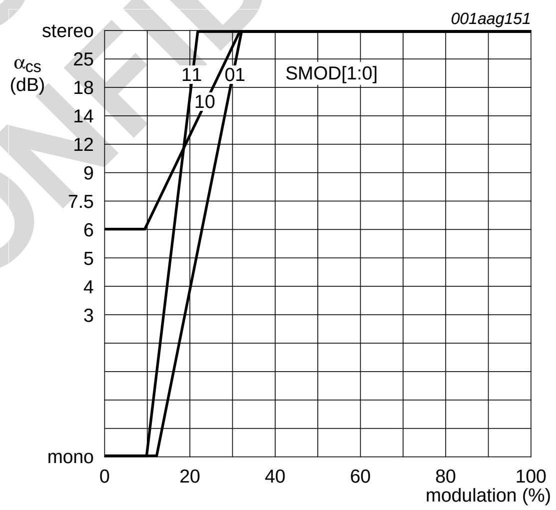


Fig 25. Stereo blend controlled by modulation

Table 60. Stereo blend attack time

SAT2	SAT1	SAT0	Stereo blend attack time
0	0	0	60 ms
0	0	1	125 ms
0	1	0	250 ms
0	1	1	0.5 s
1	0	0	1 s
1	0	1	2 s
1	1	0	4 s
1	1	1	8 s

8.2.14 Write mode: data byte STEREO1

Table 61. STEREO1 - data byte Bh bit allocation with default setting

7	6	5	4	3	2	1	0
SFOL	SSOL	0	SST2	SST1	SST0	SSL1	SSL0
0	0		0	0	0	0	0

Table 62. STEREO1 - data byte Bh bit description

Bit	Symbol	Description
7	SFOL	stereo blend fast on level
		0 = no fast control on level
		1 = fast control on level active
6	SSOL	stereo blend slow on level
		0 = no slow control on level
		1 = slow control on level active
5	-	not used, must be set to logic 0
4 to 2	SST[2:0]	stereo blend start on level
		000 to 111 = high threshold to low threshold of weak signal stereo blend control; see Figure 26
1 and 0	SSL[1:0]	stereo blend slope on level
		00 to 11 = low steepness to high steepness of slope of weak signal stereo blend control; see Figure 26

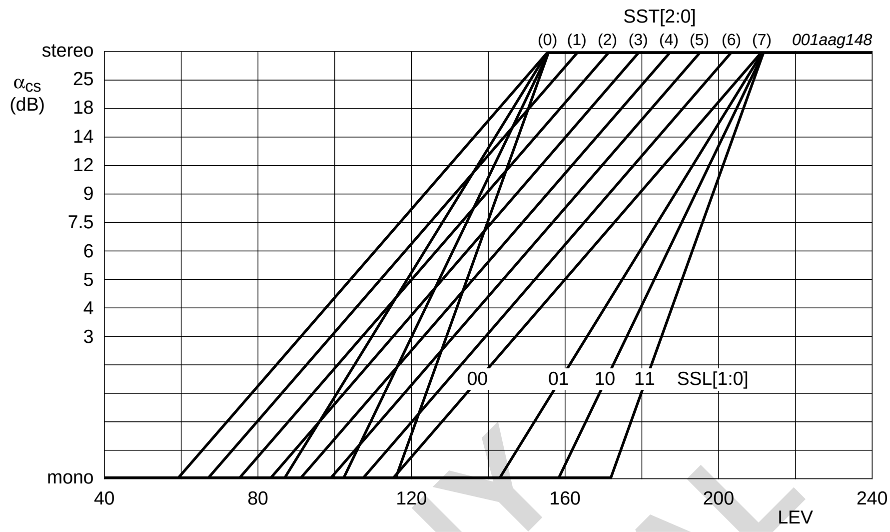


Fig 26. Stereo blend controlled by level information

8.2.15 Write mode: data byte STEREO2

Table 63. STEREO2 - data byte Ch bit allocation with default setting

7	6	5	4	3	2	1	0
SFON	SSON	SNS1	SNS0	SFOM	SSOM	SMS1	SMS0
0	0	0	0	0	0	0	0

Table 64. STEREO2 - data byte Ch bit description

Bit	Symbol	Description
7	SFON	stereo blend fast on noise (USN)
		0 = no fast control on noise (USN)
		1 = fast control on noise (USN) active
6	SSON	stereo blend slow on noise (USN)
		0 = no slow control on noise (USN)
		1 = slow control on noise (USN) active
5 and 4	SNS[1:0]	sensitivity of stereo blend on noise (USN)
		00 to 11 = weak to strong stereo blend control by FM noise (USN); see Figure 27

Table 64. STEREO2 - data byte Ch bit description *…continued*

Bit	Symbol	Description
3	SFOM	stereo blend fast on multipath (WAM)
		0 = no fast control on multipath (WAM)
		1 = fast control on multipath (WAM) active
2	SSOM	stereo blend slow on multipath (WAM)
		0 = no slow control on multipath (WAM)
		1 = slow control on multipath (WAM) active
1 and 0	SMS[1:0]	sensitivity of stereo blend on multipath (WAM)
		00 to 11 = weak to strong stereo blend control by FM multipath (WAM); see Figure 28

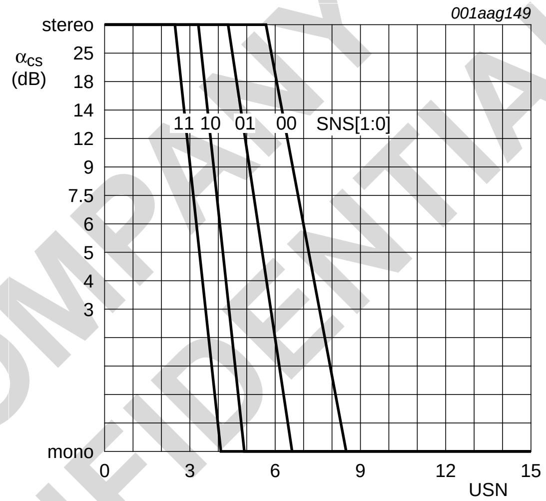


Fig 27. Stereo blend controlled by USN information

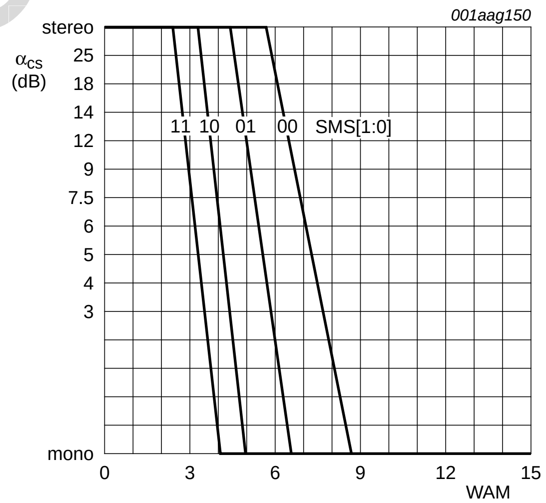


Fig 28. Stereo blend controlled by WAM information

8.2.16 Write mode: data byte CONTROL

Table 65. CONTROL - data byte Dh bit allocation with default setting

7	6	5	4	3	2	1	0
PORT	NBLIM	BWUSN1	BWUSN0	0	1	BWLEV	BWMOD
0	0	0	1			0	0

Table 66. CONTROL - data byte Dh bit description

Bit	Symbol	Description
7	PORT	switch output port
		0 = pin TEST open-circuit
		1 = pin TEST pull-down to ground
6	NBLIM	FM noise blanker pulse rate limiter
		0 = pulse rate not limited
		1 = pulse rate limited to 400 Hz
5 and 4	BWUSN[1:0]	dynamic FM bandwidth control as a function of noise
		00 = modulation handling
		01 = intention to modulation handling
		10 = intention to adjacent channel suppression
		11 = adjacent channel suppression
3	-	not used, must be set to logic 0
2	-	not used, must be set to logic 1
1	BWLEV	dynamic FM bandwidth control as a function of low level
		0 = narrow bandwidth (reduced noise)
		1 = wide bandwidth (modulation handling)
0	BWMOD	dynamic FM bandwidth control as a function of modulation
		0 = adjacent channel suppression
		1 = modulation handling

8.2.17 Write mode: data byte LEVEL_OFFSET

Table 67. LEVEL_OFFSET - data byte Eh bit allocation with default setting

7	6	5	4	3	2	1	0
0	LEVO6	LEVO5	LEVO4	LEVO3	LEVO2	LEVO1	LEVO0
	1	0	0	0	0	0	0

Table 68. LEVEL_OFFSET - data byte Eh bit description

Bit	Symbol	Description
7	-	not used, must be set to logic 0
6 to 0	LEVO[6:0]	level offset control[1]
		0 to 127 = correction of the digital level information equivalent to a level voltage shift of −1 V to +1 V

[1] The level offset can be used to correct for active antenna gain and noise level. The level correction influences the weak signal processing and the LEVEL read data via I^2C-bus. The level correction does not influence the analog voltage at pin RSSI.

8.2.18 Write mode: data byte AM_LNA

Table 69. AM_LNA - data byte Fh bit allocation with default setting

7	6	5	4	3	2	1	0
0	0	AAITT	ALAMT	0	CHSEP2	CHSEP1	CHSEP0
		0	0		1	0	0

Table 70. AM_LNA - data byte Fh bit description

Bit	Symbol	Description
7 and 6	-	not used, must be set to logic 0
5	AAITT	AM auto-injection test time
		0 = 4 ms AM mirror measurement time at auto-injection tuning
		1 = 8 ms AM mirror measurement time at auto-injection tuning
4	ALAMT	AM LNA AGC mute time; audio mute and fast AGC settling at AM LNA AGC step
		0 = 4 ms
		1 = 7 ms
3	-	not used, must be set to logic 0
2 to 0	CHSEP[2:0]	stereo channel separation alignment
		100 = default setting (no alignment)
		000 to 111 = optional channel separation

8.2.19 Write mode: data byte RDS

Table 71. RDS - data byte 10h bit allocation with default setting

7	6	5	4	3	2	1	0
NWSY	TUSY	0	0	0	0	0	0
0	1						

Table 72. RDS - data byte 10h bit description

Bit	Symbol	Description
7	NWSY	manual RDS demodulator reset control
		0 = normal operation
		1 = demodulator reset; start new demodulator synchronization, falls back to logic 0[1]
6	TUSY	automatic RDS demodulator reset control
		0 = no automatic reset
		1 = automatic demodulator reset at tuning[1]
5 to 0	-	not used, must be set to logic 0

[1] Fastest demodulator locking to a new RDS transmission can be achieved by RDS reset. TUSY automatic RDS start is active for tuning actions of preset (MODE[2:0] = 001), search (MODE[2:0] = 010), jump (MODE[2:0] = 100) and check (MODE[2:0] = 101).

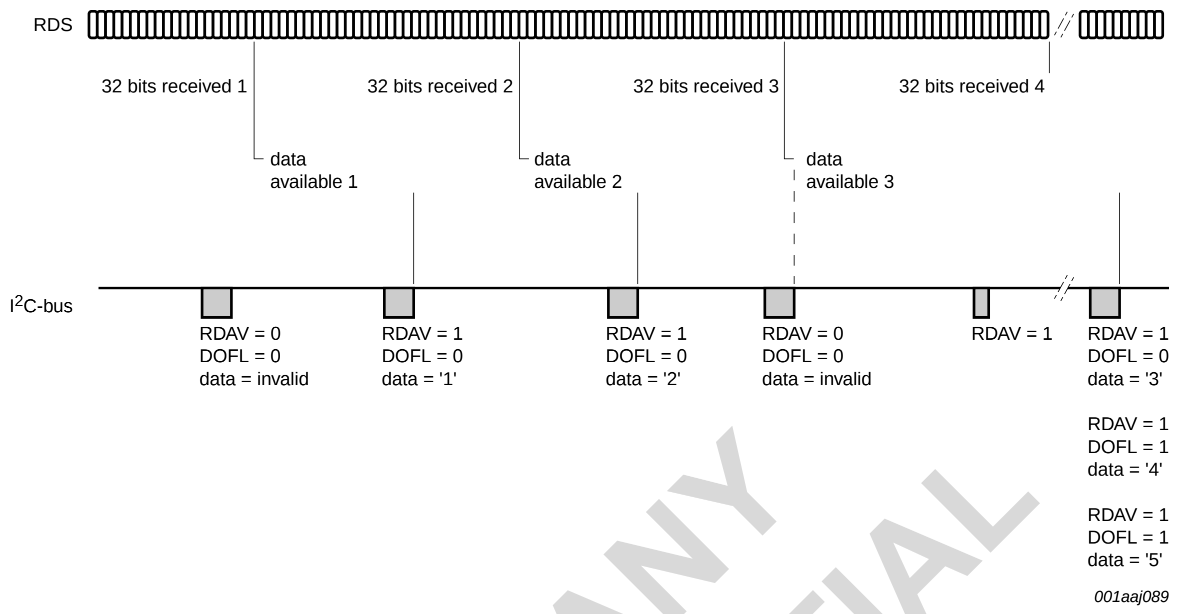


Fig 29. Example of RDS status and data by I²C-bus read

Two possible application modes of operation are supported by the TEF6614:

1. Non synchronized operation 1:

   Repeated I²C-bus read not including RDS data of read data byte 6h and higher, but checking data available status of bit RDAV in read data byte 0h or 5h

   After RDAV = 1 is read out, a full I²C-bus read including read data byte 6h and higher is performed to read the RDS data

2. Non synchronized operation 2:

   Repeated I²C-bus read including RDS data of read data byte 6h and higher

   When RDAV = 1 is read out, the RDS data is used, otherwise ignored

   To avoid data loss an I²C-bus read should be performed at least every 32 bits of RDS reception, i.e. $\leq$ 26 ms

In case of data loss, indicated by DOFL = 1, a minimum of 32 bits is lost, or a multiple of 32 bits depending on the read timing.

8.2.20 Write mode: data byte EXTRA

Table 73. EXTRA - data byte 11h bit allocation with default setting

7	6	5	4	3	2	1	0
0	0	0	0	FFL	0	0	0
				0			

Table 74. EXTRA - data byte 11h bit description

Bit	Symbol	Description
7 to 4	-	not used, must be set to logic 0
3	FFL	FM fast level mode
		0 = normal operation
		1 = for MODE[2:0] = 011 fast AF update tuning with instant I^2C-bus read data byte 1h bits LEV[7:0] result; only 4 ms full mute time with INJ[1:0] = 01 or 10; WAM, USN and IFC quality read are not supported; for MODE[2:0] = 001 to 110 instant I^2C-bus read data byte 1h bits LEV[7:0] result directly after tuning (QRS[1:0] = 00, TAS[1:0] = 00 or 11), followed by standard averaged LEV[7:0] result after 1 ms (QRS[1:0] = 01)
2 to 0	-	not used, must be set to logic 0

9. Limiting values

Table 75. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	on pins V_{CC1} and V_{CC2}	−0.3	+10	V
ΔV_{CCn}	voltage difference between any supply pins	between pins V_{CC1} and V_{CC2}	−0.3	+0.3	V
V_{FMIN1}	voltage on pin FMIN1		−0.3	+6	V
V_{FMIN2}	voltage on pin FMIN2		−0.3	+6	V
$\Delta V_{(FMIN1-FMIN2)}$	voltage difference between pin FMIN1 and pin FMIN2		−1.5	+1.5	V
V_{SCL}	voltage on pin SCL		−0.3	+6	V
V_{SDA}	voltage on pin SDA		−0.3	+6	V
$V_{AMRFDEC}$	voltage on pin AMRFDEC		−0.3	+6	V
V_{AMRFIN}	voltage on pin AMRFIN		−0.3	+6	V
$V_{AMRFAGC}$	voltage on pin AMRFAGC		−0.3	+6	V
$V_{AMIFAGC2}$	voltage on pin AMIFAGC2		−0.3	+6	V
V_{RSSI}	RSSI voltage		−0.3	+6	V
V_{VCODEC}	voltage on pin VCODEC		−0.3	+6	V
V_{PLL}	voltage on pin PLL		−0.3	+6	V
V_{PLLREF}	voltage on pin PLLREF		−0.3	+6	V
V_{TEST}	voltage on pin TEST		−0.3	+6	V
$V_{AMIFAGC1}$	voltage on pin AMIFAGC1		−0.3	+6	V
V_{VREF}	voltage on pin VREF		−0.3	+6	V
V_n	voltage on any other pin		−0.3	$+V_{CC}$	V
T_{stg}	storage temperature		−40	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	human body model [1]	−2000	+2000	V
		machine model [2]	−200	+200	V

[1] Class 2 according to JESD22-A114.

[2] Class B according to EIA/JESD22-A115.

10. Thermal characteristics

Table 76. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; single layer board with a copper thickness of 35 μm; see Figure 31	[1]	48	K/W
$\Psi_{j\text{-}top}$	thermal characterization parameter from junction to top of package			4.5	K/W

[1] The thermal resistance depends strongly on the PCB design. An application different to Figure 31 must ensure that the thermal resistance is below 54 K/W to avoid violation of the maximum junction temperature; see Table 75.

11. Static characteristics

Table 77. Static characteristics

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	on pins V_{CC1} and V_{CC2}		8	8.5	9	V
I_{CC}	supply current	into pins V_{CC1}, V_{CC2} and VREGSUP					
		FM		90	120	140	mA
		AM		100	134	150	mA
$V_{VREGSUP}$	voltage on pin VREGSUP	V_{CC} = 8.0 V; T_{amb} = −40 °C to +85 °C		6.35	-	-	V
Power-on reset							
$V_{P(POR)}$	power-on reset supply voltage	reset at power-on		6.5	6.75	7.0	V
$V_{hys(POR)}$	power-on reset hysteresis voltage			-	0.2	-	V
t_{start}	start time	series resistance of crystal R_s = 150 Ω		-	10	100	ms
Logic pin TEST							
V_{OL}	LOW-level output voltage	I_{sink} = 3 mA		-	-	0.4	V
Logic pins SDA and SCL (voltage referenced to pin GNDD)							
V_{IH}	HIGH-level input voltage		[1]	1.58	-	5.5	V
V_{IL}	LOW-level input voltage		[1]	−0.5	-	+1.04	V

[1] SDA and SCL HIGH and LOW internal thresholds are specified according to an I^2C-bus voltage of 2.5 V ± 10 % or 3.3 V ± 5 %. The I^2C-bus interface tolerates also SDA and SCL signals from a 5 V I^2C-bus, but does not fulfill the 5 V I^2C-bus specification completely. The TEF6614 complies with the fast-mode I^2C-bus protocol. The maximum I^2C-bus communication speed is 400 kbit/s.

12. Dynamic characteristics

Table 78. Dynamic characteristics

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 µs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Crystal oscillator; pins XTAL1 and XTAL2							
f_{xtal}	crystal frequency	fundamental frequency		-	4	-	MHz
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	device inaccuracy		–45	-	+45	10^{-6}
C_i	input capacitance	input capacitance from pin XTAL1 and pin XTAL2 to ground		1	3	4	pF
R_i	input resistance			-	-	–750	Ω
Tuning system							
C/N_{LO}	LO carrier-to-noise ratio	f_{LO} = 100 MHz; Δf = 10 kHz		-	98	-	dBc/√Hz
t_{tune}	tuning time	FM (Europe/USA/Japan) f_{RF} = 87.5 MHz to 108 MHz		-	1.8	2	ms
		FM (OIRT) f_{RF} = 65 MHz to 74 MHz		-	6.8	7	ms
		AM (MW) f_{RF} = 0.53 MHz to 1.7 MHz		-	9	9.2	ms
		AM (LW) f_{RF} = 0.144 MHz to 0.288 MHz		-	3.5	3.7	ms
		AM (SW) f_{RF} = 2.94 MHz to 18.135 MHz		-	3.5	3.7	ms
f_{RF}	RF frequency	FM tuning range		65	-	108	MHz
		AM (LW) tuning range		144	-	288	kHz
		AM (MW) tuning range		522	-	1710	kHz
		AM (SW) tuning range		2.94	-	18.135	MHz
$f_{tune(step)}$	step of tuning frequency	FM (Europe/USA/Japan)		-	50	-	kHz
		FM (OIRT)		-	10	-	kHz
		AM (LW and MW)		-	1	-	kHz
		AM (SW)		-	5	-	kHz
FM path							
$V_{i(sens)}$	input sensitivity voltage	(S+N)/N = 26 dB; without weak signal handling		-	5.5	-	dBµV
		(S+N)/N = 26 dB; including weak signal handling		-	5	-	dBµV
		(S+N)/N = 46 dB; including weak signal handling		-	16	-	dBµV
NF	noise figure			-	6	9	dB
$V_{L(LO)}$	LO leakage voltage	LO residue at antenna input; $R_{source(ant)}$ = 75 Ω	[1]	-	–6	-	dBµV

Table 78. Dynamic characteristics *...continued*
V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{sp(VCO)}$	VCO spurious voltage	VCO residue at antenna input; $R_{source(ant)}$ = 75 Ω	-	46	60	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 1 mV; Δf = 22.5 kHz	55	60	-	dB
α_{ripple}	ripple rejection	V_{ripple} / V_{audio}; V_{ripple} = 100 mV; f_{ripple} = 100 Hz	34	44	-	dB
f_{IF}	IF frequency		-	150	-	kHz
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	50	60	-	dB
IP3	third-order intercept point	$f_{RF(unw)1}$ = 97.5 MHz; $f_{RF(unw)2}$ = 97.9 MHz; $V_{i(RF)}$ = 80 dBμV	106	113	-	dBμV
S_{dyn}	dynamic selectivity	$V_{i(RF)}$ = 10 μV; $\Delta f_{RF(unw)}$ = 22.5 kHz; (S+N)/N = 26 dB; mono; f_{AF} = 1 kHz				
		Δf_{RF} = 100 kHz; PACS disabled	-	3	-	dB
		Δf_{RF} = 200 kHz; PACS disabled	-	55	-	dB
		Δf_{RF} = 100 kHz; PACS enabled	-	24	-	dB
		Δf_{RF} = 200 kHz; PACS enabled	-	64	-	dB
S_{stat}	static selectivity	maximum IF bandwidth; $f_{i(RF)}$ ± 100 kHz	10	14	25	dB
		maximum IF bandwidth; $f_{i(RF)}$ ± 200 kHz	54	64	-	dB
		maximum IF bandwidth; $f_{i(RF)}$ ± 300 kHz (excluding image)	65	75	-	dB
		minimum IF bandwidth; $f_{i(RF)}$ ± 100 kHz	30	38	-	dB
		minimum IF bandwidth; $f_{i(RF)}$ ± 200 kHz	63	73	-	dB
$\alpha_{sup(AM)}$	AM suppression	AM: f_{AF} = 1 kHz; m = 30 %				
		$V_{i(RF)}$ = 0.05 mV to 20 mV	45	55	-	dB
		$V_{i(RF)}$ = 20 mV to 500 mV	40	50	-	dB
$V_{start(desens)}$	desensitization start voltage	unwanted signal voltage for 6 dB desensitization; $\lvert f_{RF(unw)} - f_{RF(wanted)} \rvert$ > 400 kHz; $V_{i(RF)wanted}$ = 30 dBμV; data byte 2h bits RFAGC[1:0] = 00	-	90	-	dBμV
V_{sp}	spurious voltage	at antenna input; $R_{source(ant)}$ = 75 Ω				
		30 MHz < f < 1 GHz	-	-	50	dBμV
		1 GHz < f < 12.75 GHz	-	-	60	dBμV

Table 78. Dynamic characteristics *...continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM front-end; pins FMIN1 and FMIN2						
$R_{i(dif)}$	differential input resistance	f_{RF} = 97.1 MHz; maximum gain	200	300	400	Ω
$C_{i(dif)}$	differential input capacitance	f_{RF} = 97.1 MHz	-	4	7	pF
FM RF AGC						
$V_{start(AGC)}$	AGC start voltage	RF input voltage for first AGC step; $V_{i(RF)}$ value, at which the RF gain decreases by 6 dB with increasing $V_{i(RF)}$; data byte 2h				
		bits RFAGC[1:0] = 00	83	86	89	dBμV
		bits RFAGC[1:0] = 01	81	84	87	dBμV
		bits RFAGC[1:0] = 10	79	82	85	dBμV
		bits RFAGC[1:0] = 11	77	80	83	dBμV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	-	5	dB
$\alpha_{cr(AGC)}$	AGC control range	from step 1 (first AGC step) to step 8 (last AGC step)	39	44	-	dB
FM IF AGC						
$V_{i(RF)AGC}$	AGC RF input voltage	$V_{i(RF)}$ value, at which the IF gain decreases by 6 dB with increasing $V_{i(RF)}$; start of AGC; first step	71	76	81	dBμV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	-	6	dB
FM RSSI; pin RSSI						
V_{RSSI}	RSSI voltage	$V_{i(RF)}$ = −20 dBμV	0.65	0.8	0.95	V
		$V_{i(RF)}$ = 20 dBμV	1.65	1.9	2.15	V
		$V_{i(RF)}$ = 40 dBμV	2.6	2.9	3.2	V
		$V_{i(RF)}$ = 60 dBμV	3.45	3.75	4.1	V
$\Delta V_{RSSI}/\Delta L_{i(RF)}$	RSSI voltage difference to RF input level difference ratio	between $V_{i(RF)}$ = 20 dBμV and $V_{i(RF)}$ = 40 dBμV	45	50	55	mV/dB
FM IF counter						
$V_{i(sens)}$	input sensitivity voltage	$V_{i(RF)}$ at which IF counter starts; Δf = 0 Hz	-	2	5	μV
$f_{IFc(res)}$	IF counter frequency resolution		-	5	-	kHz
FM demodulator; pin MPXOUT						
R_o	output resistance		-	-	100	Ω
R_L	load resistance		5	-	-	kΩ
C_L	load capacitance		-	-	20	pF
Δf_{max}	maximum frequency deviation	THD = 3 %; $V_{i(RF)}$ = 10 mV	115	140	-	kHz

Table 78. Dynamic characteristics *...continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_o	output voltage	Δf = 22.5 kHz; f_{AF} = 1 kHz	155	230	300	mV
Audio part; pin MPXIN						
R_i	input resistance	data byte 3h bit LOCUT = 0 (FM or AM)	-	220	-	kΩ
		data byte 3h bit LOCUT = 1 (AM)	-	16	-	kΩ
$\alpha_{bal(ch)}$	channel balance	balance between R and L channel	−1	-	+1	dB
$\alpha_{sup(pilot)}$	pilot suppression	9 % pilot; f_{pilot} = 19 kHz; referenced to 91 % FM modulation	30	40	-	dB
m_{pilot}	modulation degree of pilot tone	threshold for pilot detection				
		stereo on	2	3.9	5.8	%
		stereo off	1.2	3.1	5	%
$\alpha_{hys(pilot)}$	pilot hysteresis		0.7	0.8	1.6	%
$t_{det(pilot)}$	pilot detection time		-	30	100	ms
Audio output; pins LOUT and ROUT						
V_o	output voltage	Δf = 22.5 kHz; f_{AF} = 1 kHz				
		data byte 3h bit OUTA = 1	200	290	410	mV
		data byte 3h bit OUTA = 0	80	120	175	mV
α_{AF}	AF attenuation	mono; pre-emphasis = 50 μs; referenced to f_{AF} = 1 kHz; without *IEC 60315-4* tuner filter				
		f_{AF} = 50 Hz	−0.6	−0.1	+0.4	dB
		f_{AF} = 15 kHz	−1.5	0	+1.5	dB
α_{cs}	channel separation	$V_{i(RF)}$ = 1 mV; data byte Fh bits CHSEP[2:0] = 100	26	40	-	dB
THD	total harmonic distortion	mono; Δf = 75 kHz; $V_{i(RF)}$ = 1 mV	-	0.4	0.8	%
		stereo; Δf = 67.5 kHz; L or R	-	-	1	%
R_L	load resistance		10	-	-	kΩ
C_L	load capacitance		-	-	20	pF
FM noise blanker						
(S+N)/N	signal plus noise-to-noise ratio	noise pulses at RF input signal t_p = 5 ns; t_r < 1 ns; t_f < 1 ns; f_p = 100 Hz; V_p = 500 mV; $V_{i(RF)}$ = 40 dBμV; quasi peak; audio filter according *“ITU-R BS.468-4”*	-	30	-	dB

Table 78. Dynamic characteristics *...continued*
V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RDS						
$V_{i(sens)}$	input sensitivity voltage	for 50 % block quality RDS reception; Δf_{RDS} = 2 kHz; AF = stereo; Δf = 22.5 kHz	-	17	-	dBμV
		for 95 % block quality RDS reception; Δf_{RDS} = 2 kHz; AF = stereo; Δf = 22.5 kHz	-	20	-	dBμV
AM path						
$V_{i(sens)}$	input sensitivity voltage	S/N = 26 dB; data byte 3h bits DEMP[1:0] = 10				
		MW	-	34	-	dBμV
		LW	-	40	-	dBμV
		SW	-	35	-	dBμV
$V_{n(i)(eq)}$	equivalent input noise voltage	C_{source} = 100 pF	-	1	-	nV/√Hz
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 10 mV	50	56	-	dB
f_{IF}	IF frequency		-	25	-	kHz
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	45	55	-	dB
$\alpha_{sup(H)LO}$	LO harmonics suppression	$f_{RF(unw)} = N \times (f_{RF(wanted)} \pm f_{IF}) \pm f_{IF}$; MW				
		N = 2, 3, 4, 5, 6	-	90	-	dB
		N ≥ 7	-	50	-	dB
$V_{L(LO)}$	LO leakage voltage	LO residue at antenna input; load capacitance at antenna input: C_{ant} = 85 pF	-	−6	-	dBμV
$B_{fltr(IF)}$	IF filter bandwidth	−3 dB bandwidth	5	6.5	8	kHz
S_{stat}	static selectivity	f_{tune} ± 10 kHz	40	48	-	dB
		f_{tune} ± 20 kHz	65	78	-	dB
$V_{i(RF)(max)}$	maximum RF input voltage	THD = 10 %; m = 80 %; active antenna 50 Ω	120	135	-	dBμV
IP2	second-order intercept point		150	170	-	dBμV
IP3	third-order intercept point	Δf = 40 kHz	116	127	-	dBμV
AM LNA and AM RF AGC; input pins AMRFIN and AMRFDEC						
R_i	input resistance	f_{RF} = 990 kHz	-	20	-	Ω
C_i	input capacitance	AGC maximum gain [2][3]	-	530	-	pF
MW band with passive antenna (measured with dummy aerial 15 pF/60 pF)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; m = 0 %; start of AGC; first step	110	113	116	dBμV

Table 78. Dynamic characteristics *...continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 µs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	4	7	dB
MW band with active antenna (measured with dummy aerial 50 Ω)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; m = 0 %; start of AGC; first step	78	81	84	dBµV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	3	6	dB
LW band with passive antenna (measured with dummy aerial 15 pF/60 pF)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; f_{RF} = 207 kHz; m = 0 %; start of AGC; first step	-	104	-	dBµV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	4	7	dB
LW band with active antenna (measured with dummy aerial 50 Ω)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; f_{RF} = 207 kHz; m = 0 %; start of AGC; first step	-	72	-	dBµV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	4	7	dB
SW bands with passive antenna (measured with dummy aerial 15 pF/60 pF)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; f_{RF} = 6.1 MHz; m = 0 %; start of AGC; first step	-	101	-	dBµV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	4	7	dB
SW bands with active antenna (measured with dummy aerial 50 Ω)						
$V_{i(RF)AGC}$	AGC RF input voltage	switched LNA AGC: $V_{i(RF)}$ value, at which the LNA gain decreases with increasing $V_{i(RF)}$; f_{RF} = 6.1 MHz; m = 0 %; start of AGC; first step	-	78	-	dBµV
$V_{i(RF)AGC(hys)}$	hysteresis of AGC RF input voltage	hysteresis of AGC start	1	4	7	dB

Table 78. Dynamic characteristics *...continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Continuous AM RF AGC						
$V_{i(RF)AGC}$	AGC RF input voltage	linear RF AGC: $V_{i(RF)}$ at which AGC starts; m = 0 %				
		data byte 2h bits RFAGC[1:0] = 00	87	90	93	dBμV
		data byte 2h bits RFAGC[1:0] = 01	85	88	91	dBμV
		data byte 2h bits RFAGC[1:0] = 10	83	86	89	dBμV
		data byte 2h bits RFAGC[1:0] = 11	81	84	87	dBμV
t_s	settling time	$V_{i(RF)}$ = 10 mV to 200 mV	-	200	-	ms
		$V_{i(RF)}$ = 200 mV to 10 mV	-	1.4	-	s
$I_{source(AGC)}$	AGC source current	AGC attack; $V_{i(RF)M}$ = 105 dBμV (peak); normal mode	25	35	50	μA
		AGC attack; fast mode after tuning and AGC switching	1.1	1.4	1.7	mA
$I_{sink(AGC)}$	AGC sink current	AGC release; normal mode	0.7	1	1.4	μA
		AGC release; fast mode after tuning and AGC switching	17.5	25	35	μA
Continuous IF AGC 1						
$V_{i(RF)AGC}$	AGC RF input voltage	linear IF AGC 1: $V_{i(RF)}$ at which AGC starts; m = 0 %	59	62	65	dBμV
$I_{source(AGC)}$	AGC source current	AGC attack; $V_{i(RF)M}$ = 80 dBμV (peak); normal mode	31	61	92	μA
		AGC attack; fast mode after tuning and AGC switching	0.875	1.25	1.75	mA
$I_{sink(AGC)}$	AGC sink current	AGC release; normal mode	0.7	1	1.4	μA
		AGC release; fast mode after tuning and AGC switching	17.5	25	35	μA
Continuous IF AGC 2						
$V_{i(RF)AGC}$	AGC RF input voltage	linear IF AGC 2: $V_{i(RF)}$ at which AGC starts; m = 0 %	19	22	25	dBμV
$I_{source(AGC)}$	AGC source current	AGC attack; $V_{i(RF)M}$ = 50 dBμV (peak); normal mode	4	6	8	μA
		AGC attack; fast mode after tuning and AGC switching	100	150	200	μA

Table 78. Dynamic characteristics *...continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{sink(AGC)}$	AGC sink current	AGC release; normal mode	0.7	1	1.4	μA
		AGC release; fast mode after tuning and AGC switching	17.5	25	35	μA
AM demodulator; pin MPXOUT						
V_o	output voltage	m = 30 %	150	230	330	mV
Audio output; pins LOUT and ROUT						
V_o	output voltage	m = 30 %; f_{AF} = 400 Hz; data byte 3h bits DEMP[1:0] = 10				
		data byte 3h bit OUTA = 1	200	270	355	mV
		data byte 3h bit OUTA = 0	85	115	150	mV
α_{AF}	AF attenuation	referenced to f_{AF} = 400 Hz; 210 mV input at pin MPXIN				
		f_{AF} = 100 Hz; data byte 3h bit LOCUT = 1	−4.5	−3	−1.5	dB
		f_{AF} = 1.5 kHz; data byte 3h bits DEMP[1:0] = 10	−4.5	−3	−2	dB
		f_{AF} = 5 kHz; data byte 3h bits DEMP[1:0] = 10	−24	−21	−18	dB
		f_{AF} = 6 kHz; data byte 3h bits DEMP[1:0] = 10	−27	−24	−21	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 1 mV; m = 80 %	-	0.7	1	%
α_{ripple}	ripple rejection	V_{ripple} / V_{audio}; V_{ripple} = 100 mV; f_{ripple} = 100 Hz	30	37	-	dB
AM noise blanker						
SINAD	signal-to-noise-and-distortion ratio	m = 30 %; f_{AF} = 1 kHz; noise pulses at RF input signal t_p = 100 ns; t_r < 1 ns; t_f < 1 ns; f_p = 100 Hz; V_p = 500 mV; $V_{i(RF)}$ = 40 dBμV	-	12	-	dB
AM RSSI; pin RSSI						
V_{RSSI}	RSSI voltage	$V_{i(RF)}$ = −20 dBμV at dummy aerial input	0.95	1.15	1.35	V
		$V_{i(RF)}$ = 14 dBμV at dummy aerial input	1.7	1.9	2.1	V
		$V_{i(RF)}$ = 34 dBμV at dummy aerial input	2.65	2.9	3.15	V
		$V_{i(RF)}$ = 54 dBμV at dummy aerial input	3.5	3.8	4.1	V
$\Delta V_{RSSI}/\Delta L_{i(RF)}$	RSSI voltage difference to RF input level difference ratio	5 μV < $V_{i(RF)}$ < 50 μV	45	50	55	mV/dB

Table 78. Dynamic characteristics *…continued*

V_{CC} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.
FM condition: all RF voltages refer to an unterminated RMS voltage with a source impedance 75 Ω; f_{mod} = 1 kHz, Δf = 22.5 kHz, de-emphasis = 50 μs, f_{RF} = 97.1 MHz; unless otherwise specified.
AM condition: all RF voltages are RMS values measured at the input of a 15 pF/60 pF dummy aerial; f_{mod} = 400 Hz, m = 30 %, f_{RF} = 990 kHz; unless otherwise specified.
All values measured in a test circuit according to Figure 32; default settings; audio signals measured at LOUT and ROUT with IEC tuner filter (200 Hz to 15 kHz; IEC 60315-4); unless otherwise specified.

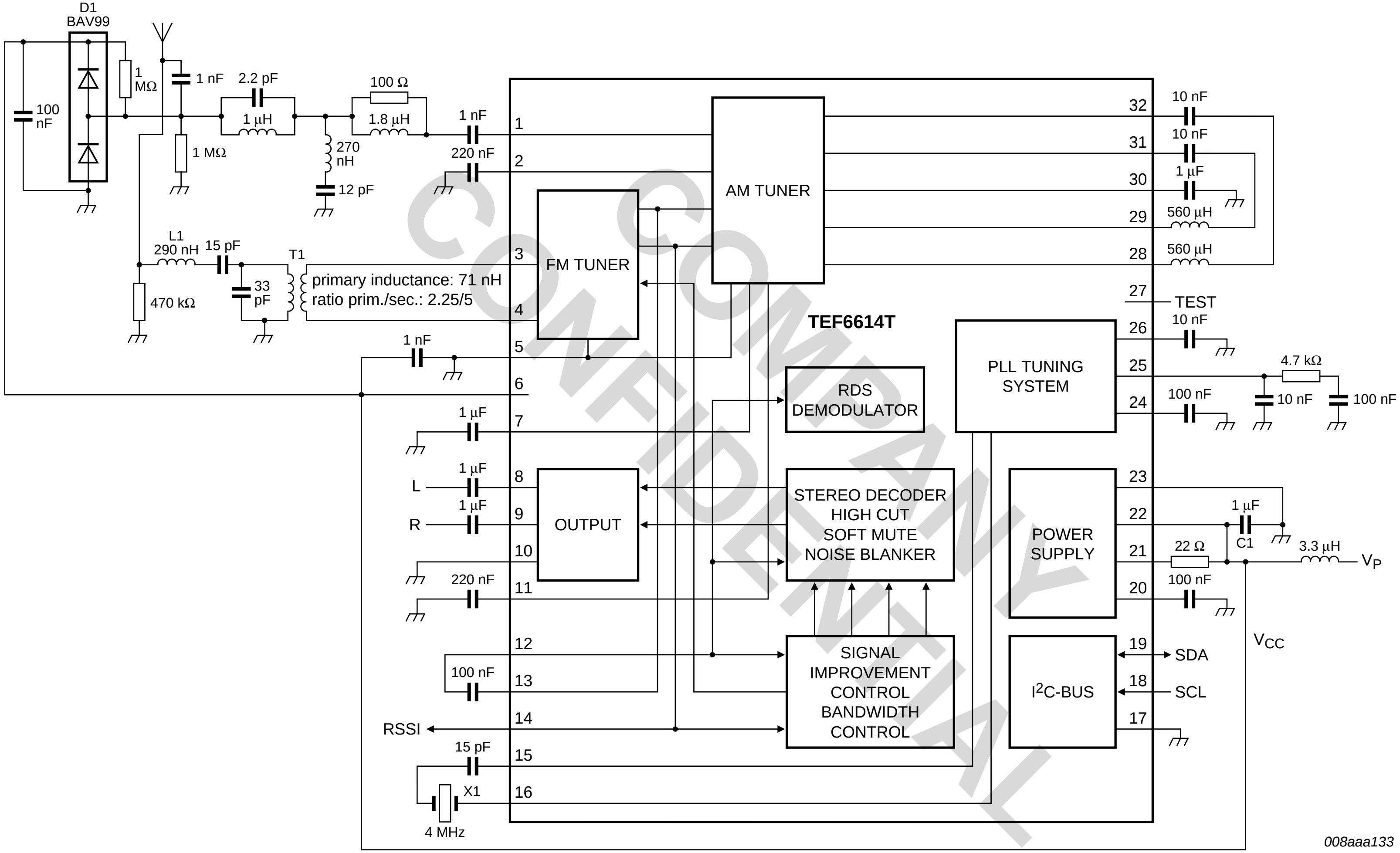
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM IF counter						
$V_{i(sens)}$	input sensitivity voltage	$V_{i(RF)}$ at which IF counter starts; m = 0 %	-	14	20	dBμV
$f_{IFc(res)}$	IF counter frequency resolution		-	500	-	Hz

[1] $f_{LO} = f_{RF} + f_{IF}$ for high injection and $f_{LO} = f_{RF} - f_{IF}$ for low injection.

[2] The switched input capacitance is part of the switched RF AGC function.

[3] The input impedance of the AM LNA depends on the AGC state.

13. Application information



For list of components see Table 79 and for crystal specification see Table 80.

Fig 30. Application diagram of TEF6614T

13.1 Printed-circuit board

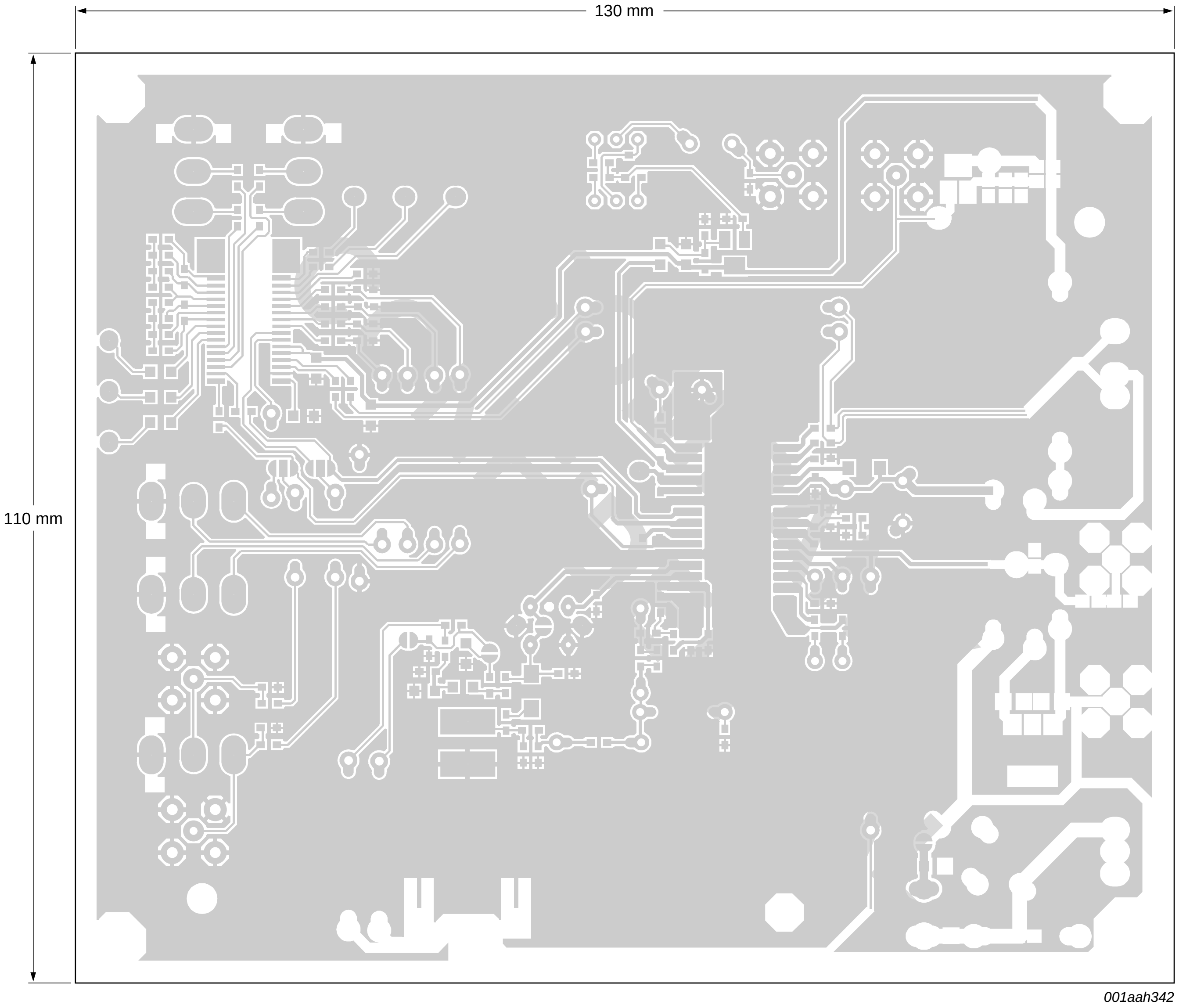
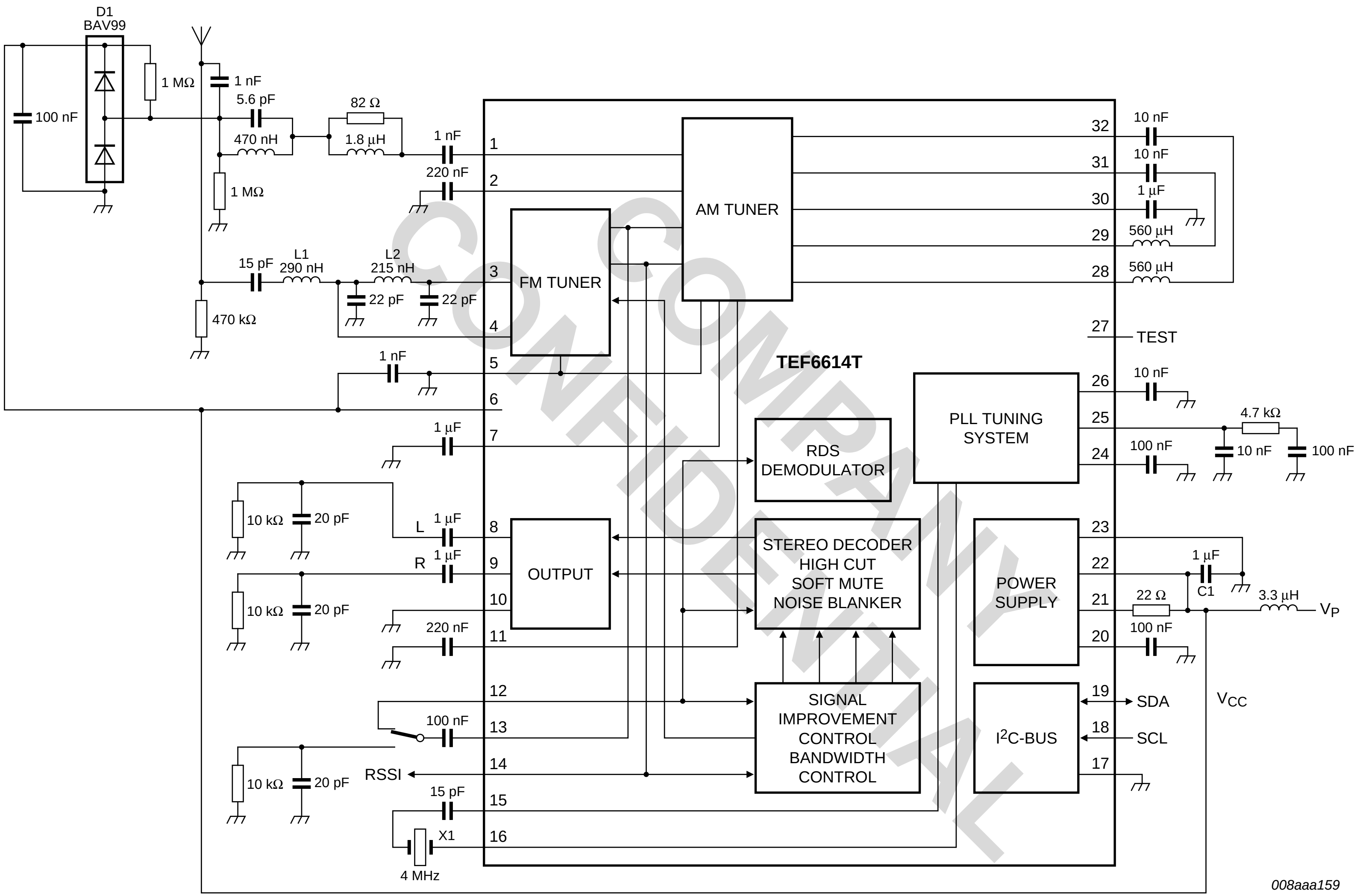


Fig 31. Printed-circuit board layout, suggested for application (this layout has been used in the NXP GH989 reference design, 35 μm)

14. Test information



For list of components see Table 79 and for crystal specification see Table 80.

Fig 32. Test circuit of TEF6614T

Table 79. List of components for Figure 30 and Figure 32

Symbol	Component	Type	Manufacturer
C1	decoupling capacitor	1 μF; X7R 0805	any
D1	ESD protection diode	BAV99	NXP Semiconductors
L1	FM RF input 1	290 nH; LQH31HNR29K03L	Murata
L2	FM RF input 2	215 nH; LQH31HNR21K01L	Murata
T1	transformer	#P600ENS-10959QH	TOKO
X1	crystal 4 MHz	LN-G102-1413	NDK

Table 80. 4 MHz crystal specification for Figure 30 and Figure 32

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	fundamental frequency	-	4.000	-	MHz
C_L	load capacitance		-	18	-	pF
C_{shunt}	shunt capacitance		-	-	7	pF
C_1	motional capacitance		-	10	-	fF
R_s	series resistance		-	-	150	Ω
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	at 25 °C	−25	-	+25	10^{-6}
		caused by ageing	−5	-	+5	10^{-6}
		caused by temperature	−30	-	+30	10^{-6}
T_{amb}	ambient temperature		−40	-	+85	°C

Table 81. DC operating points

V_{CC} = 8.5 V; $V_{i(RF)}$ = 0 μV; audio output gain low; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
AMRFIN	1	-	2.9	-	-	-	-
AMRFDEC	2	-	4.2	-	-	-	-
FMIN2	3	-	-	-	-	3.1	-
FMIN1	4	-	-	-	-	3.1	-
GNDRF	5	external GND			external GND		
V_{CC2}	6	external 8.5			external 8.5		
AMRFAGC	7	-	1.8	-	-	-	-
LOUT	8	-	3.8	-	-	3.8	-
ROUT	9	-	3.8	-	-	3.8	-
GNDAUD	10	external GND			external GND		
AMIFAGC2	11	-	-	-	-	-	-
MPXIN	12	-	3.7	-	-	3.7	-
MPXOUT	13	-	4	-	-	4	-
RSSI	14	-	1.2	-	-	0.8	-
XTAL2	15	-	6	-	-	6	-
XTAL1	16	-	6	-	-	6	-
GNDD	17	external GND			external GND		

Table 81. DC operating points *...continued*

V_{CC} = 8.5 V; $V_{i(RF)}$ = 0 μV; audio output gain low; unless otherwise specified.

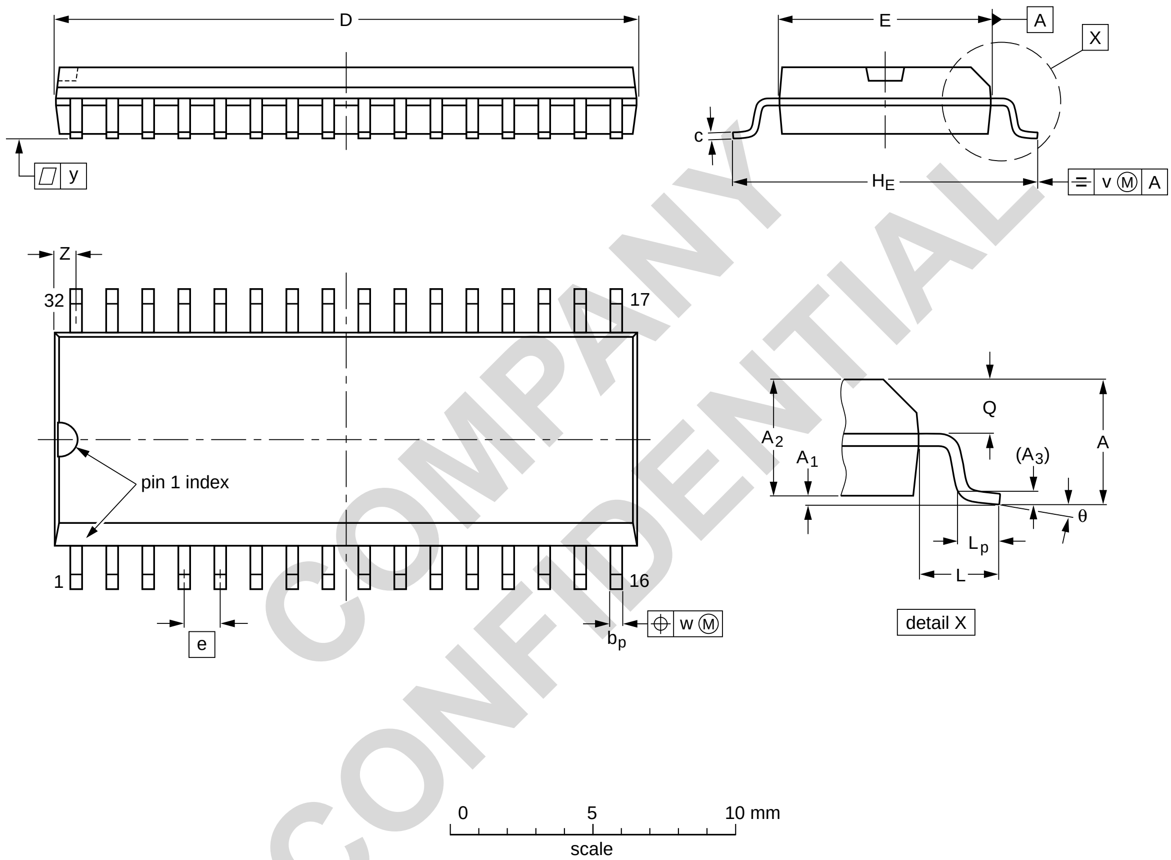
Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
SCL	18	external I²C-bus voltage			external I²C-bus voltage		
SDA	19	external I²C-bus voltage			external I²C-bus voltage		
VREF	20	3.9	4.0	4.1	3.9	4.0	4.1
VREGSUP	21	6.85	7.1	7.5	6.85	7.1	7.5
V_{CC1}	22	external 8.5			external 8.5		
GND	23	external GND			external GND		
VCODEC	24	-	5.7	-	-	5.7	-
PLL	25	1.2	-	5.5	1.2	-	5.5
PLLREF	26	-	2.25	-	-	2.25	-
TEST	27	0	-	5.5	0	-	5.5
AMSELIN1	28	1.2	1.55	1.9	-	-	-
AMSELIN2	29	1.2	1.55	1.9	-	-	-
AMIFAGC1	30	-	3	-	-	-	-
AMSELOUT1	31	6.5	6.8	7.15	-	-	-
AMSELOUT2	32	6.5	6.8	7.15	-	-	-

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 33. Package outline SOT287-1 (SO32)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 82 and 83

Table 82. SnPb eutectic process (from J-STD-020C)

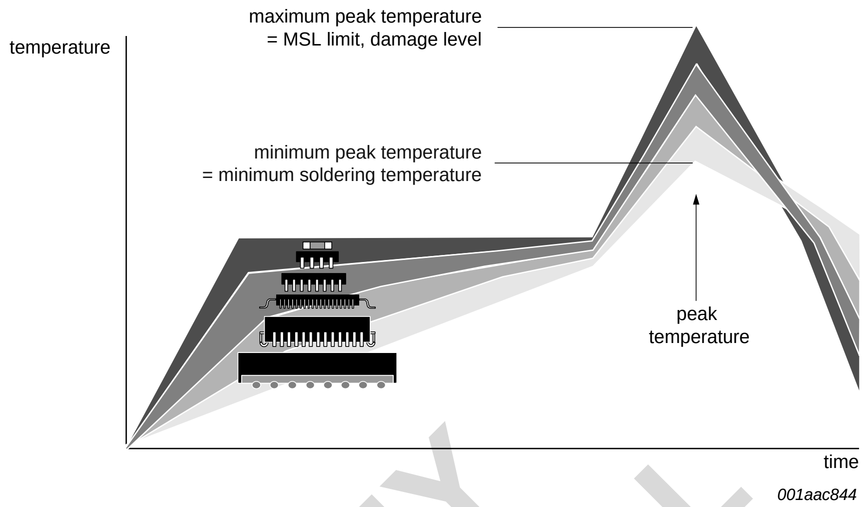
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 83. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



MSL: Moisture Sensitivity Level

Fig 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Appendix

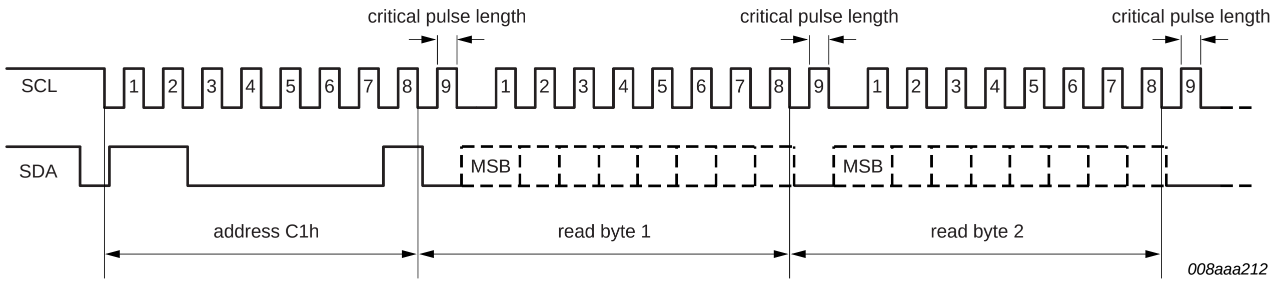
17.1 Erratum 1

In I²C-bus fast mode and under special conditions the Most Significant Bit (MSB) read information (see Section 8) from the TEF6614 can be incorrect. This can occur when the acknowledge clock pulse becomes short.

17.1.1 Problem description

The length of the I²C-bus clock pulse during acknowledge (see Figure 35) is critical for the TEF6614. When these clock pulses become short during I²C-bus readout (typically less than 1.2 μs), the MSBs can have a wrong value.

This pulse length is only critical during I²C-bus readout; for I²C-bus writing there are no special considerations.



The acknowledge clock pulse and the MSBs are shown.

Fig 35. I²C-bus traffic

17.1.2 Implication

This means if high I²C-bus speeds (greater than 100 kbit/s) are used, the length of the acknowledge clock pulse has to be verified and maybe adjusted. It should be more than 1.5 µs (see Section 17.1.3 for more details). The TEF6614 is not in line with the fast mode I²C-bus specification in this respect. On all other items, such as the timing requirements of other pulses, the TEF6614 complies with the fast mode I²C-bus specification.

With an advanced implementation of the workaround 400 kbit/s can be achieved, but the combination of platform limitations and this new constraint can limit the speed to lower values.

17.1.3 Workaround

To ensure a correct value of the MSB, all acknowledge clock pulses during reading should be at least 1.5 µs long. This time refers to the time the I²C-bus master sets the clock level to HIGH. Furthermore the parameters of the I²C-bus should be equal or better than the parameters mentioned at the end of this section.

To achieve fastest I²C-bus communication, only the indicated acknowledge clock pulse should show a width of 1.5 µs while the other clock pulses can be shorter. Alternatively, a fixed length for all clock pulses can be used and the duty cycle and clock speed are chosen such that the 1.5 µs requirement is fulfilled.

The 1.5 µs pulse width refers to 60 pF capacitance to ground and pull-up resistors of 4.7 kΩ for 3.3 V or 5 V I²C-bus voltage or 2.2 kΩ for 2.5 V I²C-bus voltage. Lower values for the capacitance or pull-up resistors will result in better I²C-bus characteristics.

18. Abbreviations

Table 84. Abbreviations

Acronym	Description
AF	Audio Frequency
AGC	Automatic Gain Control
ESD	ElectroStatic Discharge
HCC	High-Cut Control
I^2C-bus	Inter IC bus
IF	Intermediate Frequency
LNA	Low-Noise Amplifier
LO	Local Oscillator
LW	Long Wave
MPX	Multiplex
MSB	Most Significant Bit
MW	Medium Wave
PACS	Precision Adjacent Channel Suppression
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RSSI	Received Signal Strength Indication
SW	Short Wave
USN	UltraSonic Noise
VCO	Voltage-Controlled Oscillator
WAM	Wideband AM

19. Revision history

Table 85. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEF6614 v.3	20111011	Product data sheet	-	TEF6614_2
Modifications:	• Section 17: added • Legal texts have been updated			
TEF6614_2	20091029	Product data sheet	-	TEF6614_1
TEF6614_1	20090429	Preliminary data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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