1 Introduction

- 10-bit PWM controller written in Verilog
- SPI control interface
- Spread-spectrum output
- Configurable number of channels

1.1 Design hierarchy

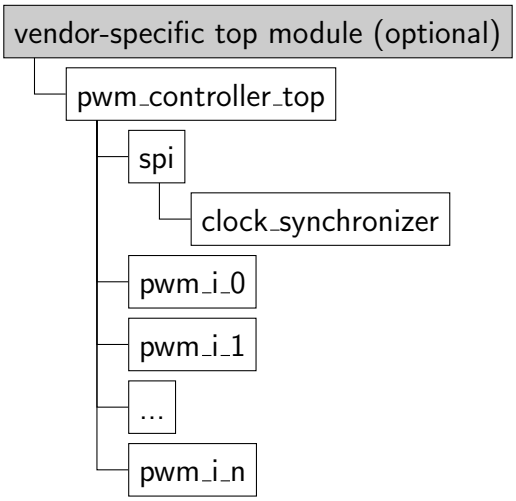

Figure 1: Design hierarchy

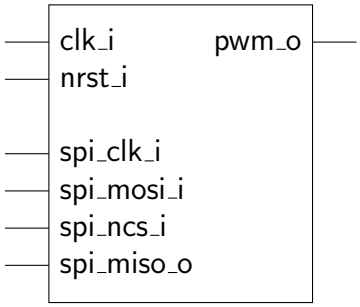

Figure 2: Top-level module symbol

1.2 Ports description

Port	Description
clk_i	Clock input
nrst_i	Reset input (negative)
spi_clk_i	SPI clock
spi_mosi_i	SPI MOSI
spi_miso_o	SPI MISO
spi_ncs_i	SPI chip select

Table 1: Module ports description

2 Control interface

The device is meant to be controller via SPI control interface. Each SPI transaction consists of two bytes: a command byte and a data byte.

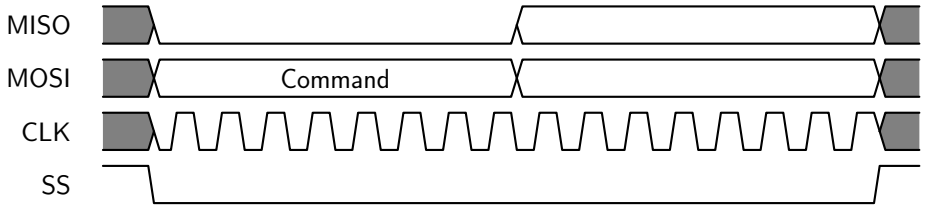

Figure 3: Generic SPI transaction

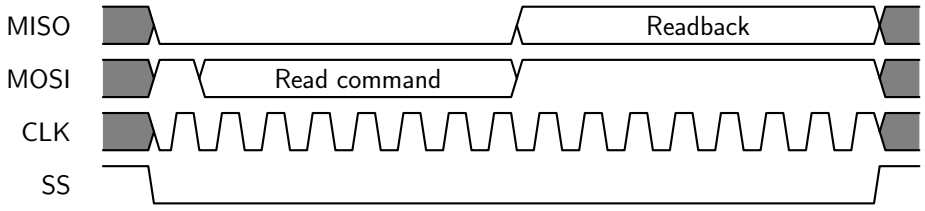

Figure 4: SPI read diagram

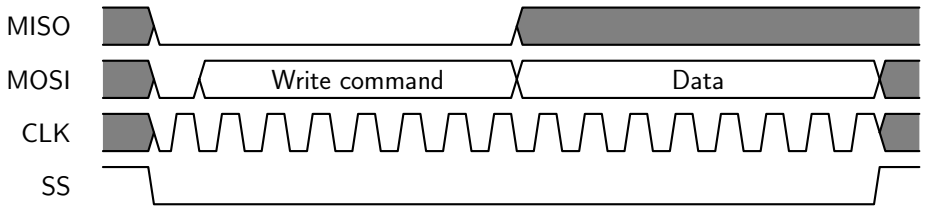

Figure 5: SPI write diagram

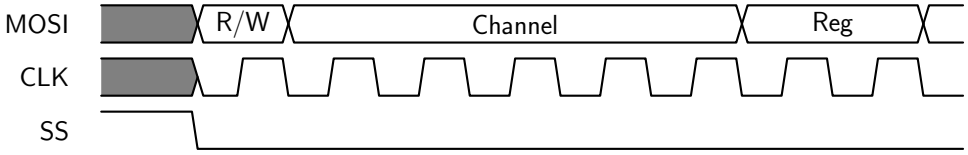

Figure 6: Command structure

Field	**Description**
`RW[7]`	Read/write. Set to 1 when performing a read transaction.
`CH[6:2]`	Channel. Refers to instance of `pwm` module within the top-level architecture.
`ADDR[1:0]`	Target register address.

Table 2: Command structure

3 Register map

Address	**Description**
`0x00`	Control register
`0x01`	Duty cycle upper byte
`0x02`	Duty cycle lower byte

Table 3: Register address mapping

Field	EN	—					DEV	
Default	0	—					00	
R/W	RW	—					RW	
	7	6	5	4	3	2	1	0

Table 4: Control register

Field	**Description**
EN	Enable `pwm` instance
DEV	Set duty cycle deviation

Table 5: Control register fields

Field	—						DC[9:8]	
Default	—						00	
R/W	—						RW	
	7	6	5	4	3	2	1	0

Table 6: Duty cycle upper byte

Field	DC[7:0]							
Default	00000000							
R/W	RW							
	7	6	5	4	3	2	1	0

Table 7: Duty cycle lower byte