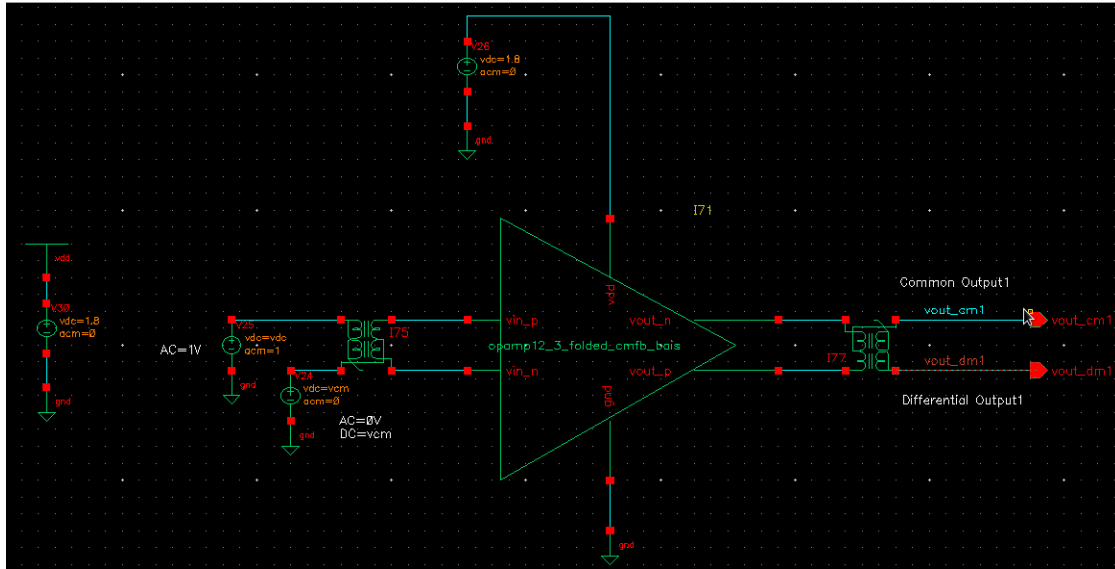
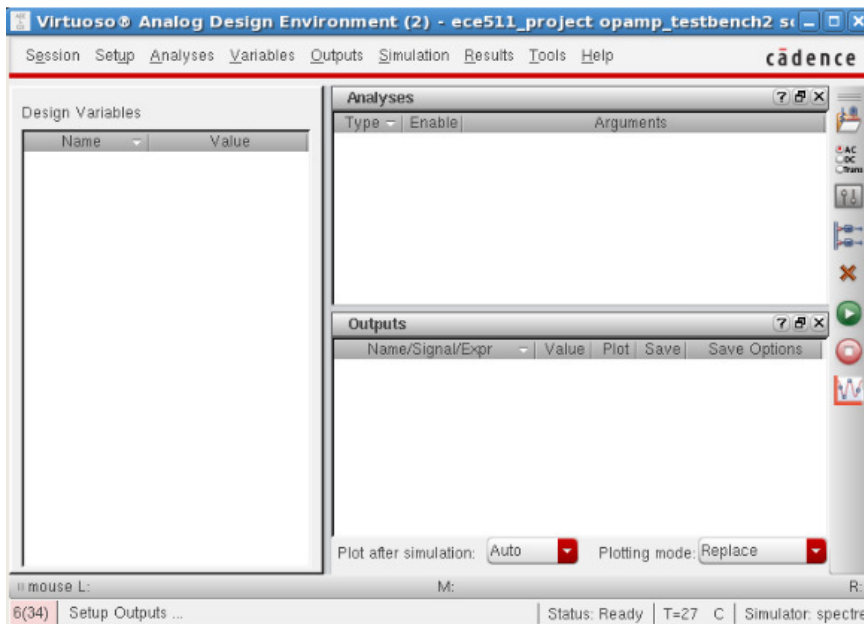


1. Open loop gain, Phase Margin, Unity Gain Frequency Simulation

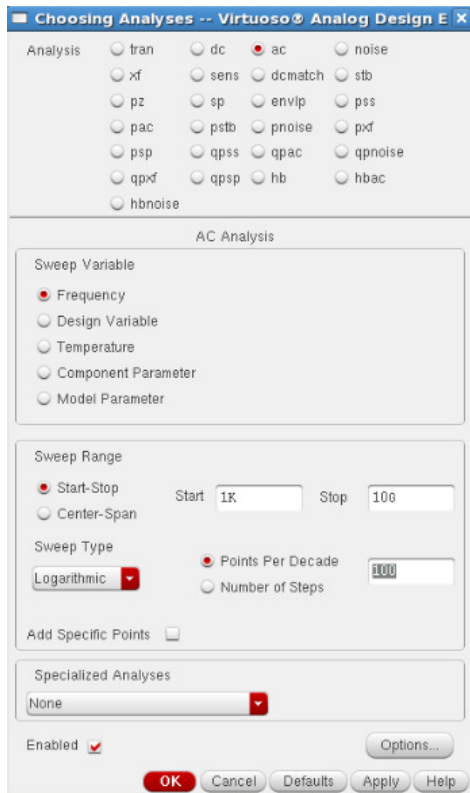
- Testbench schematic: Differential Input AC = 1V ; Common Input AC = 0V, DC = vcm



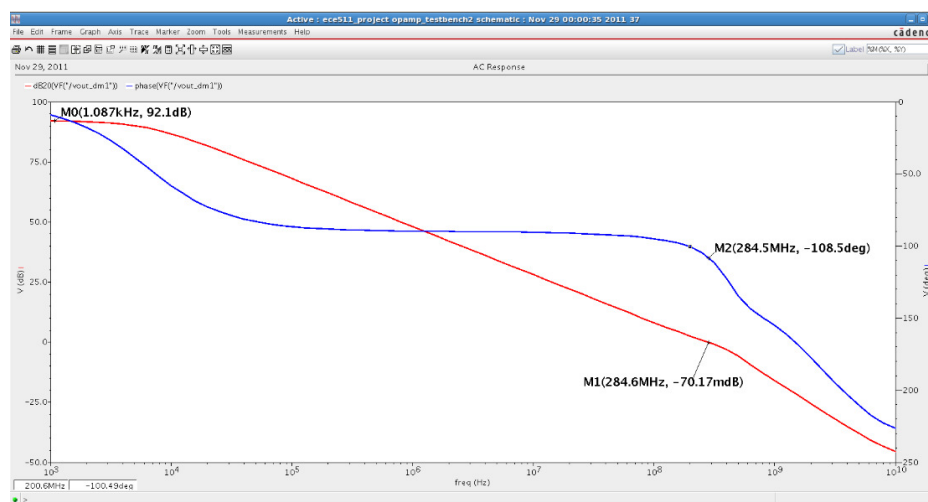
- Analog Design Environment



- Analyses->Choose->then set up the AC simulation as shown below



- Run AC simulation
- Choose Plotting Mode as "Append"
- Result -> Direct Plot -> AC dB20 and AC Phase -> Click Differential Output1-> Esc (Blue line is the gain and Red line is the phase)
- Session -> Save State (Please save the graphs for the project verification)

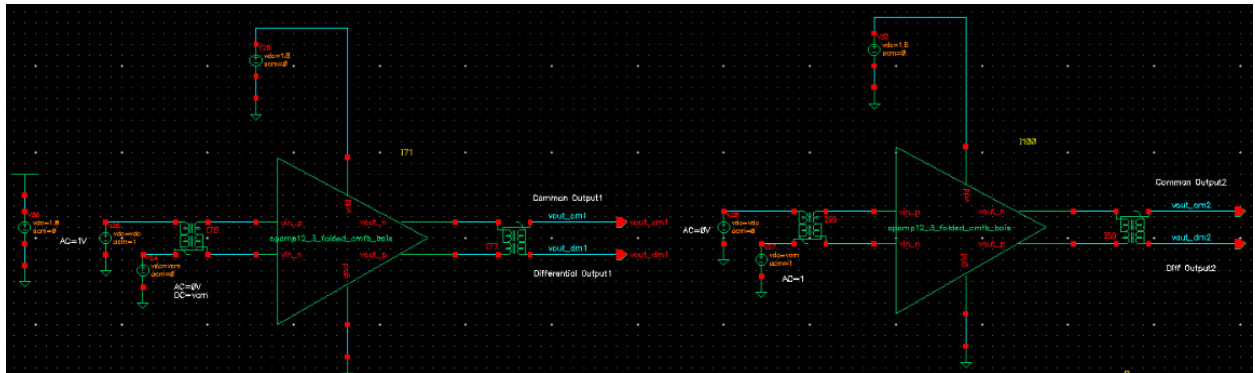


2. CMRR Simulation

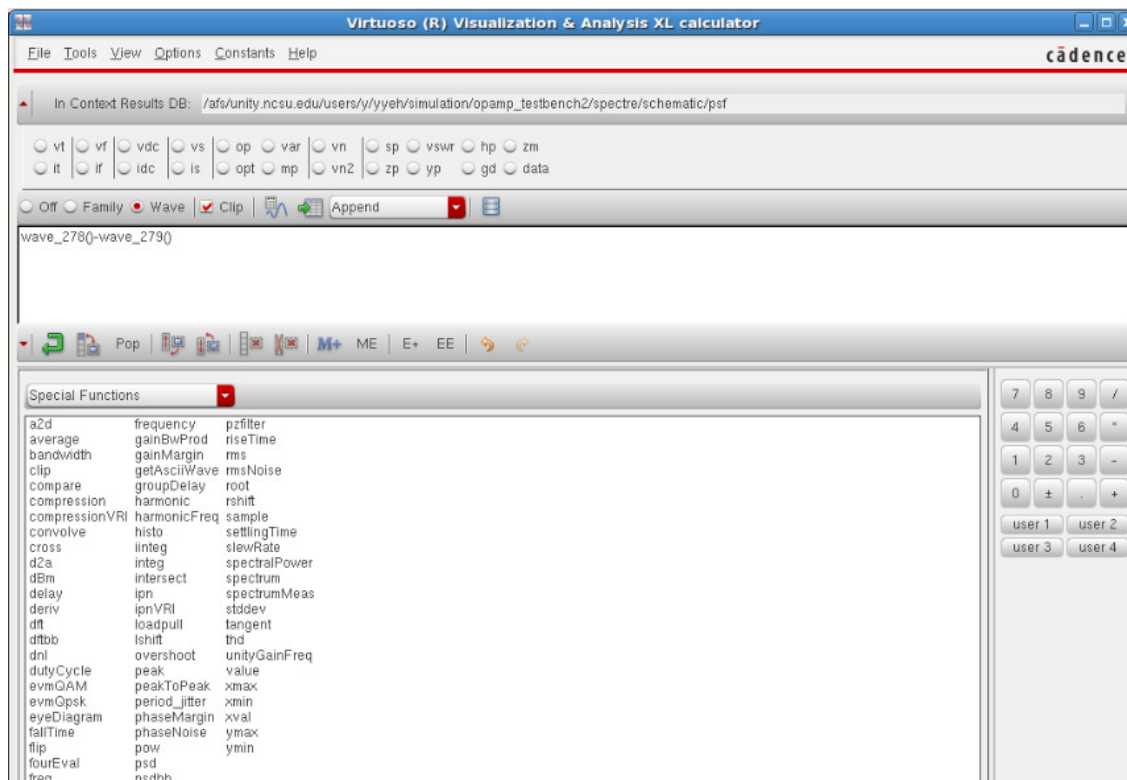
- Testbench Schematic

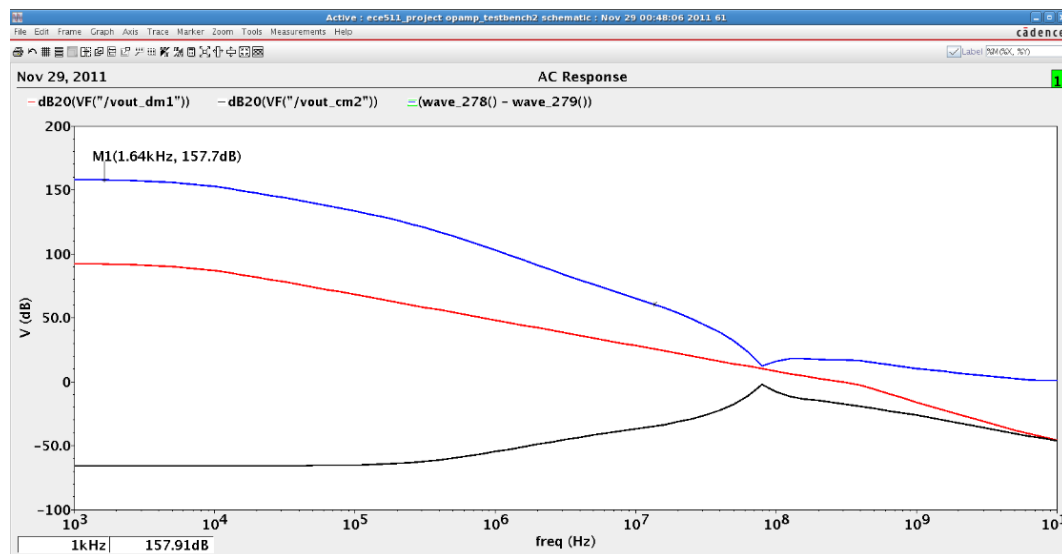
Left Opamp is for Diff gain simulation => Diff Input1 AC =1V; CM Input1 AC = 0V;

Right Opamp is for Common gain simulation => Diff Input2 AC =0V ; CM Input2 AC = 1V;



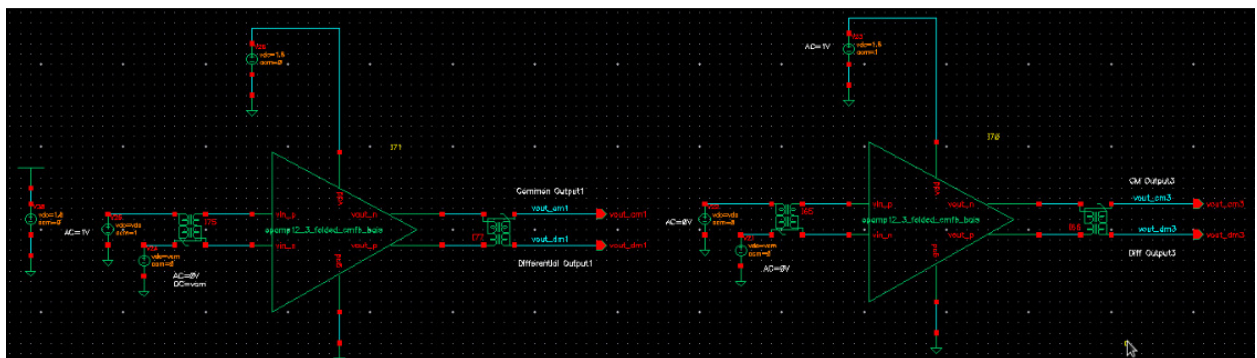
- Run AC Simulation
- Result -> Direct Plot -> AC dB20 -> Click Differential Output1 for Diff Gain and Common Output2 for CM Gain -> Esc
- Tool -> Calculator -> Click waveform -> $CMRR = \text{Diff Gain} - \text{CM Gain}$
(Blue line is CMRR; Red line is Diff Gain; Black line is CM Gain)
- Session -> Save State



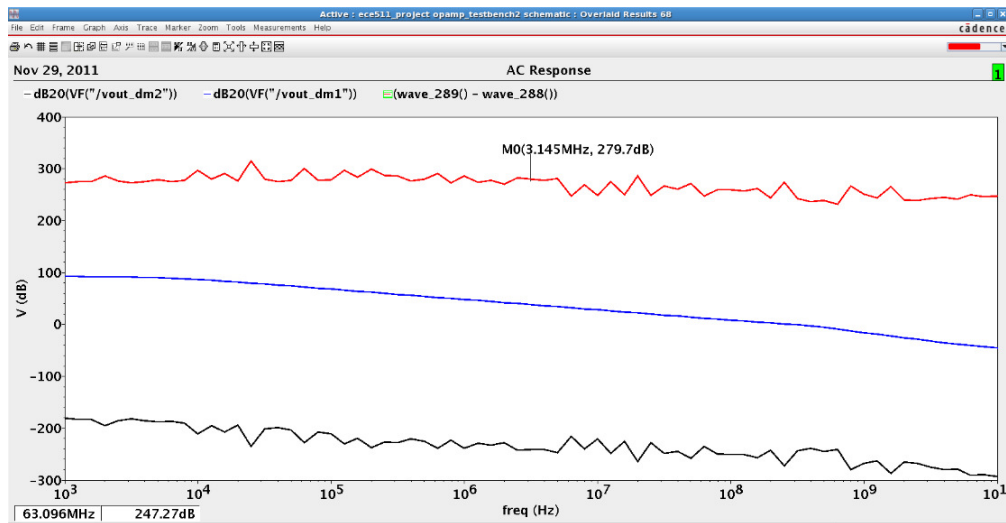


3. PSRR Simulation:

- Testbench Schematic
Left Opamp is for Diff gain simulation => Diff Input1 AC = 1V; CM Input1 AC = 0V; VDD AC = 0V;
Right Opamp is for Vdd gain simulation => Diff Input3 AC = 0V; CM Input3 AC = 0V; VDD AC = 1V;

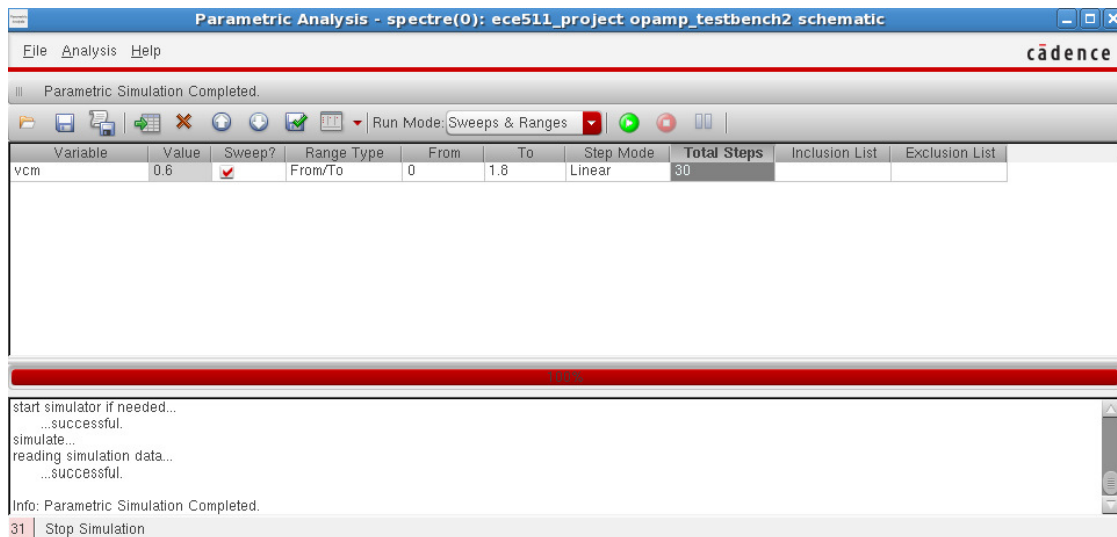


- Run AC Simulation
- Result -> Direct Plot -> AC dB20 -> Click Diff Output1 for Diff Gain and Diff Output3 for Vdd Gain -> Esc
- Tool -> Calculator -> Click waveform -> $\text{PSRR+} = \text{Diff Gain} - \text{Vdd Gain}$
(Red line is PSRR+; Blue line is Diff Gain; Black line is Vdd gain)
- Session -> Save State

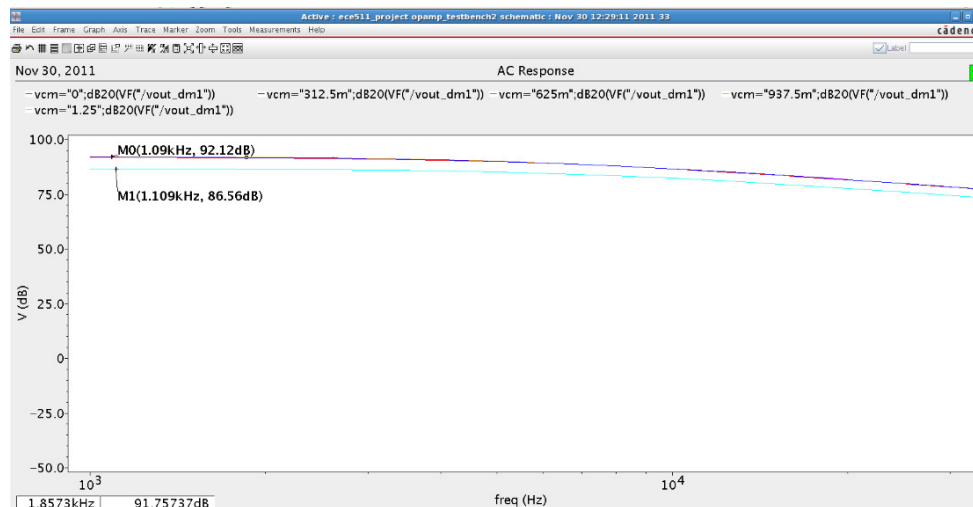


4. Input Common Mode Range:

- Please give a DC voltage variable ("vcm") in your common input voltage source.
- Setup AC analysis and run AC simulation -> Please also give AC = 1V to the differential input.
- Tool -> Parametric Analysis -> choose the variable "vcm" as shown below



- Result -> Direct Plot -> AC dB20 -> Click Diff Output1 for Diff Gain v.s. vcm-> Esc
- Find the input common range where the low frequency gain is within +- 6dB of the nominal value
- Once you know some input common voltages are out of the range of +-6dB of your low frequency gain, you can narrow the vcm range and simulate it again until the vcm range is with the range of +- 6dB of the gain.
- Session -> Save State



5. Output Swing Range:

- Please give a DC voltage variable ("vdc") in your differential input voltage source.
- Analyses->Choose->then set up the DC simulation as shown below.
- The numbers below are just for reference so you can give whatever numbers you want in the simulation.

Choosing Analyses -- Virtuoso® Analog Design E

Analysis

☐ tran ☒ dc ☐ ac ☐ noise

☐ xf ☐ sens ☐ dcmatch ☐ stb

☐ pz ☐ sp ☐ envlp ☐ pss

☐ pac ☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac ☐ qpnoise

☐ qpxf ☐ qpdp ☐ hb ☐ hbac

☐ hbnoise

DC Analysis

Save DC Operating Point ☒

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start Stop

☐ Center-Span

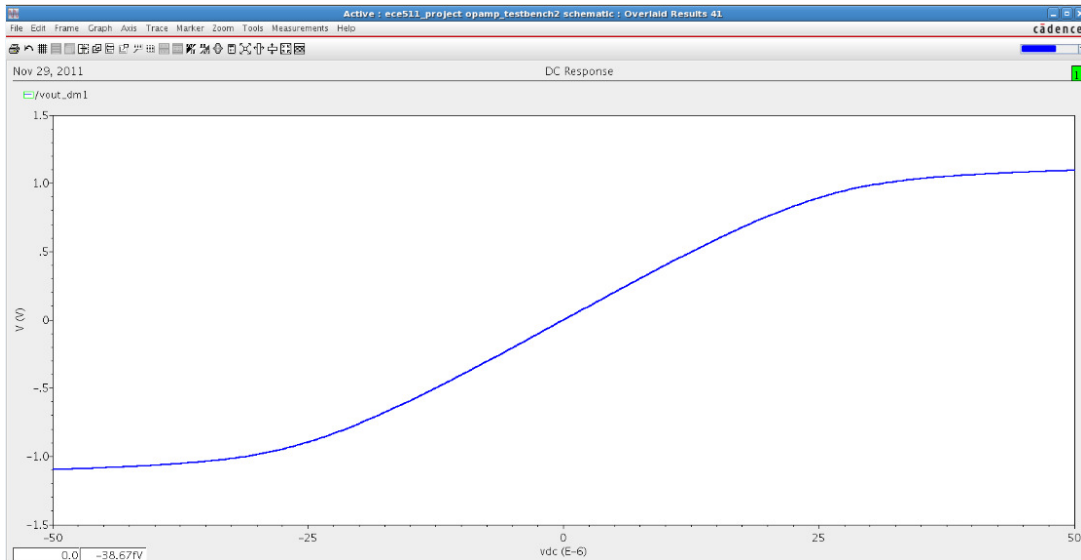
Sweep Type

☒ Number of Steps

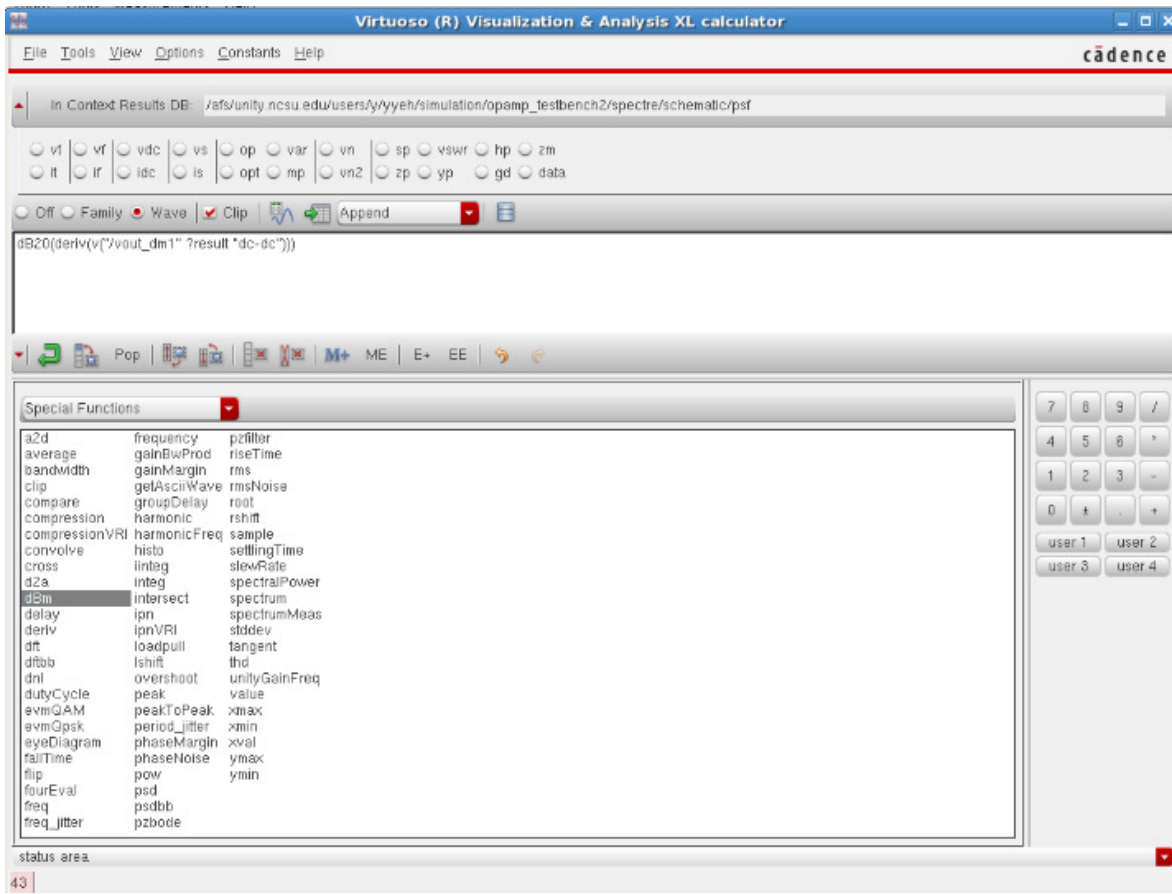
Add Specific Points ☐

Enabled ☒

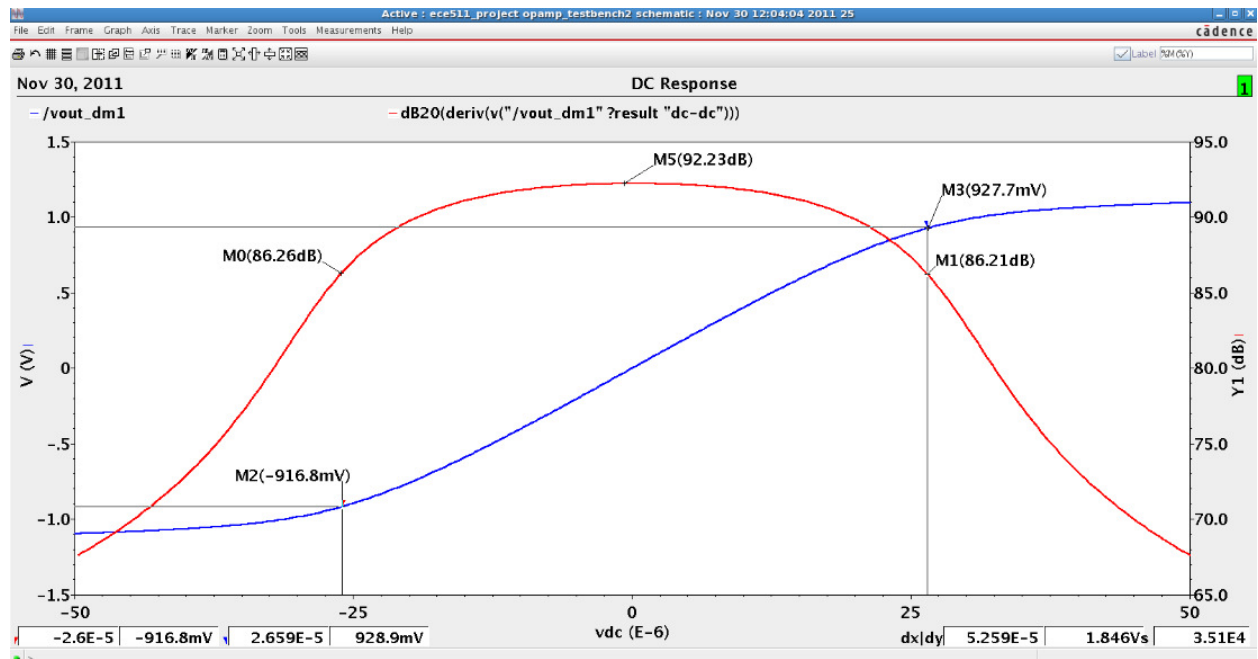
- Output -> To Be Plotted -> Select on Schematic for Differential Output 1 node
- Run DC simulation -> It will show the differential output1 voltage swing



- Tool -> Calculator -> Click waveform -> dB20(deriv(vout swing waveform))



- Find the output swing points where the gain is 6dB less than the maximum gain (Blue line is the differential output and Red line is the 20dB of the slope)
- Session -> Save State (Please save the graphs for the project verification)



6. Noise simulation

- Please give Differential Input AC = 1V ; Common Input AC = 0V
- Analyses->Choose->then set up the Noise simulation as shown below
Please choose Output Noise as "voltage"; Please click the differential output on your schematic as Positive Output Node and click the ground on your schematic as Negative Output Node.
Please choose Input Noise as "Voltage"; Please click the differential input voltage source on the schematic as Input Voltage Source.

Choosing Analyses -- Virtuoso Analog Design E

Analysis: ☐ tran ☐ dc ☐ ac ☒ noise

☐ xf ☐ sens ☐ dcmatch ☐ stb

☐ pz ☐ sp ☐ envlp ☐ pss

☐ pac ☐ pstb ☐ pnoise ☐ pxf

☐ psp ☐ qpss ☐ qpac ☐ qpnoise

☐ qpxf ☐ qpdp ☐ hb ☐ hbac

☐ hbnnoise

Noise Analysis

Sweep Variable: ☒ Frequency ☐ Design Variable ☐ Temperature ☐ Component Parameter ☐ Model Parameter

Sweep Range: ☒ Start-Stop Start: 1 Stop: 100M ☐ Center-Span

Sweep Type: ☒ Logarithmic ☐ Points Per Decade: 100 ☐ Number of Steps

Add Specific Points: ☐

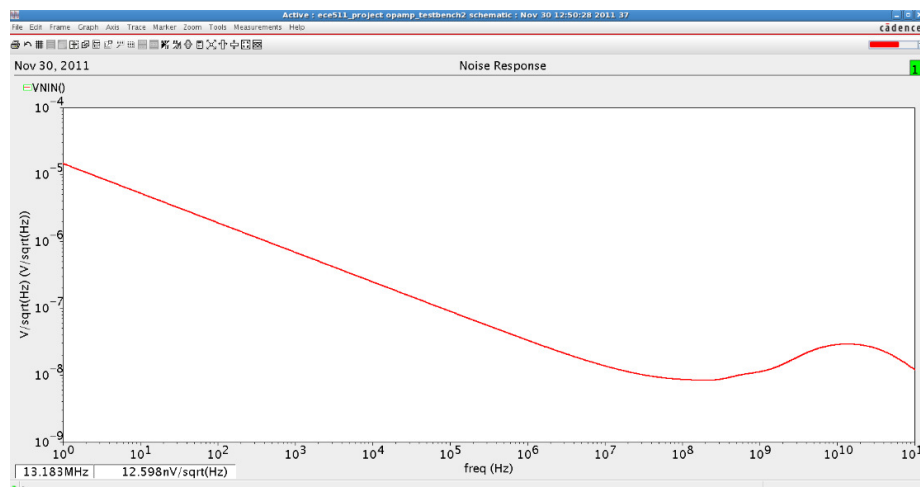
Output Noise: ☒ voltage Positive Output Node: /vout_dnl Select Negative Output Node: /gnd! Select

Input Noise: ☒ voltage Input Voltage Source: /V13 Select

Enabled: ☒ Options...

OK Cancel Defaults Apply Help

- Run Noise simulation
- Result -> Direct Plot -> Equivalent Input Noise
- Please click the vertical axis and choose "Log" on the graph screen



- For the integrated noise analysis, please go to Result -> Print -> Noise Summary



Print the output noise of 'noise' analysis

Type ☐ spot noise ☒ integrated noise noise unit **V**

From (Hz) **1K** To (Hz) **100**

weighting ☒ flat ☐ from weight file

FILTER

Include All Types Include None

b3w3
resistor

include instances Select Clear

exclude instances Select Clear

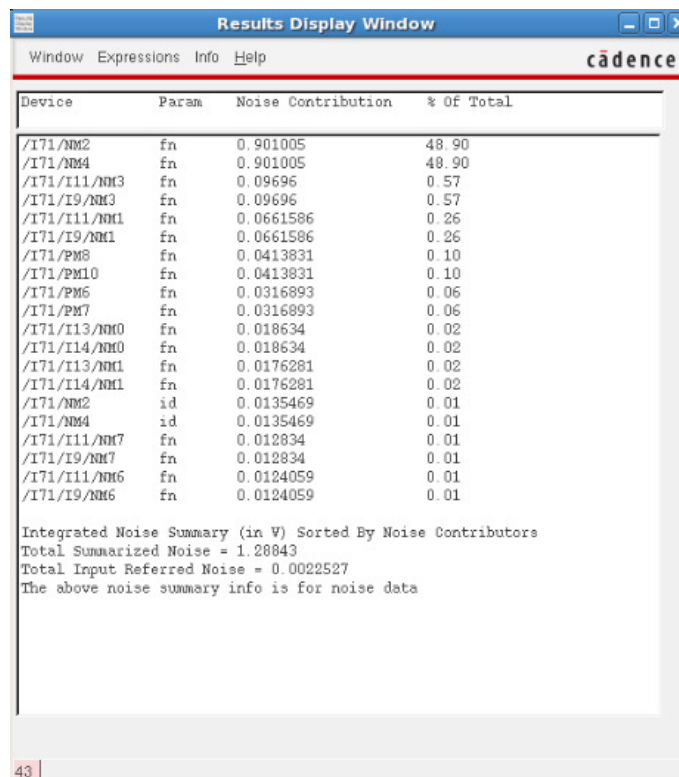
TRUNCATE & SORT

truncate **by number** top **20**

sort by ☒ noise contributors ☐ composite noise ☐ device name

OK Cancel Apply Help

- Click OK, Then it will show you the total integrated output, input referred noise and the noise contributors from which transistors in your circuits.
- Session -> Save State



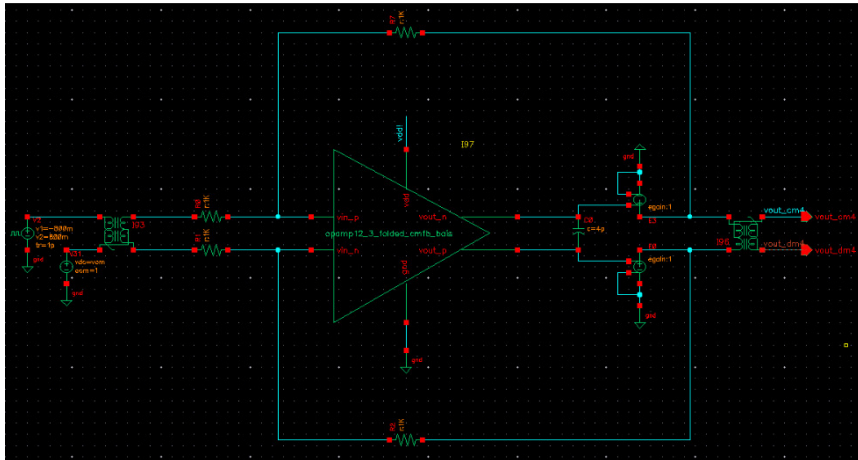
Device	Param	Noise Contribution	% Of Total
/I71/NM2	fn	0.901005	48.90
/I71/NM4	fn	0.901005	48.90
/I71/I11/NM3	fn	0.09696	0.57
/I71/I9/NM3	fn	0.09696	0.57
/I71/I11/NM1	fn	0.0661586	0.26
/I71/I9/NM1	fn	0.0661586	0.26
/I71/PM8	fn	0.0413831	0.10
/I71/PM10	fn	0.0413831	0.10
/I71/PM6	fn	0.0316893	0.06
/I71/PM7	fn	0.0316893	0.06
/I71/I13/NM0	fn	0.018634	0.02
/I71/I14/NM0	fn	0.018634	0.02
/I71/I13/NM1	fn	0.0176281	0.02
/I71/I14/NM1	fn	0.0176281	0.02
/I71/NM2	id	0.0135469	0.01
/I71/NM4	id	0.0135469	0.01
/I71/I11/NM7	fn	0.012834	0.01
/I71/I9/NM7	fn	0.012834	0.01
/I71/I11/NM6	fn	0.0124059	0.01
/I71/I9/NM6	fn	0.0124059	0.01

Integrated Noise Summary (in V) Sorted By Noise Contributors
 Total Summarized Noise = 1.28843
 Total Input Referred Noise = 0.0022527
 The above noise summary info is for noise data

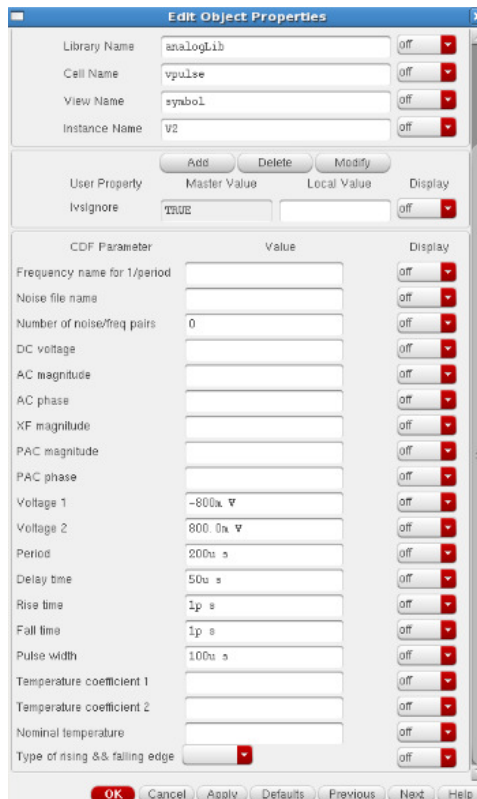
7.Settling time and Slew Rate

- Testbench schematic:

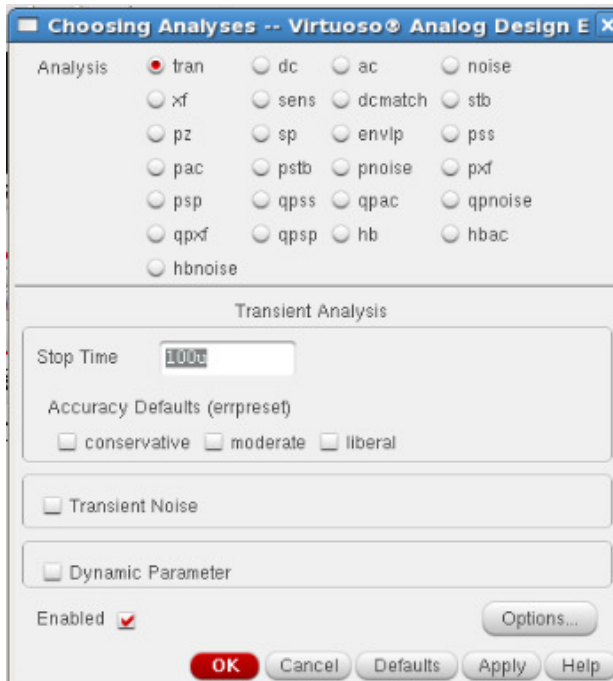
Please add 3pF cap cross the two outputs; Please use vcvs sources as an ideal voltage buffers with the gain of 1 at the two outputs. Please give the same values for the 4 resistors in order to implement the unity-gain feedback;



- Please inject a vpulse source into the differential input as shown below.



- Analyses->Choose-> tran -> Setup the stop time



- Output -> To Be Plotted -> Select the differential output on your schematic.
- Run Tran Simulation

The settling time is the time from the beginning of the step to the specified percentage of the step (1%); Slew rate is the slope of the ramp of the step.

