ECE511: Design Project: Due Friday 12/06/2019 by 11:55pm

In two-person teams, you are to design a **CMOS instrumentation amplifier (In-Amp)** using custom-designed operational amplifiers and *high-voltage transistors from the 45nm GPDK*. The design should meet or exceed the performance achieved by the Texas Instruments INA188 design. You can refer its datasheet for more information. The instrumentation amplifier (In-Amp), shown in Fig. 1, is a commonly used circuit to provide input buffering and programmable differential gain. It is useful for test and measurement applications. Your In-Amp should realize a programmable gain of $1+50k/R_{gain}$, where R_{gain} is an off-chip resistor which sets the gain. Note that EOL students may work individually or in teams of two.

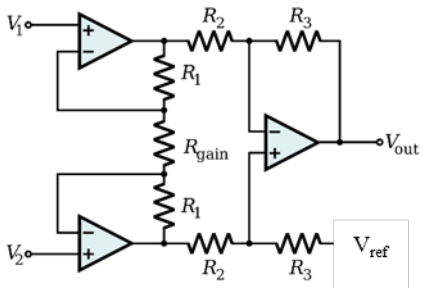

Fig 1: Schematic of the instrumentation amplifier, from Wikipedia. R_{gain} is used to set the gain.

Your In-Amp should meet or exceed the performance metrics of the TI 188 In-Amp that are listed below. Additionally, you should work to minimize power consumption and maximize common-mode input range. The specs below are reported for the following conditions, unless otherwise noted: T_A = 25°C, R_L = 10 kΩ, V_{REF} = mid-supply, and G = 1. You should also use these same conditions for evaluating the results.

Parameter	Condition	TI INA188 Result	Additional Requirement
Gain Range (G)		1 to 1000 V/V	Programmable: $1+50k/R_{gain}$
Gain Accuracy	G=1	0.007% <5 ppm/°C	Check the absolute error Check from T=25 to 100°C (okay if you exceed spec, just simulate and report)
3dB BW	G=1	600 kHz	
	G=10	95 kHz	
	G=100	15 kHz	
	G=1000	1.5 kHz	
Slew Rate	G=1	0.9 V/us	
	G=10	Not reported	
	G=100	0.17 V/us	
	G=1000	Not reported	
Settling Time	G=1	50 us	
	G=100	400 us	
Common-mode Input Range		Vss+0.1 to Vdd-1.5 V	This should be maximized
Output Swing		Vss+0.22 to Vdd-0.22	
Input Noise Floor		12.5 nV/rt(Hz)	
CMRR	G=1	90 dB	
	G=100	120 dB	
PSRR+	G=1	0 dB	
	G=100	40 dB	
Power Supply and Vdd		TBD	These should be minimized (4mA/1.5V likely possible)
Phase Margin of all loops			Must be > 80 deg.

Acknowledgment: This design was proposed by former ECE 511 students Parvez Ahmmed and Mahsa Lynch. They completed an independent study class in May 2017 where they investigated and completed the design of numerous alternative projects for ECE 511. Parvez is a PhD student here at NC State whereas Mahsa is an engineer at Analog Devices Inc. I thank them for their help in exploring many new project options.

Additional Requirements: Your In-Amp design is to be completed using Cadence for all circuit simulation. Tutorials are provided on-line on how to set up and use these tools. You should use high-voltage transistors from the 45nm GPDK design kit from Cadence. Your circuit design must meet the following requirements:

1. Supply-independent biasing
    a. Two-person teams: No external bias other than a single power supply and common mode input voltage is allowed. You must provide your own bias circuits for currents and voltages. Points will be deducted from your project grade if ideal sources are found in your netlist.
    b. One-person EOL team: a single ideal current source is permitted.
2. You must compensate all feedback networks. All loops must have the 80-deg phase margin.
3. No resistors (or series resistor chains) larger than 50k are allowed, as they take too much area.
4. All NMOS transistor bodies must be connected to ground; PMOS transistor bodies can be connected to other voltages but must be justified in your report.
5. Your design must use hierarchy (no flat netlists), with at least the following levels
    - Testbench which includes input AC and DC sources, ideal balun (if used), the In-Amp, and R_{gain}.
    - The main In-Amp which includes op-amps as subcircuits
    - The op-amp subcircuit
    - Subcircuits for bias networks, additional amplifiers used for active cascade, etc.

Academic Integrity: These designs and reports must represent your team's own original work. The actual CMOS amplifier designs must be unique. **ABSOLUTELY NO SHARING OF SCHEMATICS, DESIGNS, PLOTS, WRITE-UPS OR REPORTS WILL BE ACCEPTED. ABSOLUTELY NO USE OF PRIOR-YEAR REPORTS OR PRIOR-YEAR DESIGNS.** Students in violation of this policy will be reported to the NC State Office of Student Conduct, with repercussions including placement on academic probation and grade penalties including but not limited to receiving a zero on the design project. Please refer to the NC State Academic Integrity Policy (see syllabus) as well as the office of student conduct for the NC State policies.

Report Requirements

You are to turn in a design report in PDF format (~15-25 pages, including figures) on the due date uploaded to the course website. Please upload separate copies of the report—one into each team member's moodle account, where **your report MUST be titled as follows: Grp_X_Lastname1_Lastname.pdf**, where X is the number of the group assigned to you, Lastname1 is student 1 last name, and Lastname2 is student 2 last name.

The report must contain the following:

1. Title page with project name, your names, date, and an academic integrity statement.
2. A single page **executive summary** (this is the most important part of any report…if I read nothing else but this section, convince me of the merit of your design).
3. A **compliance table** summarizing the simulated nominal performance of your circuit versus the specifications. Any specifications not met should be highlighted in red text.
4. Technical discussion of your design, explaining
    a. high-level design of the In-Amp, including a description of its operation and example usage;
    b. a discussion of how the individual op-amp metrics have been selected based on the In-Amp specs;
    c. a discussion of the architecture and design of the OTA and output buffer used for the op-amp;
    d. a discussion of any hand calculations used in the design;
    e. a discussion of all feedback loops in your design, how they operate, how they were compensated;
    f. a discussion of the supply-independent biasing circuit(s);
5. A section presenting and discussing the simulated performance of the op-amp and the In-Amp. The simulations **should be clear and easy to read (no screen shots)**. When presenting a result, include text to explain the result, namely what was achieved, how it was achieved, how the result compares to your expectation or hand calculation, and the overall trends (for example, explaining why values are varying as a function of the closed-loop gain). The results presented should include
    a. Op-amp
        i. Frequency response of the amplifier, indicating gain, bandwidth, and phase margin with no capacitive load (but including internal compensation).
        ii. Frequency response of any internal feedback loop, i.e., gain booster, indicating gain and phase margin. Every feedback loop must be simulated and compensated.
        iii. Step response of the amplifier, indicating settling time and slew rate.
        iv. DC/AC sweeps indicating the input range.
        v. DC/AC sweeps indicating the output range.

vi. Common-mode rejection ratio frequency response (using the ideal_balun in analogLib will be very helpful for the differential and common-mode simulations).
vii. Power-supply rejection ratio frequency response (positive supply only)
viii. Frequency response of the input equivalent noise voltage (from a NOISE analysis).

b. In-Amp
   i. Frequency response in G=1, G=10, G=100, G=1000 cases (can be separate or overlaid), indicating the gain and bandwidth
   ii. Step response in G=1, G=10, G=100, G=1000 cases indicating settling time and slew rate
   iii. DC/AC sweeps indicating the output range
   iv. Frequency response of the input equivalent noise voltage (from a NOISE analysis)
   v. CMRR for G=1 and G=100
   vi. PSRR+ for G=1 and G=100

c. Trade-Off Analysis
   i. a section which summarizes the trade-offs you observed within the design project
   ii. if particular metrics do not meet specification then add *clear discussion* in the report as to what aspects of your design are limiting the performance and the trade-offs you made.

6. Conclusion with comments of what changes would enhance the performance of your design.
7. **Two sets of schematics (<u>black on white</u> background only, no screen shots, must be legible)**
   a. one set with design values clearly labeled and easily readable parameter values
   b. the other set with DC voltages and operating points clearly readable
   c. these schematics must be for the full design hierarchy
8. Cite references in your report if you use any ideas from other sources (journals, conferences, etc.). Any figure copied from any other document must be referenced. Screen shots from other journals or even my notes are not acceptable. You should draw your own schematics when presenting the main architectures.

You will demonstrate the design to the TAs by taking them through the schematic and key simulation results. Details will be provided on the timing of this demonstration.

<u>Project Grading Rubric</u>

Performance	This is calculated by number of specifications met. Specs are as follows: Gain range (1 pt), Gain accuracy (2 pt), Phase margin (2 pt), 3dB BW (four conditions, 3 pt), slew rate (four conditions, 3 pt), settling time (two conditions, 2 pt), common-mode input range (2 pt), output range (2 pt), noise floor (2 pt), CMRR (two conditions, 2 pt), PSRR+ (two conditions, 2 pt) power consumption (2 pt, with lowest power receiving full points) (total of 25 points)
Report Write-up	This is calculated based on inclusion of all required sections and overall writing quality. Sections = abstract, table, technical discussion including each section mentioned above, simulated result discussion, and conclusions. Points are calculated based on the inclusion of all required sections and the quality of the writing, spelling, grammar, and organization. Do not underestimate the importance of this section, as evidenced that as many points are awarded here as for the actual performance of your design. As a result, please budget enough time to write a clear and descriptive report. (total of 20 points)
Schematics	This is calculated based on inclusion of all required schematics and overall figure quality. Schematics which are screenshots or hard to read have points deducted. Schematics which are not black on white will have points deducted. (total of 15 points)
Simulation Plots	This is calculated by having every required simulation plot and overall figure quality. Plots which are not black on white will have points deducted. There are 14 plots required above. Some may have multiple subfigures (as in slew rate for various gain conditions). (total of 20 points)
Discretionary	This is based on both my evaluation and the TA's evaluation of the overall quality of the design. These are difficult to max out--20 points means everything is nearly perfect. (total of 20 points)

Hints:

- Use the scientific method in your design. Form a hypotheses (i.e., predict the result) before running simulations. If the result does not match your prediction, stop to analyze why before proceeding to new simulations.
- Please read through the project suggestions document on the course website
- Derive specifications for the OTA based on the In-Amp requirements. You may find that using a behavioral version of an op-amp can help in this regard, where that behavioral op-amp can be created using a voltage-controlled current source as the Gm cell, a resistor and capacitor to set the gain and bandwdith, and a voltage-controlled voltage source as an output buffer.
- Add any gain boosters as necessary. These are likely optional, based on the requirements, but it may be fun to try. Note that the gain boosters for PMOS and NMOS should be different, as they have different common-mode input requirements.
- In the beginning, your biasing could be ideal. Once the circuit works with ideal biasing, add a real bias network. Note that no voltage-mode biasing should be used. You should not have banks of resistive dividers or even worse, diode dividers.
- Compensate the OTA. Note that lead compensation can be used (with resistor in series with capacitor).