1. Description

1.1. Project

Project Name	CameraDriver
Board Name	CameraDriver
Generated with:	STM32CubeMX 4.22.0
Date	08/10/2017

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration
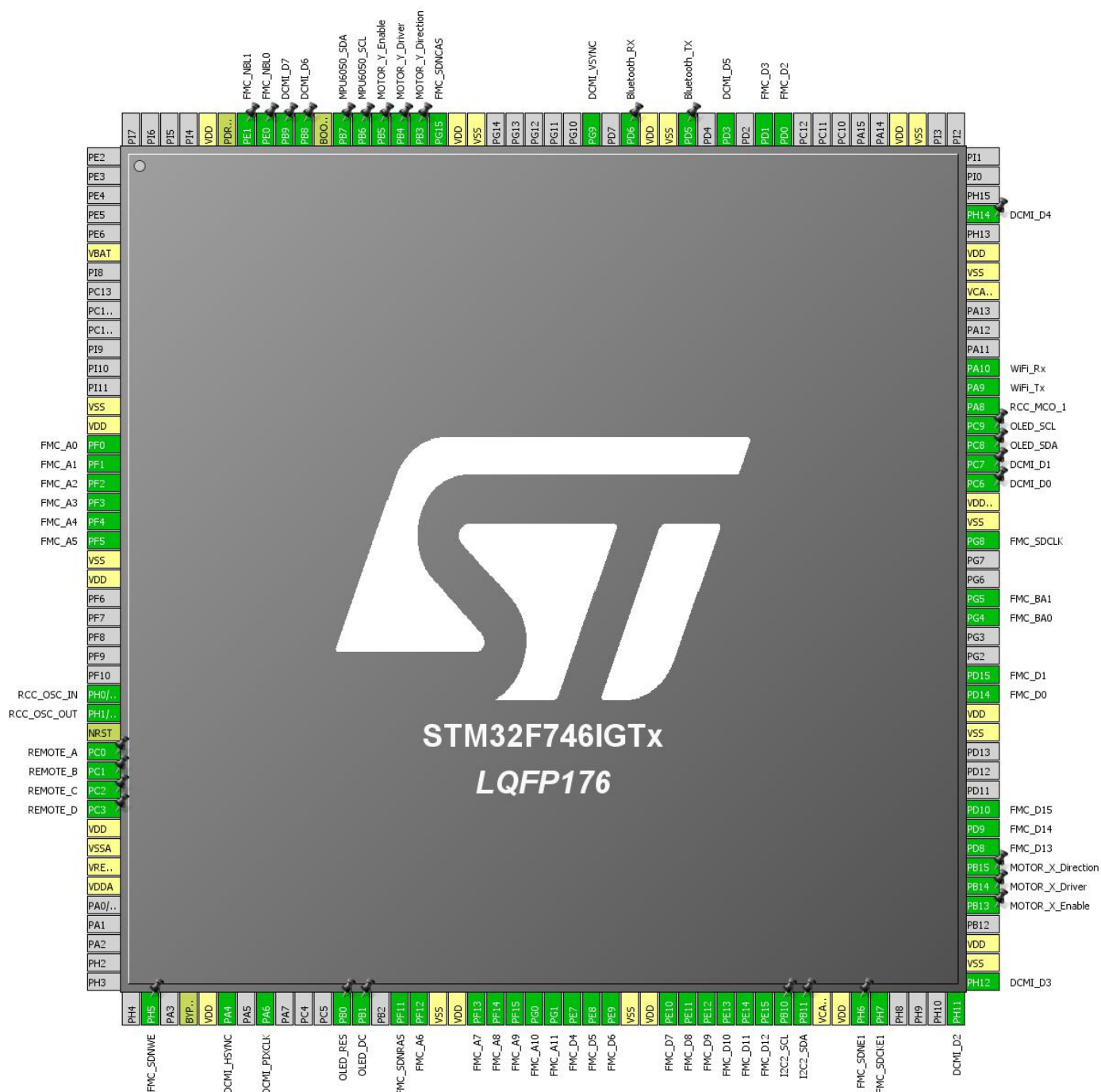
3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	GPIO_EXTI0	REMOTE_A
33	PC1	I/O	GPIO_EXTI1	REMOTE_B
34	PC2	I/O	GPIO_EXTI2	REMOTE_C
35	PC3	I/O	GPIO_EXTI3	REMOTE_D
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
46	PH5	I/O	FMC_SDNWE	
48	BYPASS_REG	Reset		
49	VDD	Power		
50	PA4	I/O	DCMI_HSYNC	
52	PA6	I/O	DCMI_PIXCLK	
56	PB0 *	I/O	GPIO_Output	OLED_RES
57	PB1 *	I/O	GPIO_Output	OLED_DC
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
79	PB10	I/O	I2C2_SCL	
80	PB11	I/O	I2C2_SDA	
81	VCAP_1	Power		
82	VDD	Power		
83	PH6	I/O	FMC_SDNE1	
84	PH7	I/O	FMC_SDCKE1	
88	PH11	I/O	DCMI_D2	
89	PH12	I/O	DCMI_D3	
90	VSS	Power		
91	VDD	Power		
93	PB13 *	I/O	GPIO_Output	MOTOR_X_Enable
94	PB14	I/O	TIM12_CH1	MOTOR_X_Driver
95	PB15 *	I/O	GPIO_Output	MOTOR_X_Direction
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
108	PG4	I/O	FMC_BA0	
109	PG5	I/O	FMC_BA1	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDDUSB	Power		
115	PC6	I/O	DCMI_D0	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
116	PC7	I/O	DCMI_D1	
117	PC8 *	I/O	GPIO_Output	OLED_SDA
118	PC9 *	I/O	GPIO_Output	OLED_SCL
119	PA8	I/O	RCC_MCO_1	
120	PA9	I/O	USART1_TX	WiFi_Tx
121	PA10	I/O	USART1_RX	WiFi_Rx
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
129	PH14	I/O	DCMI_D4	
135	VSS	Power		
136	VDD	Power		
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
145	PD3	I/O	DCMI_D5	
147	PD5	I/O	USART2_TX	Bluetooth_TX
148	VSS	Power		
149	VDD	Power		
150	PD6	I/O	USART2_RX	Bluetooth_RX
152	PG9	I/O	DCMI_VSYNC	
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
161	PB3 *	I/O	GPIO_Output	MOTOR_Y_Direction
162	PB4	I/O	TIM3_CH1	MOTOR_Y_Driver
163	PB5 *	I/O	GPIO_Output	MOTOR_Y_Enable
164	PB6 *	I/O	GPIO_Output	MPU6050_SCL
165	PB7 *	I/O	GPIO_Output	MPU6050_SDA
166	BOOT0	Boot		
167	PB8	I/O	DCMI_D6	
168	PB9	I/O	DCMI_D7	
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Reset		
172	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration

5. IPs and Middleware Configuration

5.1. DCMI

DCMI: Slave 8 bits External Synchro

5.1.1. Parameter Settings:

Mode Config:

Pixel clock polarity	**Active on Rising edge ***
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

5.2. FMC

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

5.2.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**2 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***

SDRAM common read pipe delay	**1 HCLK clock cycle ***

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

5.3. I2C2

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00C0EAFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator
mode: Master Clock Output 1

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.5. SYS

Timebase Source: SysTick

5.6. TIM3

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**3000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM7

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**100-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.8. TIM12

Channel1: PWM Generation CH1

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**3000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

5.9. USART1

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

5.10. USART2

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DCMI	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH14	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PF0	FMC_A0	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	**Pull-up ***	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	**Pull-down ***	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	**Pull-down ***	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	**Pull-up ***	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	**Pull-up ***	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE12	FMC_D9	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	**Pull-up ***	Very High	
	PH6	FMC_SDNE1	Alternate Function Push Pull	**Pull-down ***	Very High	
	PH7	FMC_SDCKE1	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	**Pull-up ***	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	**Pull-up ***	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	**Pull-up ***	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	**Pull-up ***	Very High	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_Y_Driver
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_X_Driver
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	WiFi_Tx
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	WiFi_Rx
USART2	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	Bluetooth_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD6	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High** *	Bluetooth_RX
GPIO	PC0	GPIO_EXTI0	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	REMOTE_A
	PC1	GPIO_EXTI1	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	REMOTE_B
	PC2	GPIO_EXTI2	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	REMOTE_C
	PC3	GPIO_EXTI3	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	REMOTE_D
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_RES
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_DC
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_X_Enable
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_X_Direction
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_SDA
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_SCL
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_Y_Direction
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_Y_Enable
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MPU6050_SCL
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MPU6050_SDA

6.2. DMA configuration

DMA request	Stream	Direction	Priority
DCMI	DMA2_Stream1	Peripheral To Memory	Low

DCMI: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
TIM7 global interrupt	true	4	0
DMA2 stream1 global interrupt	true	0	0
DCMI global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line3 interrupt	unused		
TIM3 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
FMC global interrupt	unused		
FPU global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746IGTx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	CameraDriver
Project Folder	E:\My works File\EC\BallPlate
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F7 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No