TUHH
Technische Universität Hamburg

HAMBURG UNIVERSITY OF TECHNOLOGY

PROBLEM-BASED LEARNING

Advanced System-on-Chip Design

author
@tuhh.de

Documentation

Wintersemester 2016/2017
Dipl.-Ing. Wolfgang BRANDT

January 29, 2017

Contents

1 Cache Simulation - Results **2**

2 Design a Finite State Machine for the Cache **3**

2.1 Finite State Machine - Write Allocate Policy 3

2.2 Finite State Machine - Example 6

3 Appendix **8**

Table 1: Cache Simulation of Column Major

Placement (Policy)	Cache Block Size (Words)	Cache Hit Count	Cache Miss Count	Cache Hit Rate
Direct Mapping	2	0	256	0
Direct Mapping	4	0	256	0
Direct Mapping	8	0	256	0
Direct Mapping	16	0	256	0
2-Way Set Associative	2	0	256	0
2-Way Set Associative	4	0	256	0
2-Way Set Associative	8	0	512	0
2-Way Set Associative	16	0	256	0
4-Way Set Associative	2	0	256	0
4-Way Set Associative	4	0	256	0
4-Way Set Associative	8	0	256	0
4-Way Set Associative	16	0	256	0

Table 2: Cache Simulation of Row Major

Placement (Policy)	Cache Block Size (Words)	Cache Hit Count	Cache Miss Count	Cache Hit Rate
Direct Mapping	2	128	128	50
Direct Mapping	4	192	64	75
Direct Mapping	8	224	32	88
Direct Mapping	16	240	16	94
2-Way Set Associative	2	128	128	50
2-Way Set Associative	4	192	64	75
2-Way Set Associative	8	224	32	88
2-Way Set Associative	16	240	16	94
4-Way Set Associative	2	128	128	50
4-Way Set Associative	4	192	64	75
4-Way Set Associative	8	224	16	88
4-Way Set Associative	16	240	16	94

1 Cache Simulation - Results

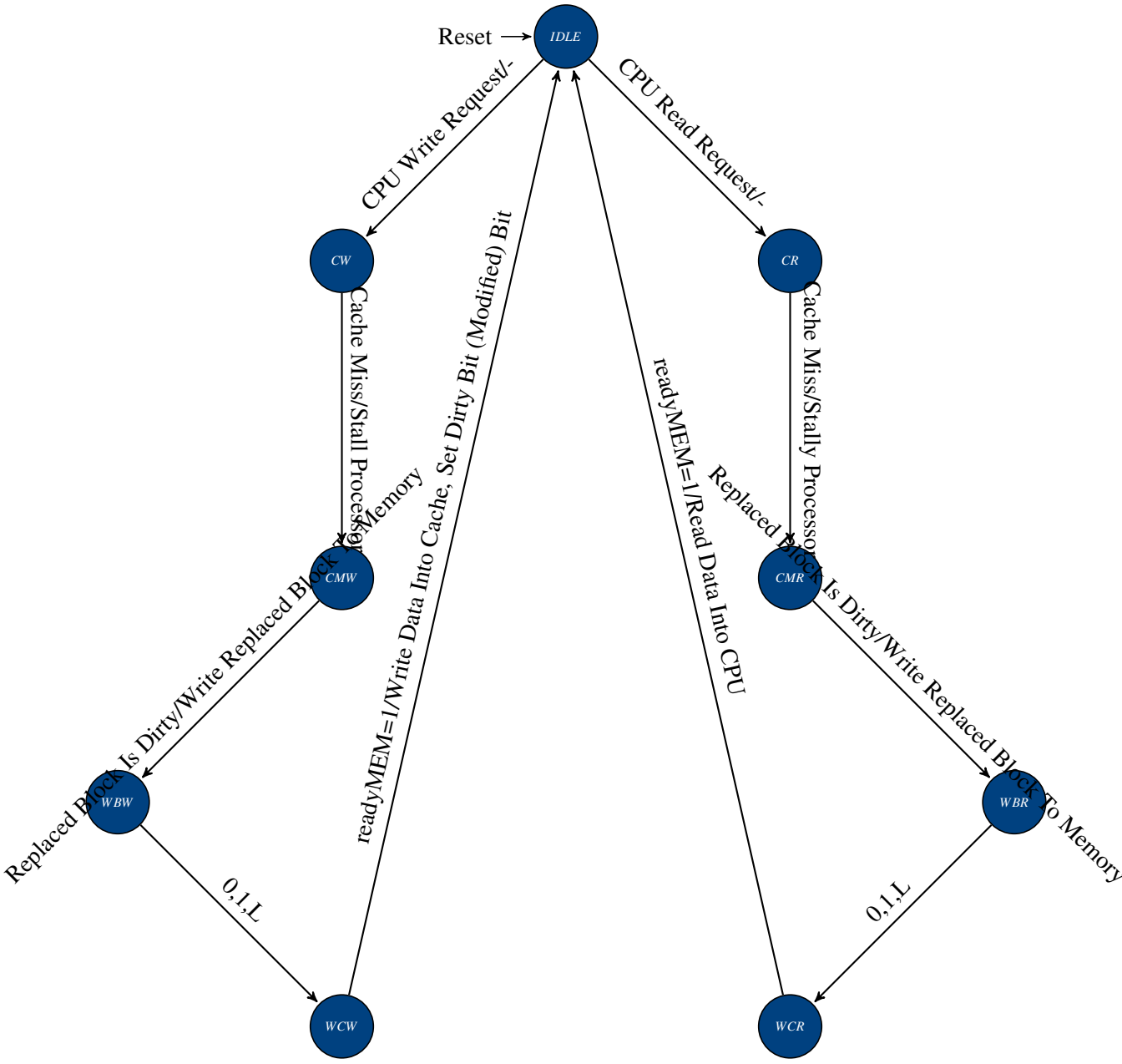
The two assembler programs *row-major.asm* and *column-major.asm* has been used for the cache simulation. 1 contains the results regarding the file *column-major.asm* and 2 illustrates the results of *row-major.asm*.
TODO Interpretation

2 Design a Finite State Machine for the Cache

2.1 Finite State Machine - Write Allocate Policy

Table 3: Overview - FSM States

Abbreviation	Name	CPU Request Mode	Description
IDLE	-	-	-
CW	COMPARE WRITE	Write Request	-
CMW	CACHE MISS WRITE	Write Request	-
WBW	WRITE BACK WRITE	Write Request	-
WCW	WRITE CACHE WRITE	Write Request	-
CR	COMPARE READ	Read Request	-
CMR	CACHE MISS READ	Read Request	-
WBR	WRITE BACK READ	Read Request	-
WCR	WRITE CACHE READ	Read Request	-



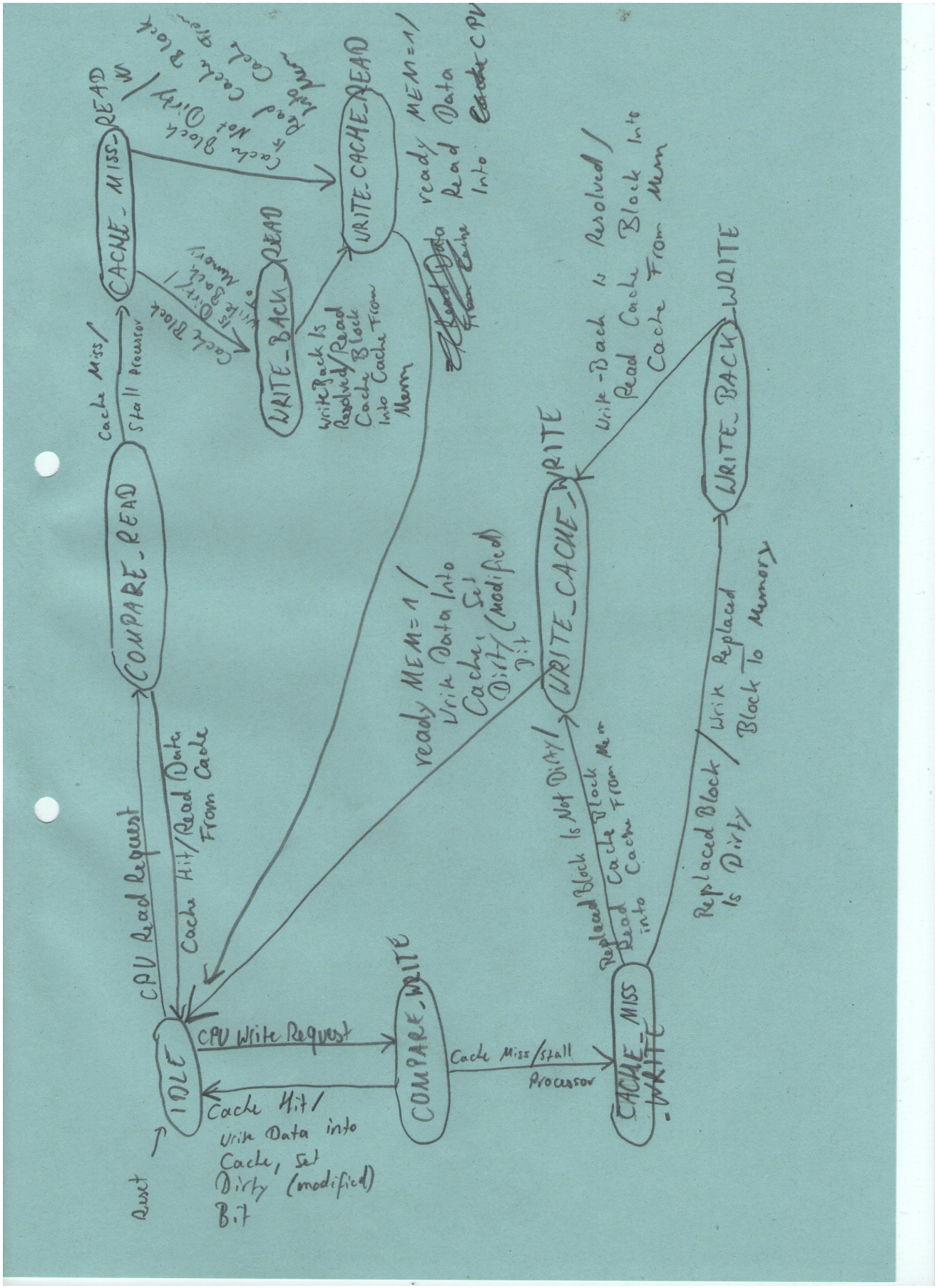
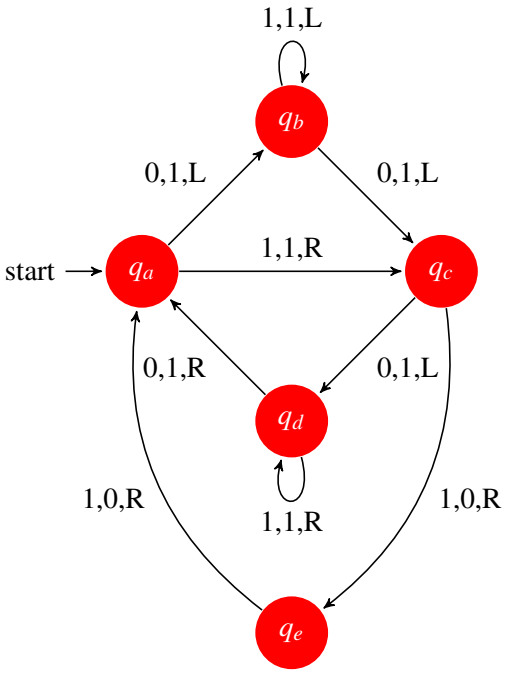


Figure 1: Sketch of Mealy Automata - Cache Controller

2.2 Finite State Machine - Example


1,1,L
q_b
0,1,L
0,1,L
start
q_a
1,1,R
q_c
0,1,R
0,1,L
q_d
1,0,R
1,1,R
1,0,R
q_e

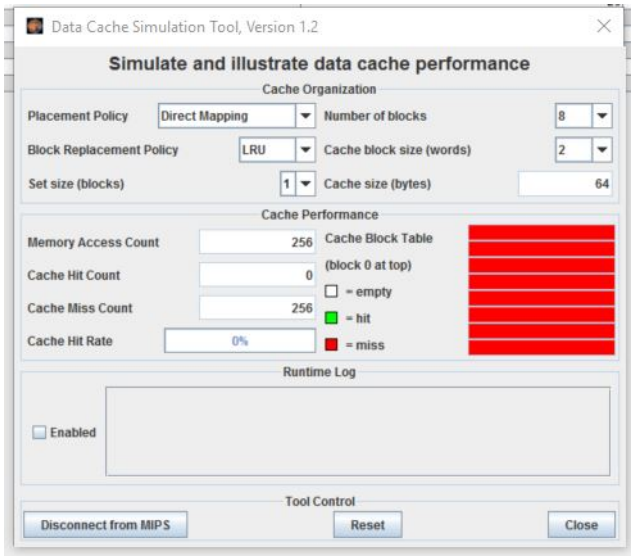


Figure 2: Column Major, Direct Mapping, Cache Block Size 2

3 Appendix

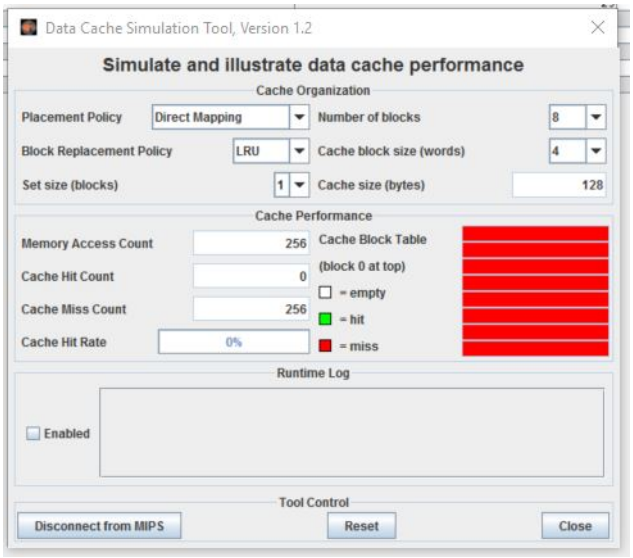


Figure 3: Column Major, Direct Mapping, Cache Block Size 4

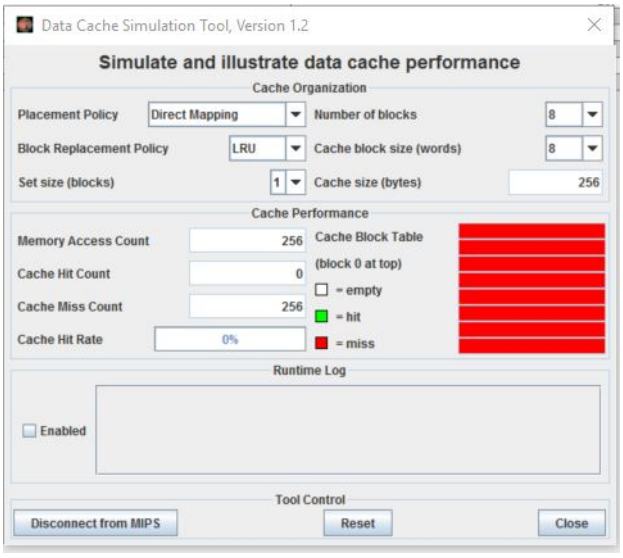


Figure 4: Column Major, Direct Mapping, Cache Block Size 8

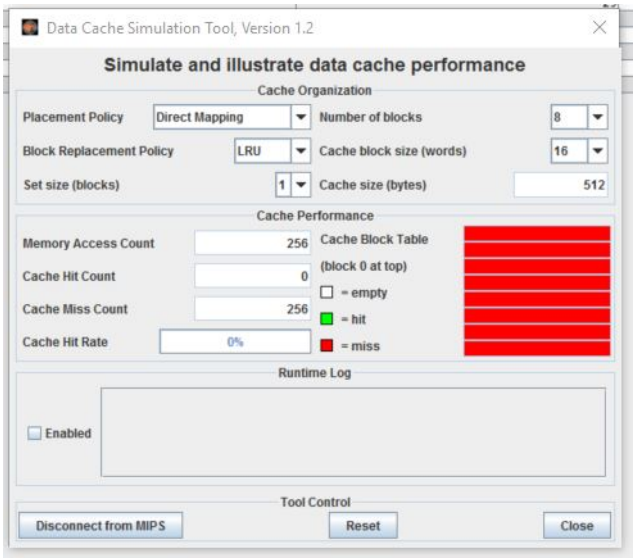


Figure 5: Column Major, Direct Mapping, Cache Block Size 16

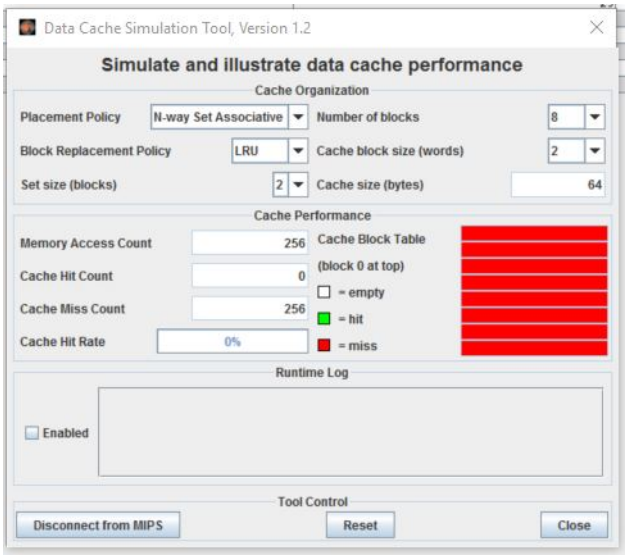


Figure 6: Column Major, 2-Way Associative, Cache Block Size 2

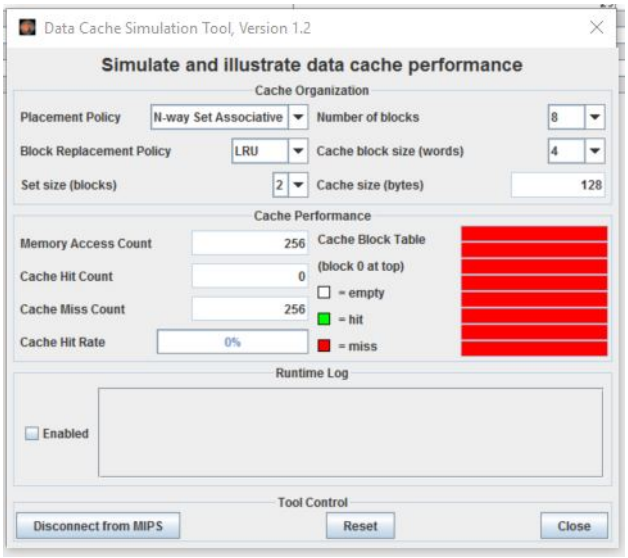


Figure 7: Column Major, 2-Way Associative, Cache Block Size 4

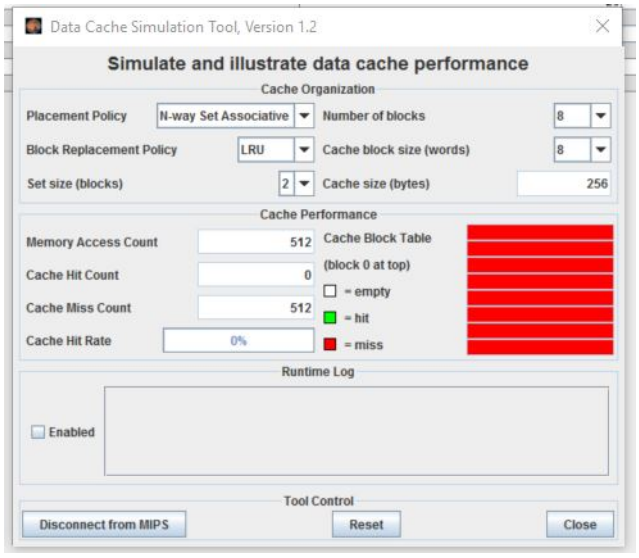


Figure 8: Column Major, 2-Way Associative, Cache Block Size 8

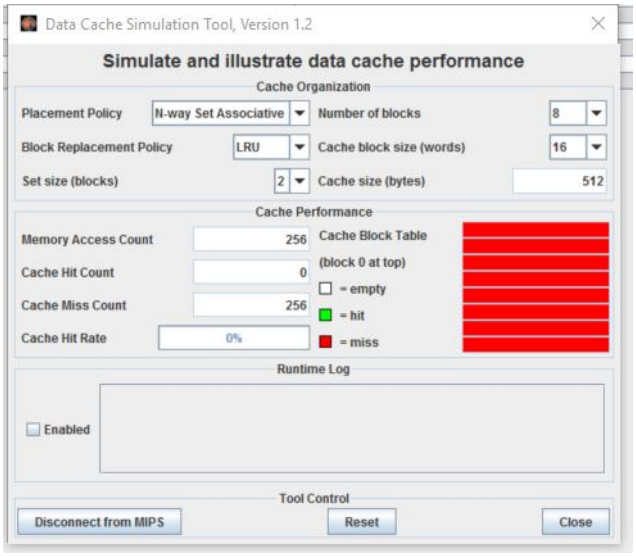


Figure 9: Column Major, 2-Way Associative, Cache Block Size 16

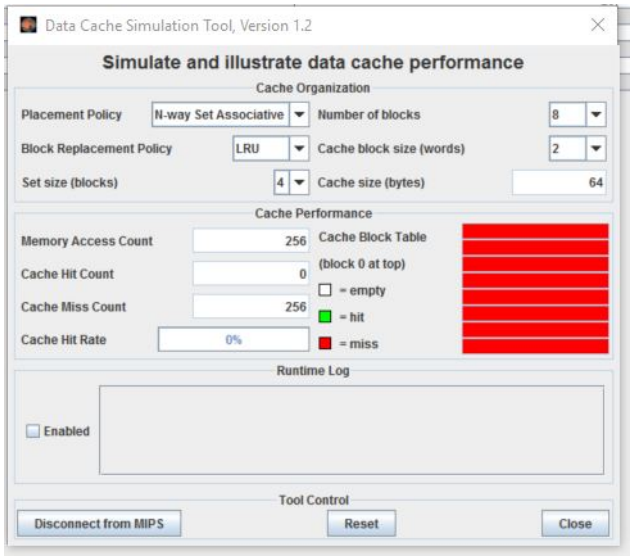


Figure 10: Column Major, 4-Way Associative, Cache Block Size 2

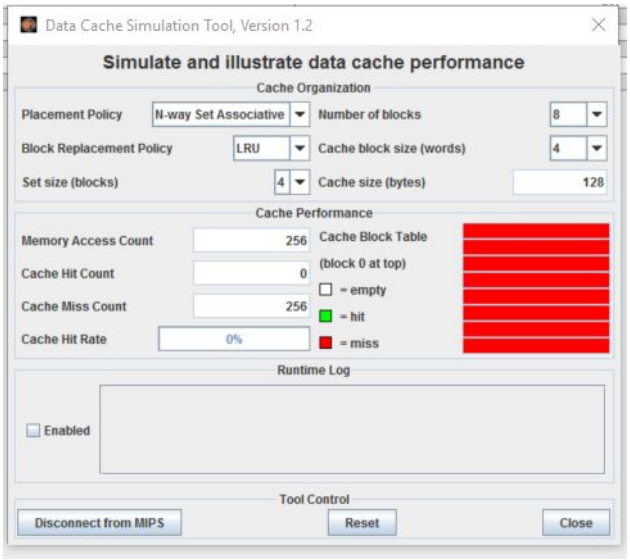


Figure 11: Column Major, 4-Way Associative, Cache Block Size 4

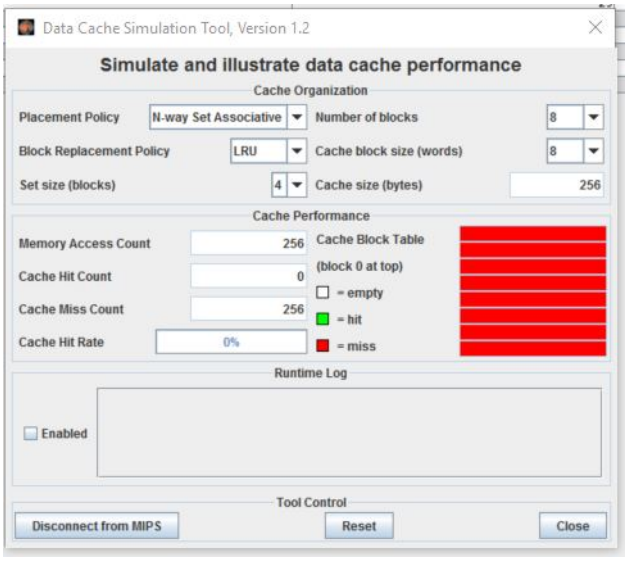


Figure 12: Column Major, 4-Way Associative, Cache Block Size 8

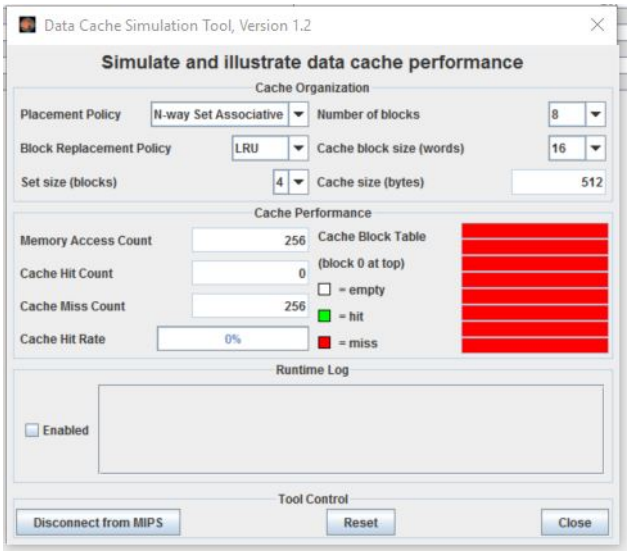


Figure 13: Column Major, 4-Way Associative, Cache Block Size 16

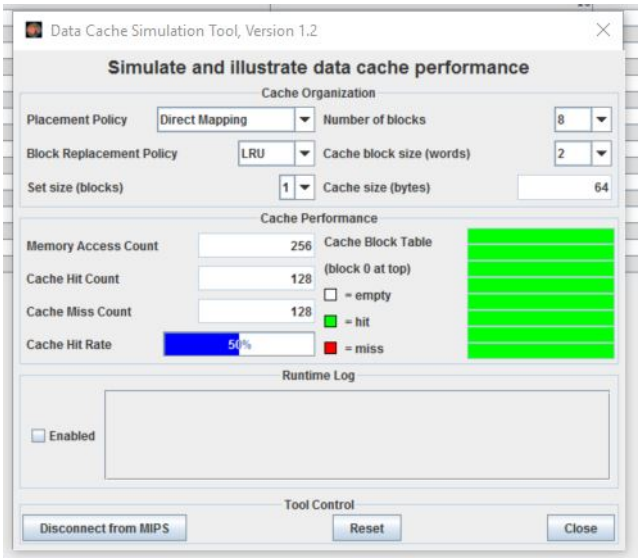


Figure 14: Row Major, Direct Mapping, Cache Block Size 2

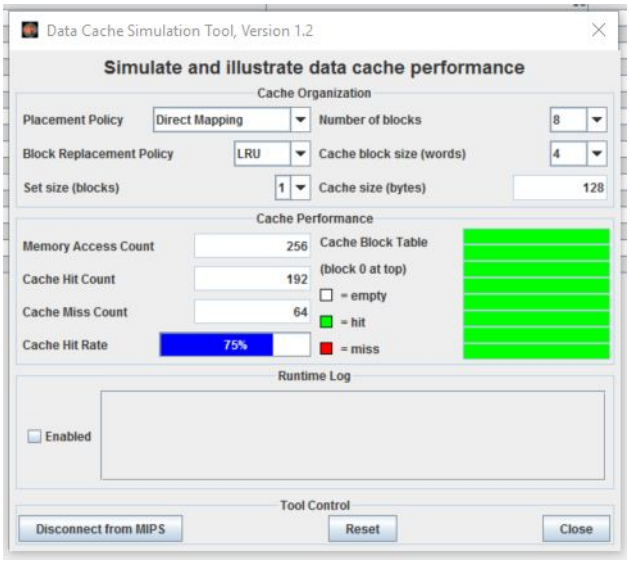


Figure 15: Row Major, Direct Mapping, Cache Block Size 4

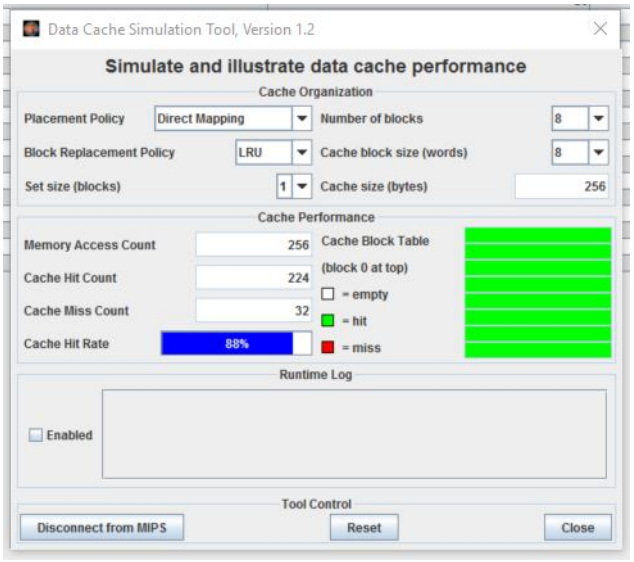


Figure 16: Row Major, Direct Mapping, Cache Block Size 8

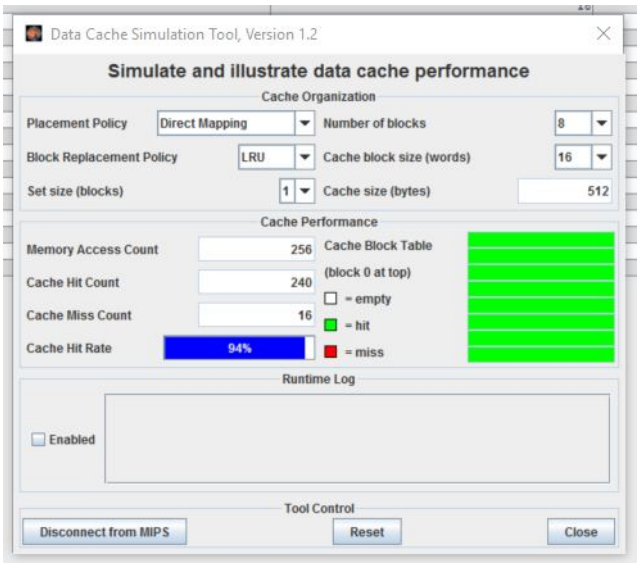


Figure 17: Row Major, Direct Mapping, Cache Block Size 16

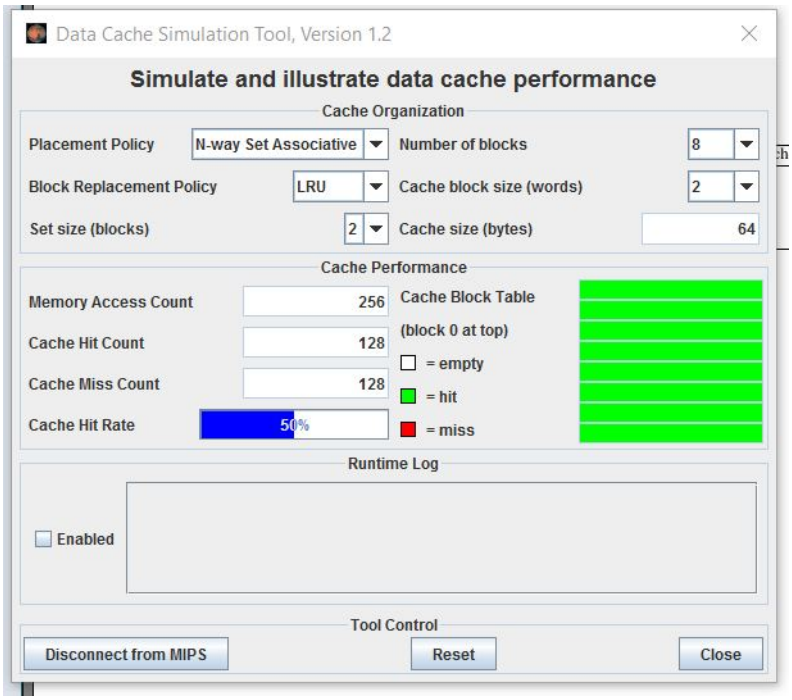


Figure 18: Row Major, 2-Way Associative, Cache Block Size 2

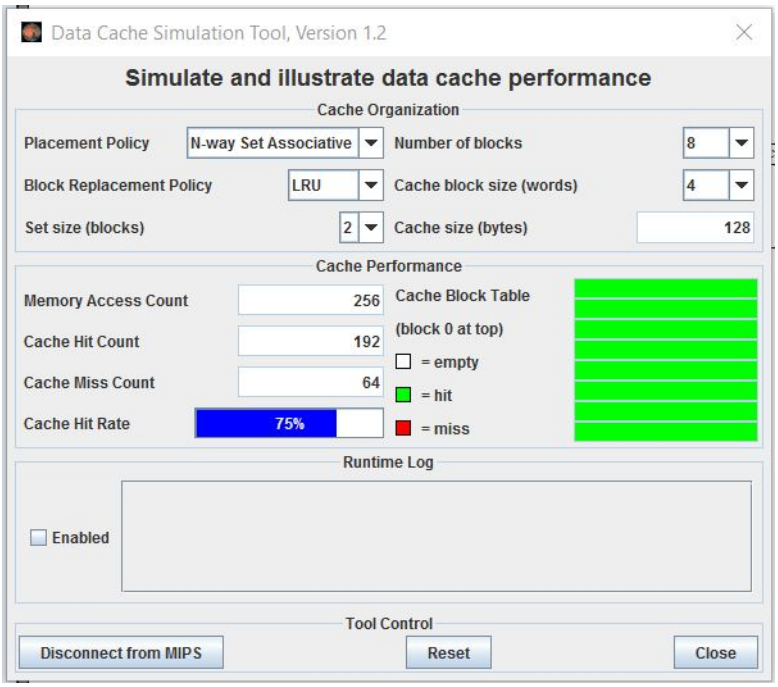


Figure 19: Row Major, 2-Way Associative, Cache Block Size 4

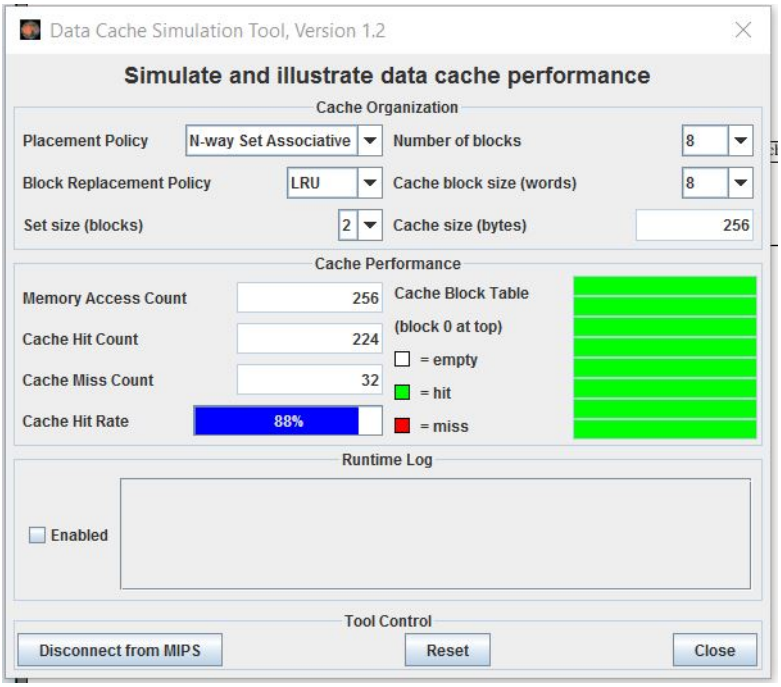


Figure 20: Row Major, 2-Way Associative, Cache Block Size 8

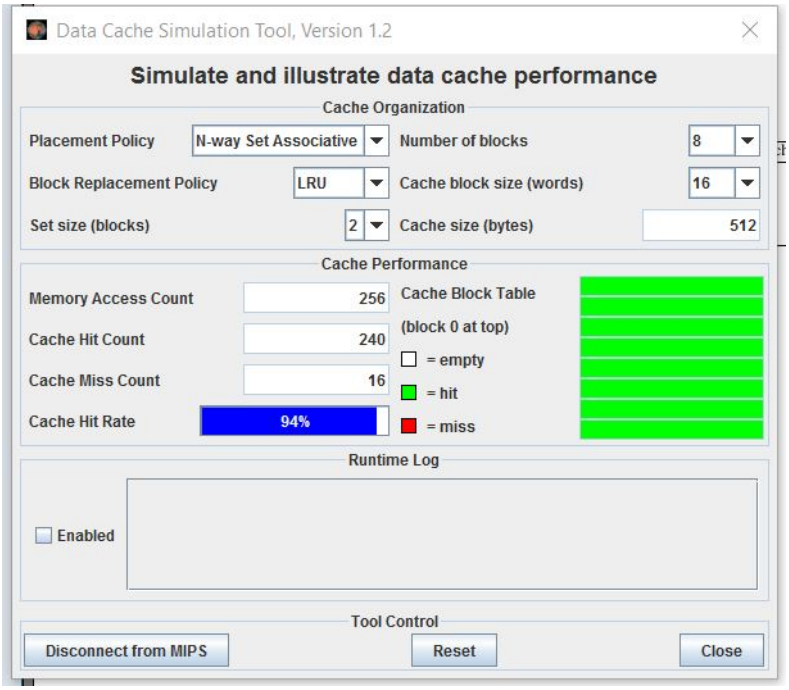


Figure 21: Row Major, 2-Way Associative, Cache Block Size 16

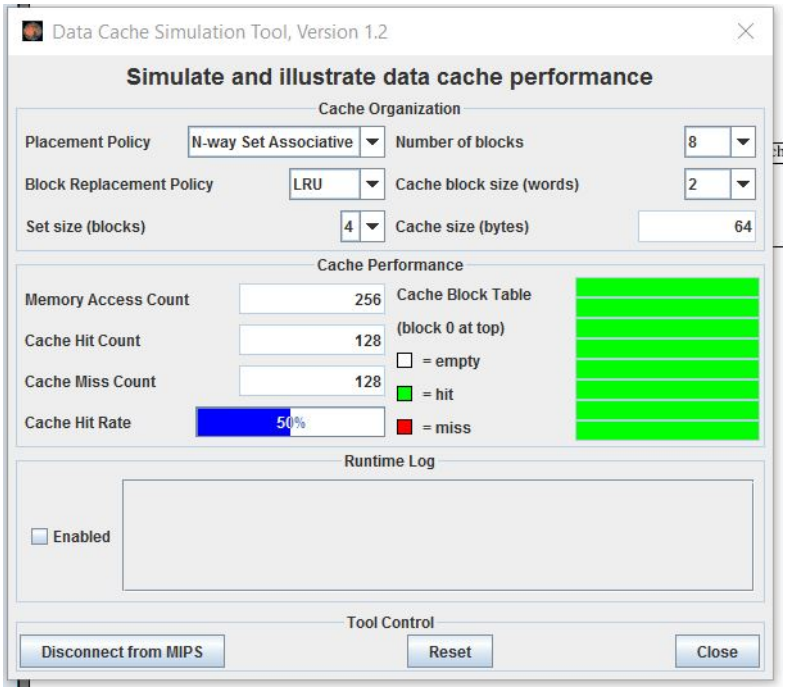


Figure 22: Row Major, 4-Way Associative, Cache Block Size 2

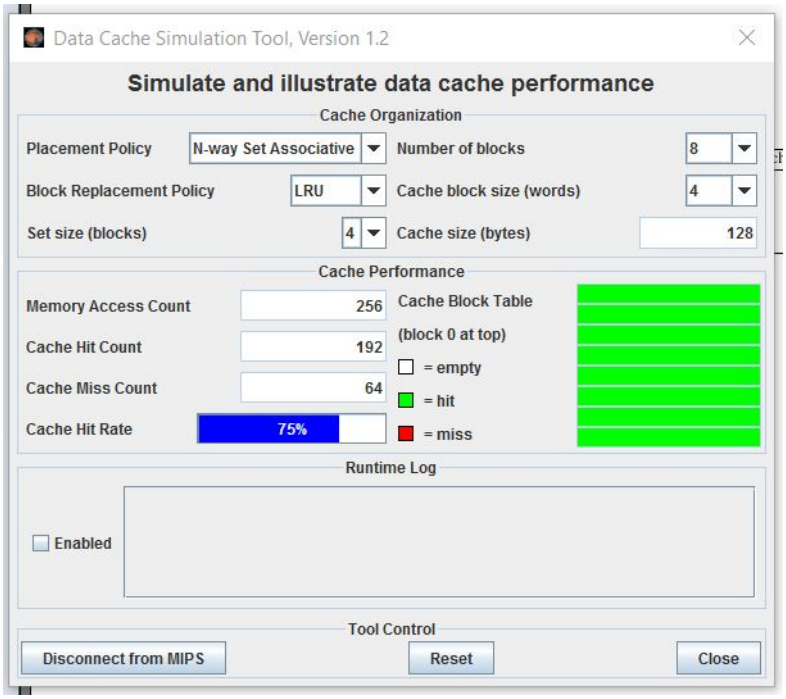


Figure 23: Row Major, 4-Way Associative, Cache Block Size 4

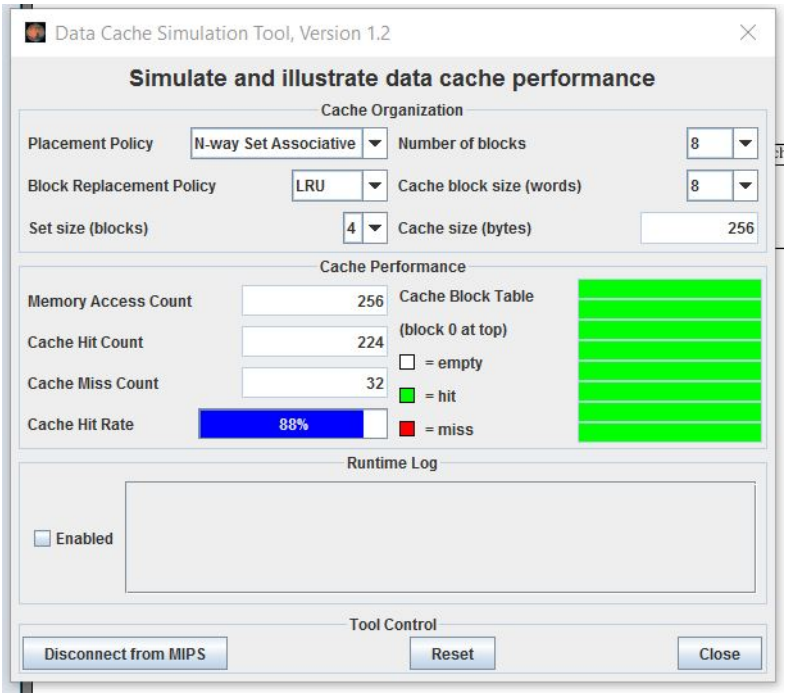


Figure 24: Row Major, 4-Way Associative, Cache Block Size 8

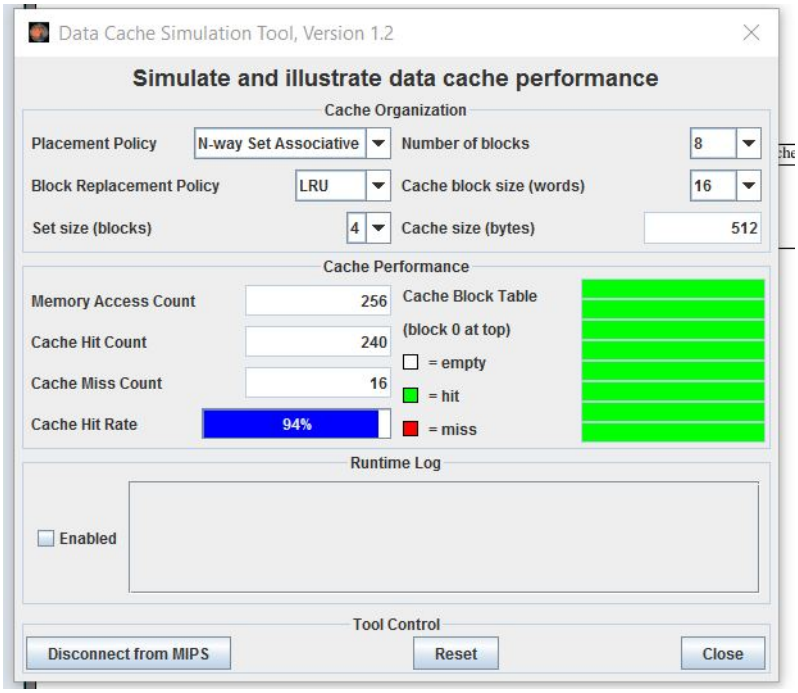


Figure 25: Row Major, 4-Way Associative, Cache Block Size 16