TUHH
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TECHNISCHE UNIVERSITÄT HAMBURG

PROBLEM-BASED LEARNING

Advanced System-on-Chip Design

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Advanced System-on-Chip Design

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Tabelle 1: Cache Simulation of Column Major

Placement (Policy)	Cache Block Size (Words)	Cache Hit Count	Cache Miss Count	Cache Hit Rate
Direct Mapping	2	0	256	0
Direct Mapping	4	0	256	0
Direct Mapping	8	0	256	0
Direct Mapping	16	0	256	0
2-Way Set Associative	2	0	256	0
2-Way Set Associative	4	0	256	0
2-Way Set Associative	8	0	512	0
2-Way Set Associative	16	0	256	0
4-Way Set Associative	2	0	256	0
4-Way Set Associative	4	0	256	0
4-Way Set Associative	8	0	256	0
4-Way Set Associative	16	0	256	0

Tabelle 2: Cache Simulation of Row Major

Placement (Policy)	Cache Block Size (Words)	Cache Hit Count	Cache Miss Count	Cache Hit Rate
Direct Mapping	2	128	128	50
Direct Mapping	4	192	64	75
Direct Mapping	8	224	32	88
Direct Mapping	16	240	16	94
2-Way Set Associative	2	128	128	50
2-Way Set Associative	4	192	64	75
2-Way Set Associative	8	224	32	88
2-Way Set Associative	16	240	16	94
4-Way Set Associative	2	128	128	50
4-Way Set Associative	4	192	64	75
4-Way Set Associative	8	224	16	88
4-Way Set Associative	16	240	16	94

1 Cache Simulation - Results

The two assembler programs *row-major.asm* and *column-major.asm* has been used for the cache simulation. 1 contains the results regarding the file *column-major.asm* and 2 illustrates the results of *row-major.asm*.
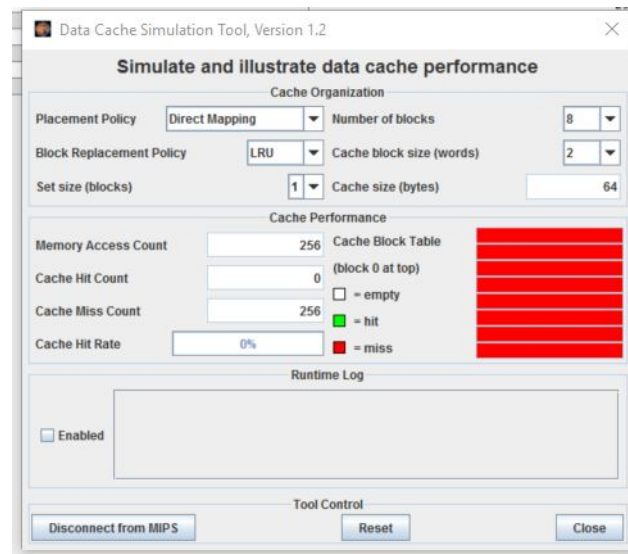TODO Interpretation

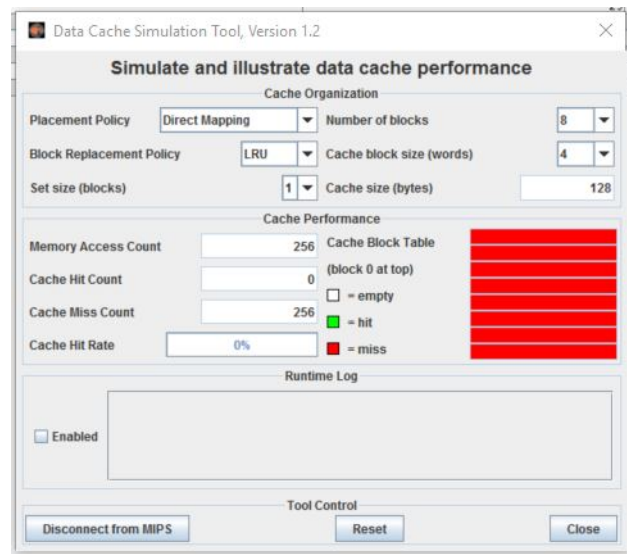Abbildung 1: Column Major, Direct Mapping, Cache Block Size 2

2 Appendix

Abbildung 2: Column Major, Direct Mapping, Cache Block Size 4
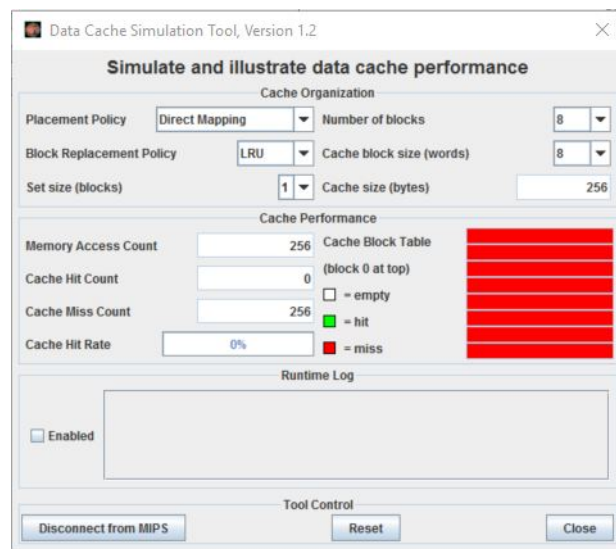

Abbildung 3: Column Major, Direct Mapping, Cache Block Size 8
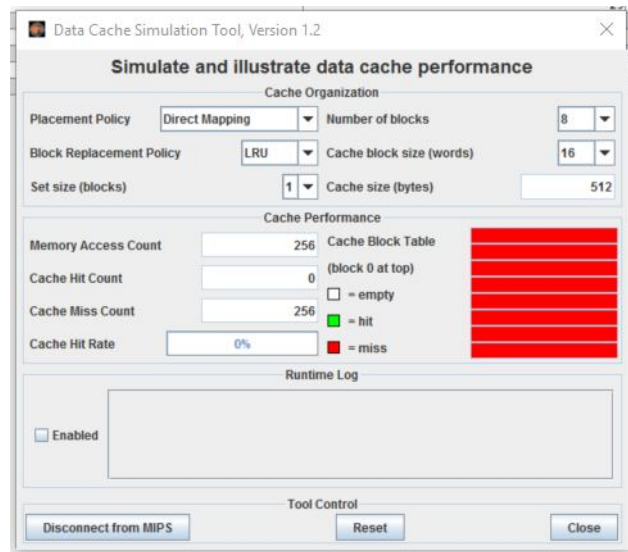
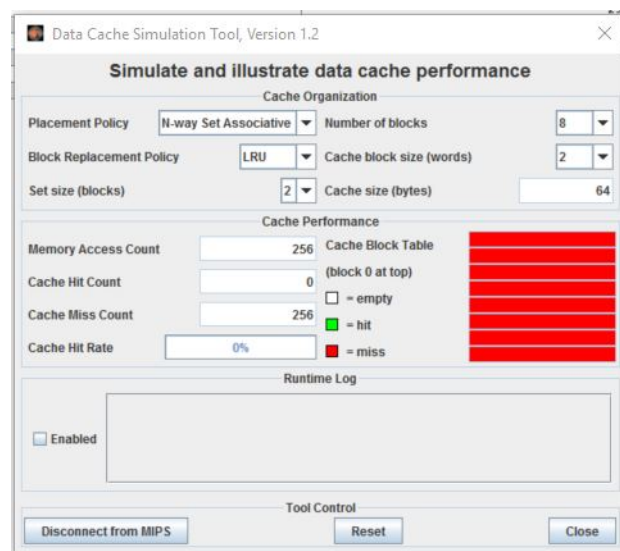Abbildung 4: Column Major, Direct Mapping, Cache Block Size 16

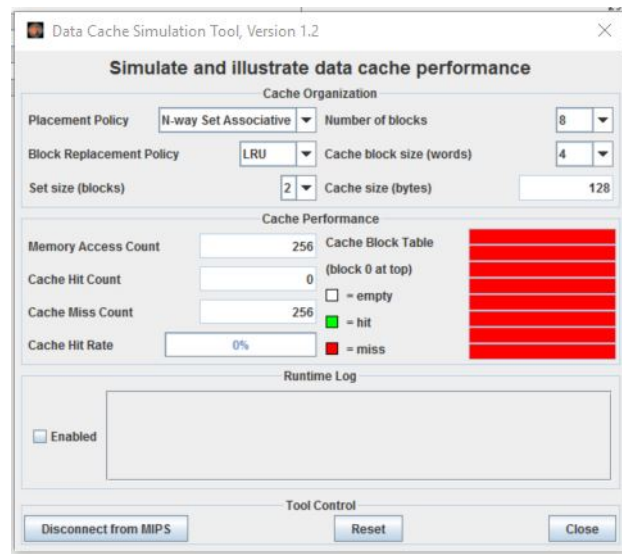Abbildung 5: Column Major, 2-Way Associative, Cache Block Size 2

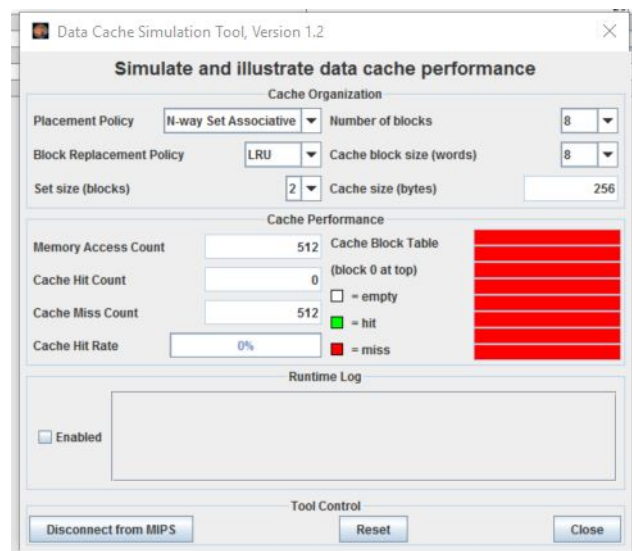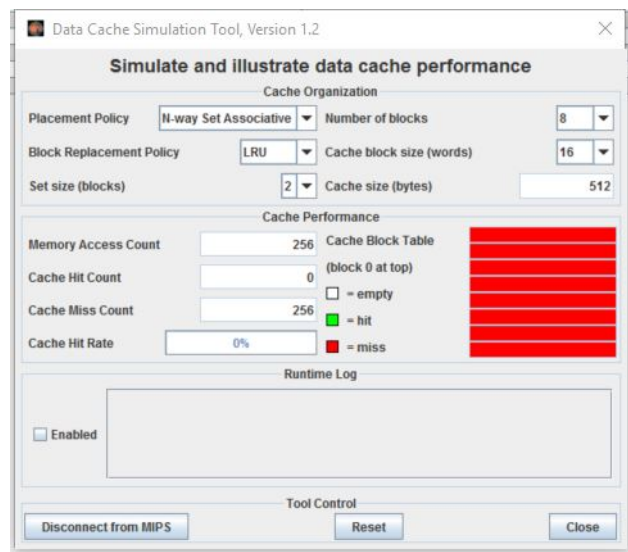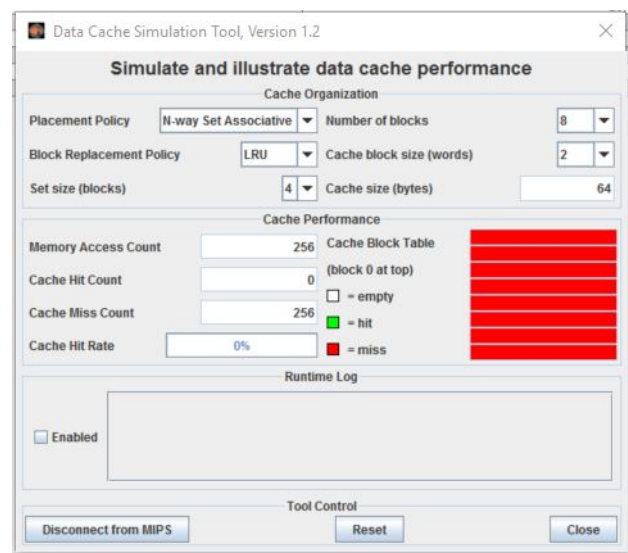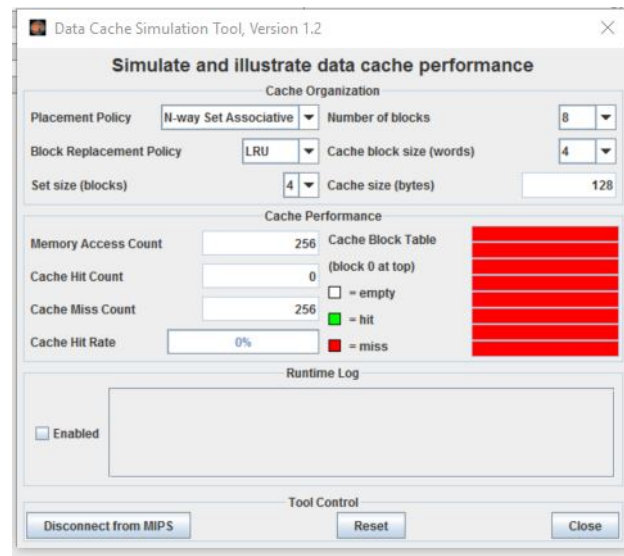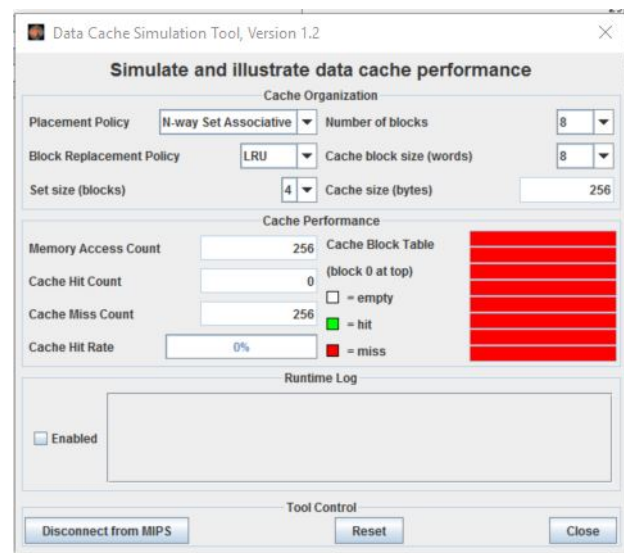Abbildung 6: Column Major, 2-Way Associative, Cache Block Size 4

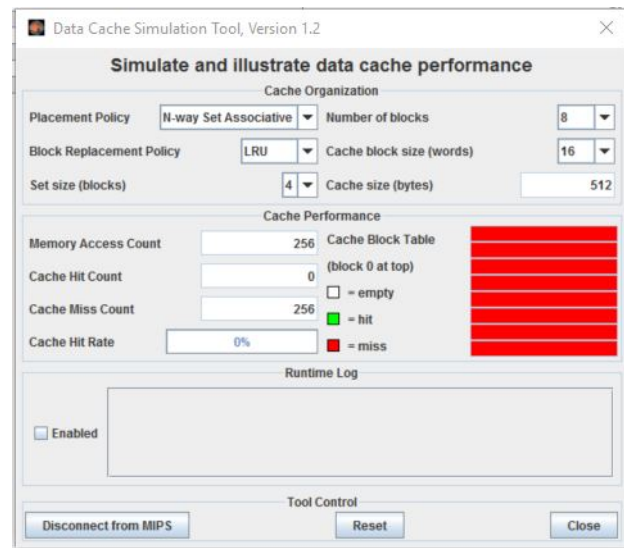Abbildung 7: Column Major, 2-Way Associative, Cache Block Size 8

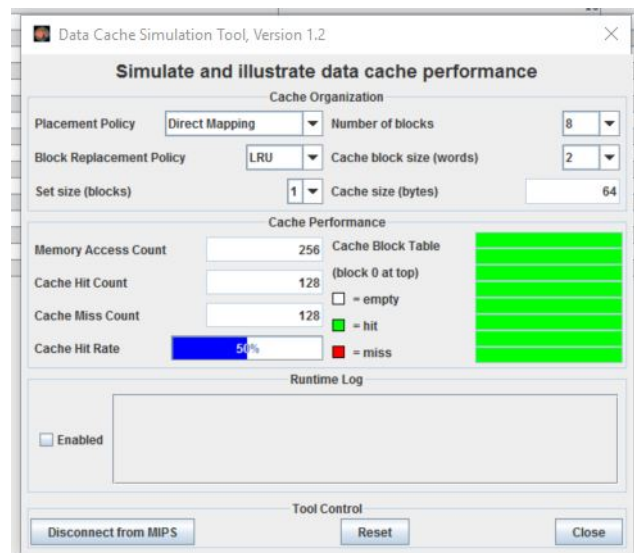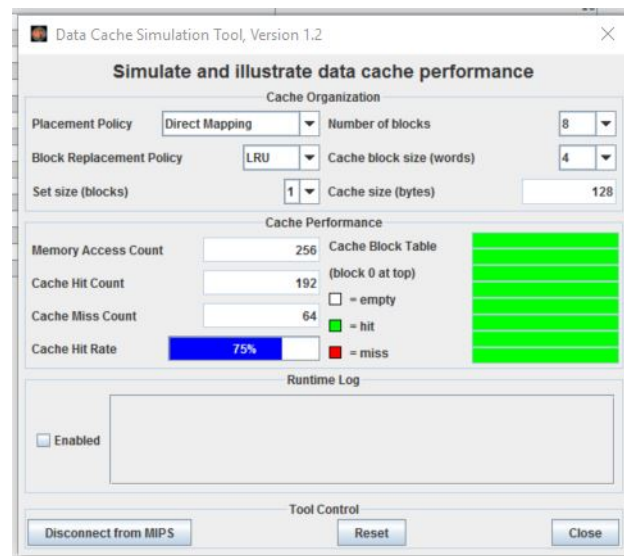Abbildung 8: Column Major, 2-Way Associative, Cache Block Size 16

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Abbildung 13: Row Major, Direct Mapping, Cache Block Size 2

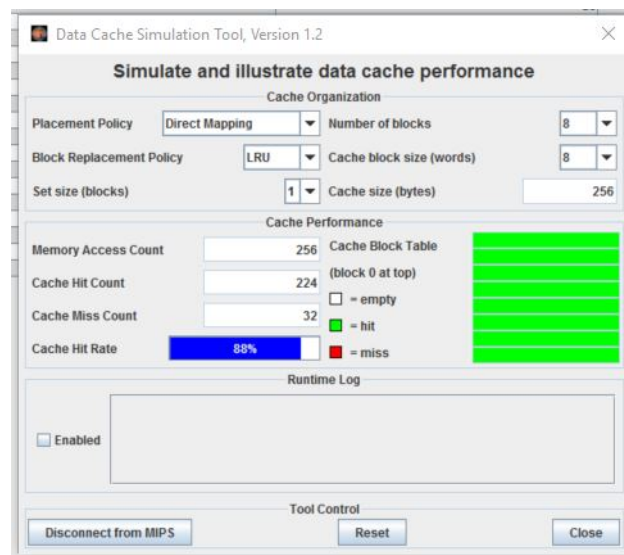Abbildung 14: Row Major, Direct Mapping, Cache Block Size 4

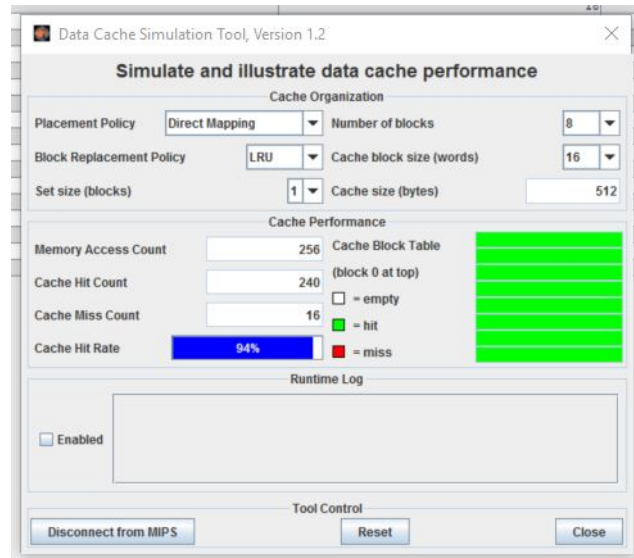Abbildung 15: Row Major, Direct Mapping, Cache Block Size 8

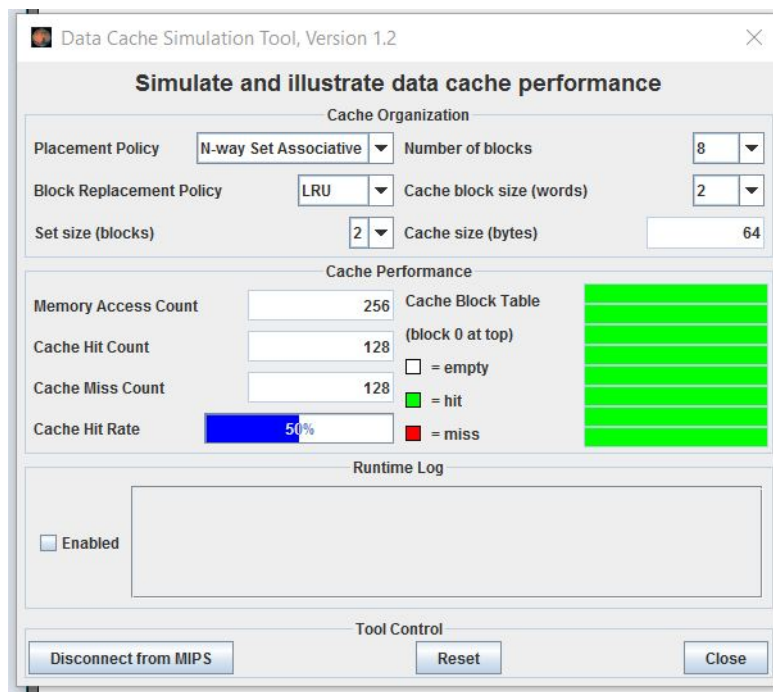Abbildung 16: Row Major, Direct Mapping, Cache Block Size 16

Abbildung 17: Row Major, 2-Way Associative, Cache Block Size 2
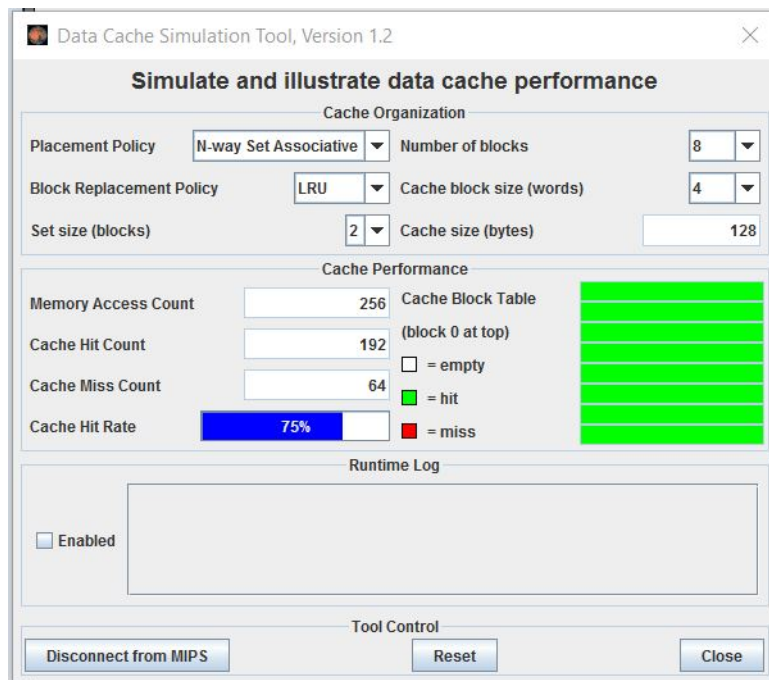
Abbildung 18: Row Major, 2-Way Associative, Cache Block Size 4
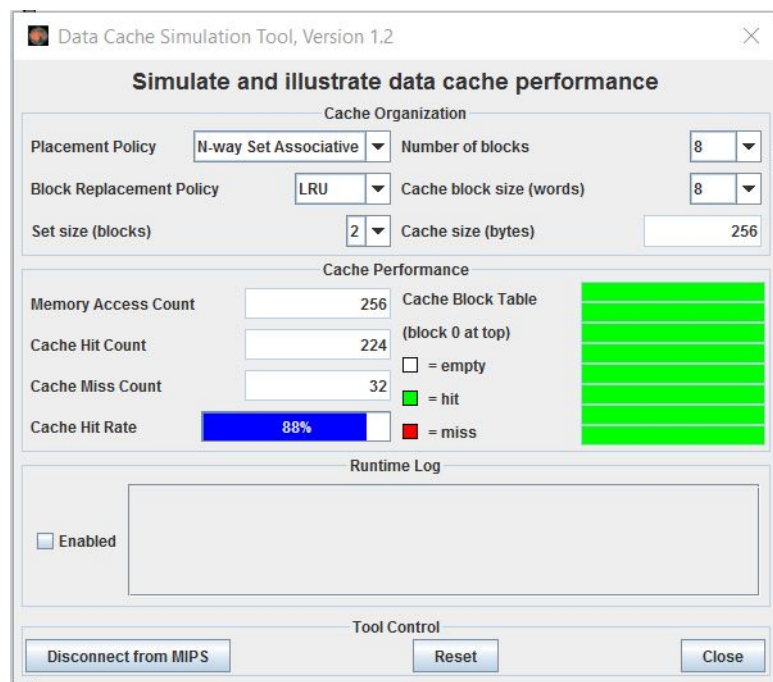

Abbildung 19: Row Major, 2-Way Associative, Cache Block Size 8
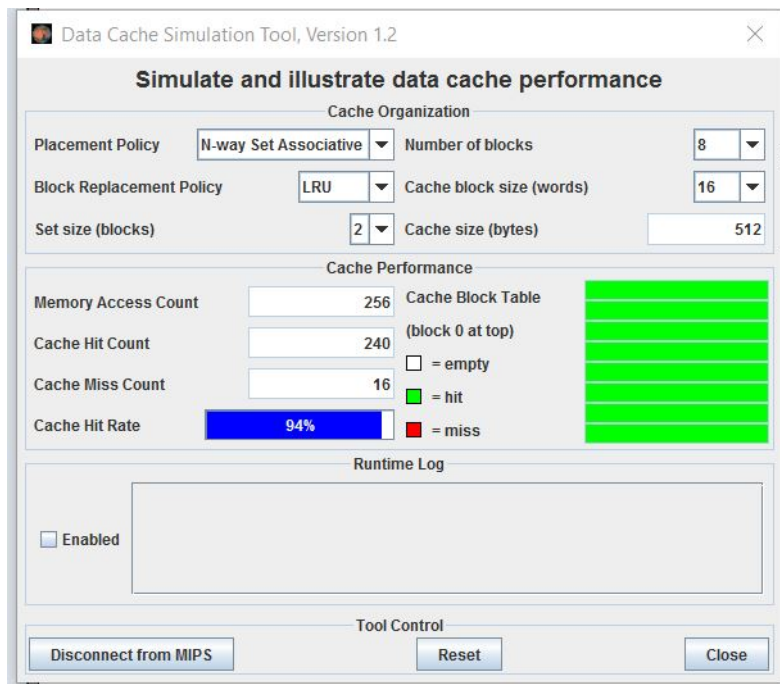
Abbildung 20: Row Major, 2-Way Associative, Cache Block Size 16
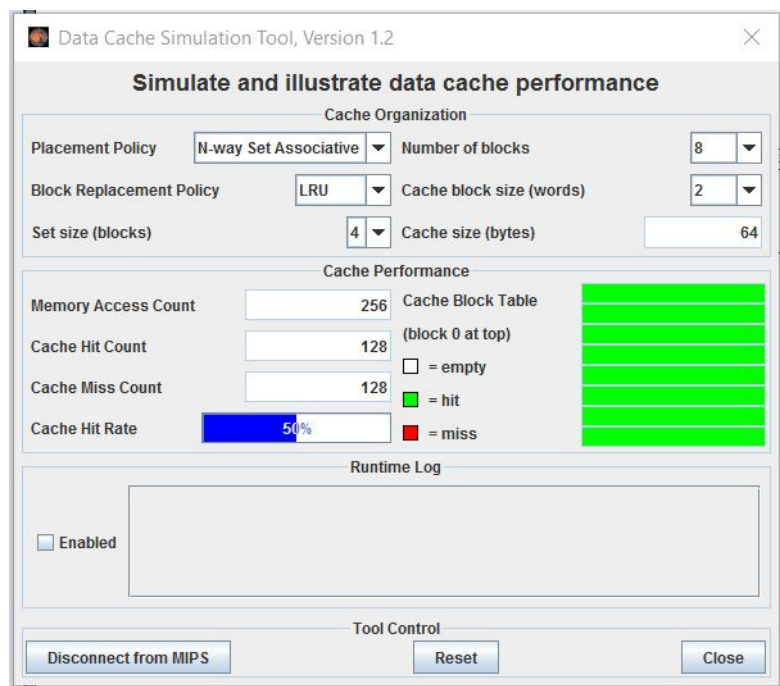

Abbildung 21: Row Major, 4-Way Associative, Cache Block Size 2
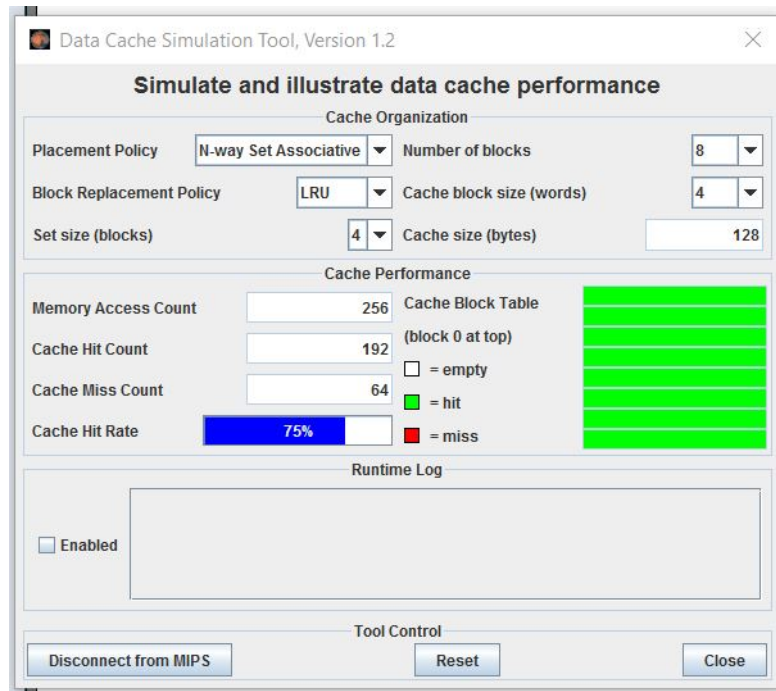
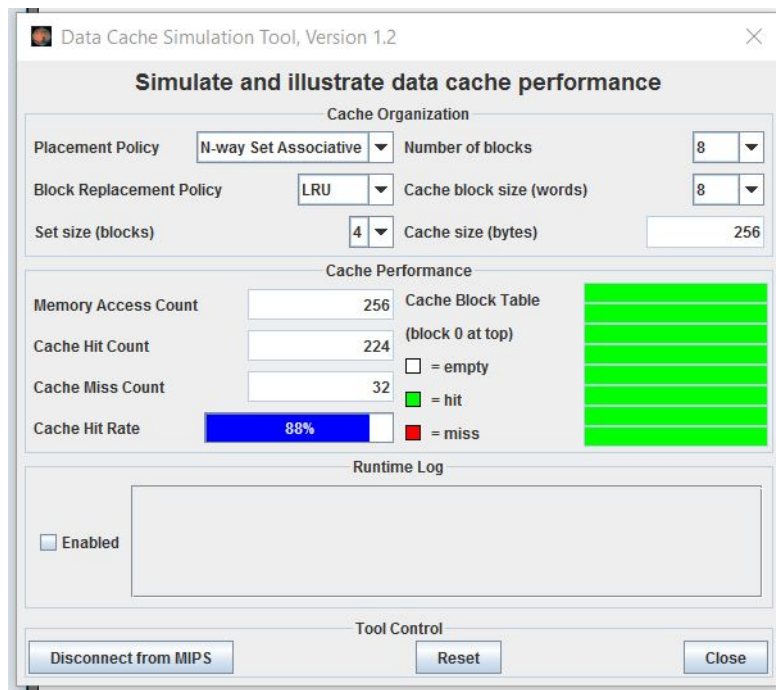Abbildung 22: Row Major, 4-Way Associative, Cache Block Size 4

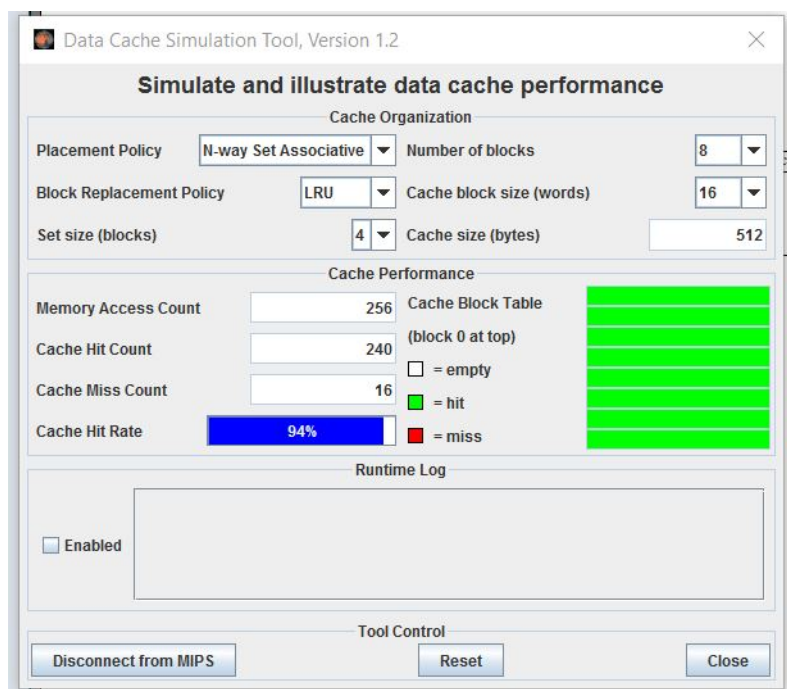Abbildung 23: Row Major, 4-Way Associative, Cache Block Size 8

Abbildung 24: Row Major, 4-Way Associative, Cache Block Size 16