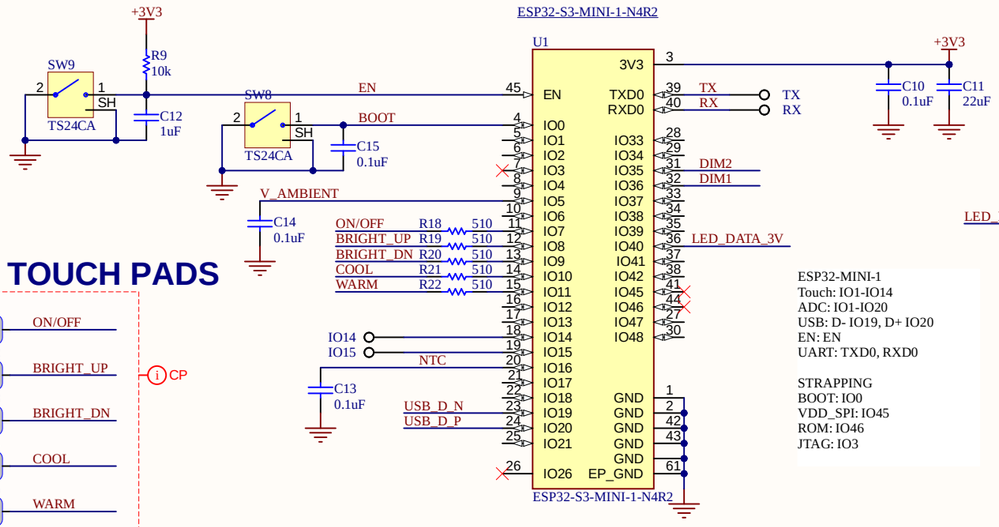
| REVISION | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| | | | |

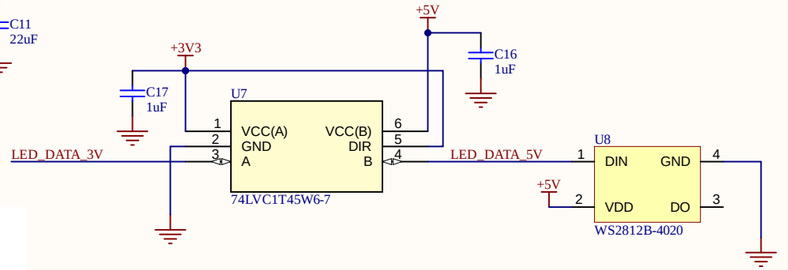
## ESP32-S3



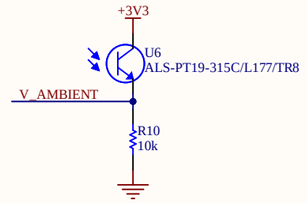

ESP32-MINI-1
Touch: IO1-IO14
ADC: IO1-IO20
USB: D- IO19, D+ IO20
EN: EN
UART: TXD0, RXD0

STRAPPING
BOOT: IO0
VDD_SPI: IO45
ROM: IO46
JTAG: IO3

## LED INDICATOR



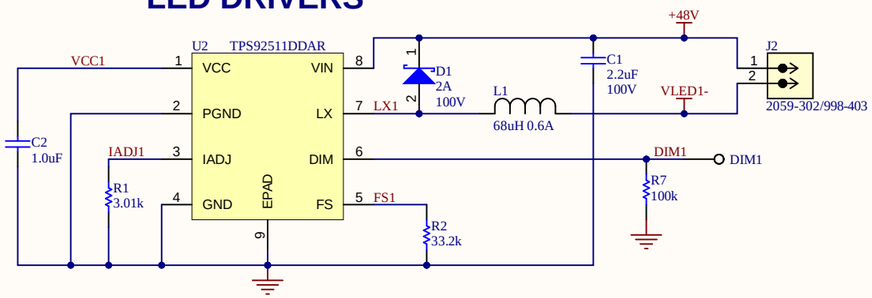

## LIGHT SENSOR

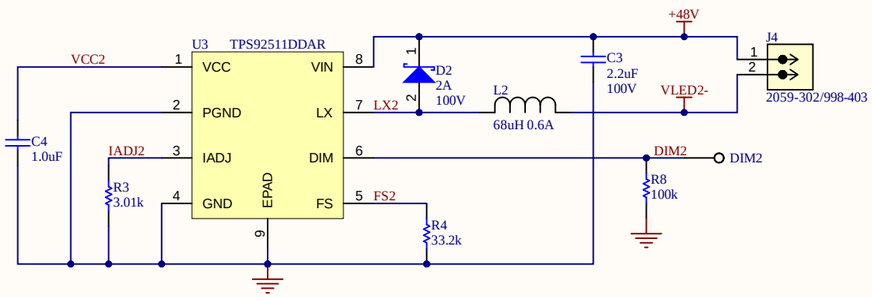



## CAPACITIVE TOUCH PADS

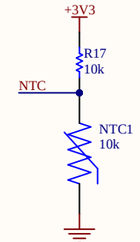



## LED DRIVERS



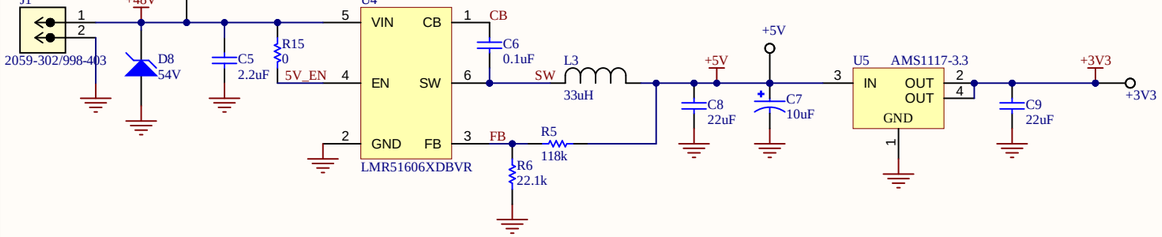

## TEMP SENSOR

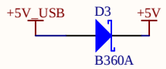



## POWER INPUT (9V-60V)

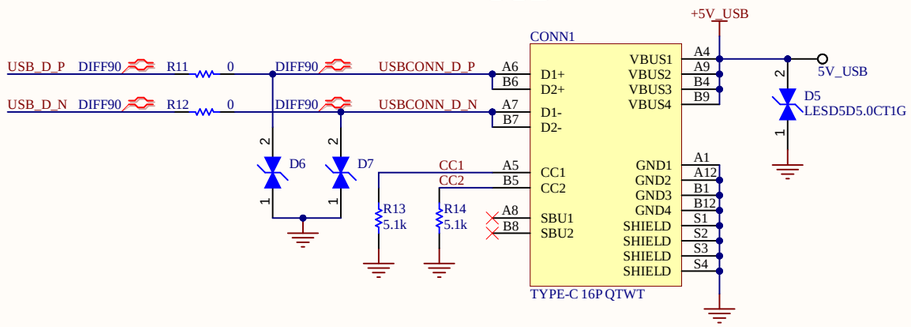
warning, no reverse polarity protection

## VOLTAGE CONVERSION




## USB




## MOUNTING STANDOFFS


ESP32-C3-MINI-1-H4

498mA max

$$I_{LED} = \frac{1500}{R_{IADJ}} A$$

**Table 1. Commonly Used $f_{SW}$ And $R_{FS}$**

| $f_{SW}$ (kHz) | $R_{FS}$ (kΩ) |
|---|---|
| 50 | 200 |
| 100 | 100 |
| 300 | 33.2 |
| 500 | 20 |

**10.1 Layout Guidelines**

- The PCB layout of the TPS92511 application circuit plays an important role in optimizing the performance.
- The external components should be placed as close to the TPS92511 as possible to minimize resistance and parasitic inductance of copper traces.
- For example, $D_1$ and $L_1$ should be near the LX pin, and $C_{VCC}$ should be near the VCC pin, and the connecting copper traces are short and thick.
- The exposed pad of the TPS92511, which is internally connected to the die substrate, should be connect to a ground plane, and the plane should be extended as much as possible on the same copper layer around the TPS92511.
- Using numerous vias beneath the exposed pad to dissipate heat to another copper layer is also a good practice.

**10.2 Layout Example**

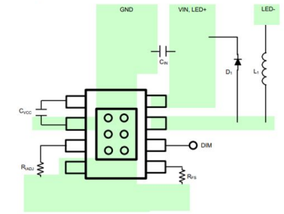



Figure 32. TPS92511 Board Layout

**10.2.1 Thermal Consideration**

$\Psi_{JT}$ (shown in session 6.4 Thermal Information) is a relatively small value for package with exposed pad since most of the heat is dissipated through the exposed pad to the copper plate of the PCB (assuming optimized PCB layout), relatively little heat goes to the top of the device. The top of the device mold compound temperature is physically close to the device junction temperature.

For example, a 30W output TPS92511 end system at 95% power efficiency (can be estimated from the efficiency curves of Figure 13), power loss is 1.6W. Assuming all the heat is generated from the TPS92511 (which is true for high $V_{LED}$) and assuming half of the heat generated is dissipated through the top of the device. Now $\Psi_{JT}$ is 11 °C/W, the device junction temperature is estimated to be higher than the package's top-surface temperature by 11 x 1.6 x 0.5 = 8.8 (°C). If the package top-surface temperature is measured to be 90 °C (for example by an IR camera), the device junction temperature is around 99 °C, which is within the 125°C maximum junction temperature requirement with margin.

| APPROVALS | DATE |
|---|---|
| ENG: Josh Horne | |
| DSN: * | |
| CHK: * | |
| REFERENCE DOCUMENTS | |
| BOM: | |
| ASSY DWG: | |
| FAB DWG: | |
| PCB DWG: | |

| | | | |
|---|---|---|---|
| PROJECT | Altium | | |
| PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM: | |
| TITLE: DIYson.SchDoc | | | |
| SIZE: B | CAGE CODE | DWG NO. | REV |
| SCALE: | FILE NAME: DIYson.SchDoc | SHEET * | OF * |