# Projects

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| **Texas Instruments GmbH** | | Freising |
|  | *Validation Engineer* | *July 2018 – June 2020* |
| Bench validation of DCDC Buck regulators with TI LPDC teams. Scripting with Python, Teststand, LabVIEW and C#. Analysis, with pre-processing of data in Python Pandas/Numpy libraries and for Spotfire Visualizations. Various Bench measurements with scripting. Use of the Python and C#/.NET Teststand adaptors | | |

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| **Dialog Semiconductor GmbH** | | Germering |
|  | *Applications Engineer* | *Oct 2017 – April 2018* |
| * Mixed signal PMIC Buck evaluation and documentation. Supported evaluation with test case scripting in Python 2.7 with an in-house API for PMIC devices | | |

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| **Texas Instruments GmbH** | | Freising |
|  | *Validation Engineer* | *Aug 2014 –Sep 2017* |
| * Deep bench validation of DCDC buck and Buck-boost devices with TI team for LCD markets. Solved bench validation carried out by hand with automation developed with Visual Studio C# | | |

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| **Intel Mobile Communications GmbH** (was Infineon Comneon) | | Nürnberg |
|  | *Hardware Baseband Engineer* | *Aug 2010 - Jan 2014* |
| * Supported 2G – 4G platform design verification. Worked on verification on baseband power blocks, selected interfaces e.g. SIM, and RF Transceiver PSU blocks. Tools included use JTAG, Lauterbach Trace, Rohde & Schwarz CMW500, Agilent/Keysight 9000, X90000 and N6705A SMU | | |

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| **ST Ericsson** (was Ericsson GmbH) | | Nürnberg |
|  | *Power Consultant* | *Jan 2006 - Dec 2009* |
| * Design and implementation of board-level power and distribution on FPGA developer boards intended for 3G and 4G protocol stack development. Worked on power concept design on an [LTE demonstrator](https://www.techradar.com/news/phone-and-communications/mobile-phones/ericsson-first-off-4g-blocks-358135), that was first shown at the 3GSM Barcelona conference live call in early 2008 | | |

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| **Texas Instruments A/S** | | Aalborg |
|  | *Mobile Platforms Designs Verification Engineer* | *Oct 2004 –Dec 2005* |
| * Supported 3G Mobile platforms design verification. Verification on ARM trace module, use of logic Analyzer, JTAG and Lauterbach power trace debugger tools | | |

# Courses

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| * MSc (distinction), BSc (hons) and HNC |
| * Cadence, RF Engineering, NI Teststand, LabVIEW and TIBCO Spotfire |

# Previous Career (UK)

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| Various roles in Electronics: Senior Electronics Engineer, Lead Engineer, Hardware Engineer and Platform Architect in Oxford, Oxfordshire, and Birmingham areas. Electronics design with Medical equipment (infusion, and diagnostics), industrial materials analyzers, vehicle traffic survey equipment and highways communication infrastructure signaling equipment |
| Nov 1980 – Jun 2003 |

# Interests

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| Mountain walking, XC Biking, Motorcycling, Photography, Science, Technology and Programming. |

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