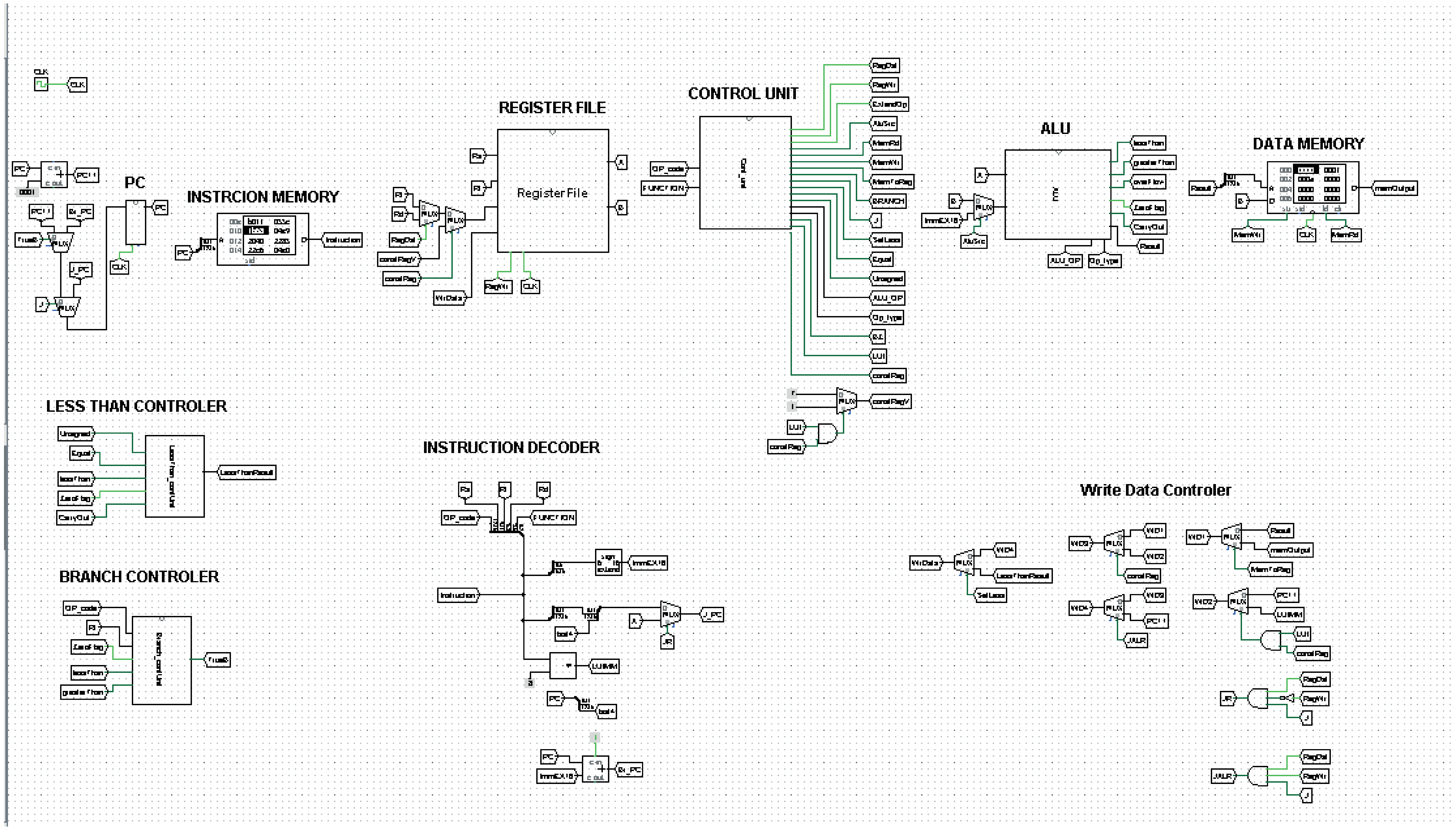
16 BIT SINGLE SYCLE PROCESSOR
PHASE : 1

TEAM: Abdlerahaman Essam - Khalid Sayed - Ali Raid - Abdlerahman Mahmoud

MAJOR: Computer Engineering

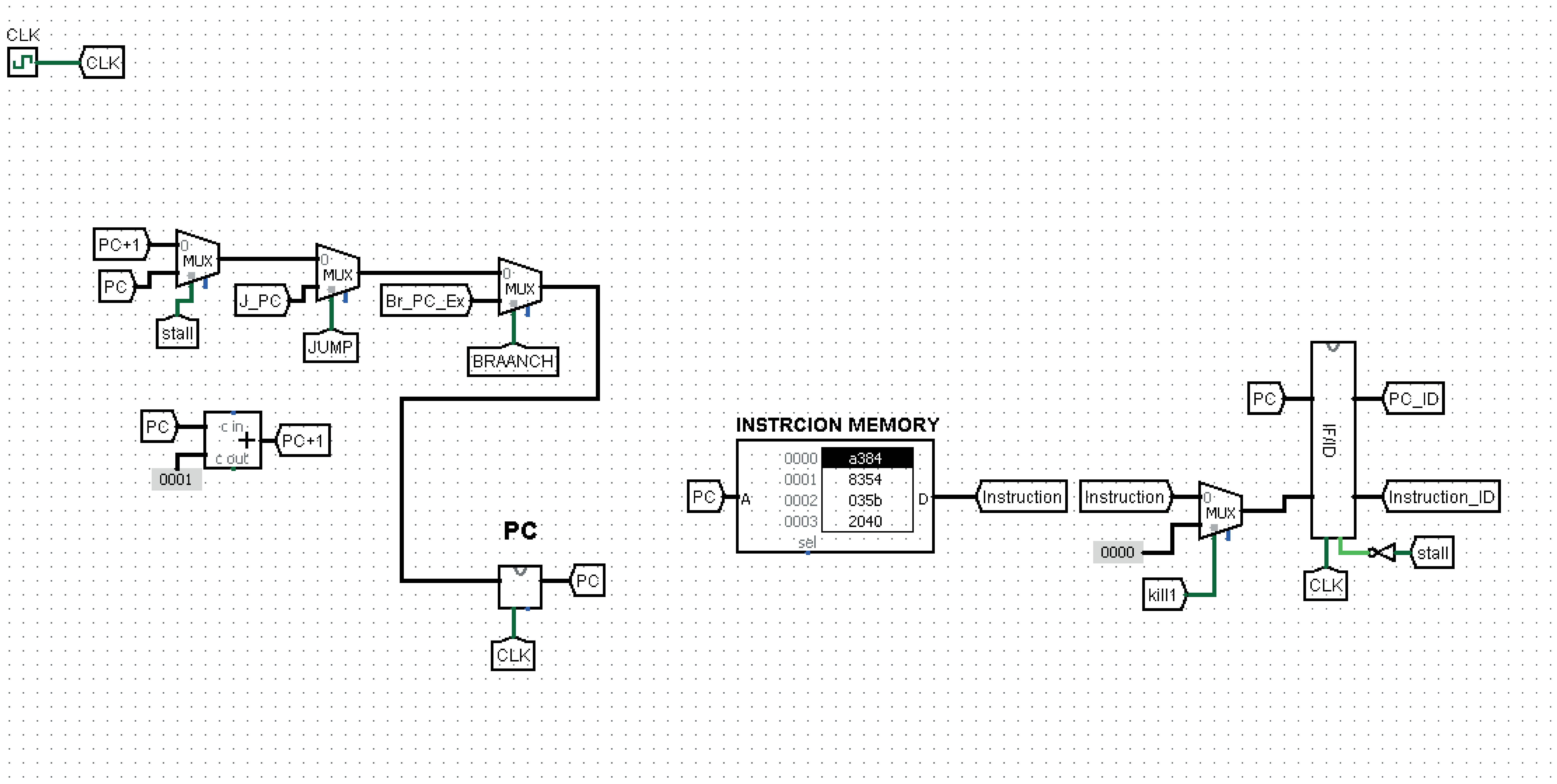
OVERALL DATAPATH :

consists of :
- 6 main parts (PC, Instruction Memory, Register File, Control Unit, ALU, DataMemory)
- 4 secondary parts (LessThan controller, Branch Controller, Instruction decoder, Data Write controller)



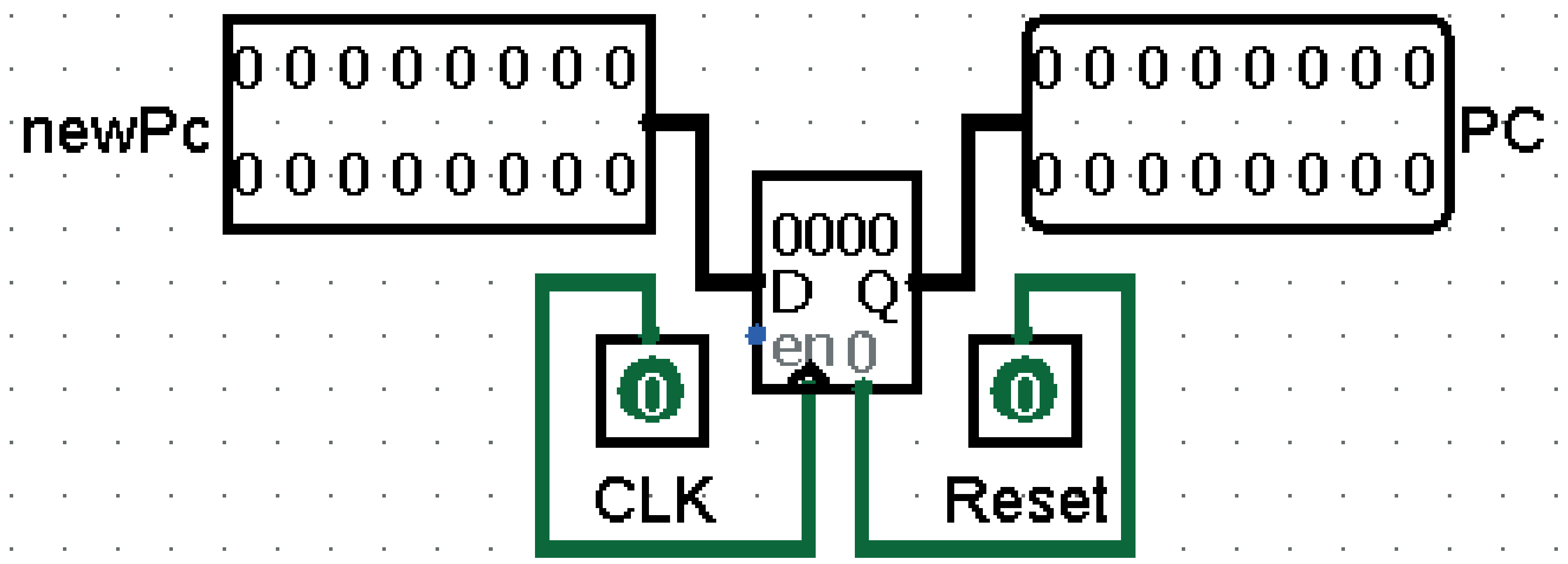
IF / ID STAGE :

1- Decides the new pc to decide which new instruction should be executed (JUMP address, BRANCH address, PC + 1).
2- fetchs the instruction from instruction memory and inject the dependecies that the DECODING stage will need.

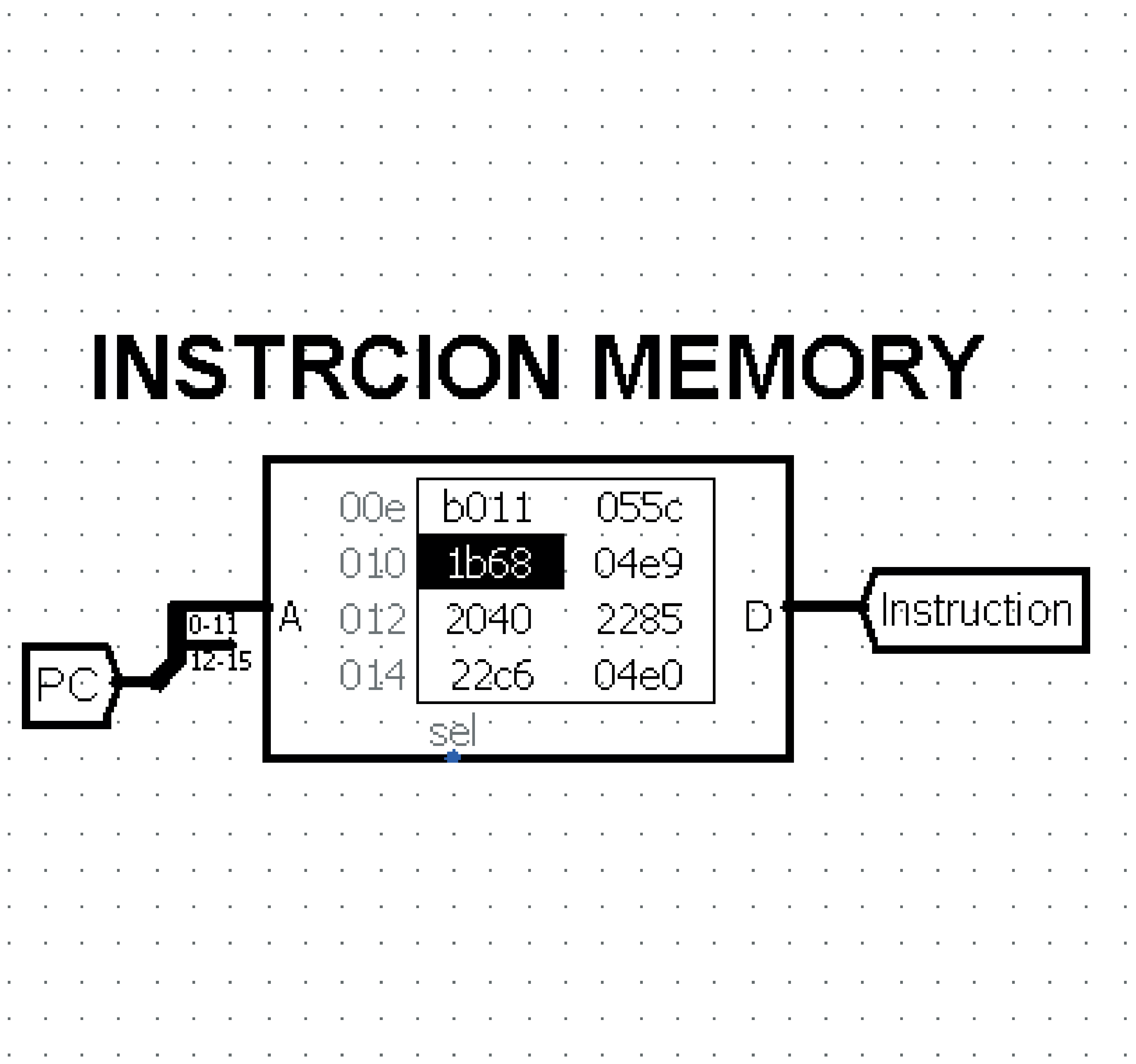


PC PART FROM INSIDE :

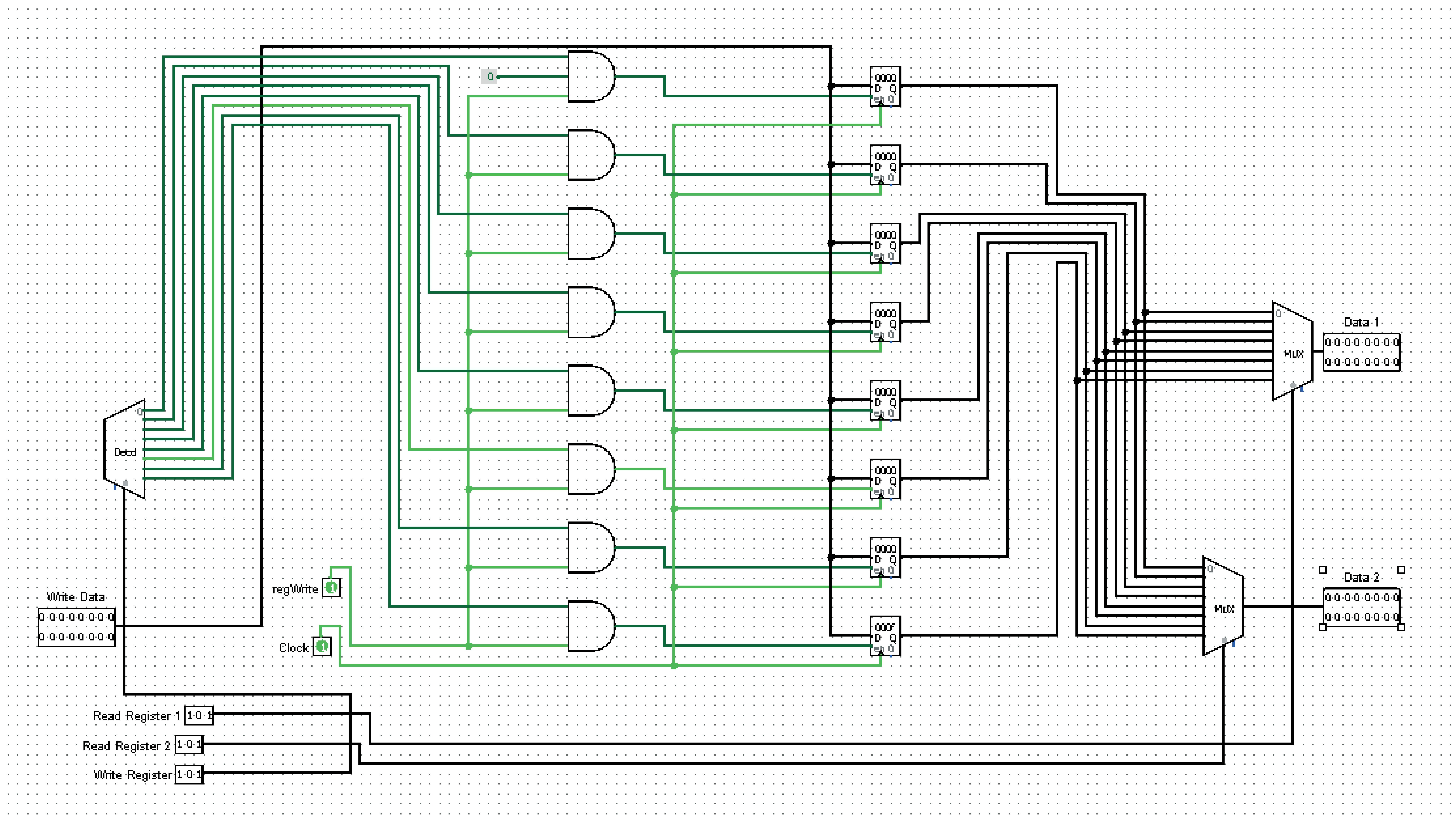
- there are MUXs before the PC input to decide which new instruction should be executed (JUMP address, BRANCH address, PC + 1)



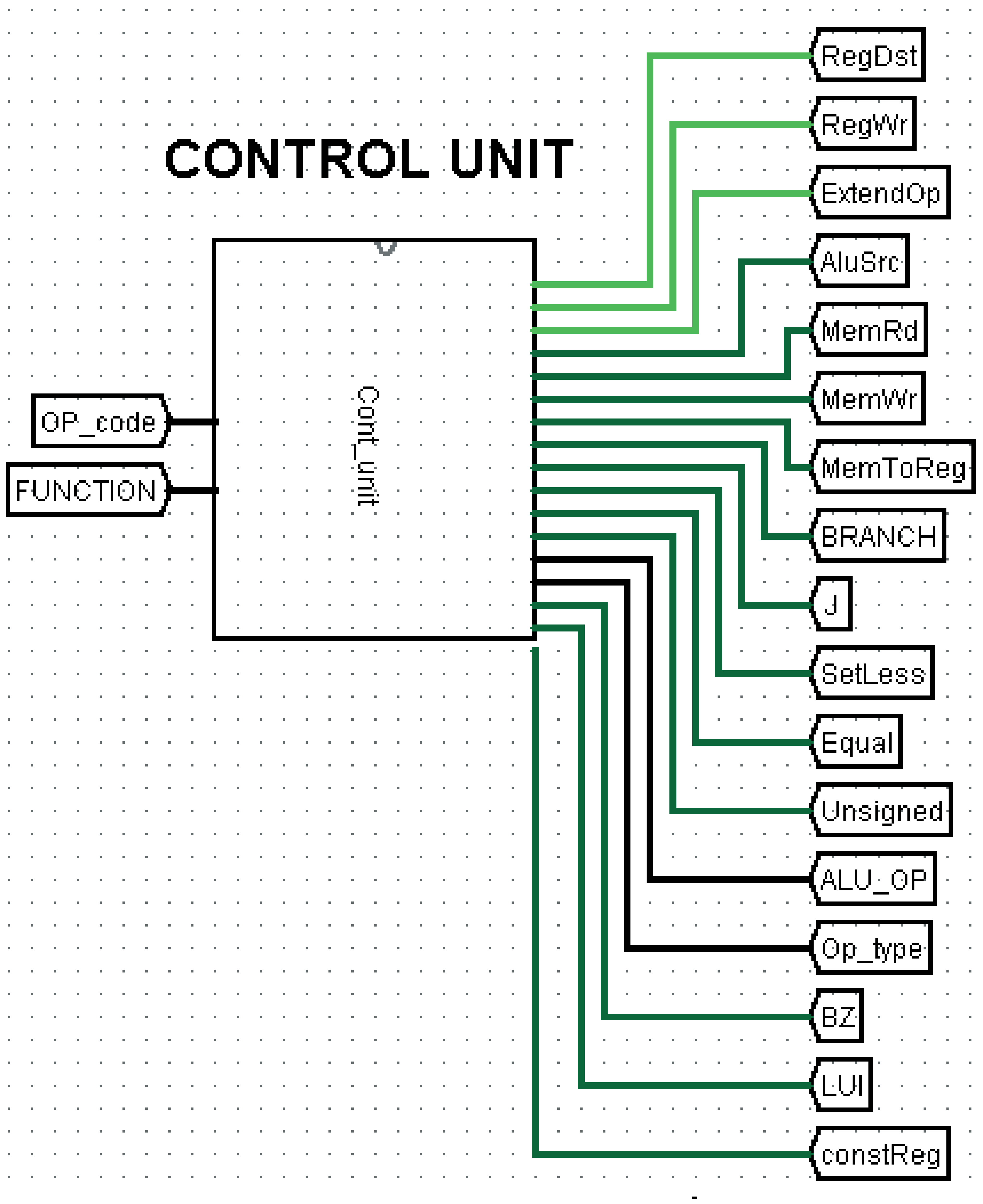
INSTRUCTION MEMEORY :



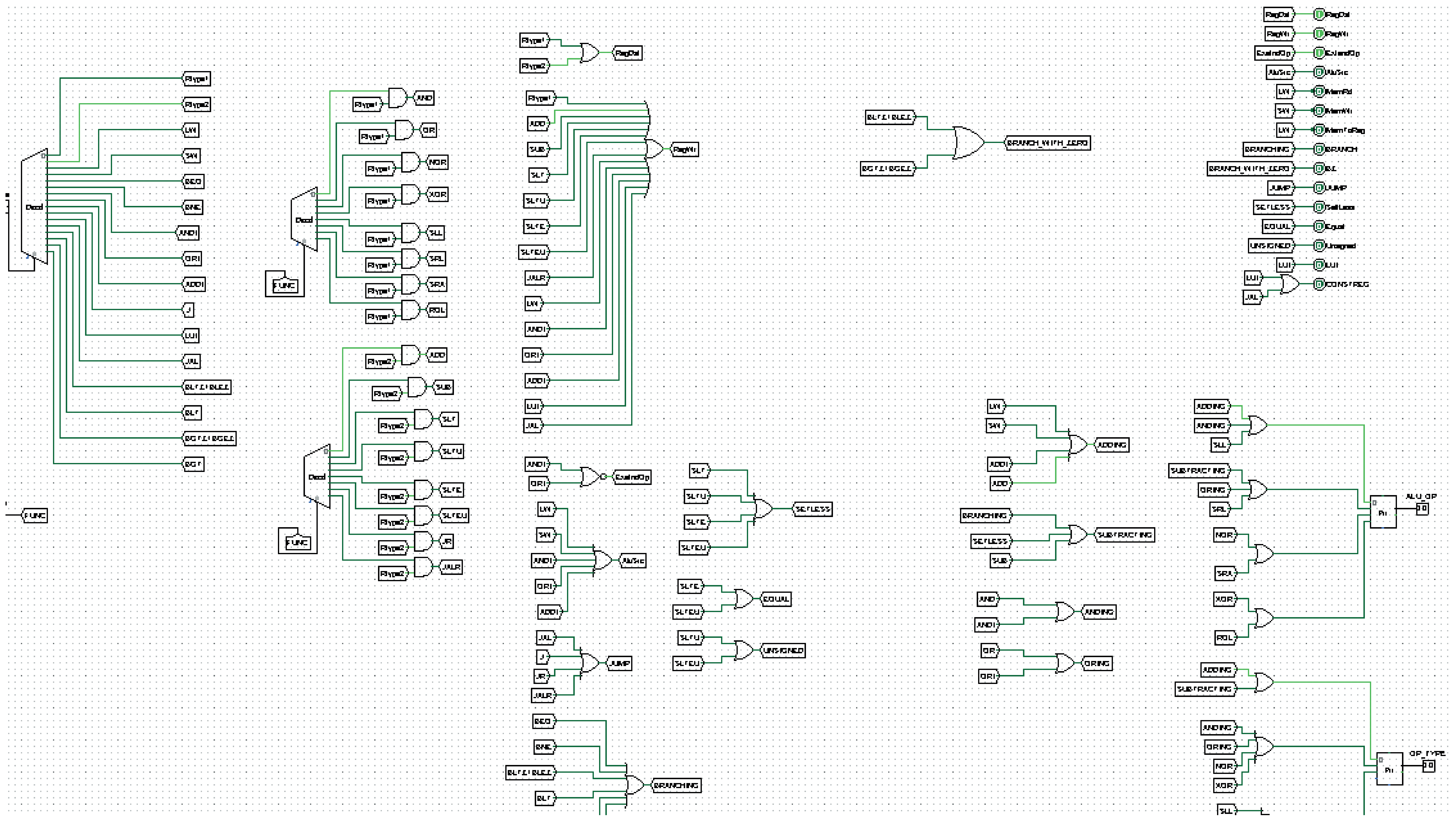
REGISTER FILE FROM INSIDE:



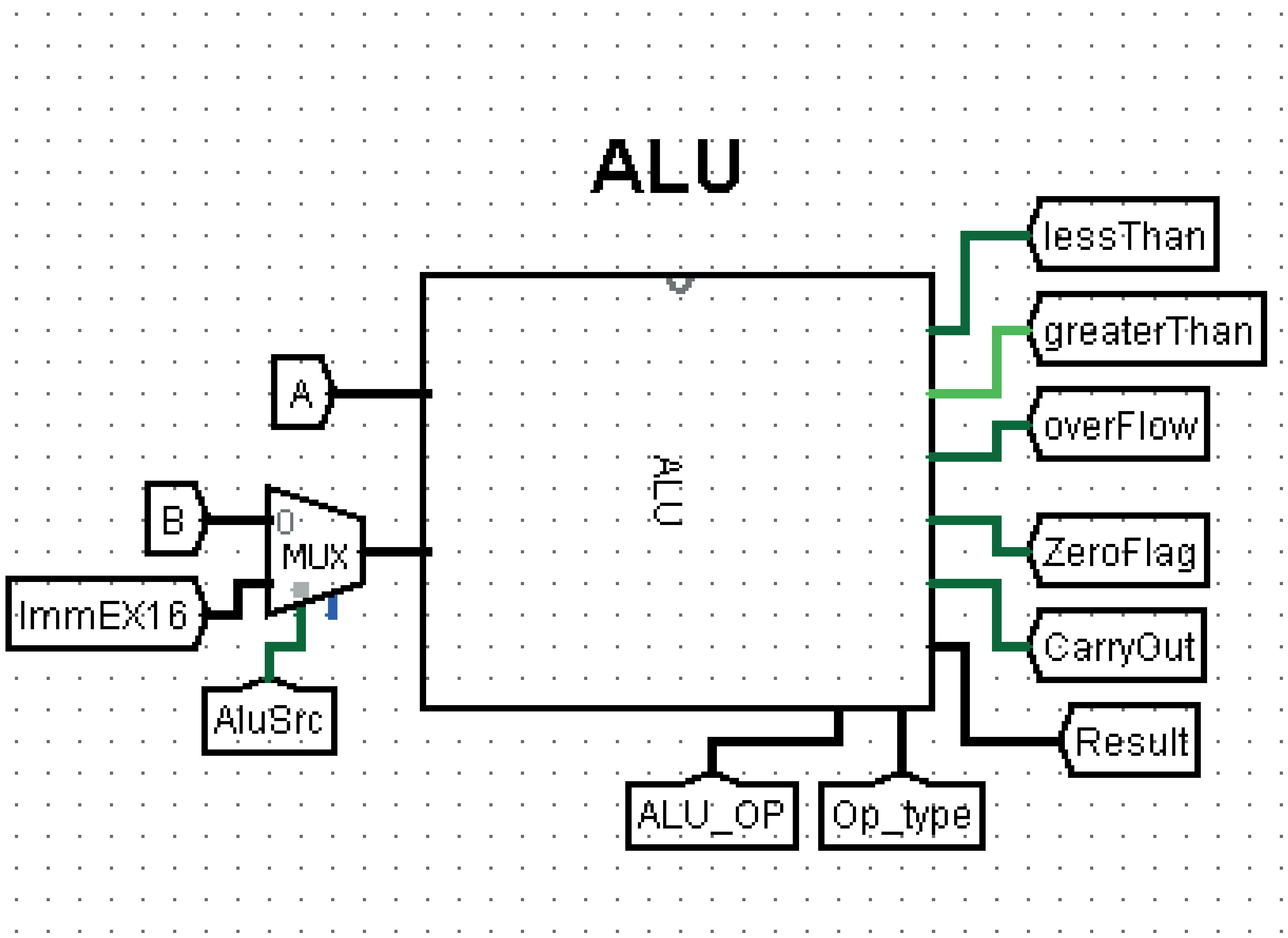
CONTROL UNIT FROM OUTSIDE:



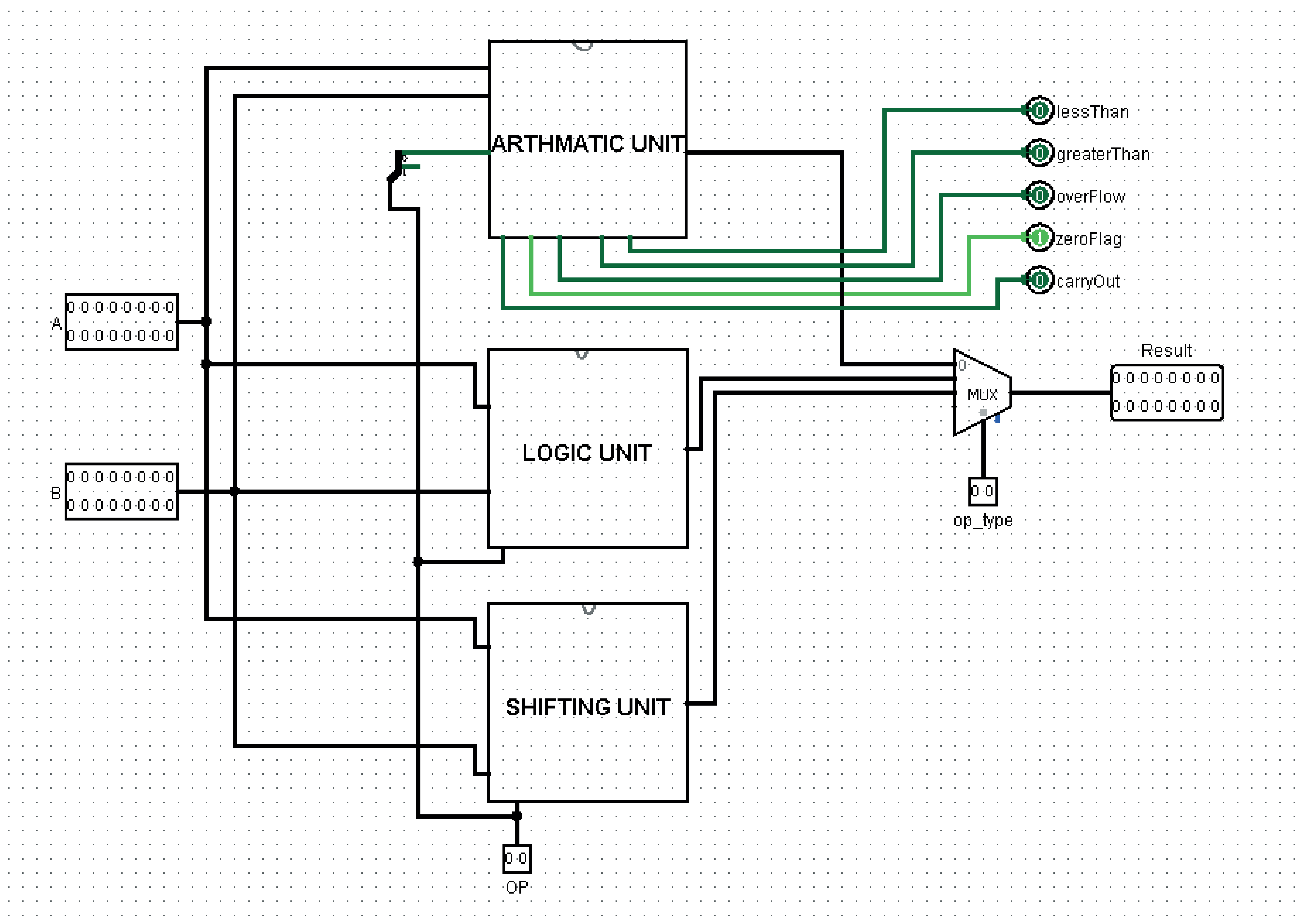
CONTROL UNIT FROM INSIDE:



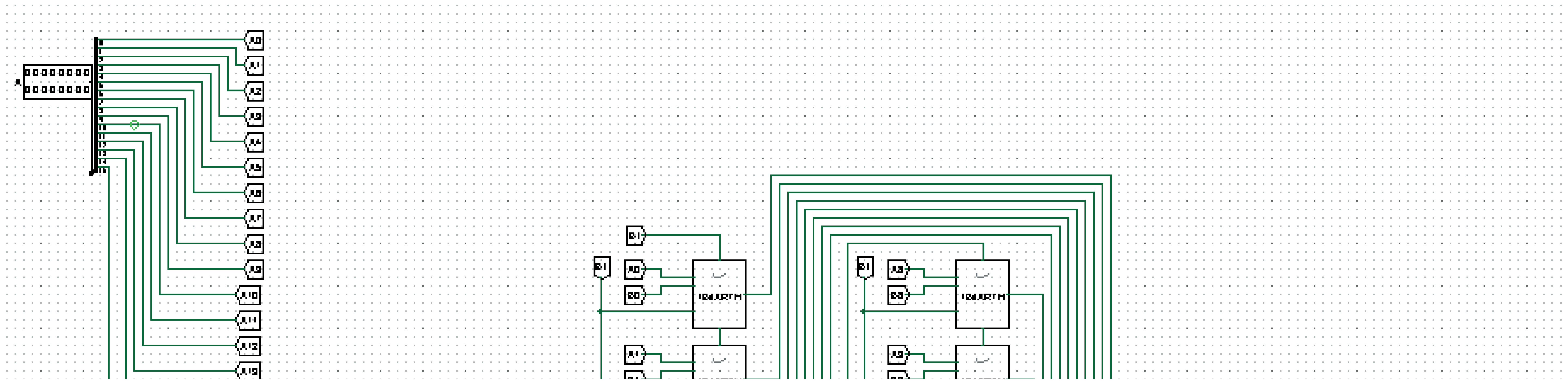
ALU FROM OUTSIDE :



ALU FROM INSIDE :



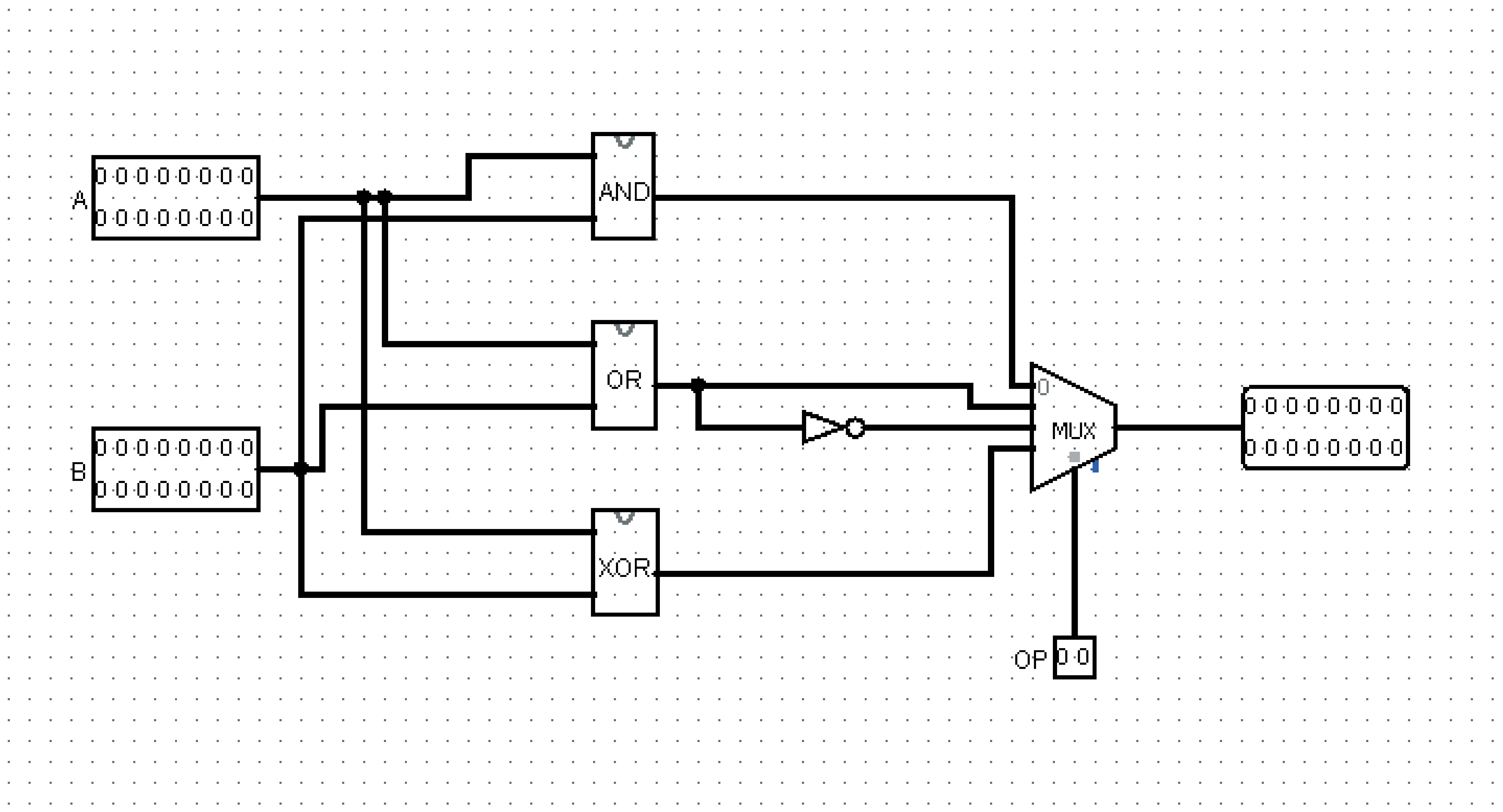
ARITHMATIC UNIT FROM INSIDE :



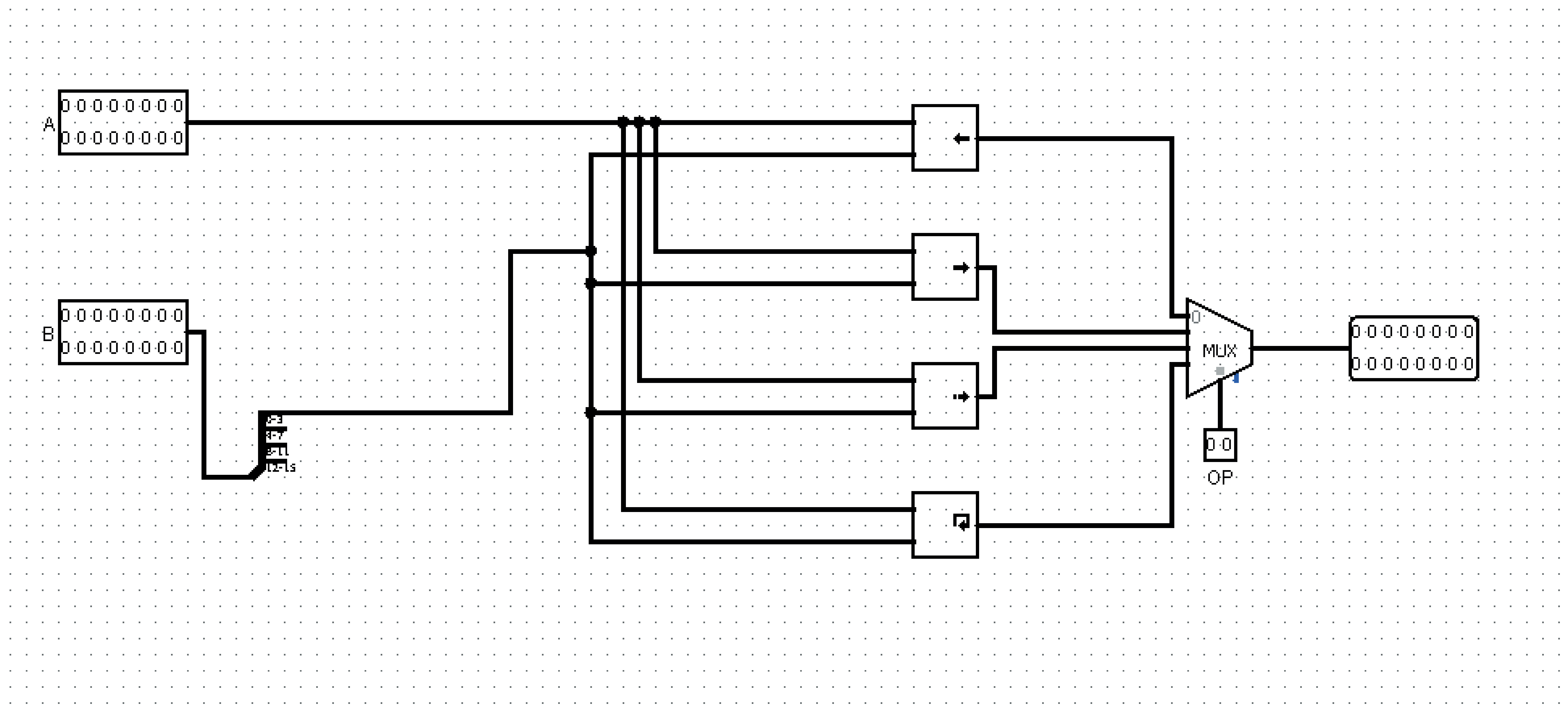
MAIN SIGNALS TABLE :

OP	RegDst	RegWr	ExtOp	AluSrc	MemRd	MemWr	MemToReg	Jmp	Branch	AluOp
AND	1	1	X	0	0	0	0	0	0	and
OR	1	1	X	0	0	0	0	0	0	or
NOR	1	1	X	0	0	0	0	0	0	nor
XOR	1	1	X	0	0	0	0	0	0	xor
SLL	1	1	X	0	0	0	0	0	0	sll
SRL	1	1	X	0	0	0	0	0	0	srl
SRA	1	1	X	0	0	0	0	0	0	sra
ROL	1	1	X	0	0	0	0	0	0	rol
	1	1	X	0	0	0	0	0	0	
ADD	1	1	X	0	0	0	0	0	0	add
SUB	1	1	X	0	0	0	0	0	0	sub
SLT	1	1	X	0	0	0	0	0	0	sub
SLTU	1	1	X	0	0	0	0	0	0	sub
SLTE	1	1	X	0	0	0	0	0	0	sub

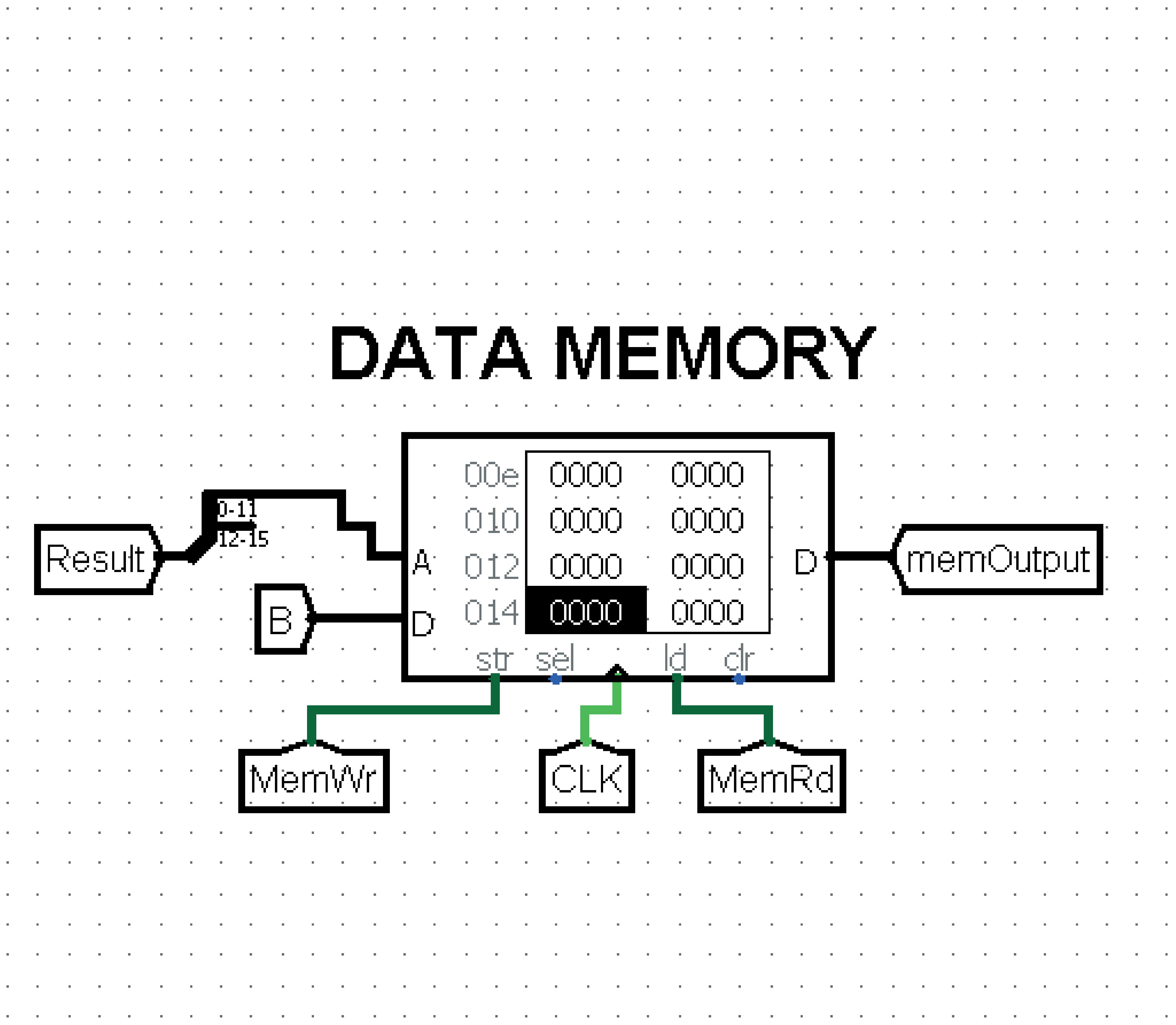
LOGIC UNIT FROM INSIDE :



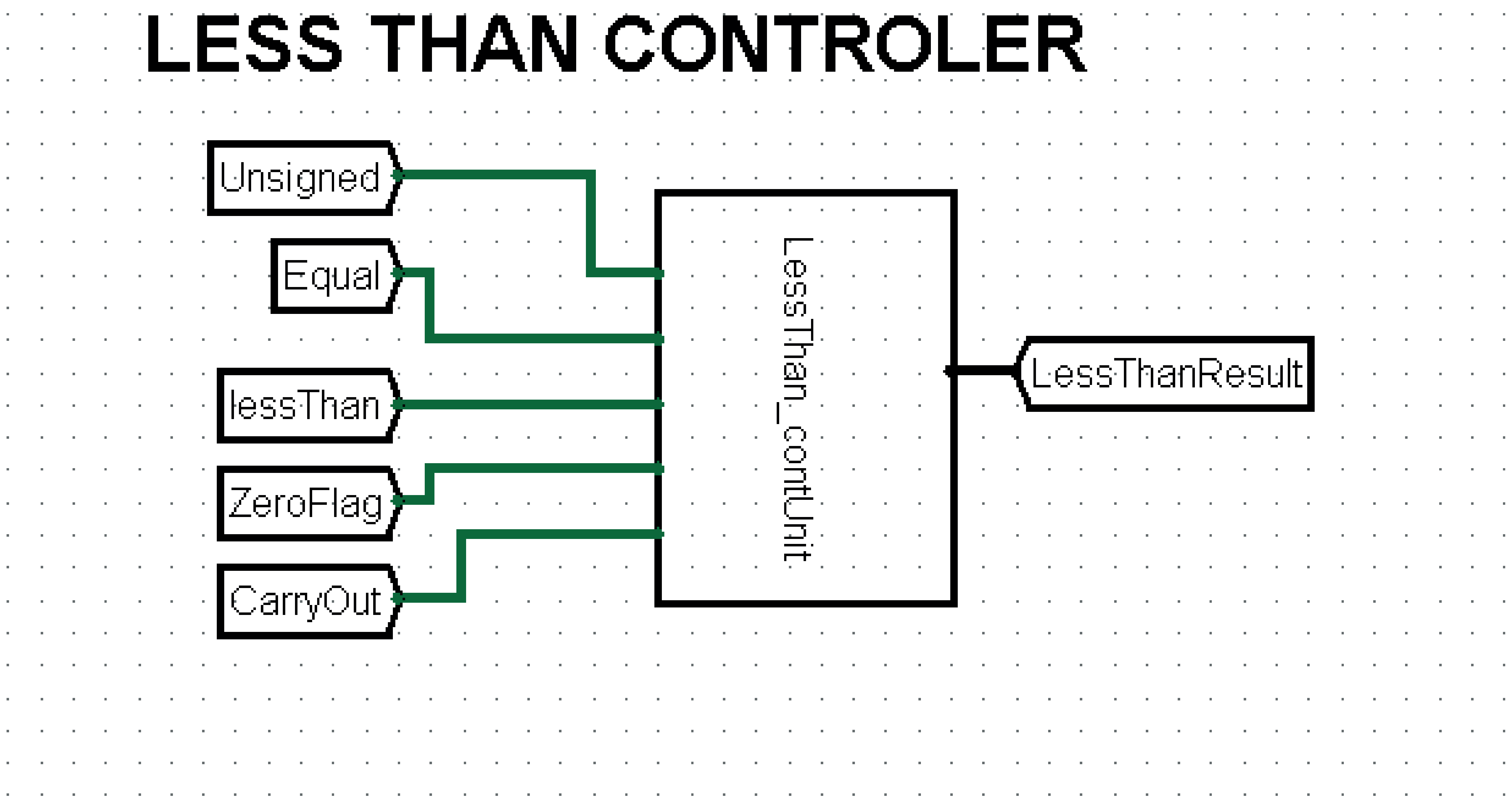
SHIFTINF UNIT FROM INSIDE :



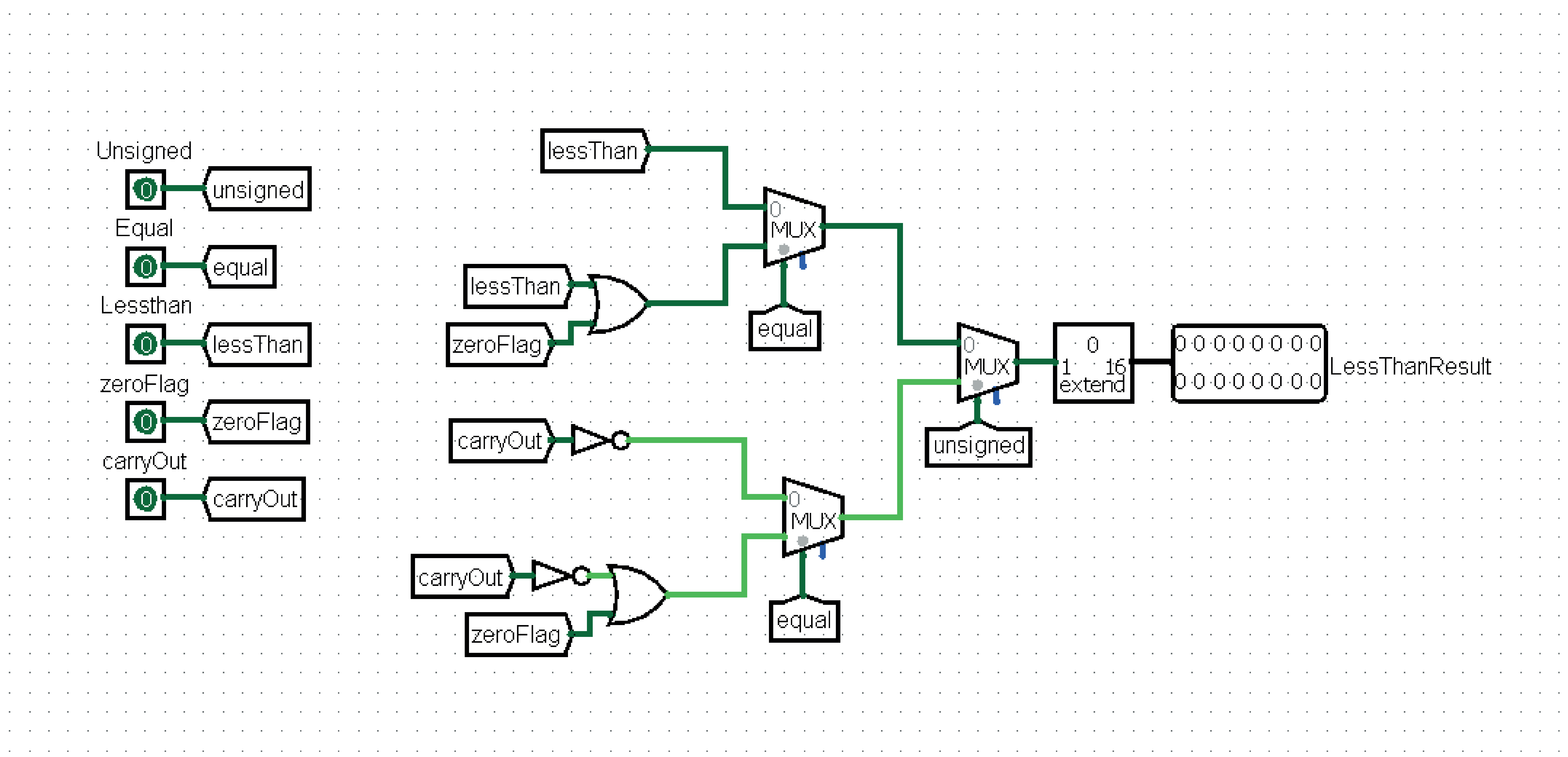
DATA MEMORY :


DATA MEMORY
Result
0-11
12-15
B
A
D
00e 0000 0000
010 0000 0000
012 0000 0000
014 0000 0000
D
memOutput
str
sel
ld
clr
MemWr
CLK
MemRd

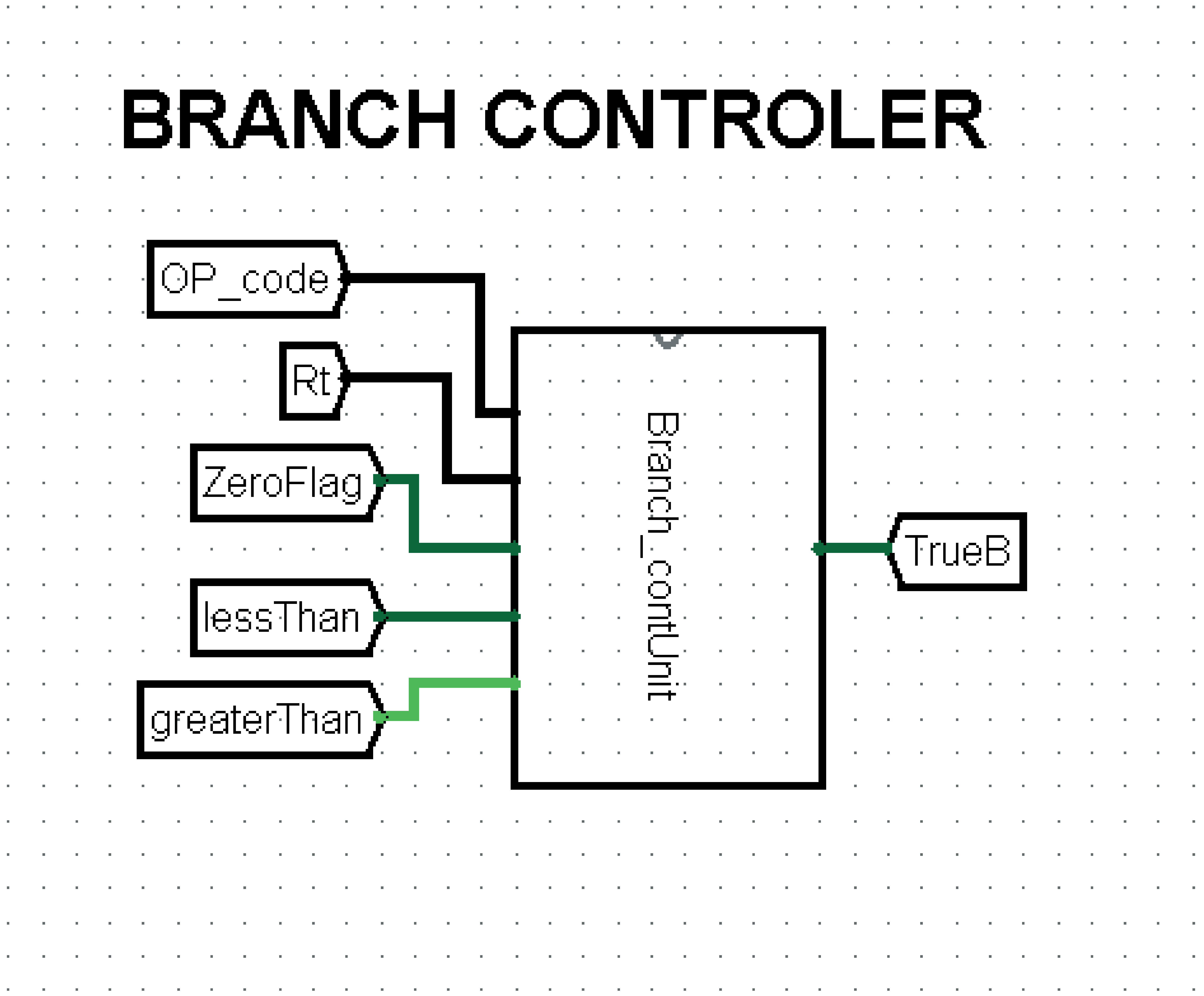
LESSTHAN CONTROLLER FROM OUTSIDE:



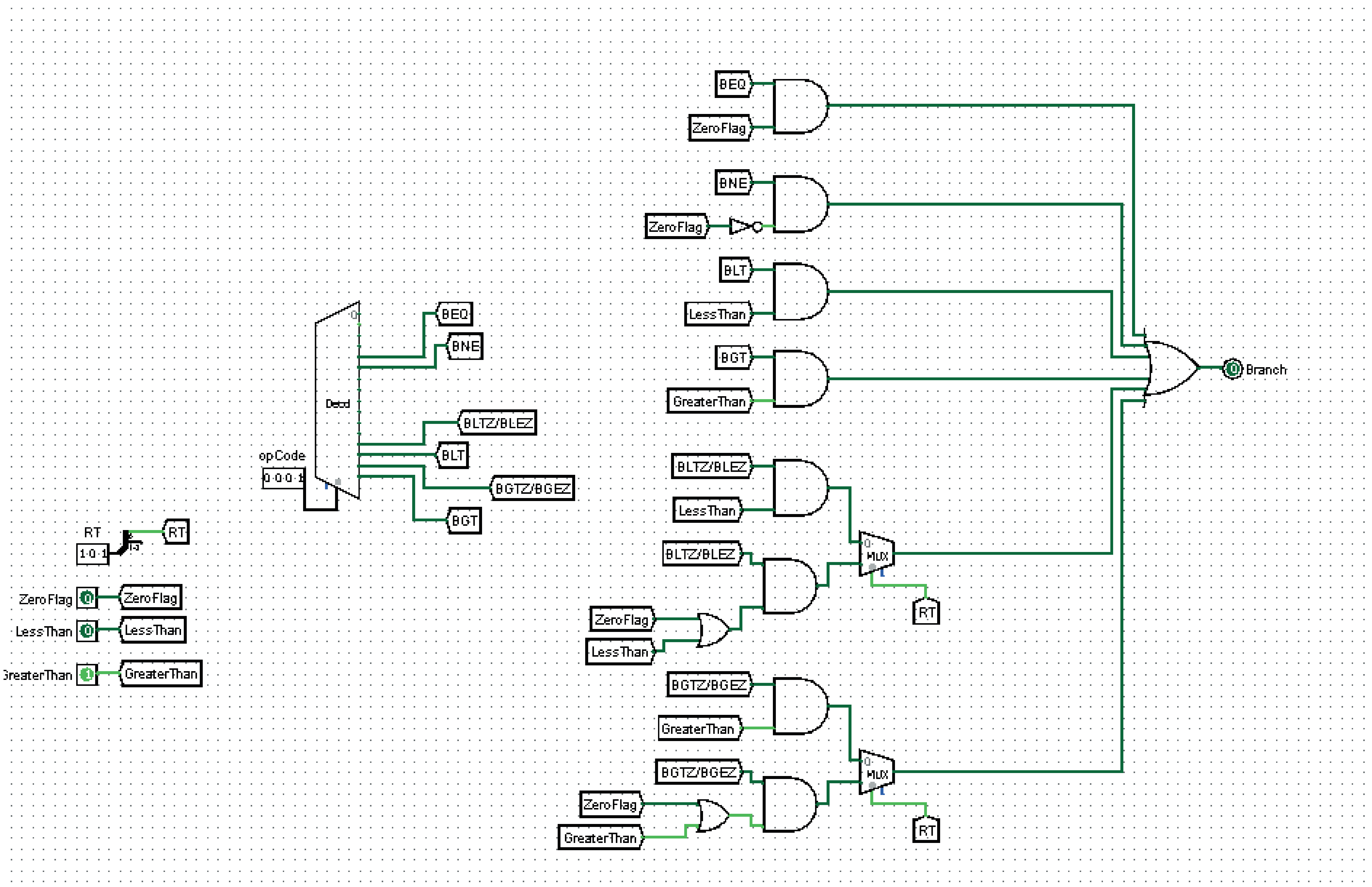
LESSTHAN CONTROLLER FROM INSIDE:



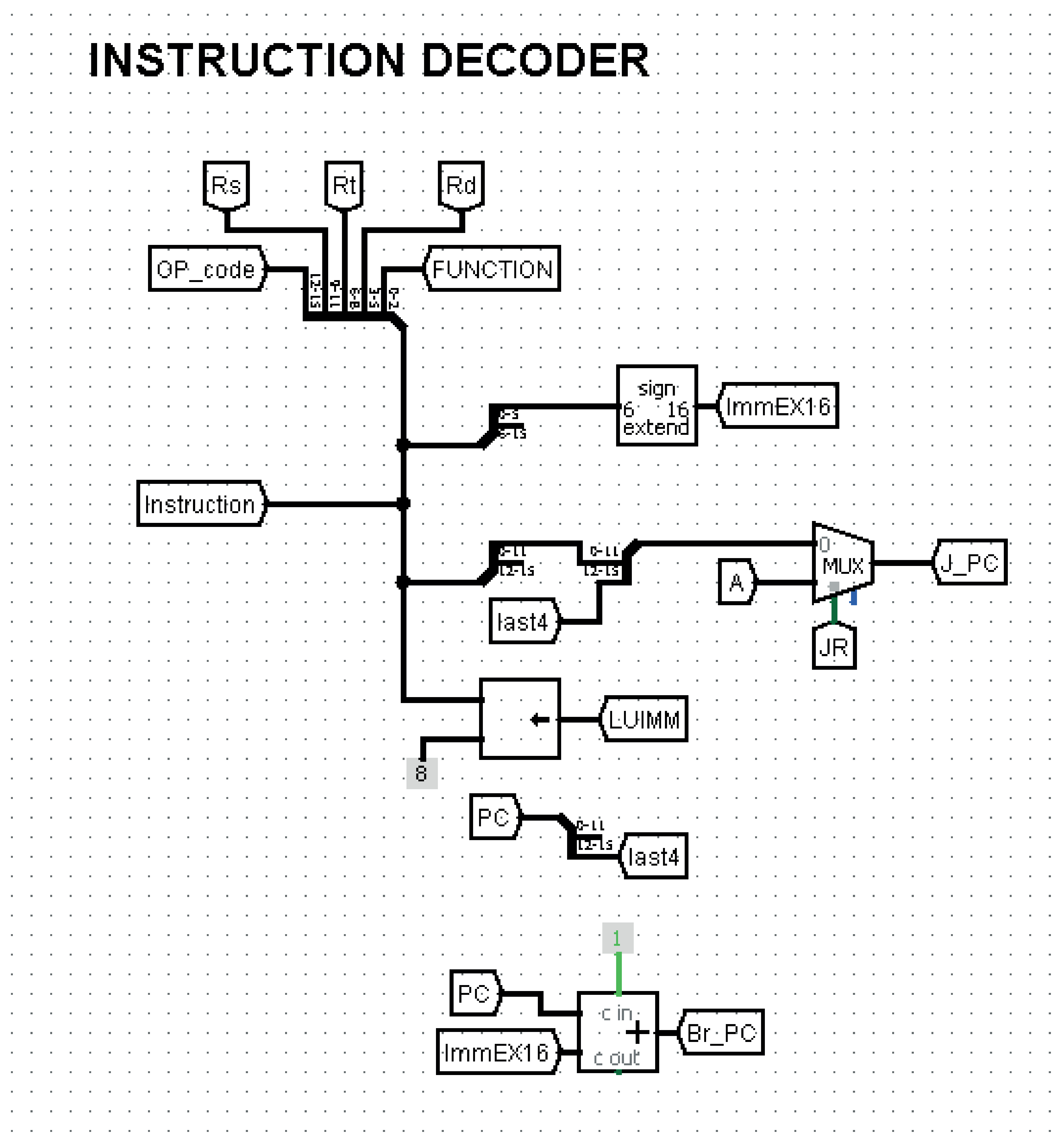
BRANCH CONTROLLER FROM OUTSIDE :



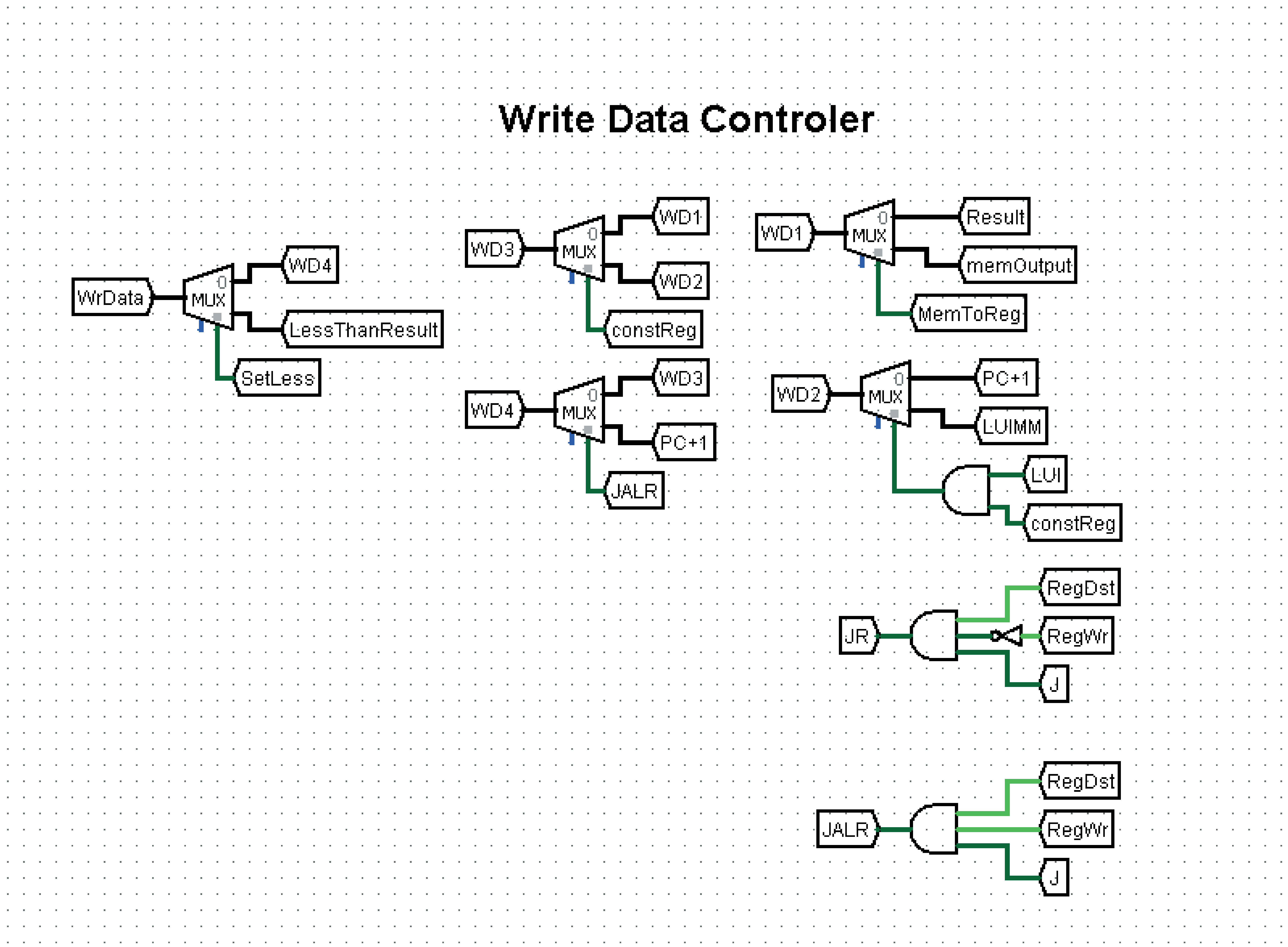
BRANCH CONTROLLER FROM INSIDE :



INSTRUCTION DECODER :



WRITE DATA CONTROLLER :



MAIN SIGNALS TABLE :

OP	RegDst	RegWr	ExtOp	AluSrc	MemRd	MemWr	MemToReg	Jmp	Branch	AluOp
AND	1	1	X	0	0	0	0	0	0	and
OR	1	1	X	0	0	0	0	0	0	or
NOR	1	1	X	0	0	0	0	0	0	nor
XOR	1	1	X	0	0	0	0	0	0	xor
SLL	1	1	X	0	0	0	0	0	0	sll
SRL	1	1	X	0	0	0	0	0	0	srl
SRA	1	1	X	0	0	0	0	0	0	sra
ROL	1	1	X	0	0	0	0	0	0	rol
	1	1	X	0	0	0	0	0	0	
ADD	1	1	X	0	0	0	0	0	0	add
SUB	1	1	X	0	0	0	0	0	0	sub
SLT	1	1	X	0	0	0	0	0	0	sub
SLTU	1	1	X	0	0	0	0	0	0	sub
SLTE	1	1	X	0	0	0	0	0	0	sub
SLTEU	1	1	X	0	0	0	0	0	0	sub
JR	X	0	X	X	0	0	0	1	0	X
JALR	1	1	X	X	0	0	0	1	0	X
I TYPE:										
OP	RegDst	RegWr	ExtOp	AluSrc	MemRd	MemWr	MemToReg	Jmp	Branch	AluOp
LW	0	1	1	1	1	0	1	X	X	add
SW	X	0	1	1	0	1	0	X	X	add
ANDI	0	1	0	1	0	0	0			and
ORI	0	1	0	1	0	0	0			or
ADDI	0	1	1	1	0	0	0	X	X	add
BEQ	X	0	1	0	0	0	0	0	1	sub
BNE	X	0	1	0	0	0	0	0	1	sub
BLT	X	0	1	0	0	0	0	0	1	sub
BGT	X	0	1	0	0	0	0	0	1	sub
BLTZ	X	0	1	0	0	0	0	0	1	sub
BLEZ	X	0	1	0	0	0	0	0	1	sub
BGTZ	X	0	1	0	0	0	0	0	1	sub
BGEZ	X	0	1	0	0	0	0	0	1	sub
J TYPE:										
OP	RegDst	RegWr	ExtOp	AluSrc	MemRd	MemWr	MemToReg	Jmp	Branch	AluOp
J	X	0	X	X	0	0	0	1	0	X
JAL	X	1	X	X	0	0	0	1	0	
							0			
LUI	X	1	X	X	0	0	0	X	X	X

16 BIT PIPELINE PROCESSOR

PHASE : 2

TEAM: Abdlerahaman Essam - Khalid Sayed - Ali Raid - Abdlerahman Mahmoud

MAJOR: Computer Engineering

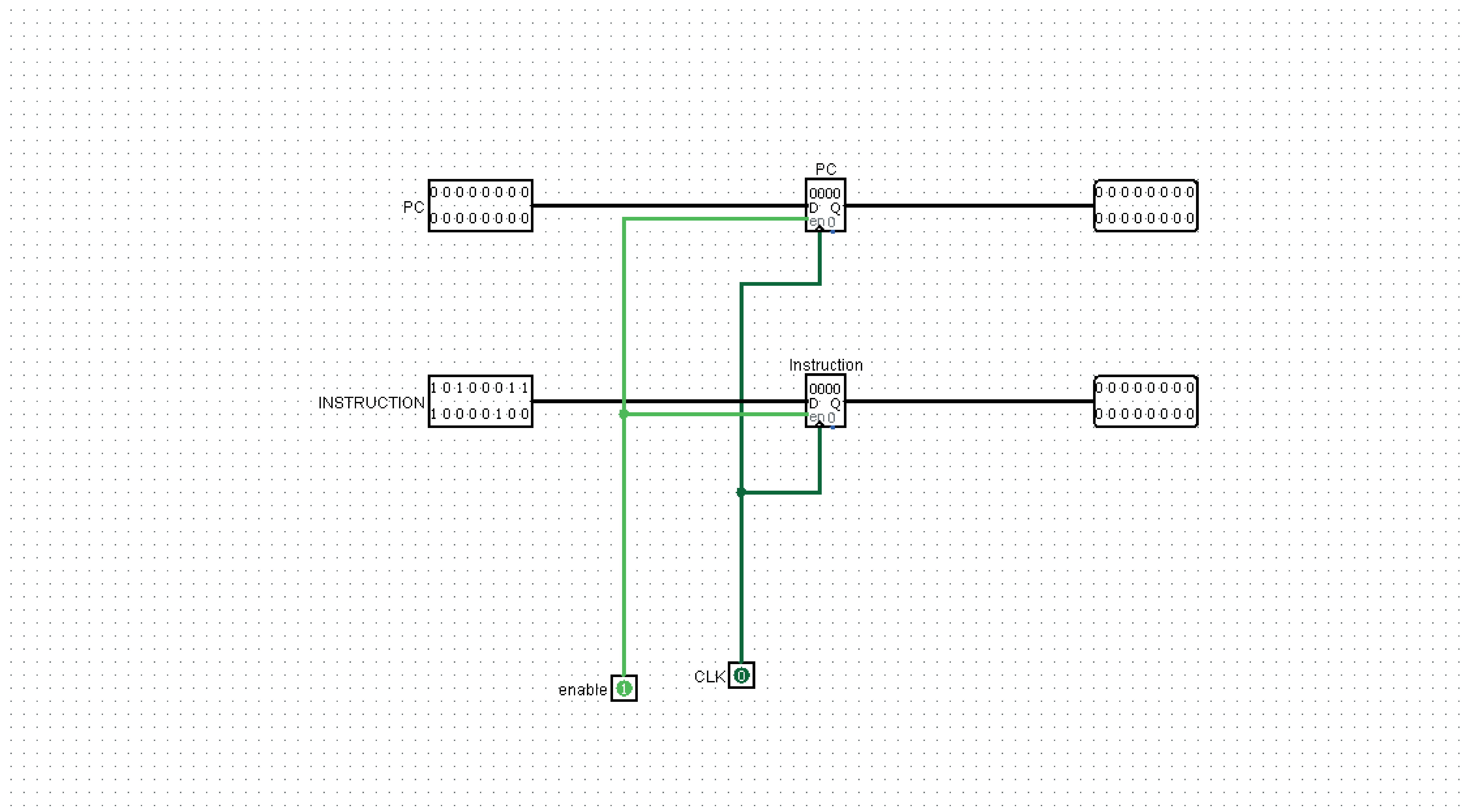
OVERALL DATAPATH :

consists of :

-five stages (IF/ID, ID/EX, EX/MEM, MEM/WB)

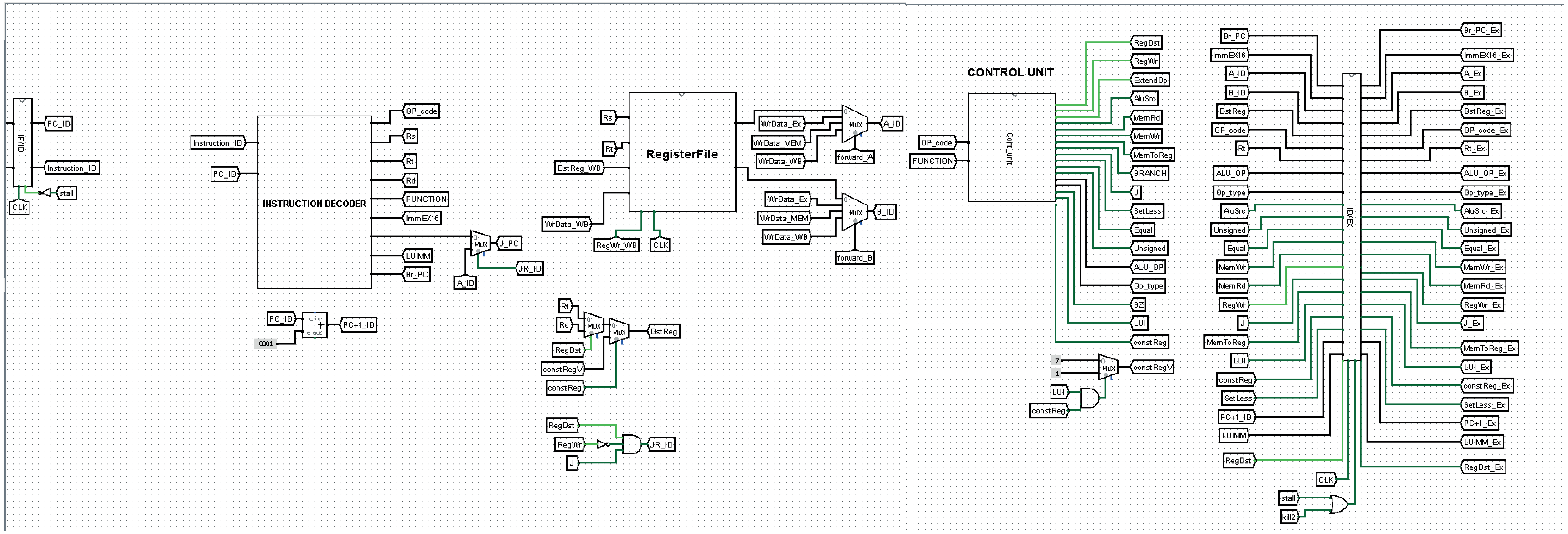
overall datapath can’t be included as the databath is so wide, so we will include each stage indivdually

IF / ID REGISTER FROM INSIDE :



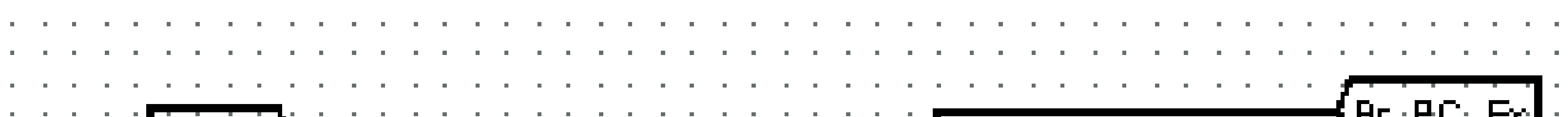
ID / IF STAGE :

1- Decodes the instruction, decide its operands and read register file.
2- Produces the control signals and inject the dependecies that the next stages will need, to execute the current instruction proberly.



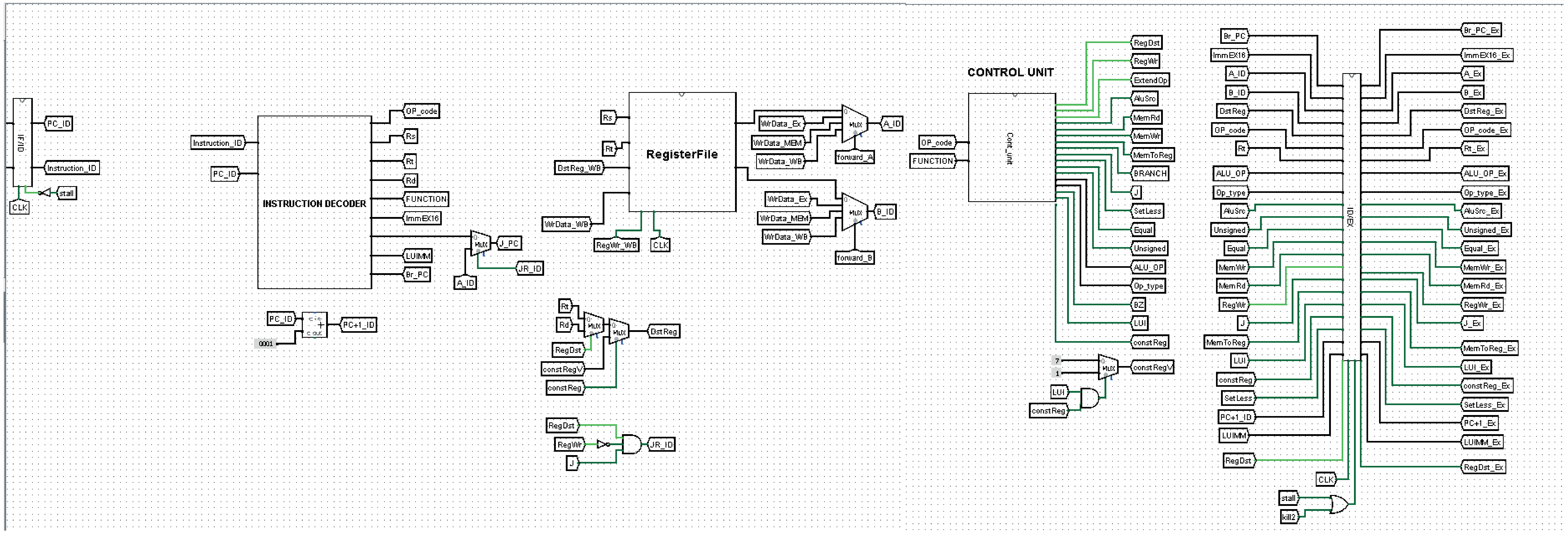
STALL IMPLEMENTATION:

1- converting all control signals



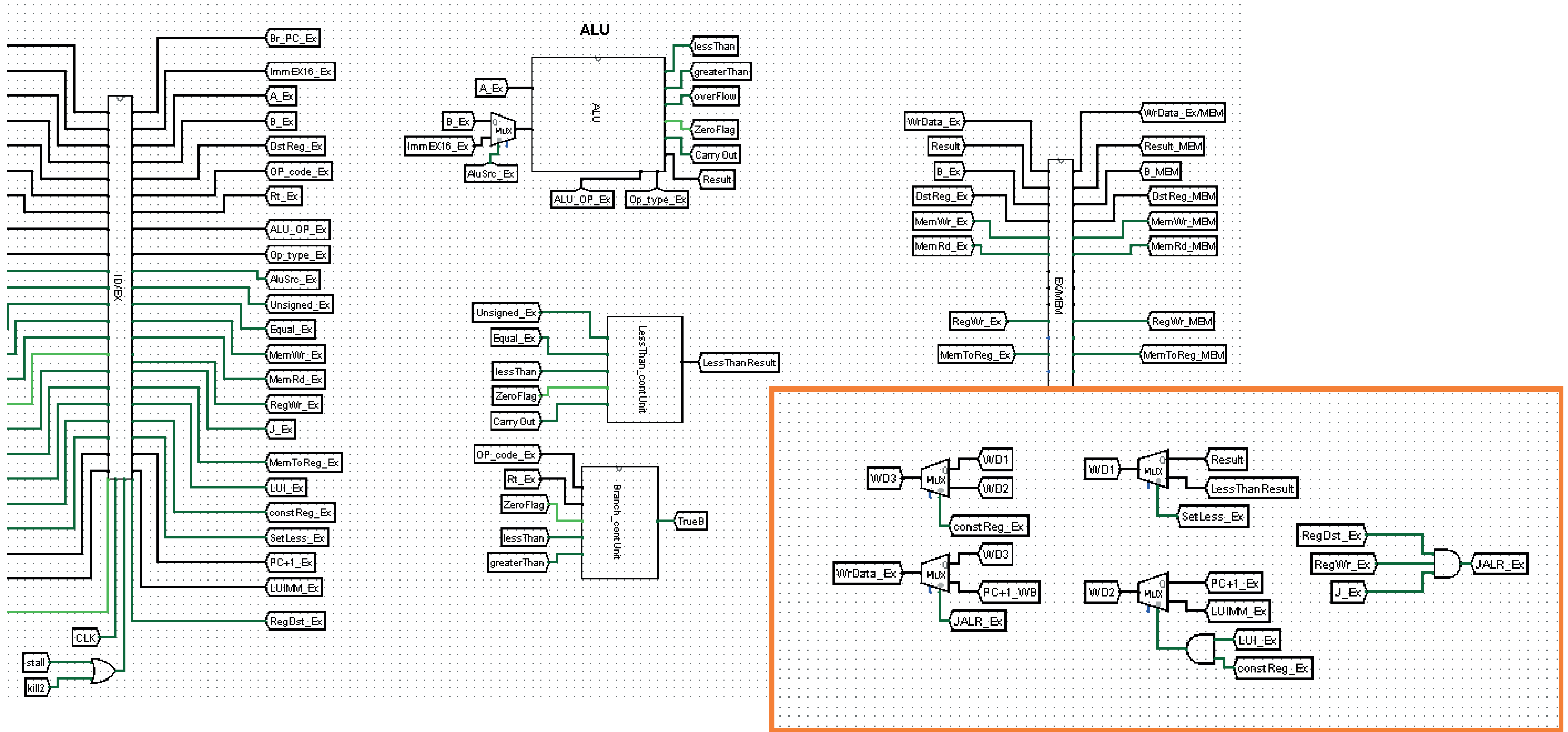
ID / EX STAGE :

1- Decodes the instruction, decide its operands and read register file.
2- Produces the control signals and inject the dependecies that the next stages will need, to execute the current instruction proberly.



EX / MEM STAGE :

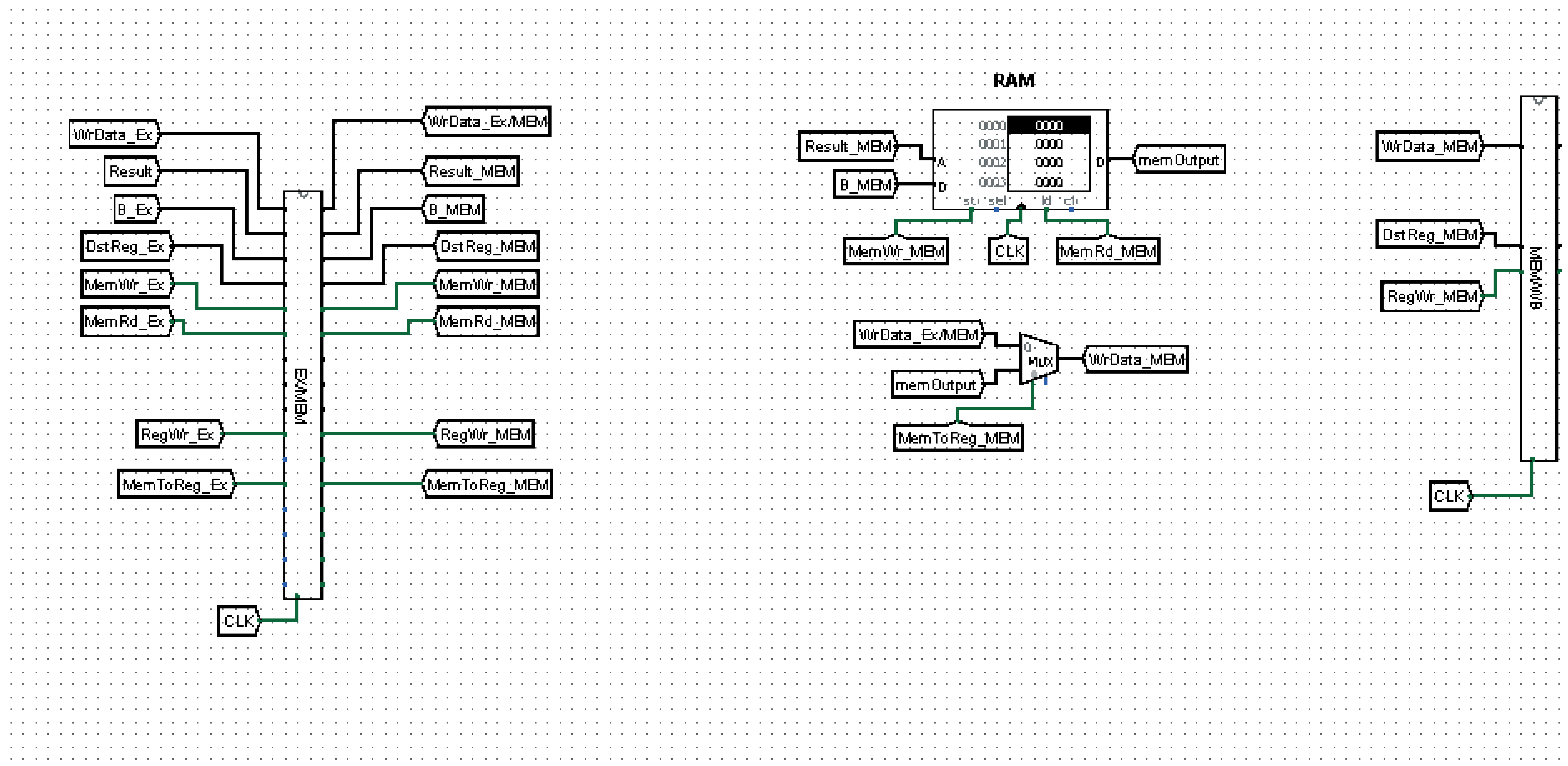
1- Executes the instruction and produce result using ALU.
2- Handles comparison instructions using LessThan_controlUnit.
3- Handles barnching instructions using Branch_controlUnit.
3- Handles result to be transefered as the outcome of the execution stage using writeData_EX decide portion.



writeData_EX decide portion

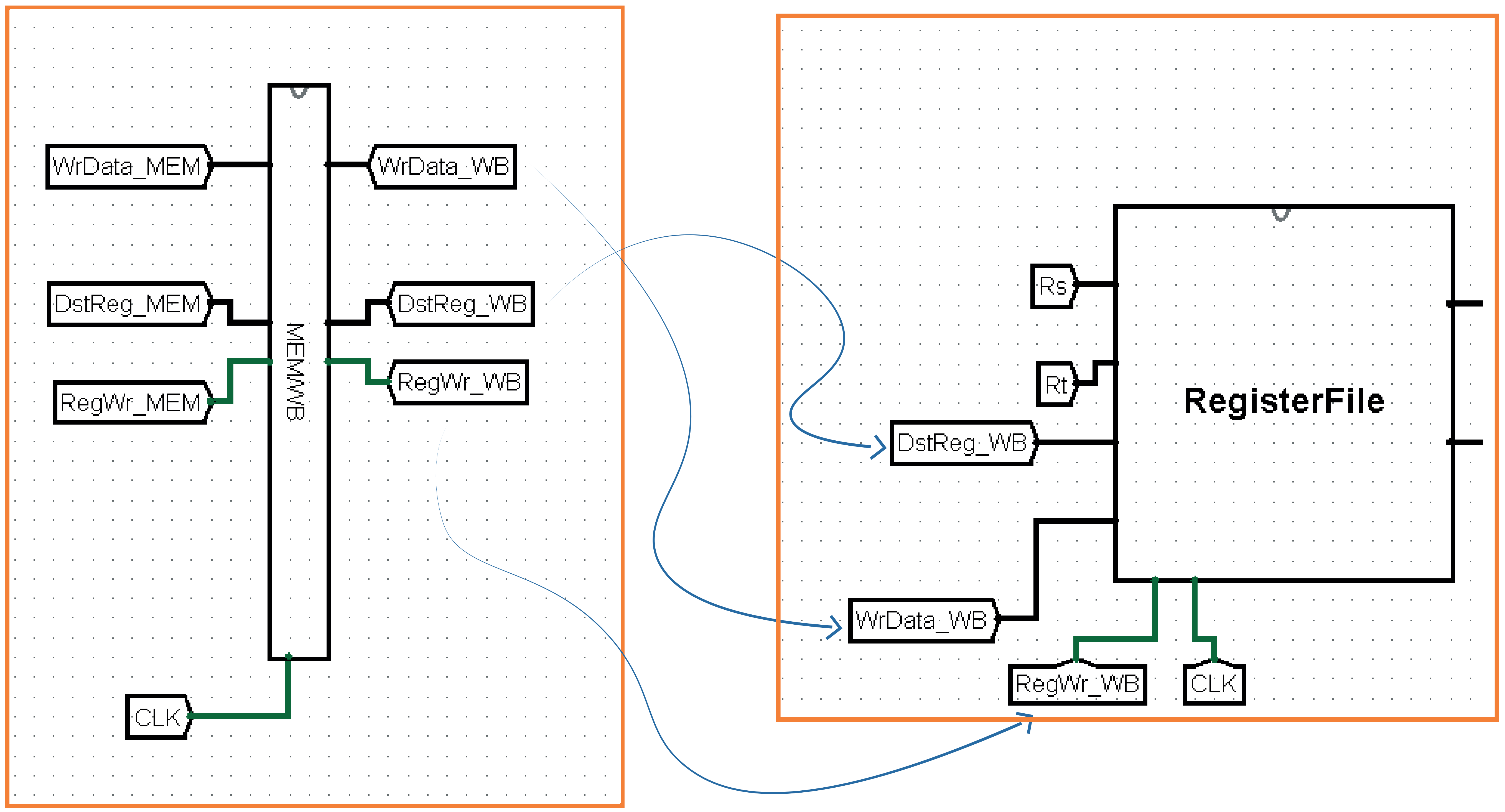
MEM/ WB STAGE :

1- Handles data memory accessing instructions (SW,LW).
2- transfers final data to writeBack stage.



WB STAGE :

1- Handles writing data back to registers.

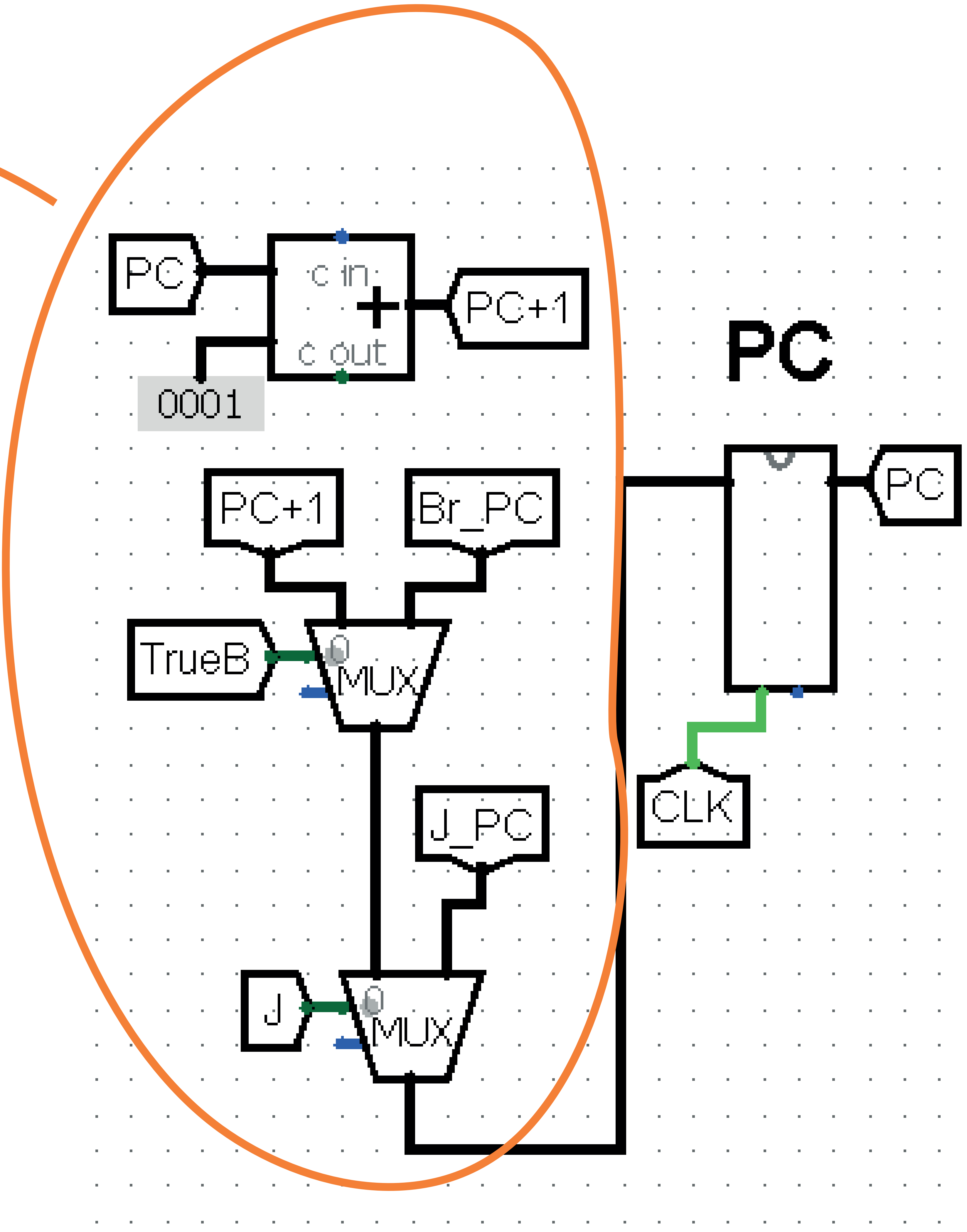


PC PART FROM OUTSIDE :

- there are MUXs before the PC input to decide which new instruction should be executed (JUMP address, BRANCH address, PC + 1)

L

to decide which new instruction should be executed

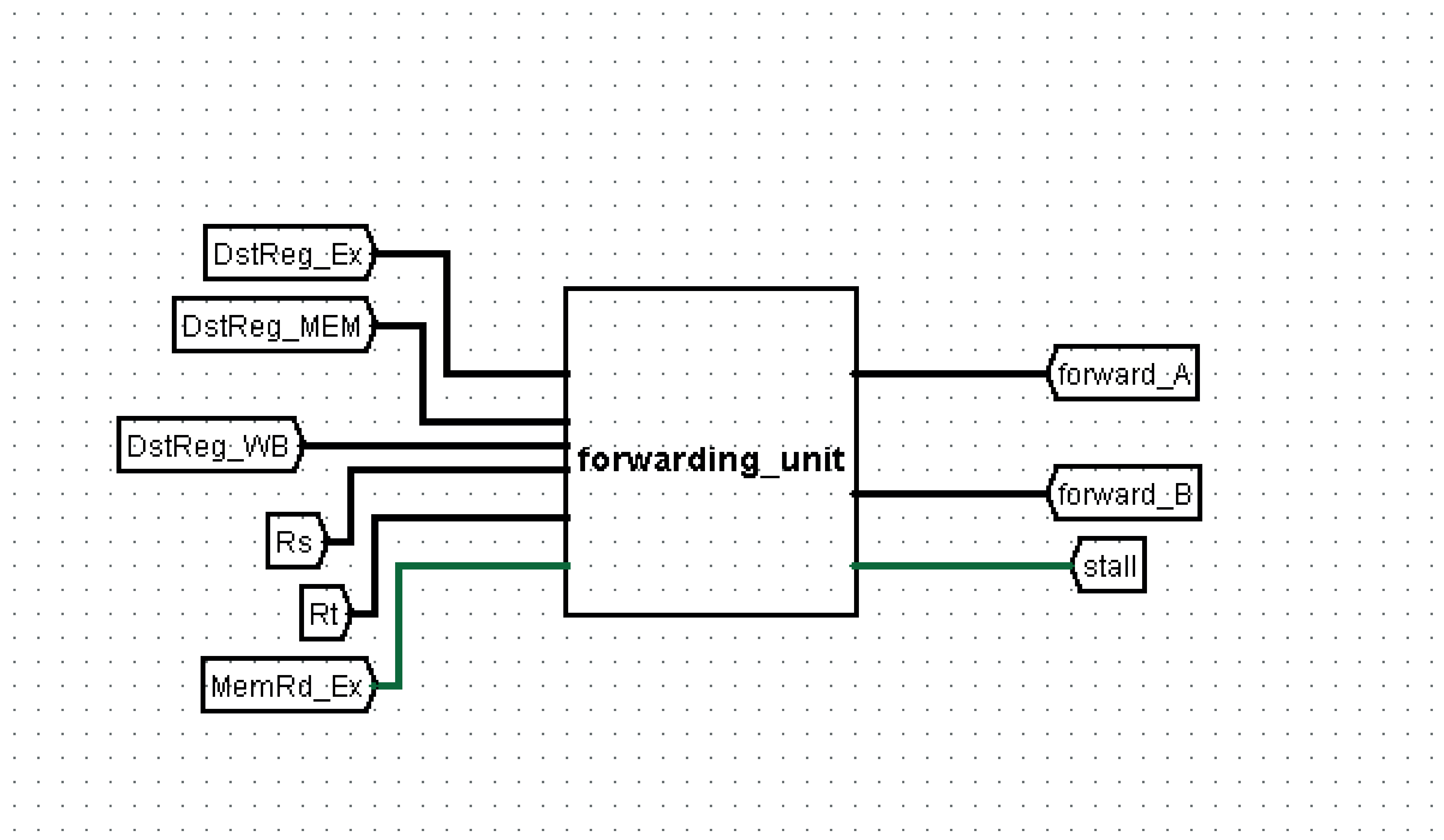


HAZARDS

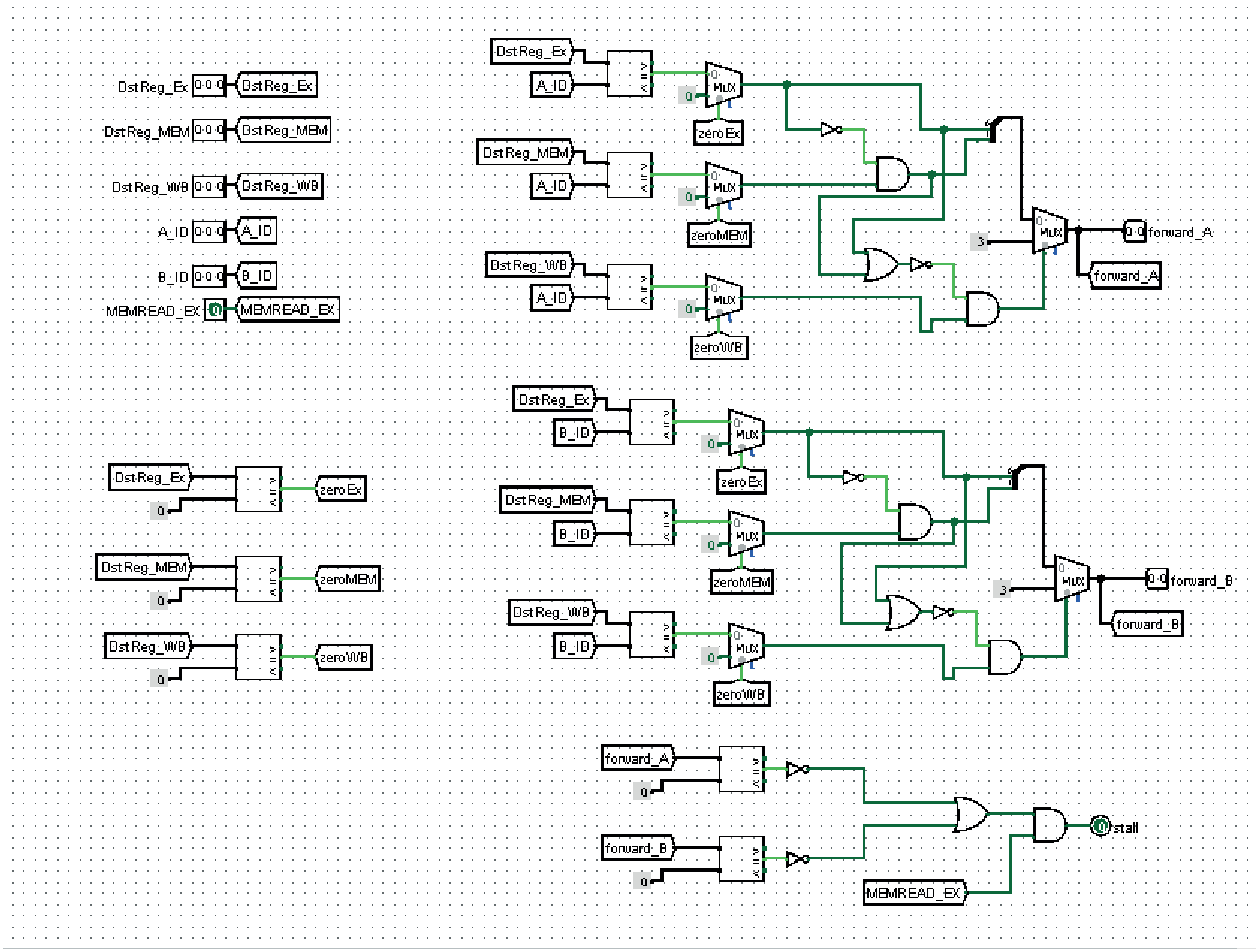
1 - Data Dependence Read-after-Write (RAW):

SOLUTION : Data forwarding.

- we made forwarding unit to forward wnated data in ID stage from (EX,MEM,WB) stages



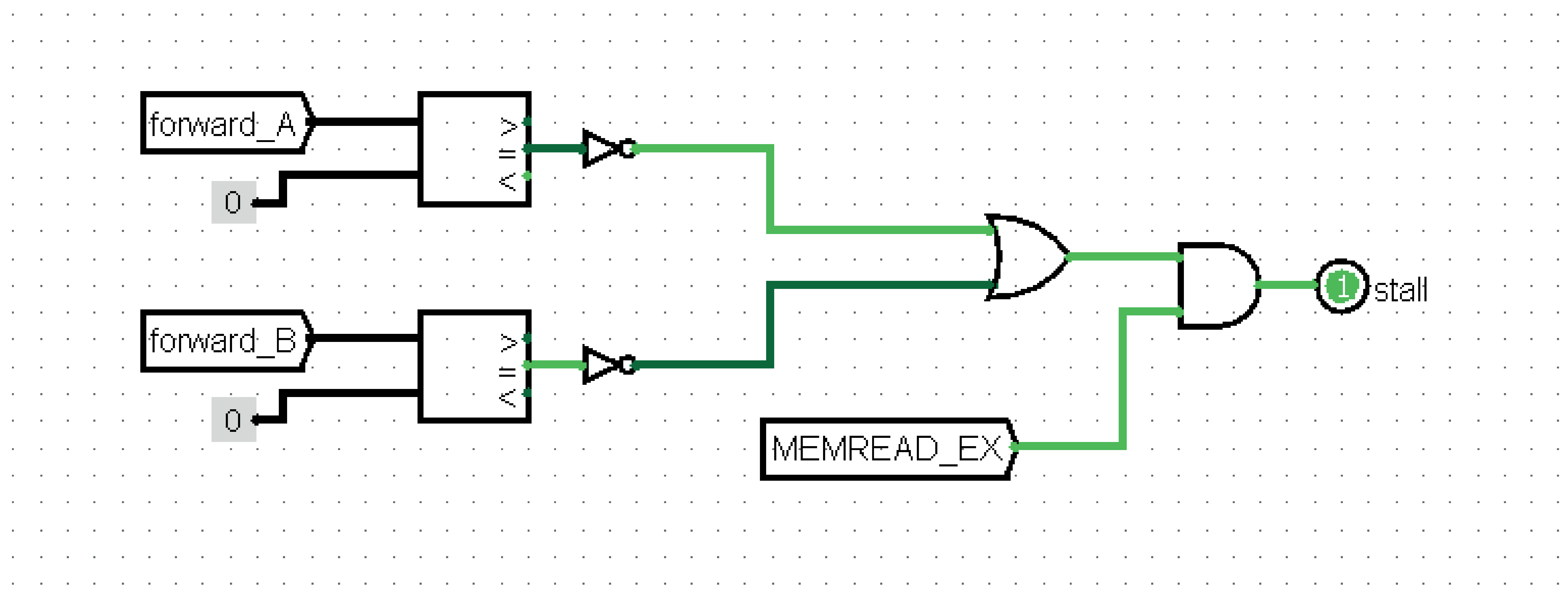
FORWARDING UNIT FROM INSIDE:



2 - RAW Hazard after Load:

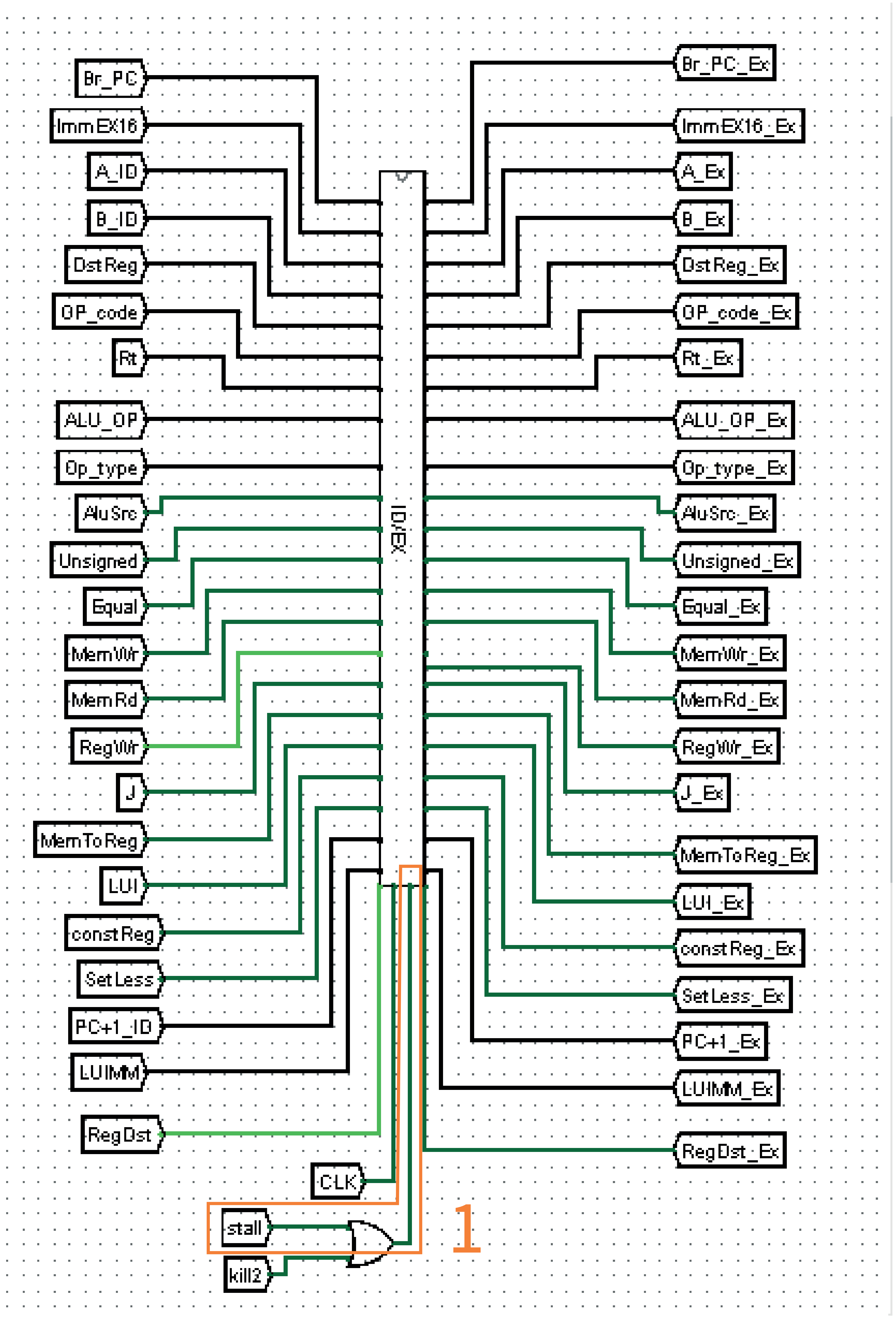
SOLUTION : Stall the Pipeline for one Cycle.

- we made detcting unit inside the forwarding unit to produce a stall flag.



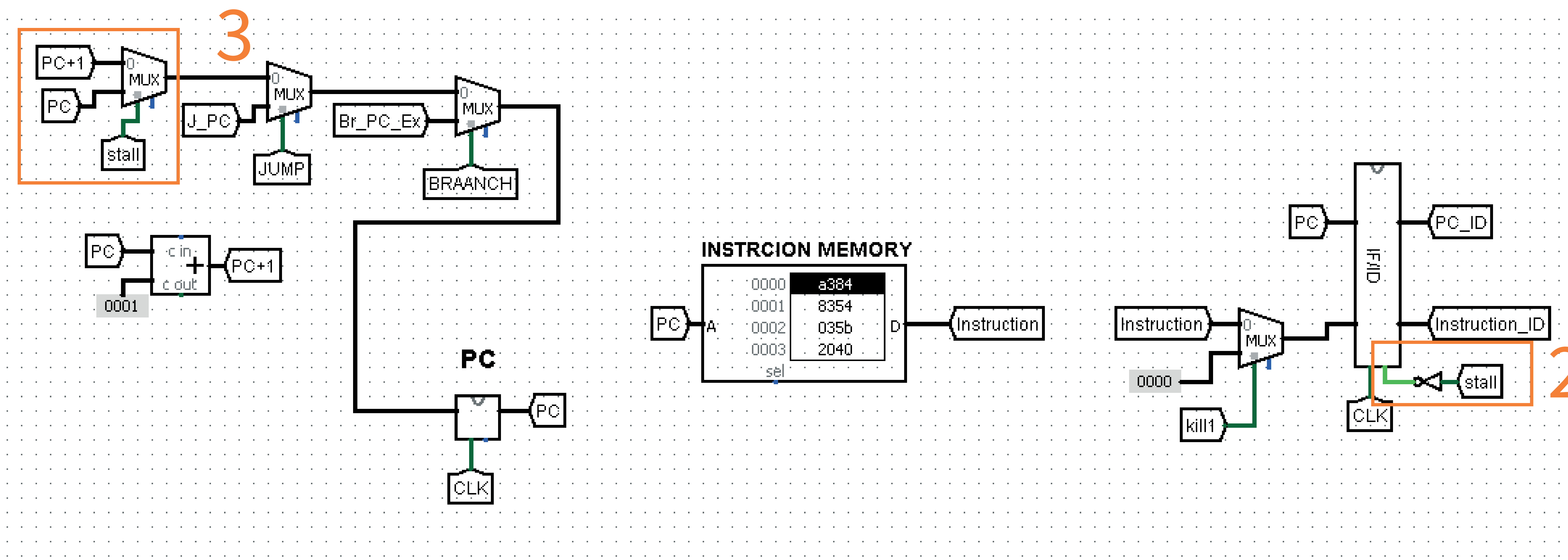
STALL IMPLEMENTATION:

1- converting all control signals and data in ID/EX stage to zeros.



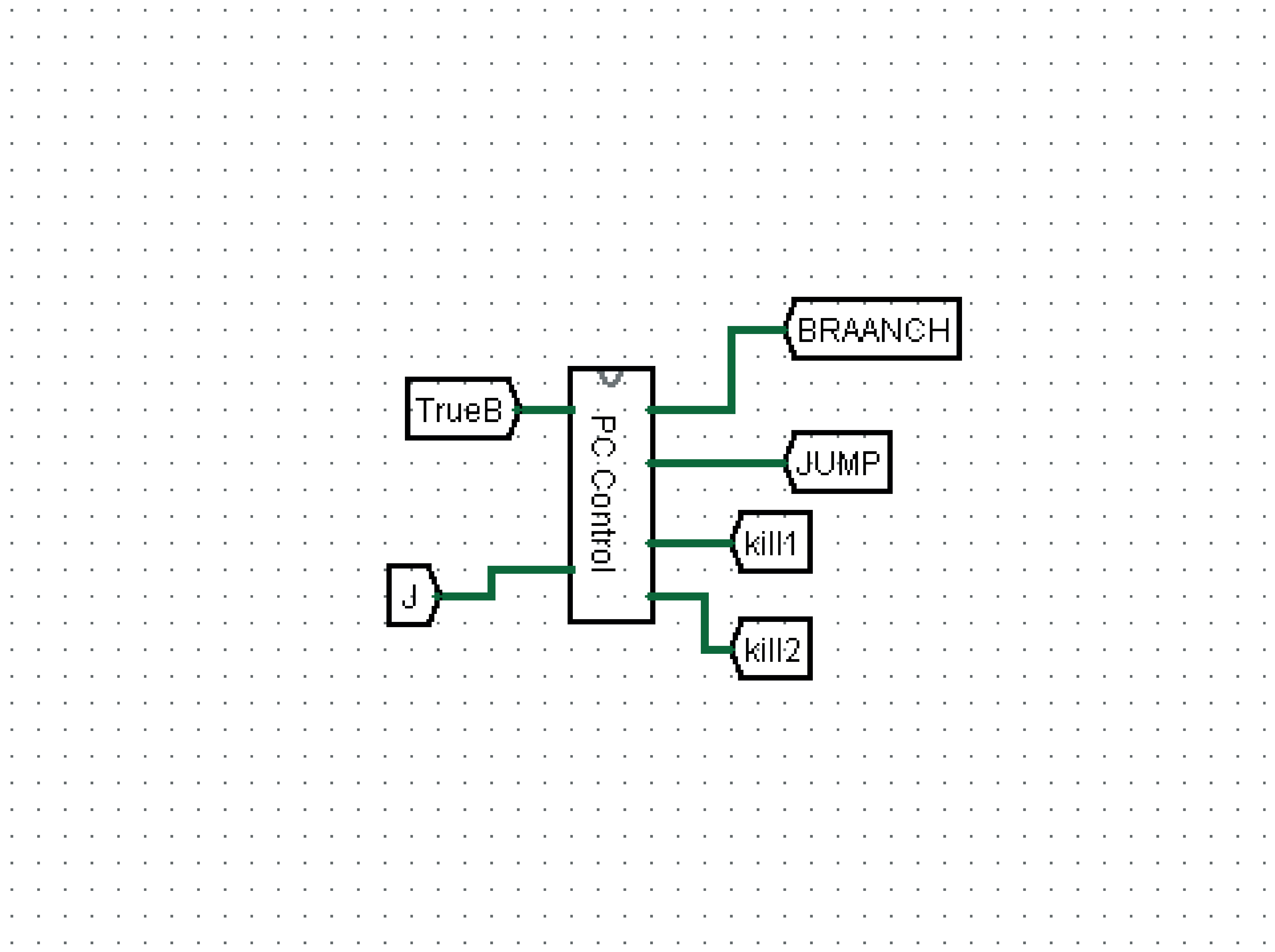
STALL IMPLEMENTATION:

2- Disabling writing to IF/ID register to redecode the instruction tha is converted into noop instruction again.
3- stop increasing the pc to make make delay by one cycle not passing an instruction.

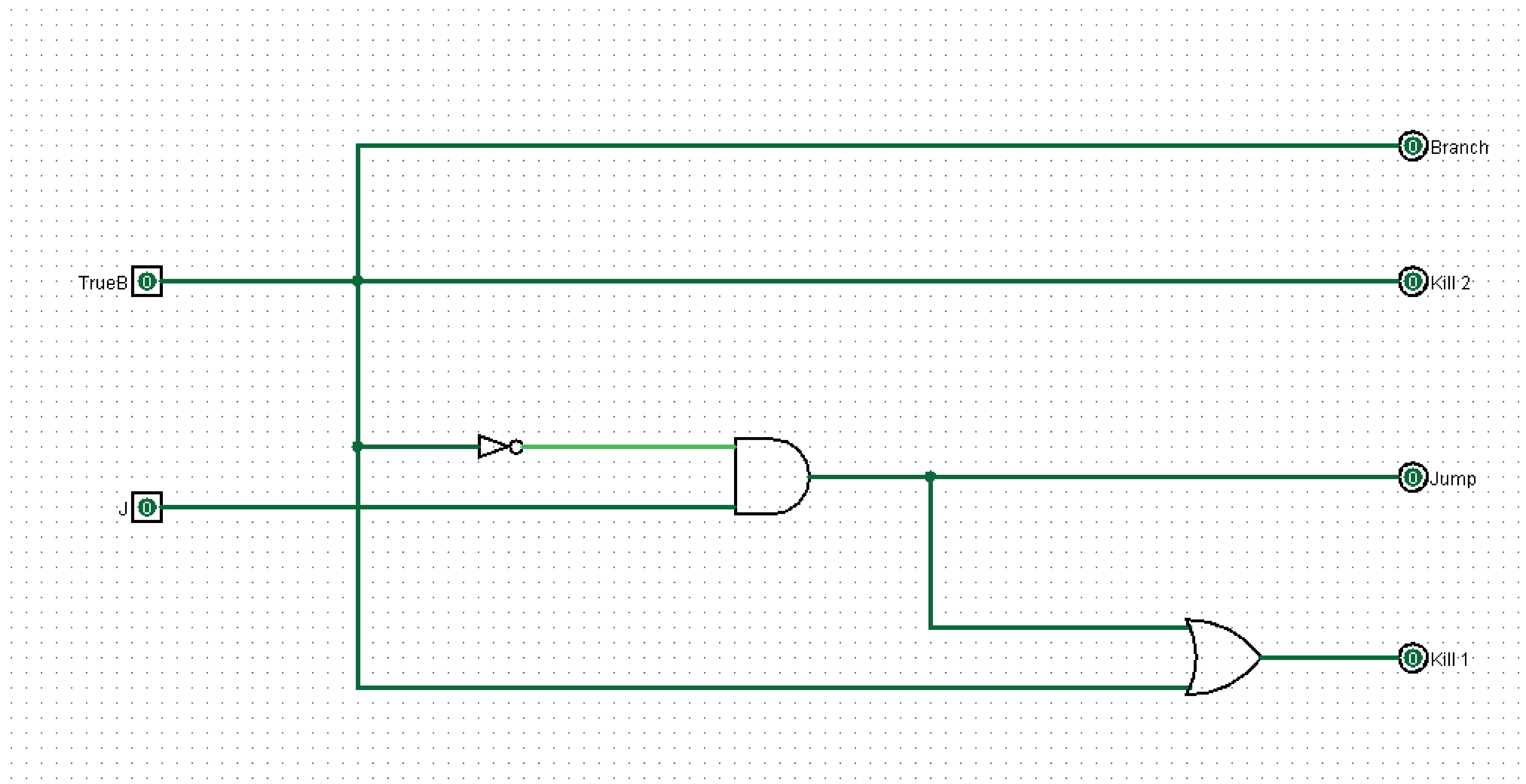


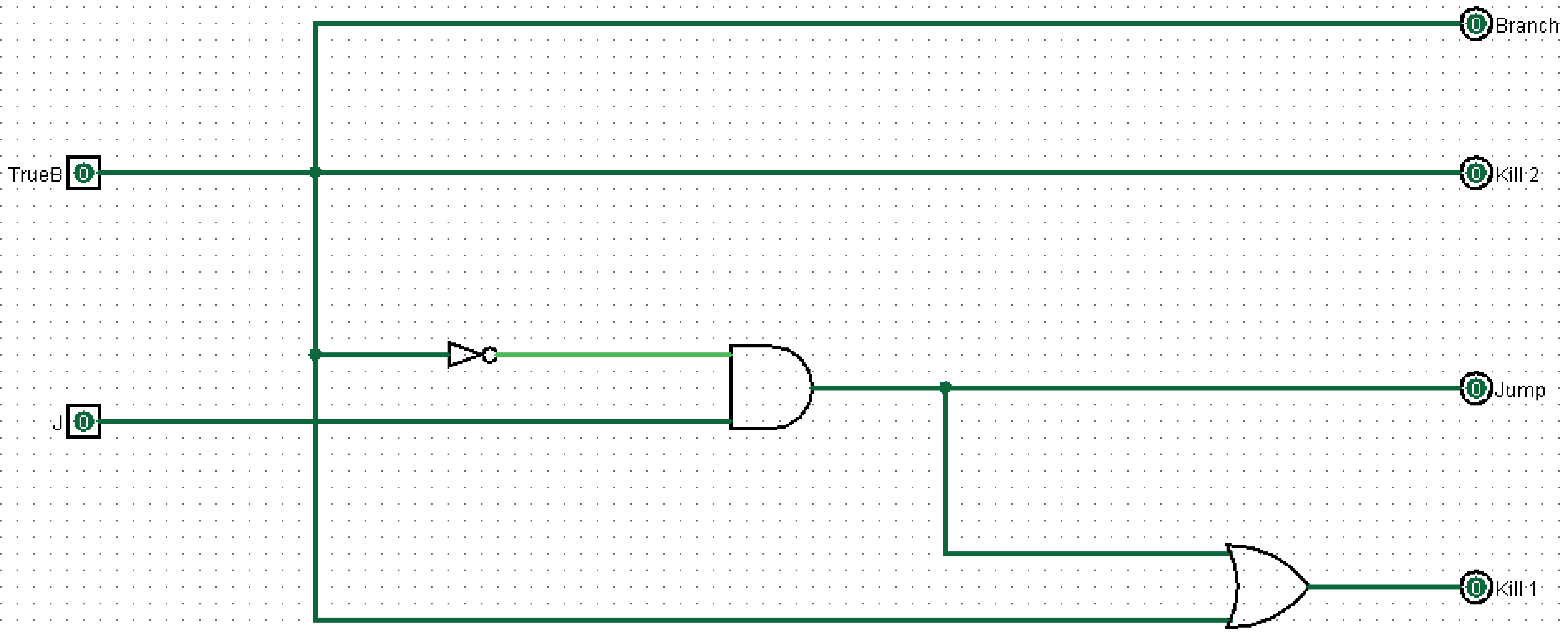
3- Control Hazards:

SOLUTION : one Cycle Delay for Jump , tow Cycle delay for branch.



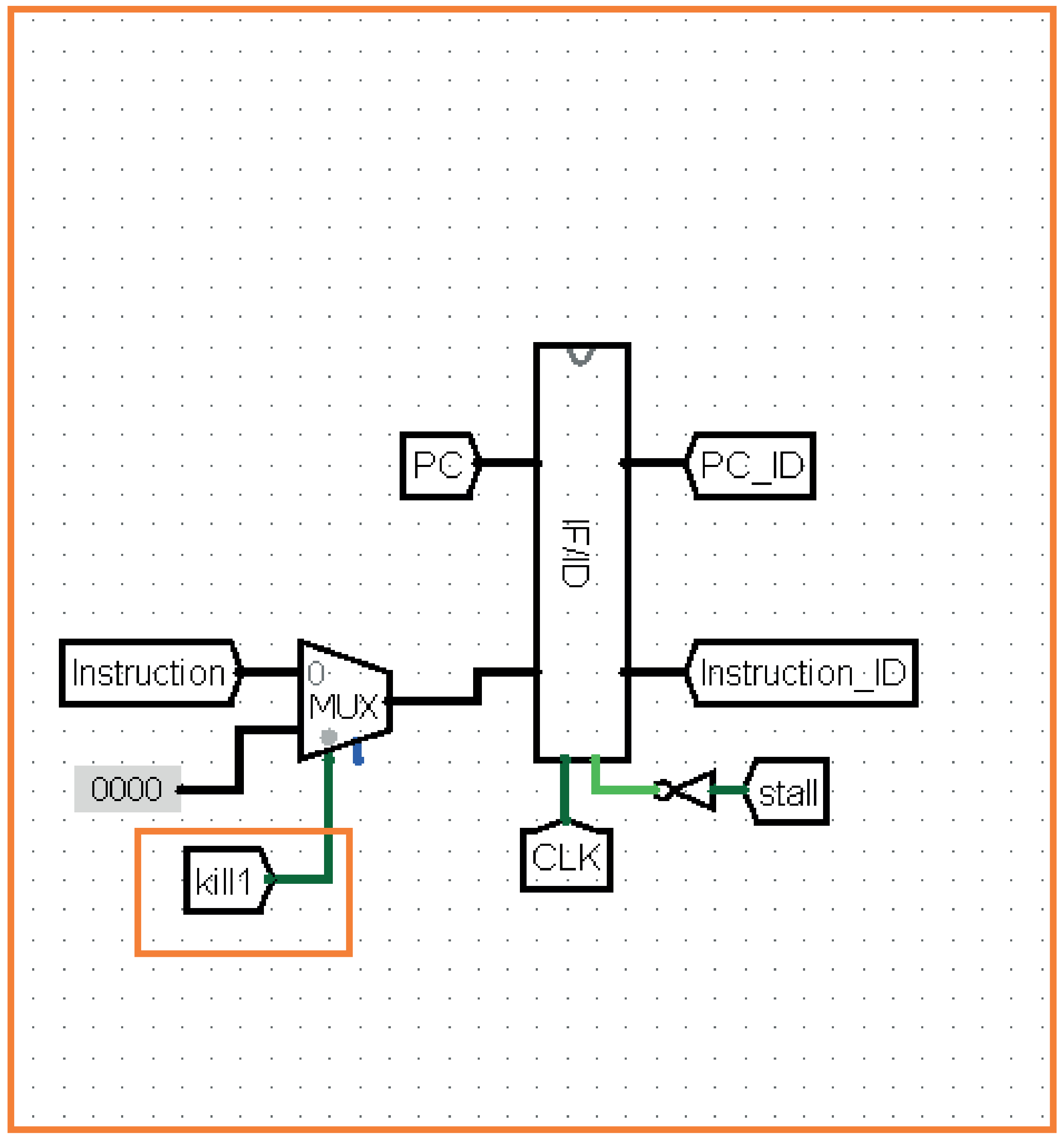
PC Control From Inside:

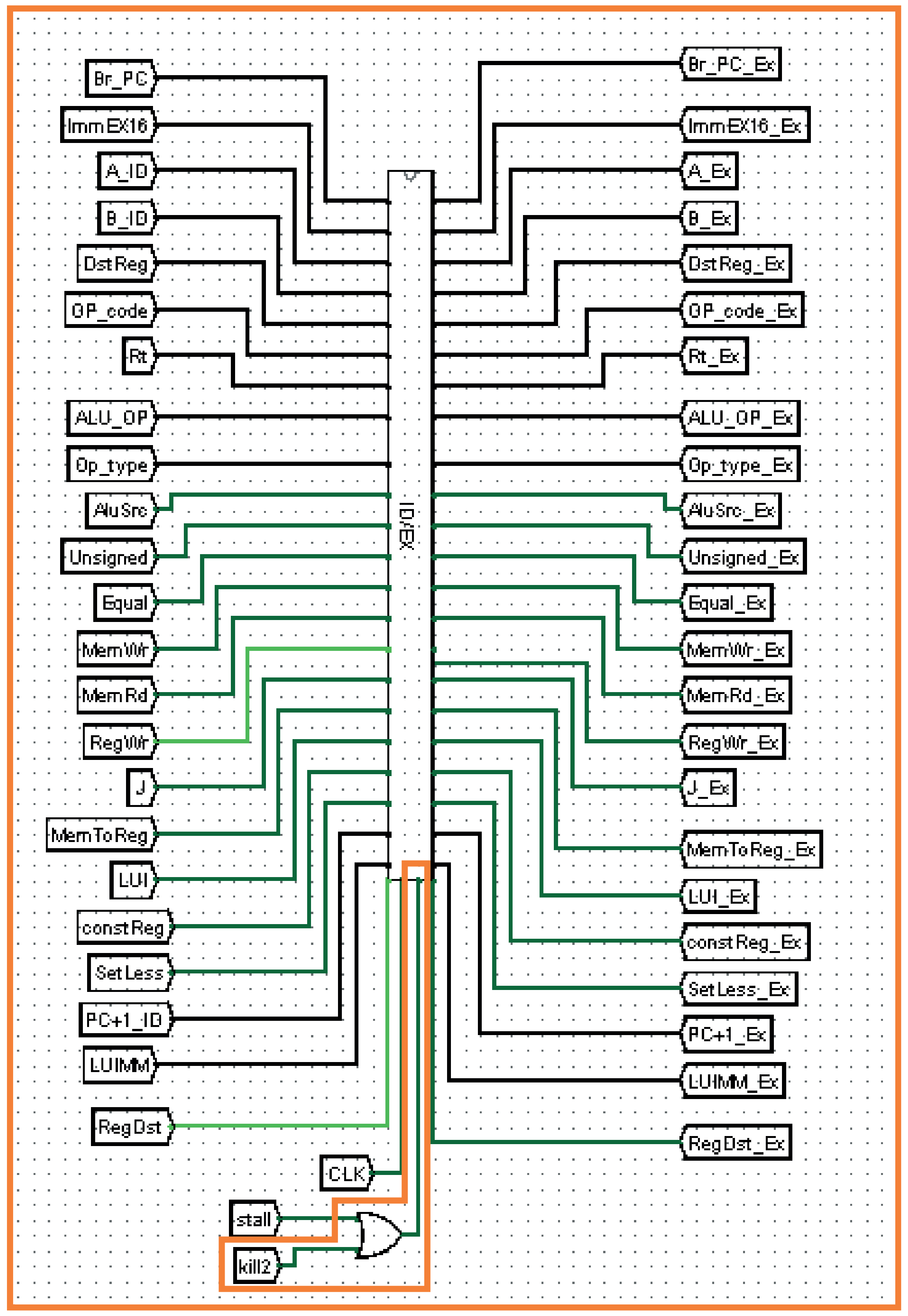



TrueB
0
J
0
0
Branch
0
Kill 2
0
Jump
0
Kill 1

Kill1 & Kill2 to flush unwanted instructions:

1- kill1 flushes Instruction in IF/ID.
2- kill2 flushes Instrucion in ID/EX.





FINALLY

THANKS FOR YOUR EFFORT
DR/ JEHAN & ENG/ GEHAD