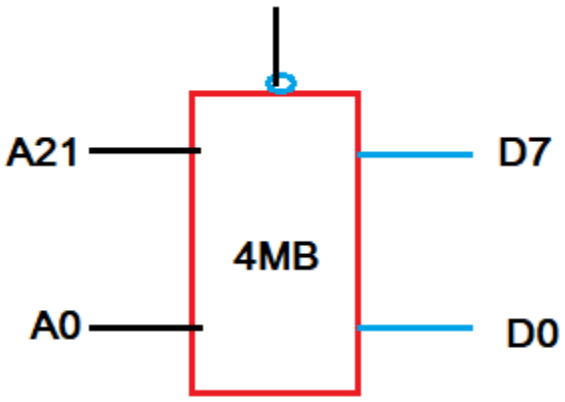
Sample questions: Lectures 5 & 6

Design a memory module of capacity 64M x 64 bits by using 4MB ICs.

4MB IC:
Number of addressable locations: 4M = 4 x 1024 x 1024 = $2^2 \times 2^{10} \times 2^{10} = 2^{22}$
Number of address lines/pins = 22
Content of each addressable location = 8 bits
Number of data lines/pins = 8

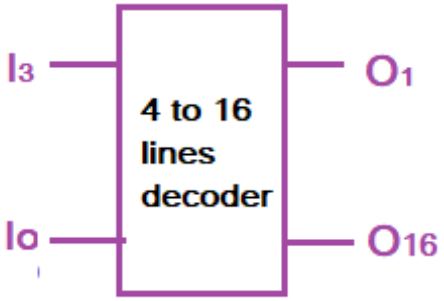


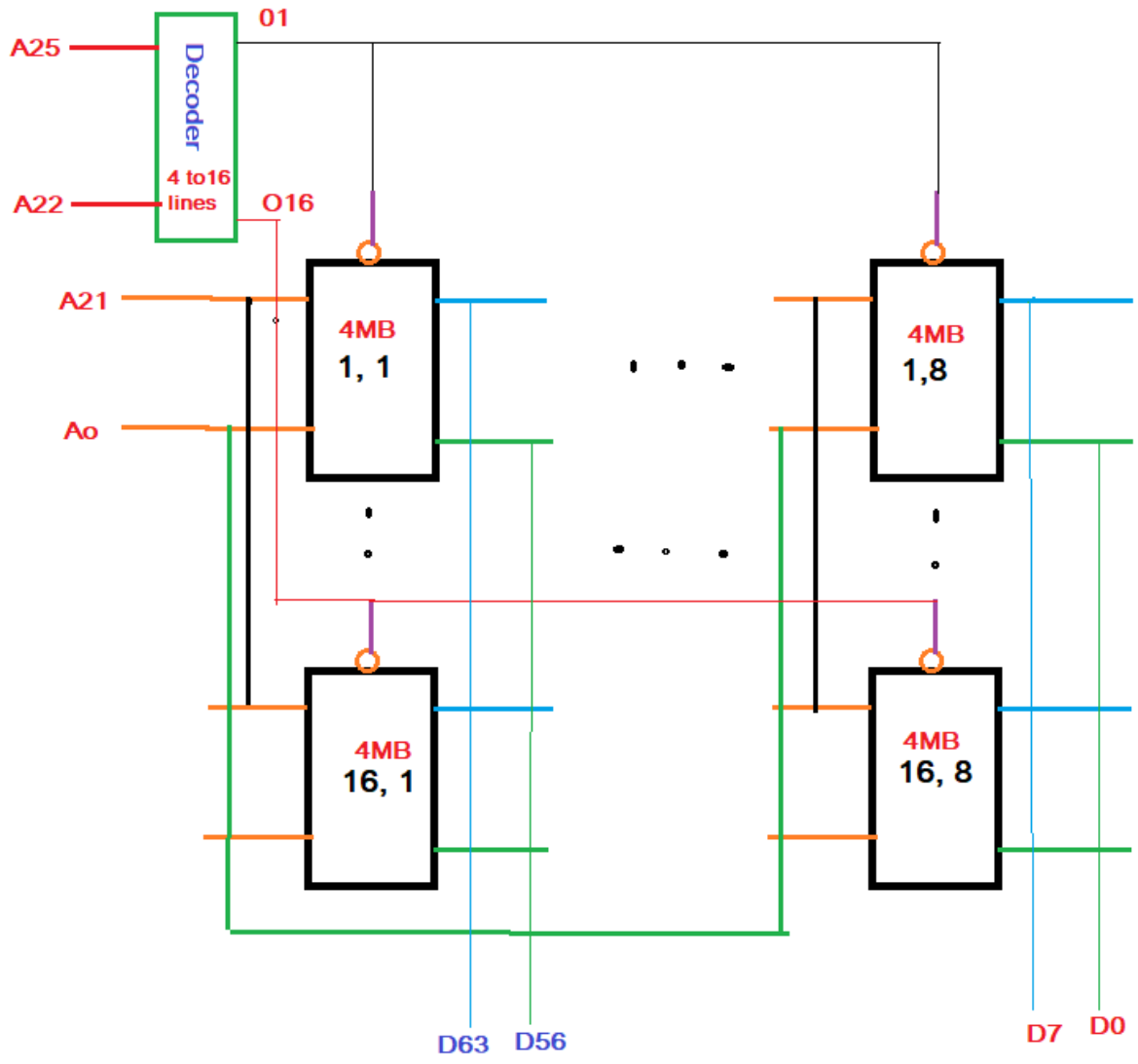
rows x cols

16 x 8

$$\text{No of ICs} = \frac{64M \times 64 \text{ bits}}{4M \times 8 \text{ bits}}$$

A decoder should be used to select ICs placed in a row out of 16 rows. The decoder must have 16 output lines. The number of input lines, n will be : $2^n = 16$; n = 4.
So the size of decoder will be 4 to 16 lines



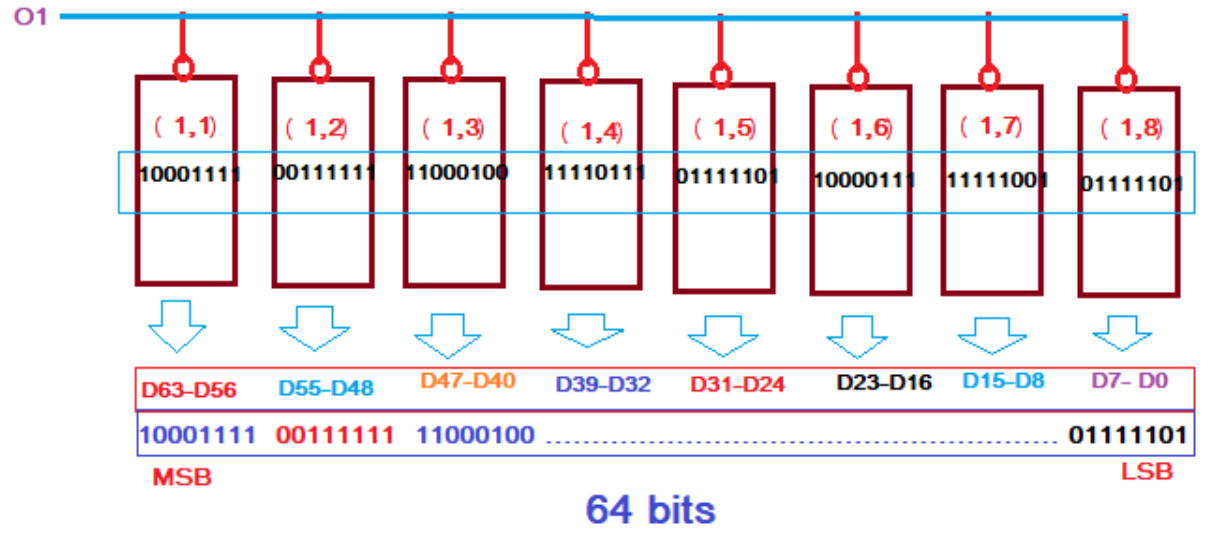


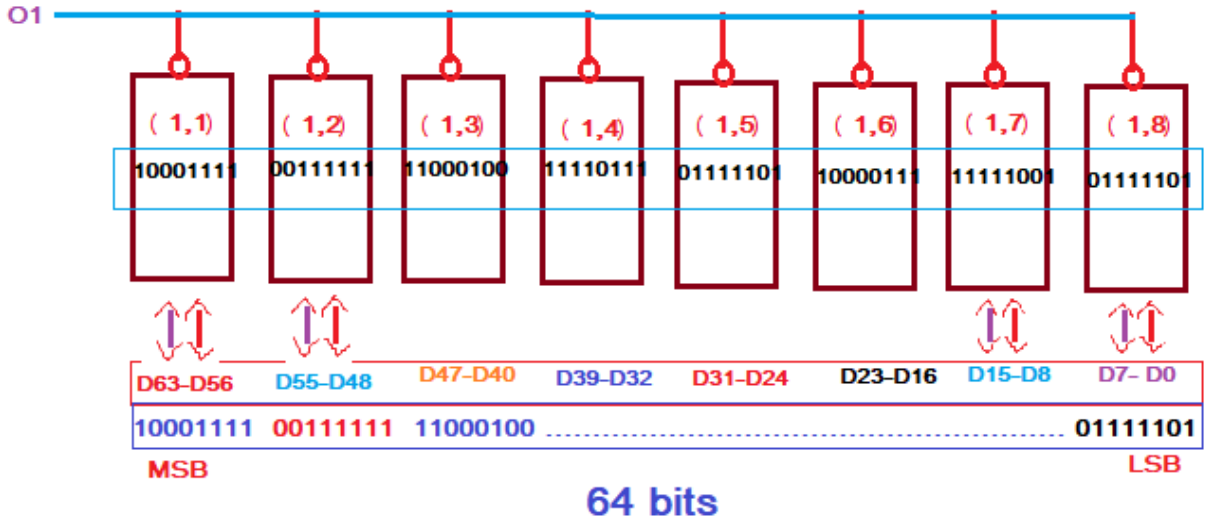
All corresponding address pins of all memory ICs should be connected. It means, all A0 pins of all 128 ICs, used in the design, should be connected. Similarly all A1's, A2's ….. A21's should be connected.

Outputs of the decoder are connected to enable pins of ICs placed in rows. First output of the decoder, O1 is connected to enable pins of ICs placed in the first row of the design. Similarly, O2, O3, …. O16 will be used to select ICs placed in rows 2, 3, ….. 16 respectively.

Notations of data pins:
The word size of the designed memory module is 64 bits. It means that, the CPU will read 64 bits data from the module. Similarly the CPU can save 64bits contents to this memory module as well. It is to be noted that the module is designed using byte addressable ICs each of 4MB. A single IC can hold only 8 bits. To extend the word size of the module to 64 bits, eight 4MB ICs are placed in each row and are selected for read or write. During a read operation from the module, eight ICs placed in a particular row are selected and 64 bits contents are formed by reading 8bits each from eight ICs placed in that row. The contents are placed row-wise (shown below), it means, contents of IC, placed in row-8 are read as least significant byte (LSB: D7 – D0). Likewise, contents of IC, placed in row-7 are read as higher byte (D15 – D8), contents of IC, placed in row-6 are read as higher byte (D23 – D16) so on. The contents of IC, placed in row-1 are read as most significant byte (MSB: D63 – D56).

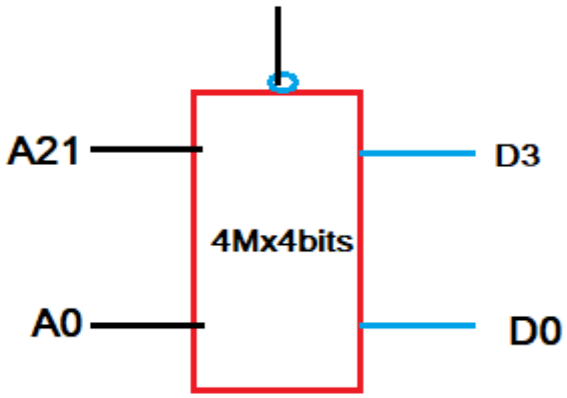
Notations of data pins of ICs placed in columns are denoted accordingly (see diagrams). Data pins of ICs placed in column-8 are indicated by D7 – D0, Data pins of ICs placed in column-7 are indicated by D15 – D8 and so on. Data pins of ICs placed in column-1 are indicated by D63 – D56.





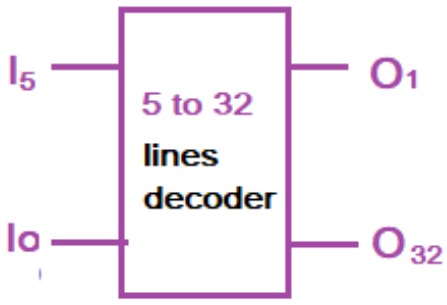
Design a memory module of capacity 128M x 64 bits by using 4M x 4 bits ICs.

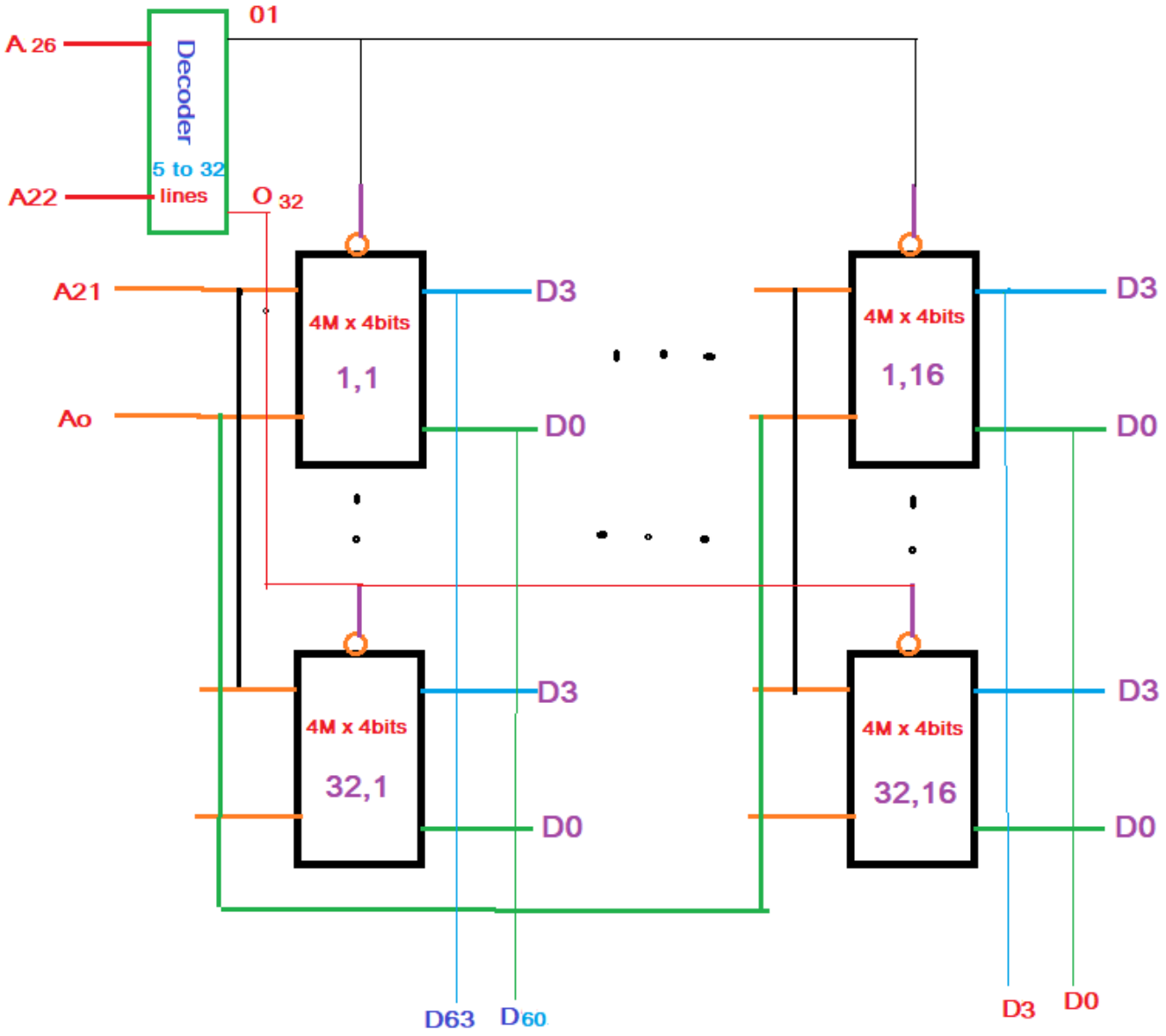
4M x 4bits IC:
Number of addressable locations: 4M = 4 x 1024 x 1024 = $2^2 \times 2^{10} \times 2^{10} = 2^{22}$
Number of address lines/pins = 22
Content of each addressable location = 4 bits
Number of data lines/pins = 4



$$\text{No of ICs} = \frac{\text{rows x cols}}{\frac{128M \times 64 \text{ bits}}{4M \times 4 \text{bits}}} = \frac{32 \times 16}{}$$

A decoder should be used to select ICs placed in a row out of 32 rows. The decoder must have 32 output lines. The number of input lines, n will be: $2^n = 32$; n = 5.
So the size of decoder will be 5 to 32 lines



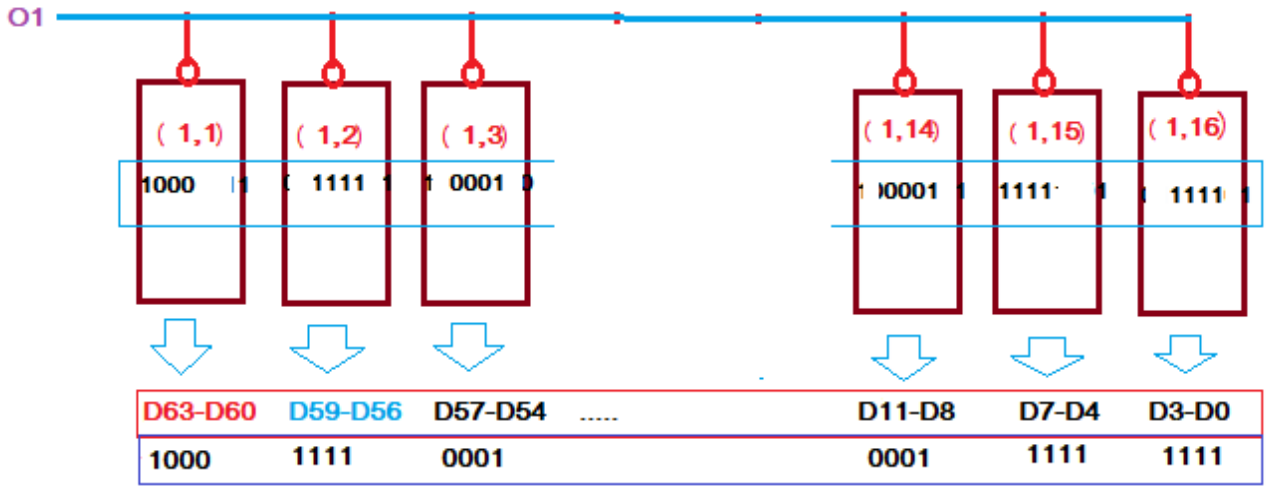


All corresponding address pins of all memory ICs should be connected. It means, all A0 pins of all 128 ICs, used in the design, should be connected. Similarly all A1's, A2's ….. A21's should be connected.

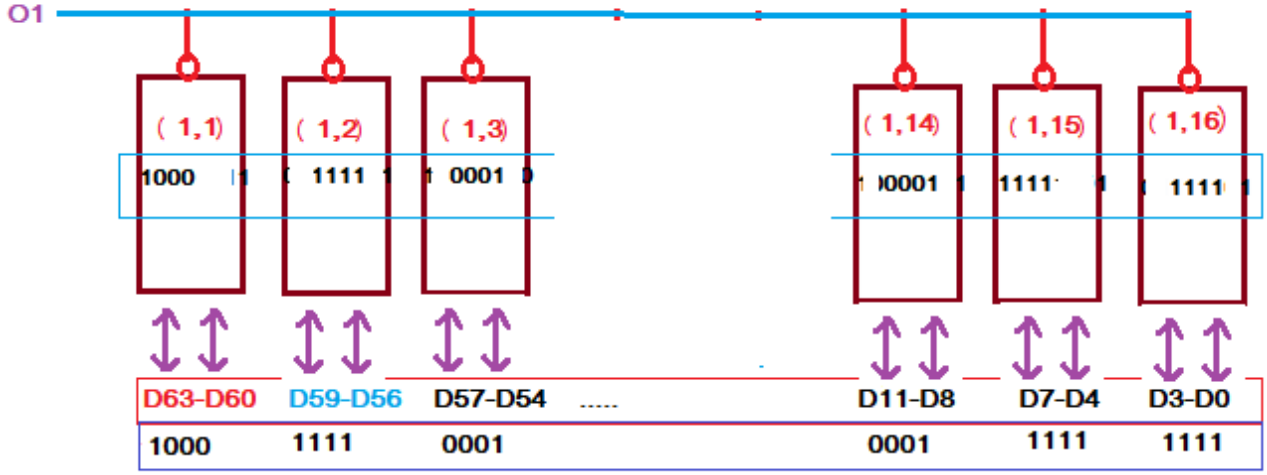
Outputs of the decoder are connected to enable pins of ICs placed in rows. First output of the decoder, O1 is connected to enable pins of ICs placed in the first row of the design. Similarly, O2, O3, …. O32 will be used to select ICs placed in rows 2, 3, ….. 32 respectively.

Notations of data pins:
The word size of the designed memory module is 64 bits. It means that, the CPU will read 64 bits data from the module. Similarly the CPU can save 64bits contents to this memory module as well. It is to be noted that the module is designed using ICs each of 4M x4bits. A single IC can hold only 4 bits. To extend the word size of the module to 64 bits, sixteen 4M x 4bits ICs are placed in each row and are selected for read or write. During a read operation from the module, sixteen ICs placed in a particular row are selected and 64 bits contents are formed by reading 4bits each from sixteen ICs placed in that row. The contents are placed row-wise (shown below), it means, contents of IC, placed in row-16 are read as least four bits (D3 – D0). Likewise, contents of IC, placed in row-15 are read as higher four bits (D7 – D4), contents

of IC, placed in row-14 are read as four bits (D11 – D8) so on. The contents of IC, placed in row-1 are read as most significant four bits (D63 – D60).
Notations of data pins of ICs placed in columns are denoted accordingly (see diagrams). Data pins of ICs placed in column-16 are indicated by D3 – D0, Data pins of ICs placed in column-15 are indicated by D7 – D4 and so on. Data pins of ICs placed in column-1 are indicated by D63 – D60.

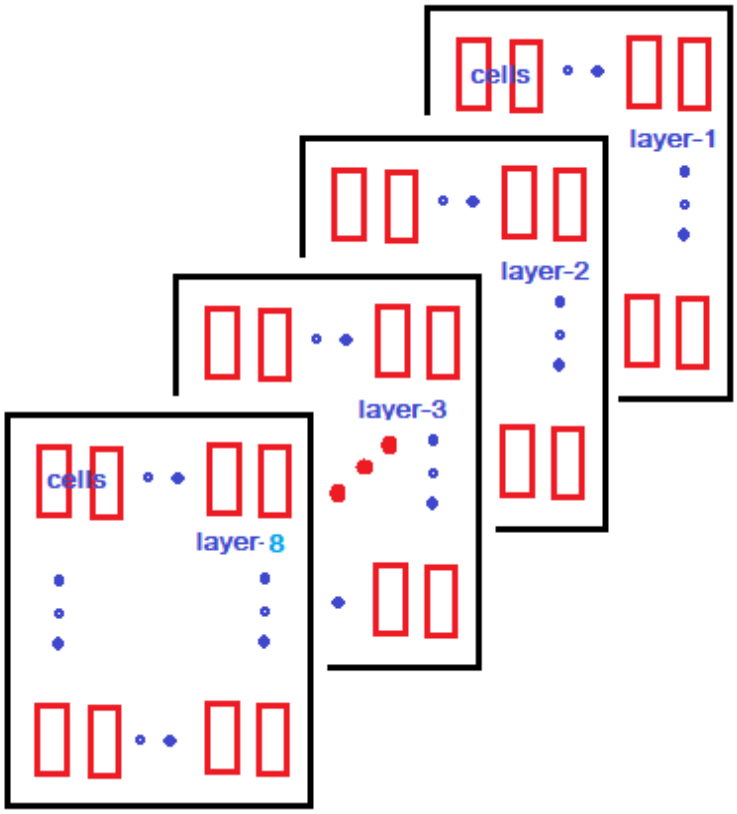


64 bits



64 bits

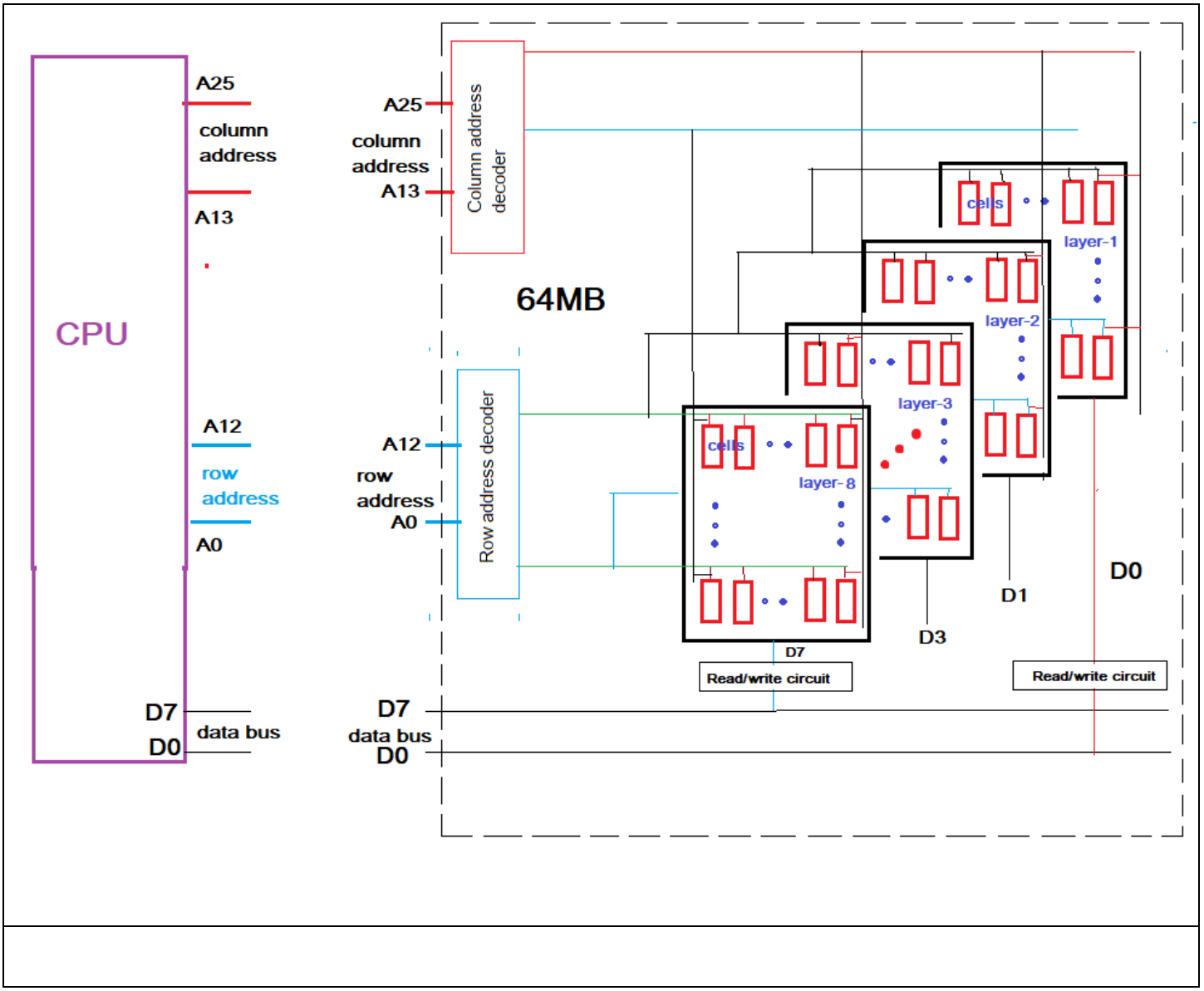
How cells are fabricated in high density DRAM IC?
To reduce the surface area of IC, cells are fabricated in layers, shown below. Moreover, in each layer, cells are fabricated in matrix-like structure having equal number of rows and column for ease of design and fabrication. For example, in a 64MB DRAM IC, cells (total = 64 x 1024 x 1024 x 8) are fabricated on eight surfaces, each surface contains: 64 x 1024 x 1024 cells. On each surface cells are arranged in 8 x 1024 rows and 8 x 1024 columns.

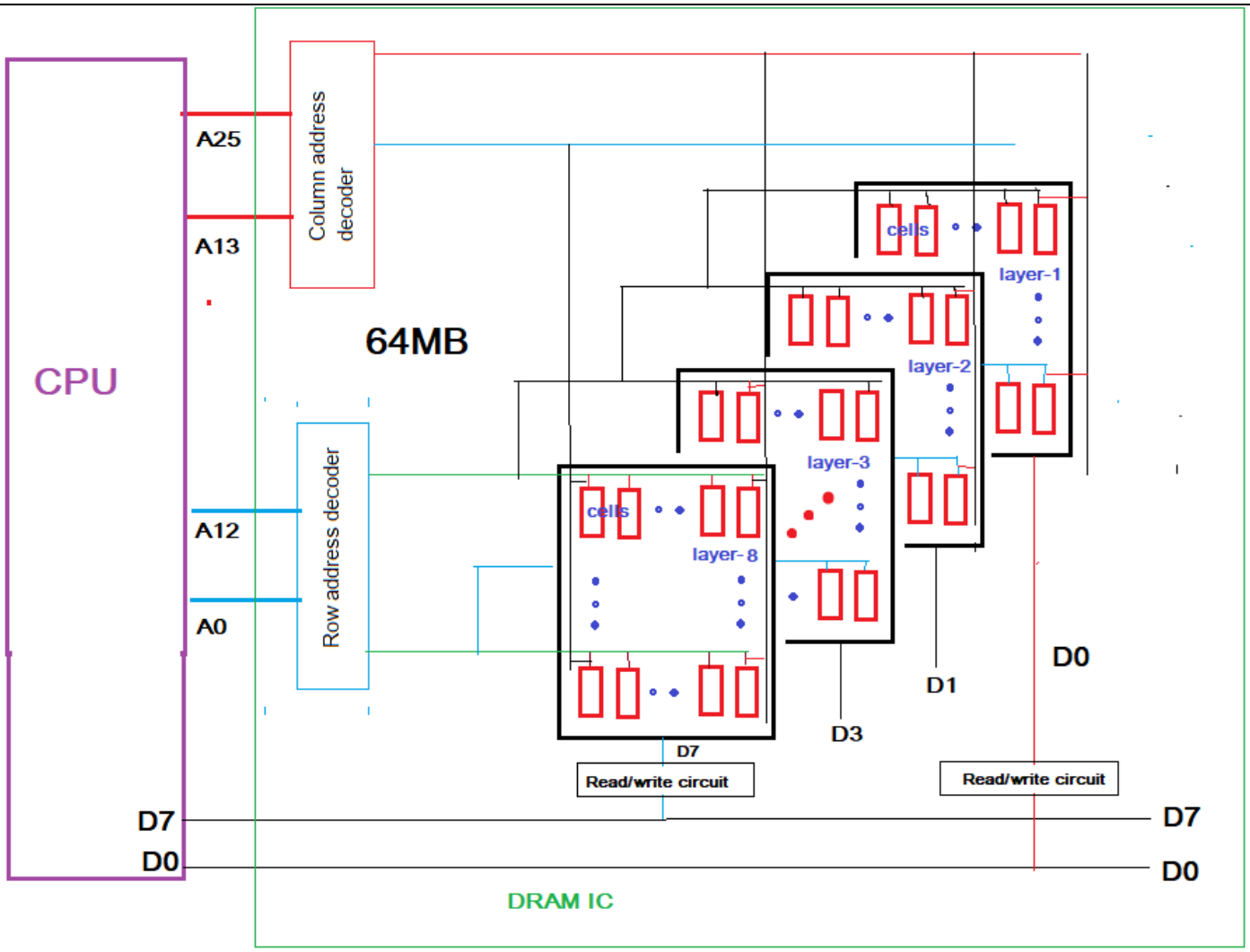


How does CPU read from high density DRAM ICs?

For example, in a 64MB DRAM IC, cells (total = 64 x 1024 x 1024 x 8) are fabricated on eight surfaces, each surface contains: 64 x 1024 x 1024 cells. On each surface cells are arranged in 8 x 1024 rows and 8 x 1024 columns. There are two address decoders inside the DRAM IC each of 13 input lines to 8 x 1024 output lines. These are called row address decoder and column address decoder. The 26-bits memory address generated by the CPU is split into row address and column each of 13 bits are sent to memory.

Assume that the DRAM has separate lines to receive row address and column address at the decoders, shown below. In this case, the DRAM would require 26 address pins to receive row and column address from the CPU. Any 26-bits memory address, sent by the CPU will be placed on row address decoder and column address decoder at the same time. As a result, only one cell from each layer will be selected and contents are read through data pins. It is noted that a data line is connected to all cells of a layer. Data line 1 is connected to all cells of layer-1. Similarly data line-2 is connected to all cells of layer-2, data line 8 is connected to all cells of layer-8. There are read/write circuits associated with data lines and CPU sends Read/write control signal to read/write circuits.


CPU
A25
column address
A13
A12
row address
A0
D7
D0
data bus
A25
column address
A13
Column address decoder
64MB
A12
row address
A0
Row address decoder
cells
layer-1
layer-2
layer-3
layer-8
D0
D1
D3
D7
Read/write circuit
Read/write circuit
D7
data bus
D0



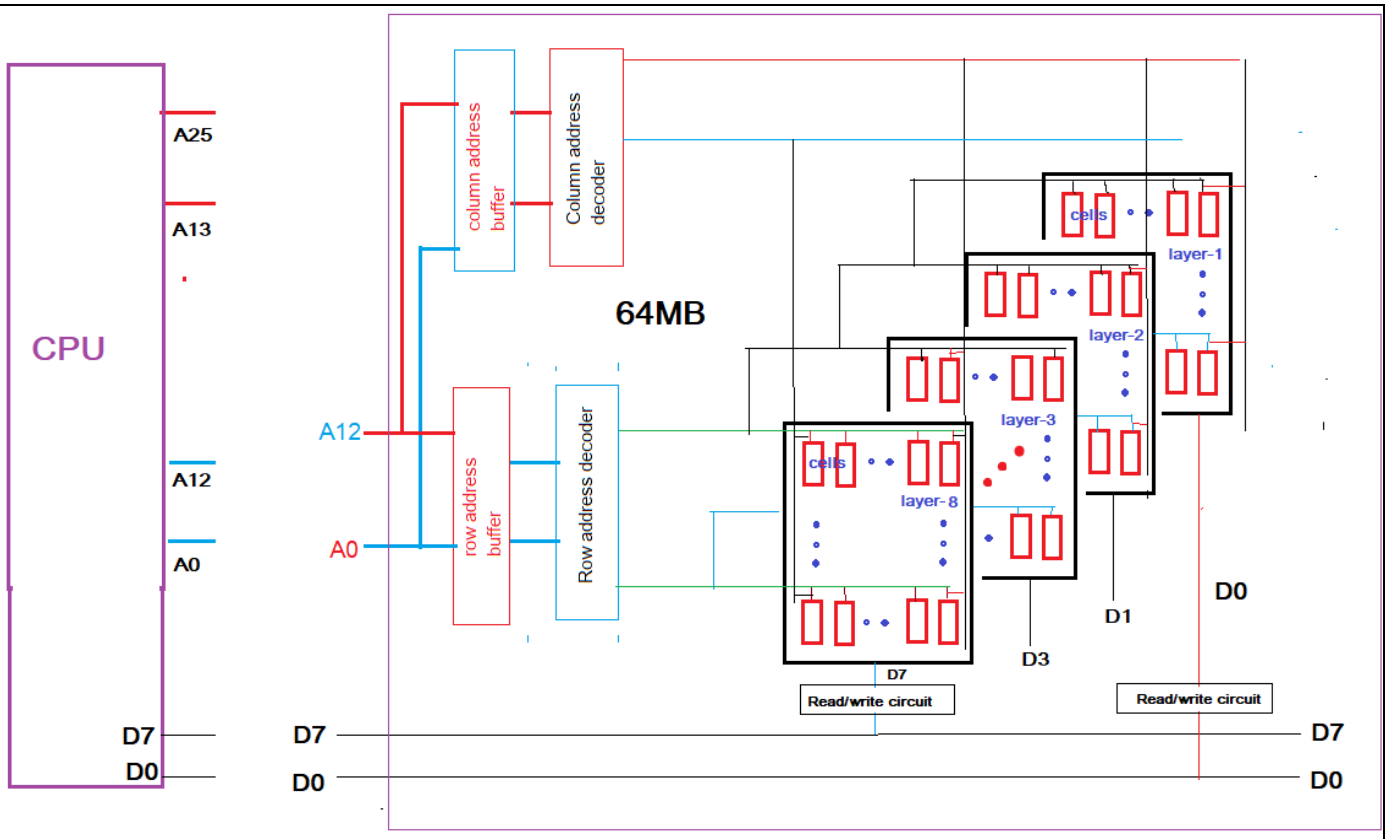
How to reduce pins and signals of DRAM IC?

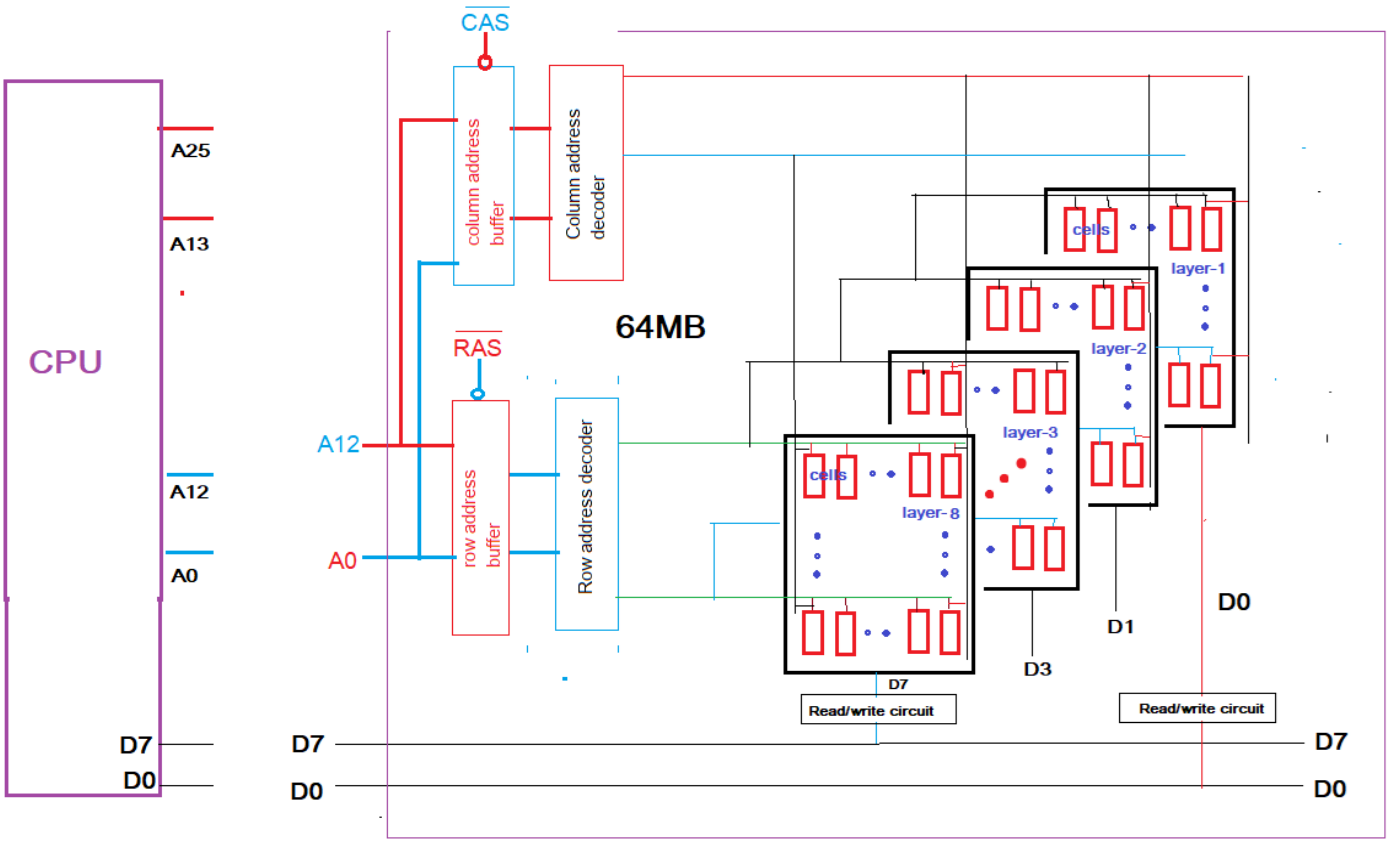
For high capacity DRAM ICs, the number of address pins is significantly more compared to a low capacity RAM ICs. Example: for 16KB IC, the number of address pin is 14 whereas for 64MB DRAM, the required number of address pin will be 26. For both ICs, the number of data pin would remain same and it is 8.

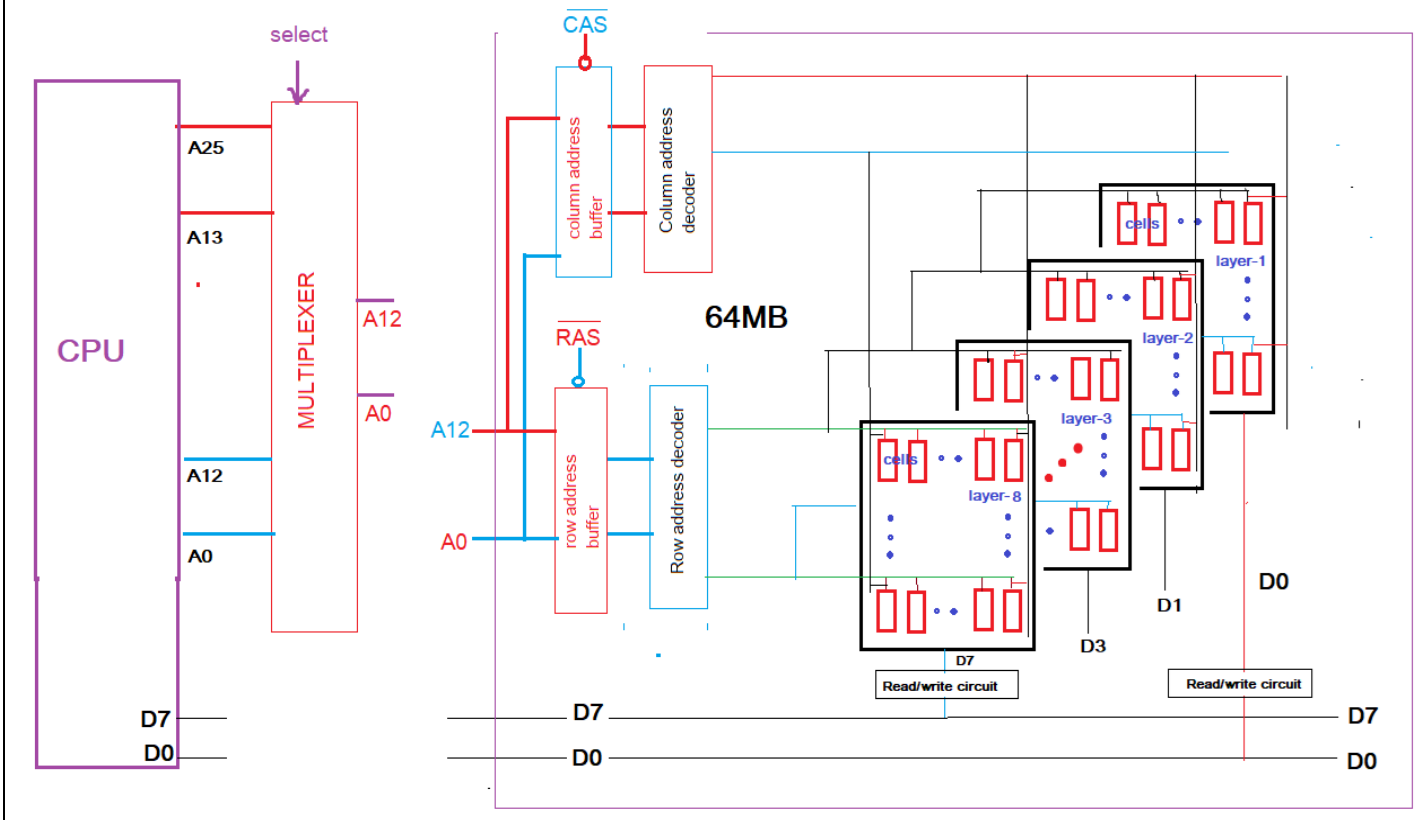
Higher number of address pin would require higher surface area for contact and this would increase IC surface area.

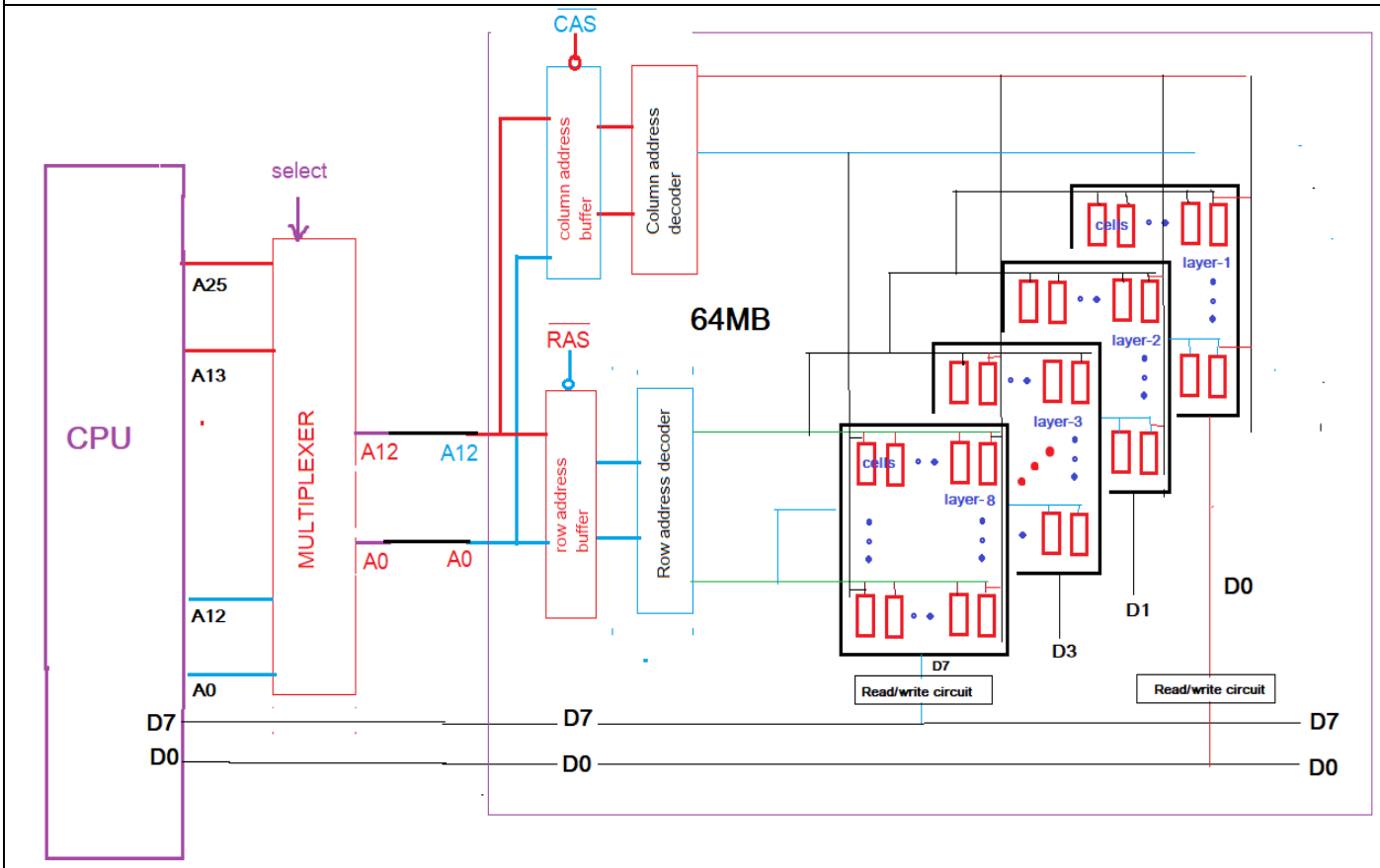
To reduce the number of pins and signals of DRAM ICs, the number of address pin is reduced to half and two additional buffers are used; one to store row address and another to hold column address until the completion of read/write operation. Two more control signals are required to activate buffers, namely Row Address Strobe (RAS) and Column Address Strobe (CAS).

In such case, the 64MB DRAM has only 13 address lines (A0 – A12), only half of actually required. The 26-bit memory address generated by the CPU is placed on 13-bit DRAM address bus in two steps, through a multiplexer. The row address is placed on DRAM memory address bus A0 – A12 and then RAS is activated. As a result, the contents on DRAM address bus is saved to row address buffer. After a while, the column address is placed on same DRAM address lines and then CAS is activated. The contents of DRAM address lines are stored in column address buffer. Buffers are connected to address decoders and activates a particular cell on each layer.


CPU
A25
A13
A12
A0
D7
D0
column address buffer
Column address decoder
64MB
A12
A0
row address buffer
Row address decoder
cells
layer-1
layer-2
layer-3
layer-8
D7
D3
D1
D0
Read/write circuit
Read/write circuit
D7
D0
D7
D0

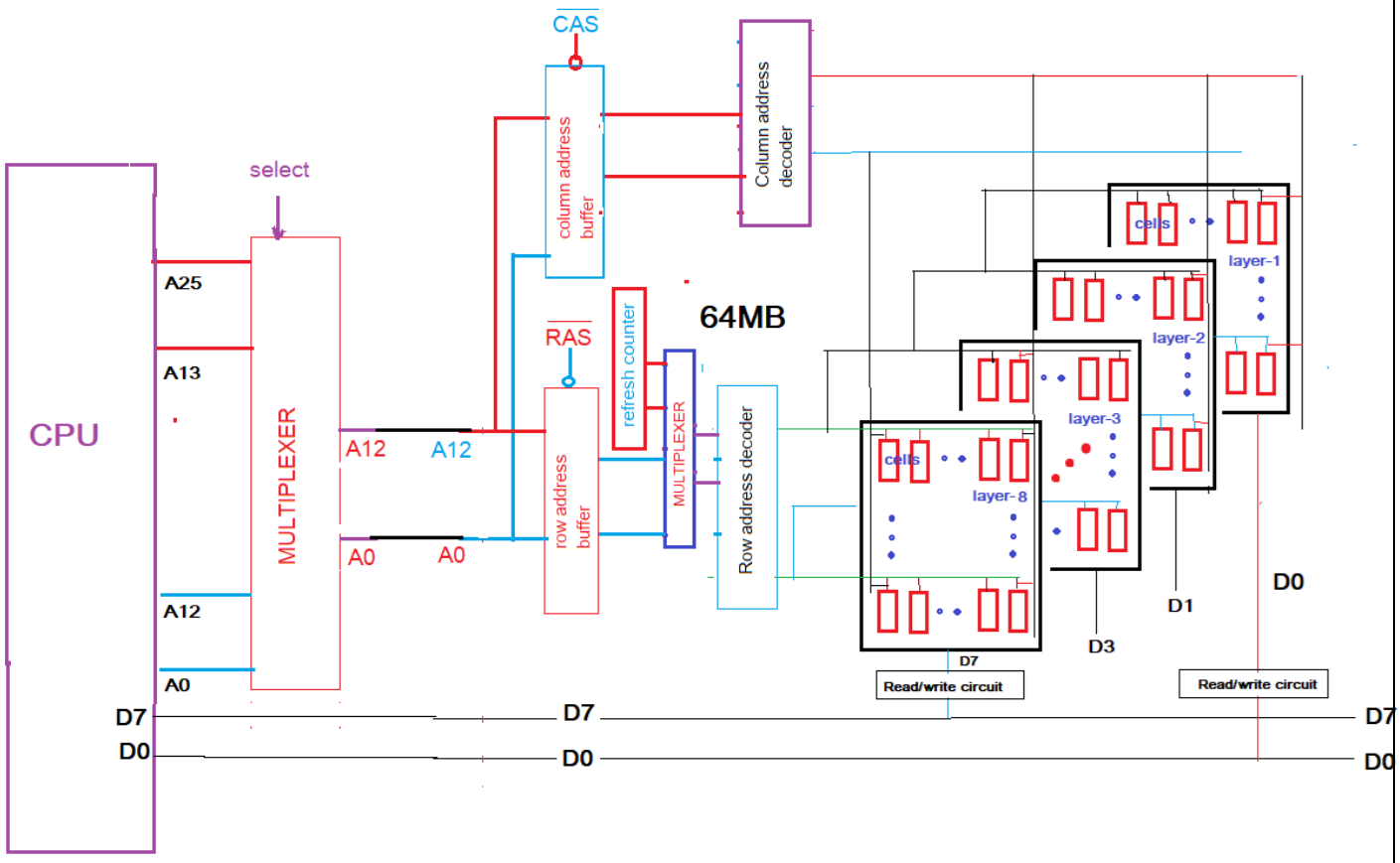

CAS
CPU
A25
A13
A12
A0
D7
D0
column address buffer
Column address decoder
64MB
RAS
A12
A0
row address buffer
Row address decoder
cells
layer-1
layer-2
layer-3
layer-8
D0
D1
D3
D7
Read/write circuit
Read/write circuit
D7
D0
D7
D0

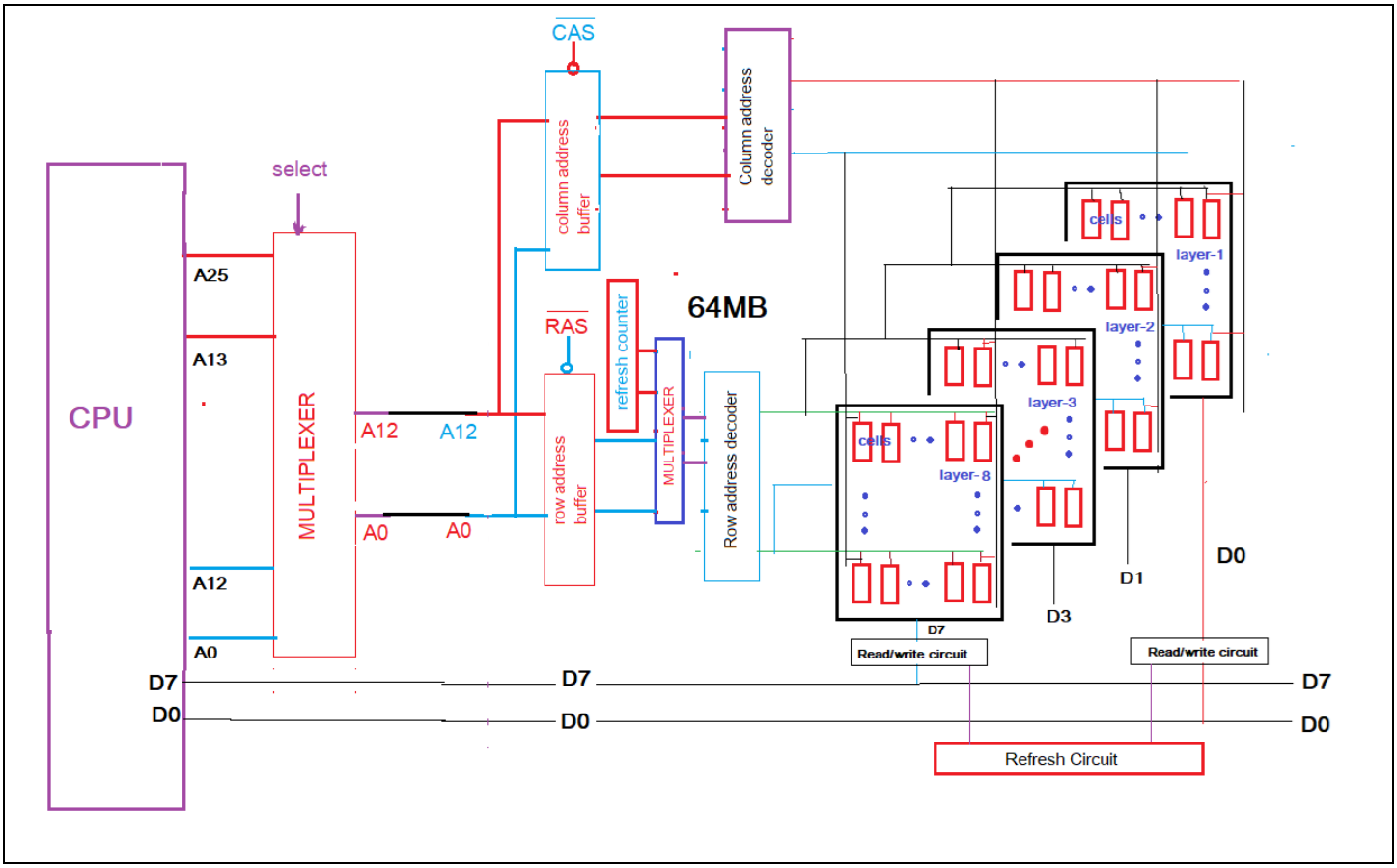

select
CAS
CPU
A25
A13
A12
A0
MULTIPLEXER
A12
A0
column address buffer
Column address decoder
RAS
row address buffer
Row address decoder
64MB
cells
layer-1
layer-2
layer-3
layer-8
D0
D1
D3
D7
Read/write circuit
Read/write circuit
D7
D0
D7
D0
D7
D0


CAS
select
CPU
A25
A13
A12
A0
MULTIPLEXER
A12
A12
A0
A0
column address buffer
Column address decoder
RAS
row address buffer
Row address decoder
64MB
cells
layer-1
layer-2
layer-3
layer-8
D0
D1
D3
D7
Read/write circuit
Read/write circuit
D7
D0
D7
D0
D7
D0

What is Refresh circuit? Why it is used? And how it is used?

In DRAM ICs, a capacitor is used to design a cell to hold a single bit. A charged capacitor represents binary '1' while a discharged capacitor represents binary '0'. A charged capacitor discharges through leakage current even the power is on. To prevent capacitors from discharging and to retain/preserve the contents of cells, specially holding '1's , a refresh mechanism is used in DRAM IC. The refresh operation is repeated at a rate, faster than the time taken by capacitors to discharge to a low value. The refresh operation is performed row-wise and a counter is used to generate row address, starting from 0. It means, cells of first row of all layers are refreshed first followed by cells of 2nd rows of all layers and it continues. During refresh operation, the row address, generated by counter is placed to row address decoder through a multiplexer. The refresh circuit is used with read/write circuit.




CAS
Column address decoder
column address buffer
select
CPU
A25
A13
A12
A0
MULTIPLEXER
A12
A12
A0
A0
RAS
row address buffer
refresh counter
MULTIPLEXER
Row address decoder
64MB
cells
layer-1
layer-2
layer-3
layer-8
D7
D3
D1
D0
Read/write circuit
Read/write circuit
D7
D0
D7
D0
D7
D0
Refresh Circuit