CSE332: Problems & Solutions

1. Consider three different processors P1, and P2 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 2.2. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Answer:

For P1: Number of cycles = 3×10^{10} ; Number of Instructions: 2×10^{10}

For P2: Number of cycles = 2.5×10^{10}; Number of Instructions: 1.136×10^{10}

Consider two different machines, with two different instruction sets, using two compilers runs a program having following distribution of instructions.

Instruction Type	Machine-A (Clock rate 250MHz)		Machine-B (Clock rate 300MHz)	
	Instruction Count in Millions	CPI	Instruction Count in Millions	CPI
ARITHMETIC	8	1	7	1
LOAD	6	5	8	4
BRANCH	2	4	2	5
STORE	4	2	3	3

Determine the average CPI, MIPS rate, and execution time for each machine. Do MIPS ratings reflect the true relative performances of Machines A & B, justify your answer with reference to other values and performance measures.

Solution:

Machine-A

Average CPI: $(8\times1+6\times5+2\times4+4\times2)/20 = 54/20 = 2.7$

Execution time: $20 \times10^{6}\times 2.7 \times (1/250 \times 10^{6}) = 0.216$ sec

MIPS = $f /(CPI \times 10^{6}) = (250 \times 10^{6})/(2.7 \times 10^{6}) = 92.59$

Machine-B

Average CPI: $(7\times1+8\times4+2\times5+3\times3)/20 = 58/20 = 2.9$

Execution time: $20 \times10^{6}\times 2.9 \times (1/300 \times 10^{6}) = 0.193$ sec

MIPS = $f /(CPI \times 10^{6}) = (300 \times 10^{6})/(2.9 \times 10^{6}) = 103.44$

Here, MIPS ratings reflect the true relative performances of Machines A & B. Machine-B is faster since execution time is lower.

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
ARITHMETIC	45000	1
DATA TRANSFER	32000	2
FLOATING POINT	15000	2
CONTROL TRANSFER	8000	2

Determine the Average CPI, MIPS rate, and execution time for this program.

Solution:

Average CPI = (45000 × 1 + 32000 × 2 + 15000 × 2 + 8000 × 2)/100000 = 1.55

Execution time = $100000 \times 1.55 \times (1/40 \times 10^6) = 0.003875$ sec = 3.875 ms

MIPS = $(100000 \times 40 \times 10^6)/(100000 \times 1.55 \times 10^6) = 25.80$

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

MACHINE - A	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	8	1
	LOAD and STORE	4	3
	BRANCH	2	4
	OTHERS	4	3

.....

MACHINE - B	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	10	1
	LOAD and STORE	8	2
	BRANCH	2	4
	OTHERS	4	3

Determine the Average CPI, MIPS rate, and execution time for each machine.

Machine-A : Average CPI: (8×1+4×3+2×4+4×3)/18 = 40/18 = 2.22

Execution time: $18 \times 2.22 \times (1/200 \times 10^6) = 0.198 \times 10^{-6}$ sec

MIPS = f /(CPI × 10^6) = (200 × 10^6)/(2.22 × 10^6) = 90.09

Machine-B: Average CPI: (10×1+8×2+2×4+4×3)/24 = 46/24 = 1.92

Execution time: 24 × 1.92 × (1/200 × 10^6) = 0.23 × 10^{-6} sec

MIPS = f /(CPI × 10^6) = (200 × 10^6)/(1.92 × 10^6) = 104.16

2. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with an instruction count of 1.0x 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

What is the global CPI for each implementation?

Answer:

For P1: Average CPI = 2.6 ; Execution time: 1.04 × 10^{-3} sec

For P2: Average CPI = 2 ; Execution time: 0.66 × 10^{-3} sec

P2 is faster

Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	CLOCK RATE	CPI class A	CPI class B	CPI class C	CPI class D
P1	2.5 GHz	1	2	3	3
P2	3 GHz	2	2	2	2

a) Given a program with 106 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

b) What is the global CPI for each implementation?

c) Find the clock cycles required in both cases.

Solution:

Class A: 10%

Class B: 20%

Class C: 50%

Class D: 20%

For P1: CPI = 0.1× 1+ 0.2× 2 + 0.5 × 3 + 0.2 × 3 = 2.6

Execution Time: 106 × 2.6 × (1/2.5 × 10^9) second = 275.6 × 0.4 × 10^{-9} sec = 110.24 × 10^{-9} sec

Clock cycles: 2.6 × 106 = 275.6

For P2: CPI = 0.1× 2+ 0.2× 2 + 0.5 × 2 + 0.2 × 2 = 2.0

Execution Time: $106 \times 2.0 \times (1/3 \times 10^9)$ second = $212 \times 0.33 \times 10^{-9}$ sec = 69.96×10^{-9} sec

Clock cycles: 2.0× 106 = 212

a) P2 implementation is faster

b) For P1: Global CPI = 2.6

For P2: Global CPI = 2.0

c) For P1: Clock cycles: 275.6

For P2: Clock cycles: 212

A RISC machine uses a clock of 3GHz. It runs a program containing 1.5×10^6 instructions and the program contains following instruction mix:

Instruction type	CPI	Frequency of Instructions in the program
ALU	3	20%
Load	5	30%
Store	5	35%
Branch	6	15%

If a CPU design enhancement reduces CPI values of load and branch instructions by 2 and 3 respectively. What is the resulting performance improvement from this enhancement?

The following table shows the number of instructions for a program.

	ARITH	STORE	LOAD	BRANCH	TOTAL
A.	650	100	600	50	1400
B.	750	250	500	500	2000

a) Assuming that arithmetic instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?

b) Find the CPI for the program.

c) If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

Solution:

	ARITH	STORE	LOAD	BRANCH	TOTAL

A.	650	100	600	50	1400
B.	750	250	500	500	2000
	CPI=1	CPI=5	CPI=5	CPI=2	

For A:

Average CPI for A: $(650 \times 1 + 100 \times 5 + 600 \times 5 + 50 \times 2)/1400 = 4200/1400 = 3$

Execution time for A: $1400 \times 3 \times 1/(2 \times 10^9) = 4200 \times 0.5 \times 10^{-9}$ sec = 2100 ns

If the number of load instructions can be reduced by one half,

Average CPI for A: $(650 \times 1 + 100 \times 5 + 300 \times 5 + 50 \times 2)/1400 = 2700/1100 = 2.45$

Speed up = $(1400 \times 3 \times 1/(2 \times 10^9))/ (1100 \times 2.45 \times 1/(2 \times 10^9)) = 4200/2695 = 1.55$

For B:

Average CPI for B: $(750 \times 1 + 250 \times 5 + 500 \times 5 + 500 \times 2)/2000 = 5500/2000 = 2.75$

Execution time for A: $2000 \times 2.75 \times 1/(2 \times 10^9) = 2750$ ns

If the number of load instructions can be reduced by one half,

Average CPI for B: $(750 \times 1 + 250 \times 5 + 250 \times 5 + 500 \times 2)/1750 = 4250/1750 = 2.42$

Speed up = $(2000 \times 2.75 \times 1/(2 \times 10^9))/ (1750 \times 2.42 \times 1/(2 \times 10^9)) = 5500/4235 = 1.30$

You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark program, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	CPI
Loads & Stores	30%	6
Arithmetic Instructions	50%	4
All Others	20%	3

a) Calculate the CPI for Benchmark program.

b) What is the MIPS rating of the processor speed?

c) The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

d) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

e) How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

Solution:

a) CPI: $0.3 \times 6 + 0.5 \times 4 + 0.2 \times 3 = 4.4$

b) MIPS = $(200 \times 10^6)/(4.4 \times 10^6) = 45.45$

c) Old Cycle time : $1/(200 \times 10^6) = 0.005 \times 10^{-6}$sec

New Cycle time: 0.005×10^{-6}sec + 0.001×10^{-6}sec = 0.006×10^{-6}sec

New clock speed, f = $1/(0.006 \times 10^{-6}\text{sec})$ Hz = 166.66×10^6 Hz = 166.66 MHz

d) Let us assume that, initially total number of instructions was = 100 (Loads & Stores = 30, Arithmetic = 50 and Others = 20).

Half the number of Loads & Stores = 30/2 = 15

New CPI: $(15 \times 6 + 50 \times 4 + 20 \times 3)/85 = (90+200+60)/85 = 350/85 = 4.11$

e) Taking c (New clock speed = 166.66 MHz and d (New CPI = 4.11) into consideration,

Execution time: $85 \times 4.11 \times 1/(166.66 \times 10^6)$ sec = 2.10×10^{-6} sec

A computer M_2 has the following CPIs for instruction types A thru D, and a program P_3 has the following mix of instructions.

M_2: Type A $CPI_A = 1.7$ Type B $CPI_B = 2.1$ Type C $CPI_C = 2.7$ Type D $CPI_D = 2.4$

P_3: Type A = 22% Type B = 29% Type C = 17% Type D = remaining %

a) Calculate the average CPI of Machine M_2

b) Calculate the runtime of P_3 on M_2 if IC = 22,311 and clock rate is 3.3 GHz

Solution:

a) Average CPI: $0.22 \times 1.7 + 0.29 \times 2.1 + 0.17 \times 2.7 + 0.32 \times 2.4 = 0.374 + 0.609 + 0.459 + 0.768 = 2.21$

b) Run time: $22311 \times 2.21 \times (1/3.3 \times 10^9) = 14.94 \times 10^{-6}$ sec

A RISC machine uses a clock of 3GHz. It runs a program containing 1.5×10^6 instructions and the program contains following instruction mix:

Instruction type	CPI	Frequency of Instructions in the program	Fraction of Inst	Fraction execution time	
ALU	3	20%	0.2	0.126	
Load	5	30%	0.3	F1= 0.315	
Store	5	35%	0.35	0.368	
Branch	6	15%	0.15	F2= 0.189	

If a CPU design enhancement reduces CPI values of load and branch instructions by 2 and 3 respectively. What is the resulting performance improvement from this enhancement?

Average CPI: 0.2x3+0.3x5+0.35x5+0.15x6 = 4.75

% of time for ALU Instructions: (0.2x3)/4.75 = 0.1263

For Load Instructions: S1= 5/3 = 1.66

For Branch Instructions: S2 = 6/3 = 2

Speedup = 1/[(1-F1-F2)+(F1/S1) +(F2/S2)] = 1/[0.496 +0. 189 + 0.0945] = 1/0.7795 = 1.282

Assume a new web-server with a CPU being 5 times faster on computation than the previous web-server. I/O performance is not improved compared to the old machine. The web-server spends 60% of its time in computation and 40% in I/O. How much faster is the new machine overall?

Answer:

Speedup = 1/[(1-0.6) + (0.6/5)] = 1/[0.4 + 0.12] = 1/0.52 = 1.923

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	1	2	40%
B	2	4	30%
C	4	3	30%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	4	3	45%
B	2	4	30%
C	1	2	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock rate of 120 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	3	3	30%
B	2	3	45%
C	4	5	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Instruction Class	Machine M1	Machine M2	% of Instructions

			Cycles/Instruction class	Cycles/Instruction class	

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

A	1	2	40%
B	2	4	30%
C	4	3	30%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	4	3	45%
B	2	4	30%
C	1	2	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock

rate of 120 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	3	3	30%
B	2	3	45%
C	4	5	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Using Amdahl's Law, show which is better: making 20% of the instructions in a program 80% faster, or making 80% of the instructions 20% faster.

Solution

Speed up for 20% of the instructions in a program 80% faster

S = 1/[1-0.2 + 0.2/1.8] = 1.097

Speed up for 80% of the instructions in a program 20% faster

S = 1/[1-0.8 + 0.8/1.2] = 1.15 (Better)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	1	2	40%

B	2	4	30%
C	4	3	30%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Solution:

Machine: M1:

Average CPI = 0.4x1+0.3x2+0.3x4 = 2.2

MIPS rating = $80x10^6/(2.2x\ 10^6)$ = 36.36

Machine: M2:

Average CPI = 0.4x2+0.3x4+0.3x3 = 2.9

MIPS rating = $100x10^6/(2.9x\ 10^6)$ = 34.48

Machine M2 has smaller MIPS rating.

If CPI of Instruction class B is reduced by 1

Then, new Average CPI for M2: 0.4x2+0.3x3+0.3x3 = 2.6

New MIPS rating = $100x10^6/(2.6x\ 10^6)$ = 38.46

Using Amdahl's Law, show which is better: making 30% of the instructions in a program 70% faster, or making 70% of the instructions 30% faster.

Solution

Speed up for 30% of the instructions in a program 70% faster

S = 1/[1-0.3 + 0.3/1.7] = 1.141

Speed up for 70% of the instructions in a program 30% faster

S = 1/[1-0.7 + 0.7/1.3] = 1.193 (Better)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	4	3	45%
B	2	4	30%
C	1	2	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Solution:

Machine: M1:

Average CPI = 0.45x4+0.3x2+0.25x1 = 2.65

MIPS rating = $90x10^6/(2.65x\ 10^6)$ = 33.96

Machine: M2:

Average CPI = 0.45x3+0.3x4+0.25x2 = 3.05

MIPS rating = $100x10^6/(3.05x\ 10^6)$ = 32.78

Using Amdahl's Law, show which is better: making 25% of the instructions in a program 75% faster, or making 75% of the instructions 25% faster.

Solution

Speed up for 25% of the instructions in a program 75% faster

S = 1/[1-0.25 + 0.25/1.75] = 1.121

Speed up for 75% of the instructions in a program 25% faster

S = 1/[1-0.75 + 0.75/1.25] = 1.176 (Better)

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 90 MHz and M2 has a clock rate of 120 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction class	Machine M2 Cycles/Instruction class	% of Instructions
A	3	3	30%
B	2	3	45%
C	4	5	25%

Calculate the average CPI for each machine, M1, and M2.

Calculate the average MIPS ratings for each machine, M1 and M2.

Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Solution:

Machine: M1:

Average CPI = 0.3x3+0.45x2+0.25x4 = 2.8

MIPS rating = $90x10^6/(2.8x\ 10^6)$ = 32.14

Machine: M2:

Average CPI = 0.3x3+0.45x3+0.25x5 = 3.5

MIPS rating = $120x10^6/(3.5x\ 10^6)$ = 34.28

	Suppose that you currently have a computer system with the following two characteristics: There are only three components that determine the overall performance — CPU, memory, and disk. For any given computation, the system spends 30% of the time for CPU, 40% of the time for memory, and 30% of the time for disk. Now suppose that you want to purchase a new system that improves the performance in the following ways: The new system spends 1/4 of the memory time compared to your current system. The new system spends 1/5 of the disk time compared to your current system. Everything else is the same. Using Amdahl's Law, calculate the overall speedup of the new system over your current system.
1	We wish to consider the performance of two different machines: M1 and M2. The clock frequencies for machines M1 and M2 are 800 MHz and 1000 MHz respectively. A program was run on both machines and the following measurements were made: Time on M1 Time on M2 2.5 seconds 2 seconds In addition, the following additional measurements were made: No. of Instructions Executed on M1 $100x10^6$ No. of Instructions Executed on M2 $125x10^6$ Finally, the frequency that instructions occur in the program for M1 and M2 are shown below

Instruction	M1%	M2%
ADD	40	60
MULT	10	8
CMP	20	12
SUB	30	20

a) Find the clock cycles per instruction (CPI or average CPI) for Program on both machine

b) How much faster will the program run on M1 and M2 respectively if we

i. reduce the execution time of the ADD instruction by 20%, assuming that an ADD instruction requires 5 cycles on both machines

ii. reduce the execution time of the MULT instruction by 20%, assuming a MULT instructions requires 20 cycles on M1 and 25 cycles on M2

Which is better for M1 and which for M2?

Solution:

2. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark B, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	Cycles
Loads & Stores	30%	6 cycles
Arithmetic Instructions	50%	4 cycles
All Others	20%	3 cycles

Calculate the CPI for Benchmark B.

If we say that there are 100 instructions, then:

30 of them will be loads and stores.

50 of them will be arithmetic instructions.

20 of them will be all others.

$(30 \times 6) + (50 \times 4) + (20 \times 3) = 440$ cycles/100 instructions

Therefore, there are 4.4 Cycles per instruction.

The CPU execution time on the benchmark is exactly 11 seconds. What is the ``native MIPS" processor speed for the benchmark in millions of instructions per second?

The formula for calculating MIPS is:

$$\text{MIPS} = \text{Clock rate}/(\text{CPI} \times 10^6)$$

The clock rate is 200MHz so...

$\text{MIPS} = (200 \times 10^6)/(4.4 \times 10^6) = 45.454545$

The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

Clock time = 1/Cycle Time

Cycle Time = 1/Clock Time

Cycle Time = $1/(200 \times 10^6) = 5 \times 10^{-9}$

The cycle time is then increased by 20%:

$(5 \times 10^{-9}) \times 1.2 = 6 \times 10^{-9}$

The new clock rate is thus:

$1/(6 \times 10^{-9}) = 166.667 \times 10^6$ or 166.667 MHz

The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

There were 100 instructions in part b, so we will reduce the number of loads and stores by half, and this will reduce the total number of instructions. So the new instruction mix will be:

15 Loads and Stores

50 Arithmetic Instructions

20 All Others

The total number of instructions is now 85, so the answer is:

$((15 \times 6) + (50 \times 4) + (20 \times 3)) / 85 = 350$ cycles/ 85 instructions = 4.12 CPI

How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

CPU seconds = (Number of instructions × Number of Clocks per instructions)/Clock Rate

First thing we need to do, is calculate the number of instructions which execute in 11 seconds on the new benchmark - the one with half the number of loads and stores.

To do this, we will need to figure out how many instructions execute on the original benchmark in 11 seconds. Since we know the MIPS or how many *Millions of Instructions Per Second* for the original benchmark, we say:

$(45.45 \times 10^6) \times 11 = 500 \times 10^6$ instructions in 11 seconds

Now we need to figure out how many of those are Loads and Stores so:

$(500 \times 10^6) \times .3 = 150 \times 10^6$ are Load and Store instructions because the chart says that 30% of all instructions are Loads and Stores. Now we need to cut this number in half, because the new benchmark says that we have half the number of loads and stores, but the cycle time increases by 20%. Therefore there are only 75×10^6 loads and stores. This also means that there are now less total instructions, 425×10^6 total instructions.

The final solution is:

$((425 \times 10^6) \times 4.12)/(166.667 \times 10^6) = 10.548$ seconds

Memory operations currently take 30% of execution time. A new strategy called a "cache" speed up 80% of memory operations by a factor of 4.

A second new strategy called a "L2 cache" speeds up 1/2 the remaining 20% by a factor or 2.

What is the total speed up?

Combine both the L1 and the L2

memory operations = 0.3

SL1 = 4

xL1 = 0.3*0.8 = .24

SL2 = 2

xL2 = 0.3*(1 - 0.8)/2 = 0.03

StotL2 = 1/(xL1/SLl + xL2/SL2 + (1 - xL1 - xL2))

StotL2 = 1/(0.24/4 + 0.03/2 + (1-.24-0.03)) = 1/(0.06+0.015+.73)) = 1.24 times

The table below shows the instruction type breakdown and the CPI of each instruction type of a given application running on a 3GHz processor.

Instruction Type	Percentage of Instruction Count	CPI	
Integer	55%	1	
Load/Store	30%	3	
Branch	15%	4	

Assume the application has a total of 2×10^9 instructions. Please answer the following questions:

What is the total execution time of the given benchmark?
Total execution time = CPI × Number of Instructions × clock cycle period
= $(0.55\times1 + 0.30\times3 + 0.15\times4) \times 2\times10^{9} \times 0.33\times10^{-9}$
= 1.367

A revision of processor raises the clock rate to 4GHz, but also increases the CPI of Load/Store instructions to 12. What's the speedup of this revision vs the original?

Total execution time = CPI × Number of Instructions × clock cycle period
= $(0.55\times1 + 0.30\times12 + 0.15\times4) \times 2\times10^{9} \times 0.25\times10^{-9}$
= 2.375s
Speed Up = new time/old time = 1.367/2.375 = 0.576

If 20% of the program is optimized to run at 4 times and 40% of the program at 2 times, what is the total speedup?
Solution:
100 / ((20 / 2) + (40/2) + 40)) = 100 / 65 = 1.538

A software engineer decides to rewrite a portion of the program that accounts for 60% of execution time so that it can run on multiple processors in parallel. What is maximum speedup she can hope to achieve?
Solution:
Maximum speedup 100 / 40 = 2.5

We want to compare the computers R1 and R2, which differ that R1 has the machine instructions for the floating-point operations, while R2 has not (FP operations are implemented in the software using several non-FP instructions). Both computers have a clock frequency of 400 MHz. In both we perform the same program, which has the following mixture of commands:

Type of command	% of instructions in program (p1)	CPI	
		R1	R2
FP addition	16%	6	20
FP multiplication	10%	8	32
FP division	8%	10	66
Non-FP-instructions	66%	3	3

Calculate the MIPS for the computers R1 and R2.
b) Calculate the CPU program execution time on the computers R1 and R2, if there are 12000 instructions in the program?
c) At what mixture of instructions in the program will both computers R1 and R2 be equally fast?

Solution:

a) $\text{CPI} = \sum_{i=0}^{3} CPI_i * p_i$

$\text{MIPS} = \frac{f_{CPE}}{CPI*10^6}$

Computer R1:

$$\text{CPI} = \sum_{i=1}^{3} CPI_i * p_i = 0{,}16 * 6 + 0{,}1 * 8 + 0{,}08 * 10 + 0{,}66 * 3 = 4{,}54$$

Computer R1 needs an average of 4.54 clock periods for one instruction

$$\text{MIPS} = \frac{f_{CPE}}{CPI*10^6} = \frac{400*10^6}{4{,}54*10^6} = 88{,}1$$

Computer R1 executes an average of 88 100 000 instructions per second.

Computer R2:

$$\text{CPI} = \sum_{i=1}^{3} CPI_i * p_i = 0{,}16 * 20 + 0{,}1 * 32 + 0{,}08 * 66 + 0{,}66 * 3 = 13{,}66$$

Computer R2 needs an average of 13.66 clock periods for one instruction

$$\text{MIPS} = \frac{f_{CPE}}{\text{CPI}*10^6} = \frac{400*10^6}{13{,}66*10^6} = 29{,}28$$

Computer R2 executes an average of 29 280 000 instructions per second.

- Some examples:
  - We make 10% of a program 90X faster, speedup = 1 / (0.9 + 0.1 / 90) = 1.11
  - We make 90% of a program 10X faster, speedup = 1 / (0.1 + 0.9 / 10) = 5.26
  - We make 25% of a program 25X faster, speedup = 1 / (0.75 + 0.25 / 25) = 1.32
  - We make 50% of a program 20X faster, speedup = 1 / (0.5 + 0.5 / 20) = 1.90
  - We make 90% of a program 50X faster, speedup = 1 / (0.1 + 0.9 / 50) = 8.47

- Suppose we are running a set of programs on a RISC processor, for which the following instruction mix is observed:

Operation	Frequency	CPI_i	$W_i * CPI_i$	% Time
Load	20 %	5	1.00	0.48
Store	8 %	3	0.24	0.12
ALU	60 %	1	0.60	0.29
Branch	12 %	2	0.24	0.11

CPI = 2.08

1 / 2.08

We carry out a design enhancement by which the CPI of Load instructions reduces from 5 to 2. What will be the overall performance improvement?

Fraction enhanced $F = 0.48$

Fraction unaffected $1 - F = 1 - 0.48 = 0.52$

Enhancement factor $S = 5 / 2 = 2.5$

Therefore, speedup is

$$\frac{1}{(1-F) + F/S} = \frac{1}{0.52 + 0.48/2.5} = 1.40$$

- Alternate way of calculation:
  - Old CPI = 2.08
  - New CPI = 0.20 * 2 + 0.08 * 3 + 0.60 * 1 + 0.12 * 2 = 1.48

$$Speedup = \frac{XT_{orig}}{XT_{new}} = \frac{IC * CPI_{old} * C}{IC * CPI_{new} * C} = \frac{CPI_{old}}{CPI_{new}} = \frac{2.08}{1.48} = 1.40$$

- The execution time of a program on a machine is found to be 50 seconds, out of which 42 seconds is consumed by multiply operations. It is required to make the program run 5 times faster. By how much must the speed of the multiplier be improved?
  - Here, F = 42 / 50 = 0.84
  - According to Amadahl's law,

    S = 1 / (0.16 + 0.84 / S)

    or, 0.80 + 4.2 / S = 1

    or, S = 21

- The execution time of a program on a machine is found to be 50 seconds, out of which 42 seconds is consumed by multiply operations. It is required to make the program run 8 times faster. By how much must the speed of the multiplier be improved?
  - Here, $F = 42 / 50 = 0.84$
  - According to Amadahl's law,

    $8 = 1 / (0.16 + 0.84 / S)$

    or, $1.28 + 6.72 / S = 1$

    or, $S = -24$

No amount to speed improvement in the multiplier can achieve this.

Maximum speedup achievable:
$1 / (1 - F) = 6.25$

- Suppose we plan to upgrade the processor of a web server. The CPU is 30 times faster on search queries than the old processor. The old processor is busy with search queries 80% of the time. Estimate the speedup obtained by the upgrade.
  - Here, $F = 0.80$ and $S = 30$
  - Thus, speedup $= 1 / (0.20 + 0.80 / 30) = 4.41$

- The total execution time of a typical program is made up of 60% of CPU time and 40% of I/O time. Which of the following alternatives is better?
  a) Increase the CPU speed by 50%
  b) Reduce the I/O time by half

Assume that there is no overlap between CPU and I/O operations.

CPU	I/O	CPU	I/O	CPU	I/O

- Increase CPU speed by 50%
  - Here, $F = 0.60$ and $S = 1.5$
  - Speedup $= 1 / (0.40 + 0.60 / 1.5) = 1.25$

- Reduce the I/O time by half
  - Here, $F = 0.40$ and $S = 2$
  - Speedup $= 1 / (0.60 + 0.40 / 2) = 1.25$

Thus, both the alternatives result in the same speedup.

- Suppose that a compute-intensive bioinformatics program is running on a given machine X, which takes 10 days to run. The program spends 25% of its time doing integer instructions, and 40% of time doing I/O. Which of the following two alternatives provides a better tradeoff?
  a) Use an optimizing compiler that reduces the number of integer instructions by 30% (assume all integer instructions take the same time).
  b) Optimizing the I/O subsystem that reduces the latency of I/O operations from 10 µsec to 5 µsec (that is, speedup of 2).

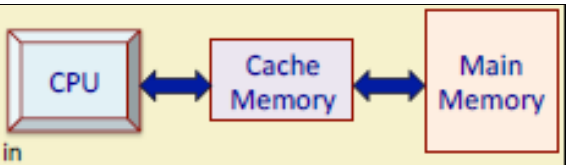
- Alternative (a):
  - Here, F = 0.25 and S = 100 / 70
  - Speedup = 1 / (0.75 + 0.25 * 70 / 100) = 1.08
- Alternative (b):
  - Here, F = 0.40 and S = 2
  - Speedup = 1 / (0.60 + 0.40 / 2) = 1.25

- General expression:
  - Assume m enhancements of fractions $F_1, F_2, \ldots, F_m$ by factors of $S_1, S_2, \ldots, S_m$ respectively.

$$\text{Speedup} = \frac{1}{(1 - \sum_{i=1}^{m} F_i) + \sum_{i=1}^{m} \frac{F_i}{S_i}}$$

Consider an example of memory system.

- Main memory and a fast memory called cache memory.
- Frequently used parts of program/data are kept in cache memory.
- Use of the cache memory speeds up memory accesses by a factor of 8.
- Without the cache, memory operations consume a fraction 0.40 of the total execution time.
- Estimate the speedup.



Solution

$$\text{Speedup} = \frac{1}{(1 - F) + F / S} = \frac{1}{(1 - 0.4) + 0.4 / 8} = 0.91$$

- Now we consider two levels of cache memory, L1-cache and L2-cache.

  Assumptions:
  - Without the cache, memory operations take 30% of execution time.
  - The L1-cache speeds up 80% of memory operations by a factor of 4.
  - The L2-cache speeds up 50% of the remaining 20% memory operations by a factor of 2.

  We want to find out the overall speedup.

- Solution:
  - Memory operations = 0.3
  - $F_{L1} = 0.3 * 0.8 = 0.24$
  - $S_{L1} = 4$
  - $F_{L2} = 0.3 * (1 - 0.8) * 0.5 = 0.03$
  - $S_{L2} = 2$

Speedup

$$\frac{1}{(1 - F_{L1} - F_{L2}) + F_{L1} / S_{L1} + F_{L2} / S_{L2}}$$

$$\frac{1}{(1 - 0.24 - 0.03) + 0.24 / 4 + 0.03 / 2}$$

$$= \mathbf{1.24}$$