Sample questions and solutions

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|  | List the subtasks required to process any basic instruction. |
|  | List the sequence of subtasks required to process ALU instructions of any RISC processor. |
|  | List the sequence of subtasks required to process following LOAD instruction  LOAD R3, M1 |
|  | List the sequence of subtasks required to process following LOAD instruction  LOAD R3, [R1] |
|  | List the sequence of subtasks required to process following LOAD instruction  LOAD R3, 16[R1] |
|  | List the sequence of subtasks required to process following STORE instruction  STORE M1, R3 |
|  | List the sequence of subtasks required to process following STORE instruction  STORE [R1], R3 |
|  | List the sequence of subtasks required to process following STORE instruction  STORE 32[R2], R3 |
|  | List the sequence of subtasks required to process ALU instructions of any CISC processor. |
|  | Show the processing of instructions on a conventional processor architecture. |
|  | What is pipelining? Show the internal architecture of a pipelined architecture. |
|  | What is a buffer? Why it is used in pipeline architecture? |
|  | How does the pipeline architecture process instructions? |
|  | List the differences between a conventional and pipelined architecture. |
|  | What does pipeline improve  Processing time of a single instruction  Processing time of a program  Throughput of a CPU  Explain |
|  | Calculate Average CPI of a pipelined architecture. |
|  | Compare the runtime of CISC and RISC processor for any program. |
|  | Compare addressing modes for ALU instructions of RISC and CISC processors. |
|  | Compare the design of control unit of RISC and CISC processors. |
|  | Compare the size of machine codes of RISC and CISC processors. |
|  | Calculate the speed up factor of a pipeline architecture compared to a conventional architecture. |
|  | List the factors that decide the speed up factor of a pipeline architecture. |
|  | Which of the following design consideration is better  Increasing the number of pipeline stages without reducing clock period  Reducing the clock period without increasing pipeline stages |
|  | How many instructions a pipeline processor can process at the first clock cycle? |
|  | How many instructions a pipeline processor can process when it is full? |