North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 07: Introduction to Multiplexers & 3 to 8 line Decoder

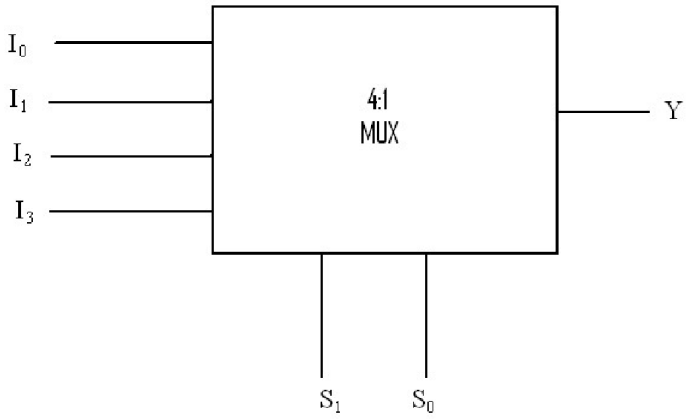
A. Introduction:

Multiplexers have the most important attributions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment the students will have to construct MUX (multiplexers) with simple logic gates.

B. Equipments:

- Trainer board
- IC 7404, IC 7411, IC 7432
- Wires for connection

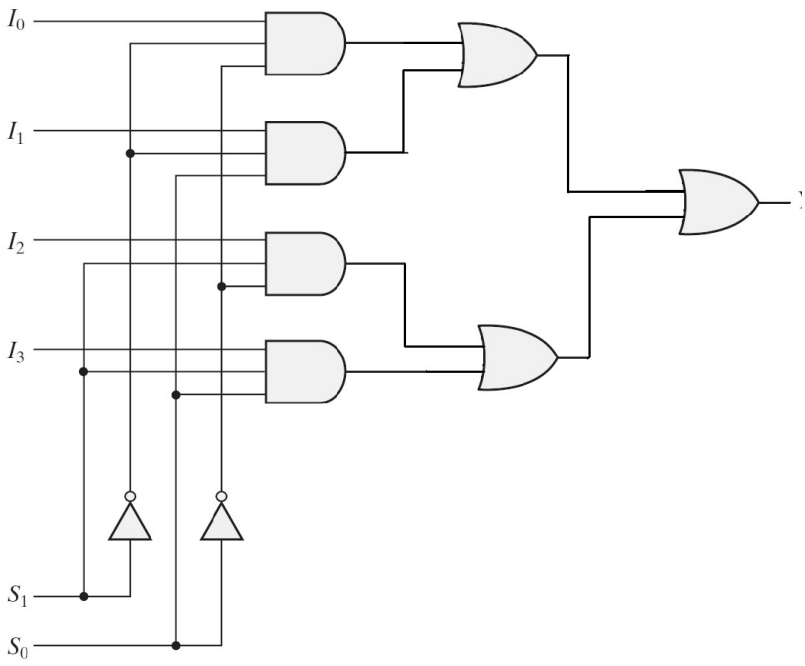
JOB 1:



S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Y= $I_0S_1'S_0'$ + $I_1S_1'S_2$ + $I_2S_1S_2'$ + $I_3S_1S_2$

Circuit diagram:



Implement this function using 4:1 MUX; F (A, B, C) = ∑ (0, 1, 5, 7) [take A as input]

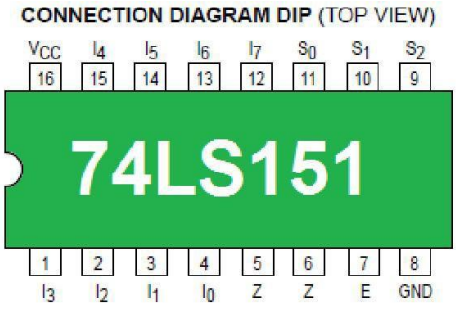
Procedure:

1) Write the truth table for 4:1 MUX.
2) Write the Boolean function for the output logic.
3) Draw the logic diagram to implement the Boolean function.
4) Select the required ICs.
5) Observe and note the output logic for all combination of inputs.

JOB 2:

Implement this function using 8:1 MUX (IC 74151);

F (A, B, C, D) = ∑ (0, 1, 3, 5, 8, 9, 14, 15) [take A as input]



JOB 3:

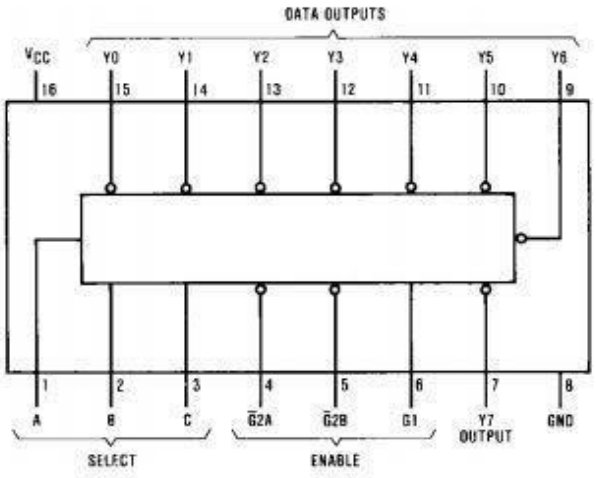
3 to 8 line Decoder:

It uses all AND gates, and therefore, the outputs are active- high. **For active- low outputs, NAND gates are used.** It has 3 input lines and 8 output lines. It is also called as binary to octal decoder it takes a 3-bit binary input code and activates one of the 8(octal) outputs corresponding to that code. The truth table is as follows:

Procedure:

Implement a 3 to 8 line decoder by using IC 74138.

Connection Diagram



Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1: $\overline{G2} = \overline{G2A} + \overline{G2B}$