North South University

Department of Electrical & Computer Engineering

PROJECT REPORT

Course Code: CSE231L

Course Title: Digital Logic Design Lab

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Group Number: 03

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Project Name: Sequential Display of "A5d_2C7"

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Sequential Display of "A5d_2C7" using SOP, JK Flip-Flops, and 555 Timer Clock

Executive Summary

This project focuses on designing a digital logic circuit to sequentially display "**A5d_2C7**" and a blank screen on a seven-segment display. The design integrates key components of digital electronics: combinational logic, sequential circuits, and clock generation. Combinational logic is used to control the seven-segment display segments, optimized using **SOP** expressions and K-maps for efficiency. Sequential logic, implemented with **JK flip-flops**, ensures proper transitions between states corresponding to the desired sequence. A 555 timer IC serves as the clock source to control the timing of these transitions.

The primary goal of the project is to demonstrate the interaction between combinational and sequential elements in practical applications. By focusing on this sequence, the project provides insights into digital circuit design principles, including truth table formulation, K-map simplification, and state diagram creation. Simulation of the circuit validates its functionality and reliability, showcasing its practical implementation.

This project is significant for educational purposes, as it emphasizes the importance of integrating theoretical knowledge with hands-on circuit design. It also highlights the versatility of seven-segment displays and their role in embedded systems and digital electronics. Overall, this work serves as a foundation for further exploration of advanced digital systems and their real-world applications.

Background

Digital circuits are the backbone of modern electronics, forming the core of devices like calculators, digital clocks, and microcontrollers. Among the fundamental concepts in digital electronics are **combinational logic**, which

determines outputs based purely on current inputs, and **sequential logic**, which adds the ability to remember past states and transition between them based on clock signals. Understanding these concepts is essential for developing reliable and efficient digital systems.

The motivation for this project arises from the practical application of these principles in designing systems capable of sequentially controlling outputs, such as displaying **dynamic information** on a seven-segment display. A seven-segment display is a widely used device for visually representing alphanumeric characters. Mastering its control requires a blend of theoretical knowledge and practical skills, such as designing truth tables, minimizing logic using Karnaugh maps (K-maps), and implementing state machines for sequence control.

This project addresses the challenge of sequentially displaying a specific alphanumeric sequence ("A5d_2C7") by combining combinational and sequential logic. The use of **JK flip-flops** for state control and a 555 timer as the clock source provides a robust framework for demonstrating these concepts. The project is not only an exercise in digital circuit design but also an opportunity to enhance skills in simulation, debugging, and practical implementation. It serves as a stepping stone for more complex designs and applications in embedded systems and digital hardware.

Overall Objective of the Project

The primary objective of this project is to design and implement a sequential digital circuit that displays the alphanumeric sequence "A5d_2C7" followed by a blank screen on a seven-segment display. This involves achieving the following specific goals:

1. **Integration of Combinational and Sequential Logic:**
    - Develop **SOP** expressions for controlling the seven-segment display.

- Use K-map optimization to simplify logic and ensure efficient circuit design.

2. **Sequential Control with JK Flip-Flops:**
   - Design a state machine for sequencing the characters "A5d_2C7."
   - Implement **JK flip-flops(7476 ic)** to manage transitions between states.
3. **Clock Signal Generation:**
   - Design and configure a 555 timer IC to provide a consistent clock signal for driving state transitions.
4. **Simulation and Validation:**
   - Simulate the circuit using digital design tools to verify its functionality.
   - Debug and refine the design based on simulation results to ensure correct outputs.
5. **Practical Application of Theoretical Concepts:**
   - Apply principles of truth table formulation, K-map minimization, and state diagram design.
   - Demonstrate how combinational and sequential logic work together in practical electronics.
6. **Educational Purpose:**
   - Provide hands-on experience with digital circuit design and analysis.
   - Prepare for more complex digital system projects by mastering fundamental techniques.

This project showcases the seamless integration of various digital components and highlights the importance of systematic design in electronics.

Work Plan

1. **Requirement Analysis and Design Phase:**
    - Identify the desired alphanumeric sequence ("A5d_2C7") and its display pattern.
    - Design truth tables for each character's seven-segment output.
    - Simplify the truth tables using Karnaugh maps (K-maps) to generate SOP expressions.
2. **Combinational Logic Design:**
    - Use the SOP expressions to design logic circuits for driving the seven-segment display.
    - Implement logic gates to control the individual segments (A-G) of the display.
3. **Sequential Logic Design:**
    - Create a state diagram for transitioning through the sequence of characters and a blank screen.
    - Use JK flip-flops to implement the state machine, designing excitation tables and transition logic.
4. **Clock Circuit Development:**
    - Configure a 555 timer IC to generate a stable clock pulse for state transitions.
    - Set the frequency of the timer to control the display timing.
5. **Simulation and Debugging:**
    - Simulate the circuit in digital design software (Logisim).
    - Test the combinational and sequential components to ensure they work together seamlessly.
6. **Implementation:**
    - Assemble the physical circuit using the designed components.
    - Connect the seven-segment display, flip-flops, and the clock circuit on a breadboard or PCB.
7. **Testing and Validation:**

- Test the circuit functionality in real-time, ensuring proper display of the sequence.
- Debug any issues to refine the circuit for accurate performance.

Required Instruments and Components

1. **Digital Components:**
   - Seven-Segment Display (Common Cathode)
   - JK Flip-Flops (7476 IC)
   - 555 Timer IC
2. **Logic Gates:**
   - AND, OR, NOT gates (or 7400-series ICs)
3. **Supporting Components:**
   - Resistors (1kΩ, 10kΩ)
   - Capacitors (100µF for the 555 timer)
   - LEDs (for debugging and visualization)
4. **Power Supply and Connectivity:**
   - 5V DC Power Supply
   - Breadboard and Jumper Wires
5. **Simulation Tools:**
   - Logisim digital circuit simulation software
6. **Testing Tools:**
   - Multimeter (for checking connections and voltage levels)

This comprehensive work plan and set of tools ensure systematic project development and accurate implementation of the desired sequence.

Combinational Part:

For the combinational part we use this truth table for each character and a blank in "**111 input** " . The truth table , k-map and the simplified boolean expression is given below :

Input			Output						
A	B	C	a	b	c	d	e	f	g
0	0	0	1	1	1	0	1	1	1
0	0	1	1	0	1	1	0	1	1
0	1	0	0	1	1	1	1	0	1
0	1	1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1	0	1
1	0	1	0	0	0	1	1	0	1
1	1	0	1	1	1	0	0	0	0
1	1	1	0	0	0	0	0	0	0

K-Maps:

For output in the "a";

A\BC	00	01	11	10
0	1	1	0	0
1	1	0	0	1

After simplify Boolean Expression for a : A`B`+AC`

For output in the “b”;

A\BC	00	01	11	10
0	1	0	0	1
1	1	0	0	1

After simplify Boolean Expression for b : C`

For output in the “c”;

A\BC	00	01	11	10
0	1	1	0	1
1	0	0	0	1

After simplify Boolean Expression for c : A`B`+BC`

For output in the “d”;

A\BC	00	01	11	10
0	0	1	1	1
1	1	1	0	0

After simplify Boolean Expression for d : A`C+A`B+AB`

For output in the “e”;

A\BC	00	01	11	10
0	1	0	0	1
1	1	1	0	0

After simplify Boolean Expression for e : A`C`+AB`

For output in the “f”;

A\BC	00	01	11	10
0	1	1	0	0
1	0	0	0	0

After simplify Boolean Expression for f : A`B`

For output in the “g”;

A\BC	00	01	11	10
0	1	1	0	1
1	1	1	0	0

After simplify Boolean Expression for g : A`C`+B`

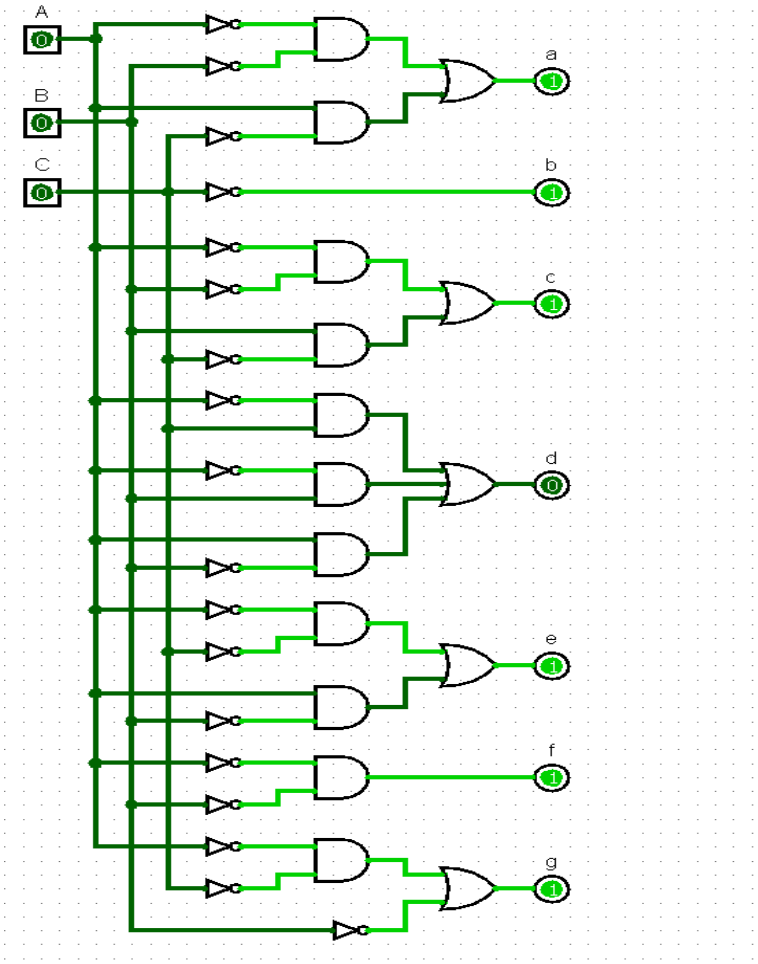

Figure 1: Combinations

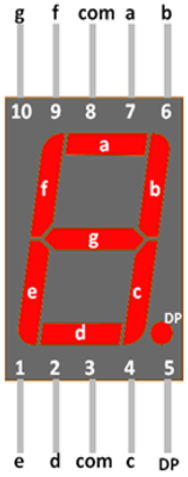

Figure 2: 7 segment display

After combining with the 7 segment display the simulation become this :

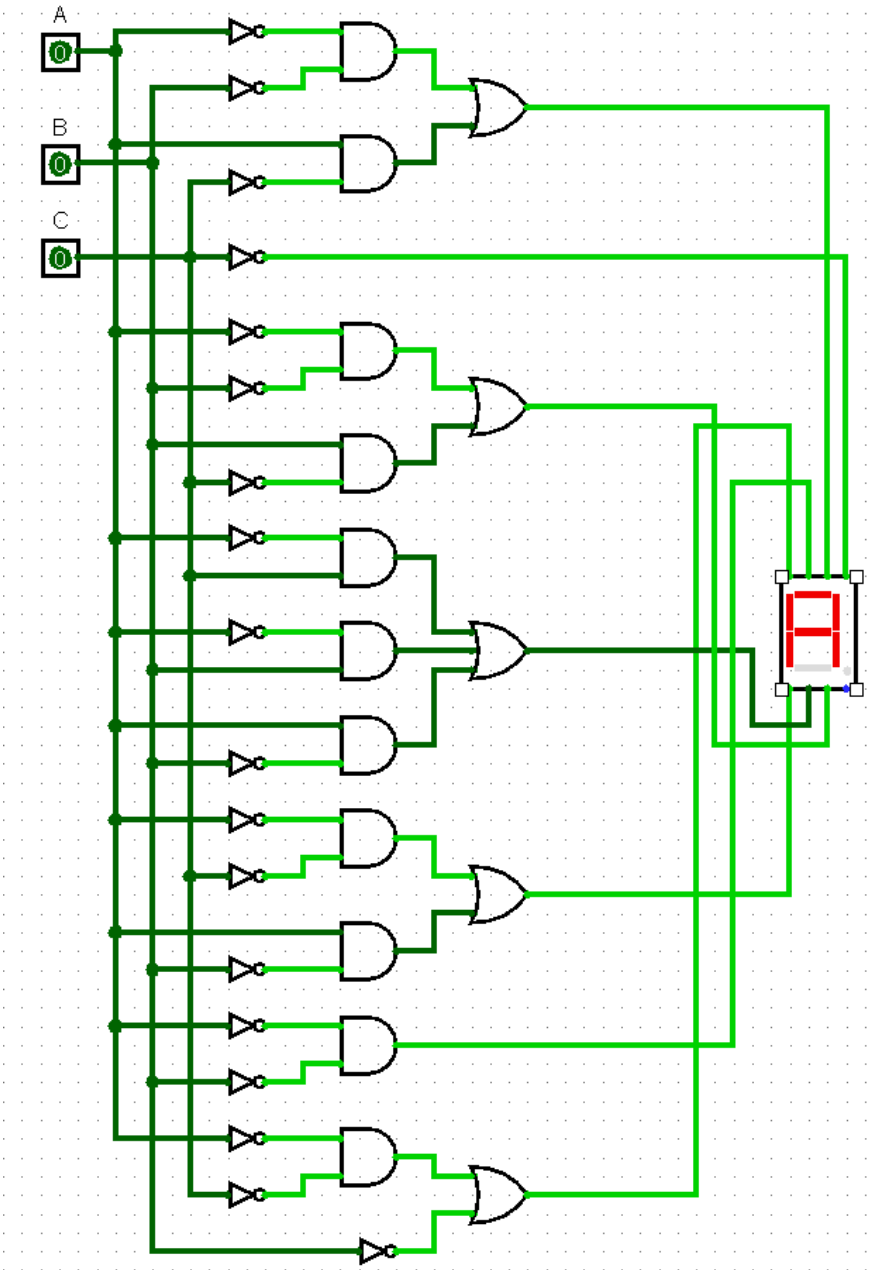

Figure 3: Combinational part connected with the 7 segment display

Sequential Part

The sequential part of the project involves designing a **state machine** to control the transition between the characters "A5d_2C7" and a blank display on a seven-segment output. This is implemented using **JK flip-flops** and 555 timer ic . The JK flip-flops will generate the **sequence** for `A5d_2C7` in binary. The **555 timer** provides the clock signal to trigger state transitions at regular intervals.

Steps for Sequential Logic Design:

Define States: Each character in the sequence ("A," "5," "d," "_","2", "C", "7") is assigned a unique binary state. For example:

1. State 000: "A"
2. State 001: "5"
3. State 010: "d"
4. State 011: "_"
5. State 100: "2"
6. State 101: "C"
7. State 110: "7"
8. State 111: All lights off.

JK Flip-Flop Design

Truth Table for JK Flip-Flop Inputs

Present State (Q2 Q1 Q0)	Next State (Q2+ Q1+ Q0+)	J2	K2	J1	K1	J0	K0
000	001	0	x	1	0	1	0
001	010	0	x	1	0	1	0
010	011	0	x	1	0	1	0

011	100	1	0	0	x	1	0
100	101	1	0	0	x	1	0
101	110	1	0	0	x	1	0
110	111	1	0	0	x	1	0
111	000	0	1	0	1	0	1

Simplified JK Flip-Flop Logic

1. **For Q2**:
   - $J2=Q1 \cdot Q0 J\_2 = Q1 \cdot Q0 J2=Q1 \cdot Q0$
   - $K2=Q2 K\_2 = Q2 K2=Q2$
2. **For Q1**:
   - $J1=Q0 J\_1 = Q0 J1=Q0$
   - $K1=Q1 K\_1 = Q1 K1=Q1$
3. **For Q0**:
   - $J0=Q0' J\_0 = Q0' J0=Q0'$
   - $K0=Q2+Q1 K\_0 = Q2 + Q1 K0=Q2+Q1$

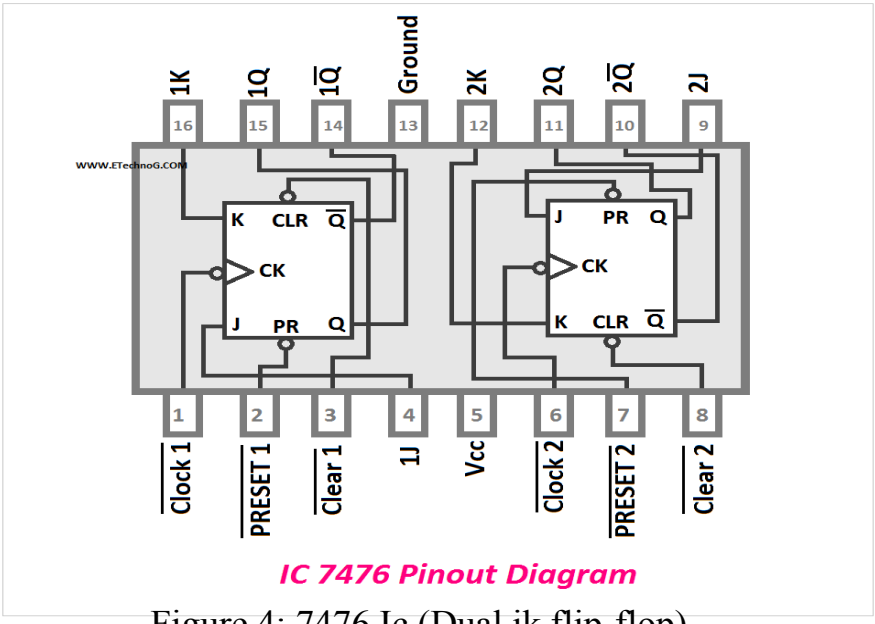

Figure 4: 7476 Ic (Dual jk flip-flop)

Integration with 555 Timer

1. **Clock Signal**:
    - The 555 timer generates clock pulses to trigger transitions between states.
2. **Frequency Adjustment**:
    - We use 100 microF Capacitor to Set the timer to a frequency of .685 Hz for smooth transitions (1.46 second per state).
3. **Connection**:
    - Pin 3 (output of the 555 timer) connects to the **CLK pins** of all JK flip-flops.

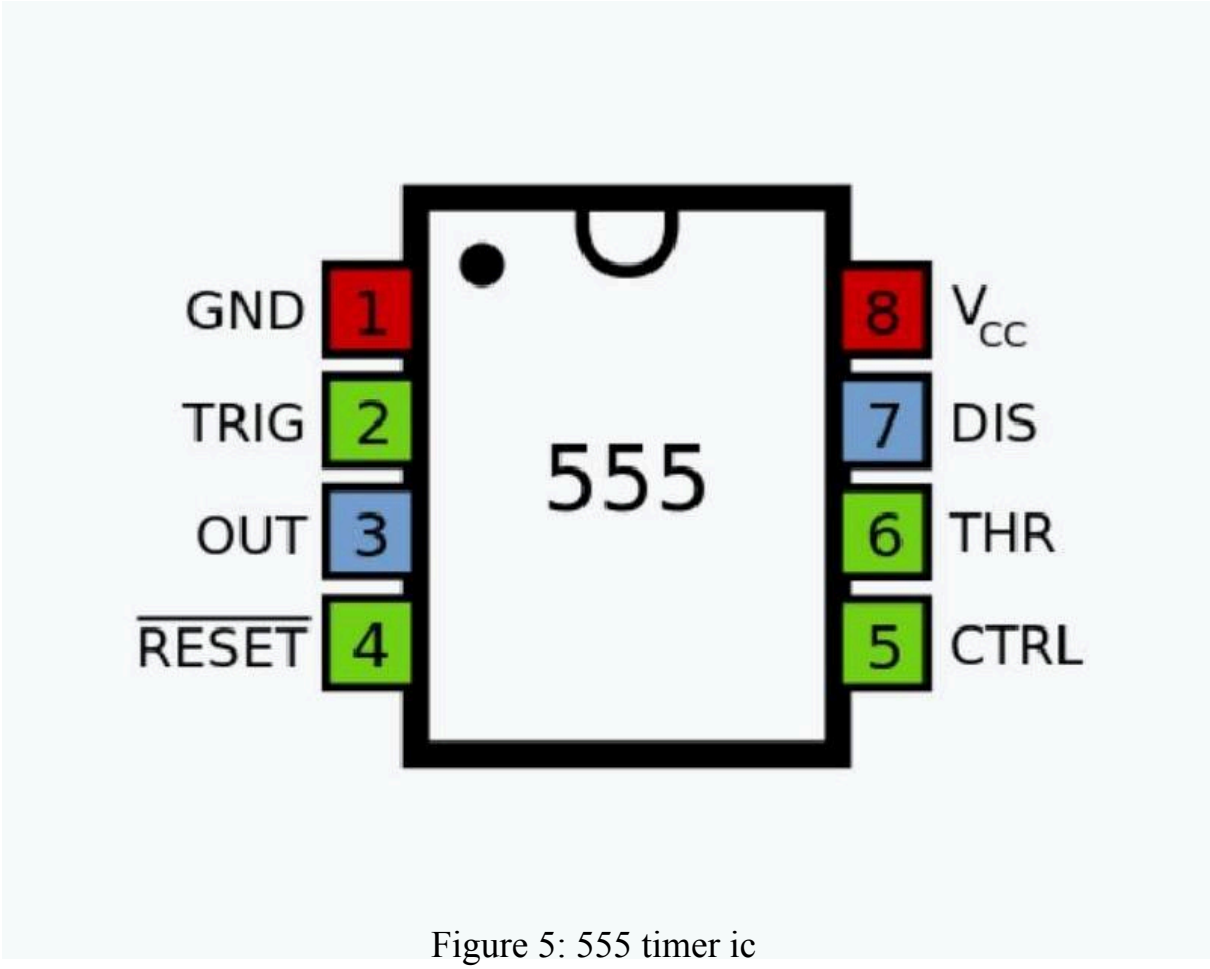

Figure 5: 555 timer ic

Connecting jk flip-flop with the clock counter :

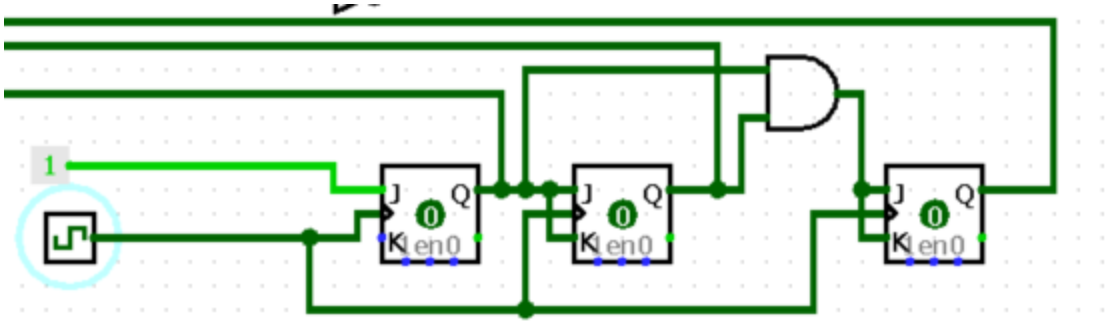

Figure 6: sequential part

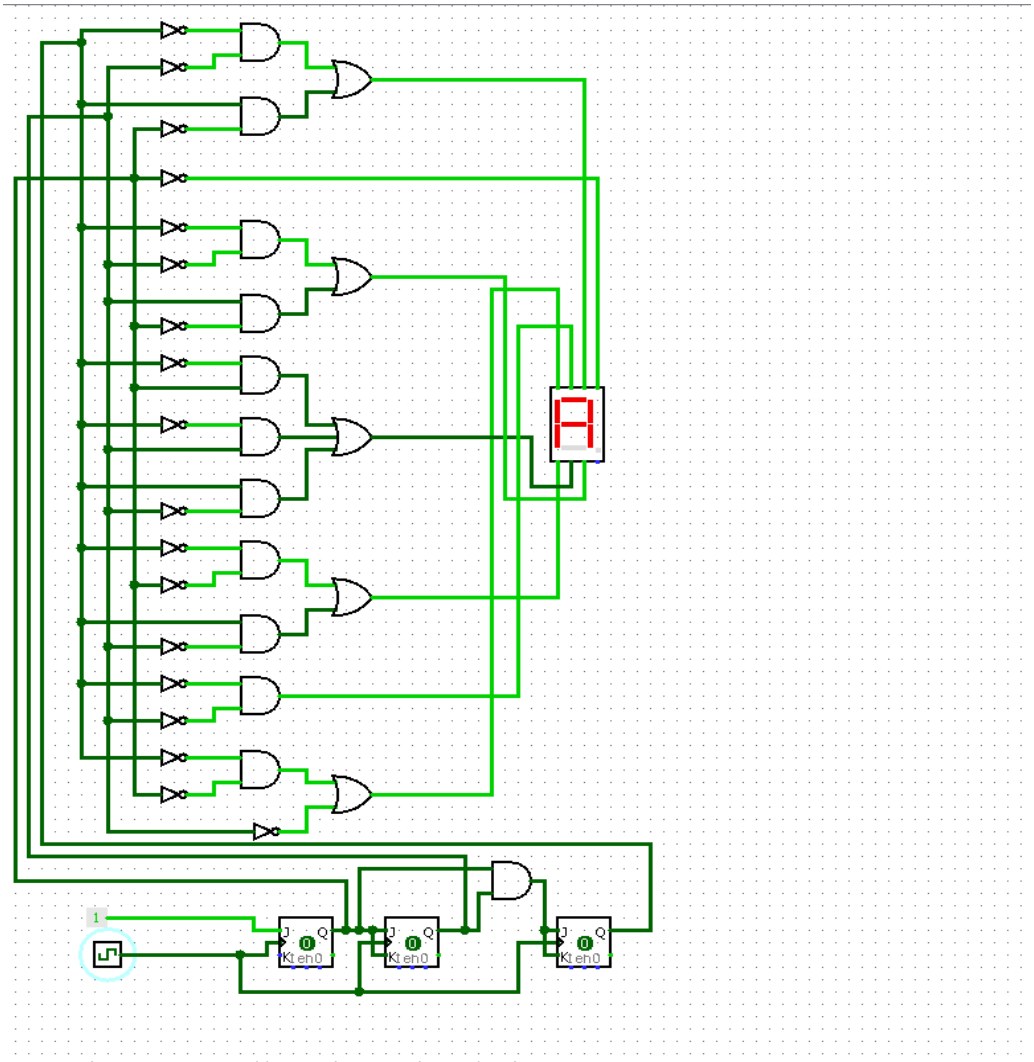

Figure 7: Full project Simulation

A real time Project overview:

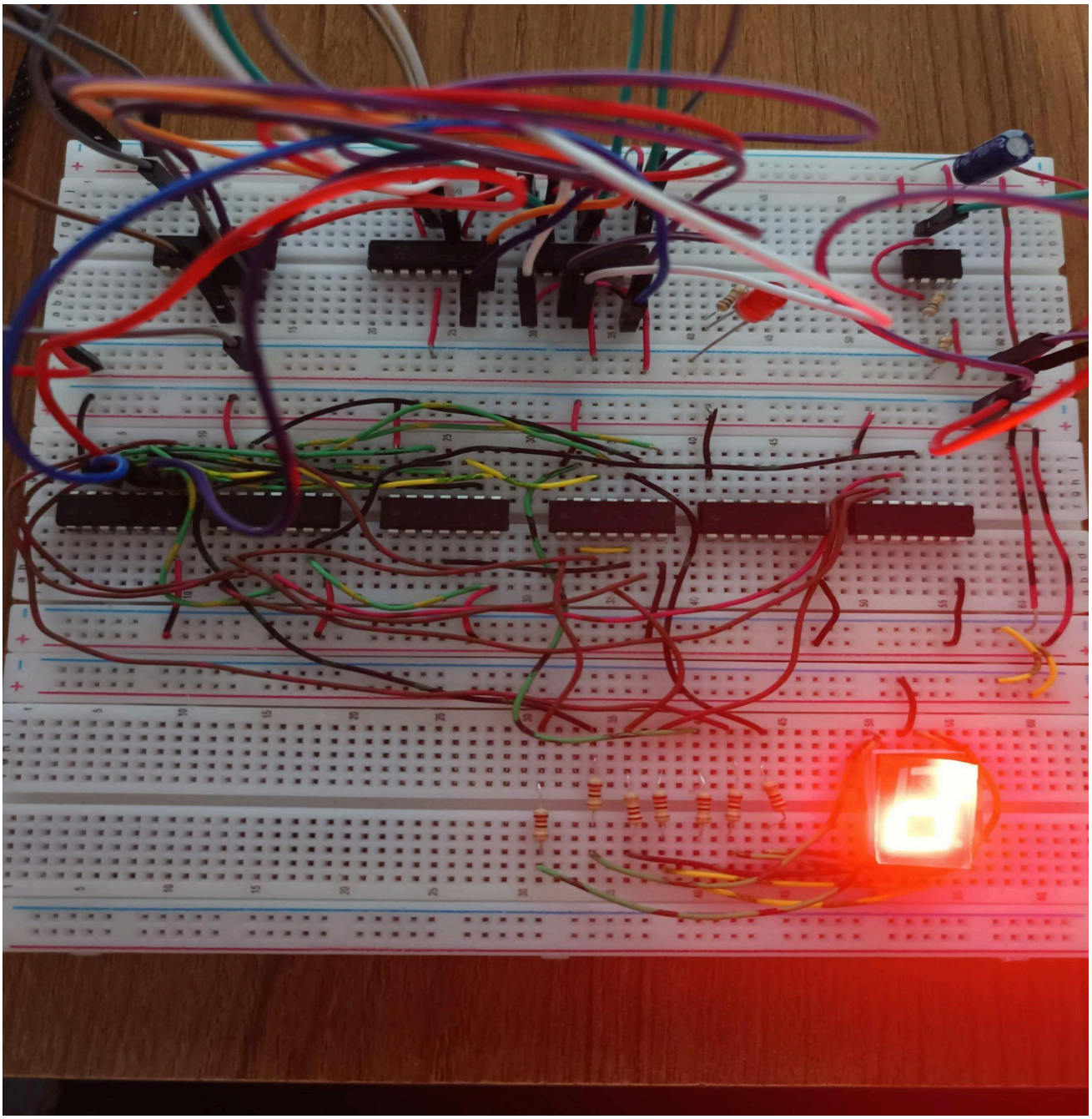

Figure 8: Real time Project overview

Team Roles:

Hossain Ahmmed Taufiq	SOP/K-map optimizations, JK flip-flop design, Project Report,wiring
Al Af Muktadir	Sequential logic,Circuit Building
Fakrul Islam Fahim	simulation,wiring
Sakib Newaz Chowdhury	Clock circuit

Budget List

1. Breadboards - 3 pcs * 120 BDT each = 360 BDT
2. 9V Battery - 1 pc * 100 BDT = 100 BDT
3. Jumper Wires (Strips) - 2 pcs * 120 BDT each = 240 BDT
4. 7476 IC (JK Flip-Flops) - 2 pcs * 40 BDT each = 80 BDT
5. 3-Input OR Gate IC - 1 pc * 35 BDT = 35 BDT
6. 7408 IC (AND Gates) - 3 pcs * 40 BDT each = 120 BDT
7. 7432 IC (OR Gates) - 2 pcs * 40 BDT each = 80 BDT
8. 555 Timer IC - 1 pc * 50 BDT = 50 BDT
9. 100 µF Capacitor - 1 pc * 20 BDT = 20 BDT
10. 220 Ω Resistors - 10 pcs * 5 BDT each = 50 BDT
11. 1 kΩ Resistor - 1 pc * 5 BDT = 5 BDT
12. 10 kΩ Resistor - 1 pc * 5 BDT = 5 BDT
13. LED - 1 pc * 10 BDT = 10 BDT
14. Normal Wires = 50 BDT

Total Budget: 1,205 BDT

Conclusion

This project demonstrates the successful implementation of a digital circuit that combines **sequential and combinational logic** to display the sequence **A5d_2C7**, followed by a blank state and a fully off state, on a seven-segment display. The use of **7476 JK flip-flops** for sequential state transitions and a **555 timer** for generating clock pulses ensured smooth operation and accurate state progression. Combinational logic gates (AND, OR) were used to decode and drive the correct segments for each state.

Key Achievements:

1. **Sequential Logic Implementation**:
    - Successfully designed a sequence controller using JK flip-flops to navigate through eight states, including character displays and an off state.
    - The clock signal generated by the 555 timer maintained precise timing for state transitions.
2. **Combinational Logic Design**:
    - Designed and optimized logic expressions for segment control using AND, OR, and NOT gates.
    - Ensured minimal hardware redundancy while achieving full functionality.
3. **Efficient Hardware Use**:
    - The circuit was built using standard ICs and readily available components, ensuring cost-effectiveness and simplicity.
4. **Scalability**:
    - The modular design allows the circuit to be easily modified for more complex sequences or additional displays.

Challenges and Resolutions:

1. **Timing Issues**: Initial challenges with timing inconsistencies were resolved by carefully selecting resistor and capacitor values for the 555 timer circuit.
2. **Power Management**: Ensured stable operation of all components with proper connections and a reliable 9V battery source.

Lessons Learned:

1. Designing sequential circuits requires careful planning of state diagrams and transitions to avoid errors or undefined states.
2. Simplicity in circuit design can significantly enhance reliability and ease of troubleshooting.
3. Practical implementation reveals potential pitfalls not apparent in theoretical designs, emphasizing the importance of simulation and testing.

This project effectively demonstrates the application of digital logic principles in solving real-world problems and serves as a foundation for more complex digital systems. It has provided invaluable hands-on experience in circuit design, implementation, and troubleshooting, paving the way for further exploration in the field of electronics.