North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 09: Synchronous Sequential Circuits

A. Objective:

To design, build and test synchronous sequential circuits.

B. Equipments:

- IC JK master-slave, T and D flip-flops
- IC type 7408 quad 2-input AND gates
- IC type 7404 NOT gates

Procedure:

1. Synchronous Sequential circuits:

a) Design, construct and test a sequential circuit whose state is shown in Figure.1. Use JK, T and D flip-flops in the design.

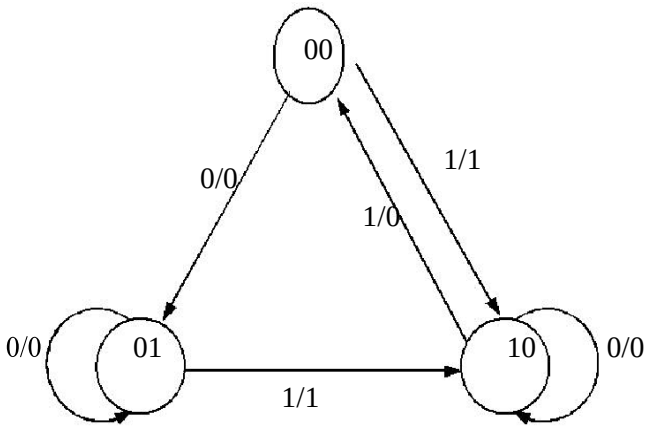

Figure: 1

The circuit has two flip-flops A, B, one input x and one output y. The circuit is to be designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting. If not suggest a solution.

b) Complete the excitation table shown in Table 1

Present state		Input	Next state		Output	Flip-flop input functions			
A	B	X	A	B	Y	JA	KA	JB	KB
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

Table 1. For JK Flip Flop Input Functions

Present state		Input	Next state		Output	Flip-flop input functions	
A	B	X	A	B	Y	DA	DB
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Table 2. For D Flip Flop Input Functions

Present state		Input	Next state		Output	Flip-flop input functions	
A	B	X	A	B	Y	TA	TB
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Table 3. For T Flip Flop Input Function

c) Using Karnaugh maps obtain minimal expressions for the flip-flop input functions JA, KA, JB, KB, DA, DB, TA, TB.

d) Build the circuits and check the output to verify the state table values.

C. Report:

Simulate the circuits using Logisim.