North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 02: Universal Gates

A. Equipments

- Trainer Board
- IC 7400 Quadruple 2-input NAND gates
- IC 7402 Quadruple 2-input NOR gates

B. Procedure

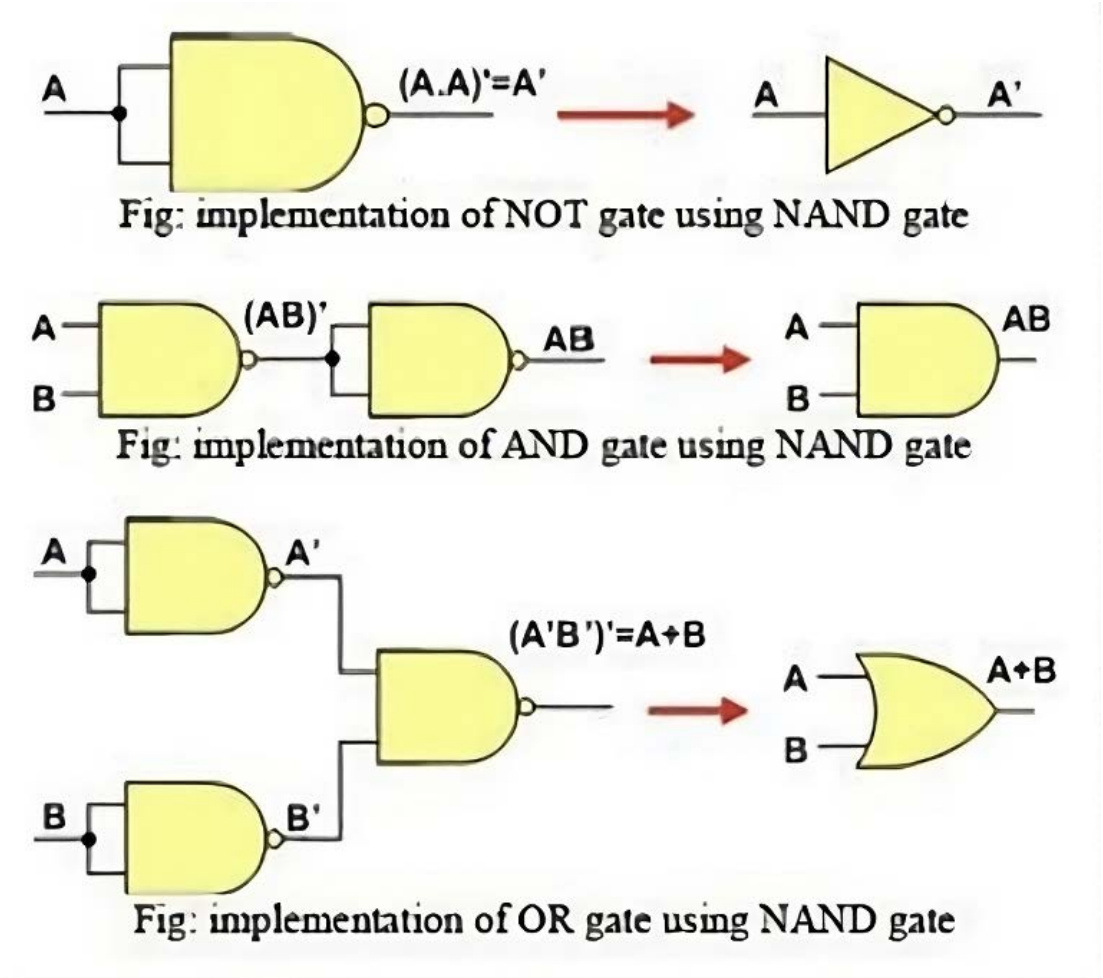

Figure B1: NAND as a universal gate

1. Verify each of the NAND gate equivalent circuits in Figure B1 to perform the same operations of the basic gates.
2. Design, construct and test the implementations of XOR and XNOR gates using NAND gates only. Show the circuits in Figure D1 (Section D), clearly labeling the pin numbers.
3. Design, construct and test the implementations of NOT, AND, OR, XOR and XNOR gates using NOR gates only. Show the circuits in Figure D2 (Section D), clearly labeling the pin numbers.

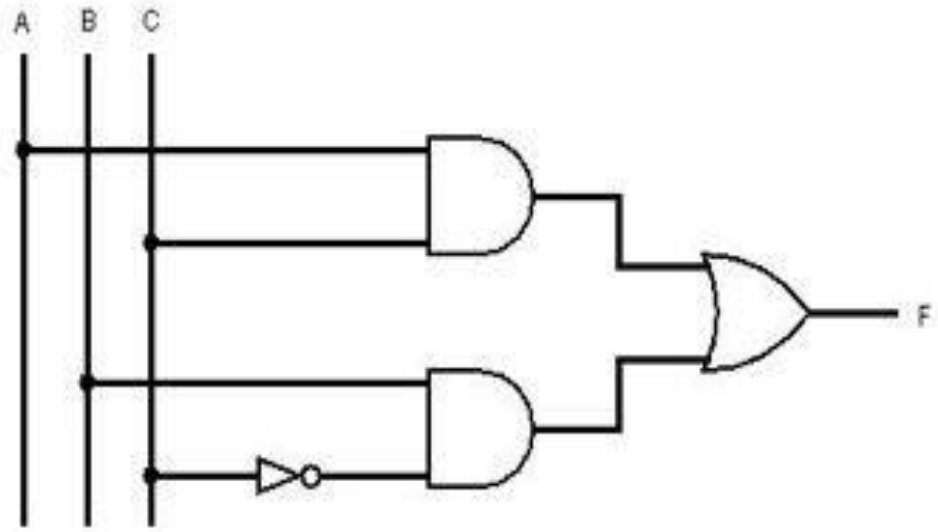

Figure B2: A combinational circuit

4. Complete the truth table for the circuit in Figure B2 in table D1 (Section D)
5. Convert the circuit in Figure B2 to a NAND gate equivalent circuit, showing the steps involved and clearly labeling the pin numbers in the final circuit design. Show your work in Figure D3 (Section D).
   (i) Replace each of the gates with its NAND gate equivalent in step 1.
   (ii) Identify any inversions that are compensated (i.e. one inverter followed by another) in step 1 and redraw the final circuit in step 2.
6. Validate the operation of the universal gate circuit from the truth table.

C. Report

2. Convert the combinational circuit of Figure B2 to a universal gate circuit using NOR gates only and simulate it using Logisim. You will need to convert the circuit to 2nd Canonical form and then minimize it before performing this conversion. Provide the Logisim circuit schematic with your report.

D. Experimental Data

Figure D1: Implementation of XOR and XNOR using NAND gates

NOT	AND	OR
XOR	XNOR	

Figure D2: Implementation of NOT, AND, OR, XOR and XNOR using NOR gates

A B C	$I_1 = A\ C$	$I_2 = B\ C'$	$F = I_1 + I_2$
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

Table D1: Truth table of combinational circuit in Figure B2

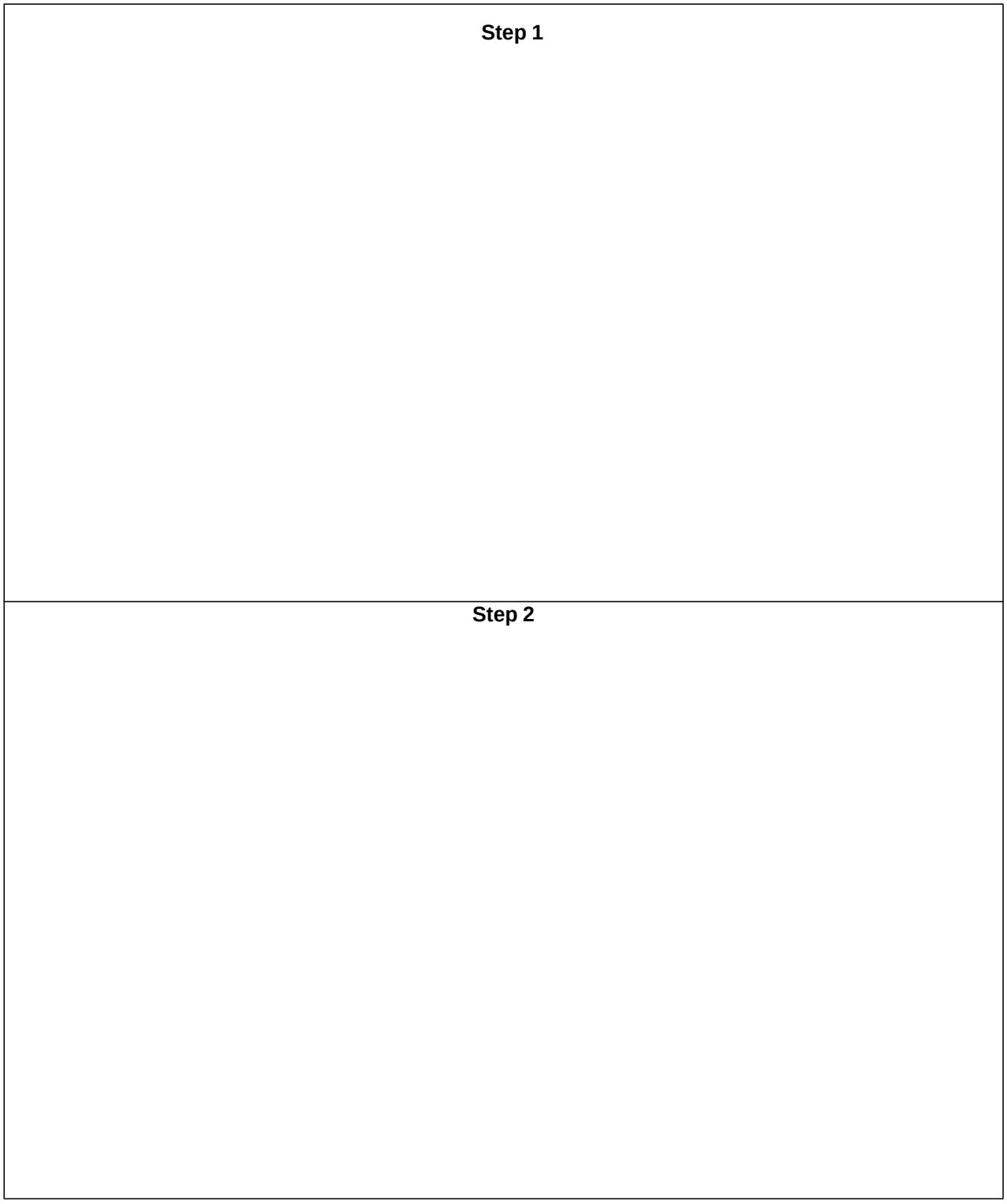

Figure D.3 Universal (NAND) gate implementation of the circuit of Figure B2