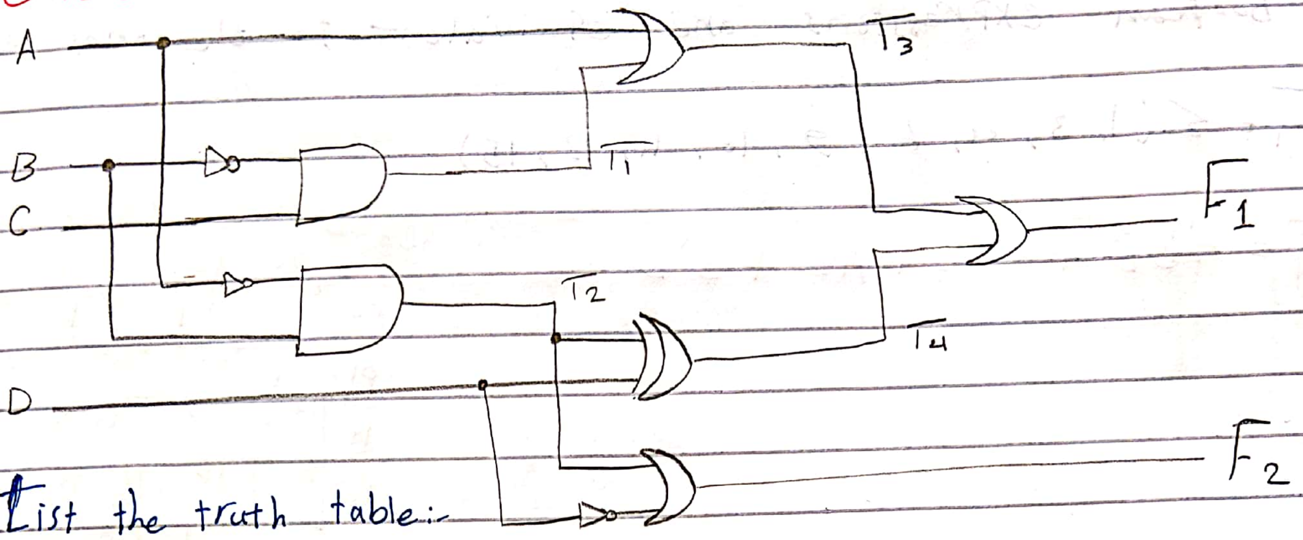
Exercise Five _ P1

1- Consider the following Combinational Circuit:-



(b) List the truth table:-

A	B	C	D	T_1	T_2	T_3	T_4	F_1	F_2
0	0	0	0	0	0	0	0	0	1 0
0	0	0	1	0	0	0	1	1 1	0
0	0	1	0	1	0	0	0	0	1 2
0	0	1	1	1	0	0	1	1 3	0
0	1	0	0	0	1	0	1	1 4	1 4
0	1	0	1	0	1	0	0	0	1 5
0	1	1	0	0	1	0	1	1 6	1 6
0	1	1	1	0	1	0	0	0	1 7
1	0	0	0	0	0	0	0	0	1 8
1	0	0	1	0	0	0	1	1 9	0
1	0	1	0	1	0	1	0	1 10	1 10
1	0	1	1	1	0	1	1	1 11	0
1	1	0	0	0	0	0	0	0	1 12
1	1	0	1	0	0	0	1	1 13	0
1	1	1	0	0	0	0	0	0	1 14
1	1	1	1	0	0	0	1	1 15	0

$T_1 = B'C$

$T_2 = A'B$

$T_3 = A + T_1$
$= A + B'C$

$T_4 = D \oplus T_2$
$= D \oplus A'B$

$F_1 = T_3 + T_4$

$F_2 = D' + T_2$
$= A'B + D'$

Scanned with CamScanner

(C) Plot the output boolean ~~expressions~~ functions obtained in part (b) on maps and show that the simplified boolean expressions are equivalent to the ones ---?

$F_1 = \Sigma(1, 3, 4, 6, 9, 10, 11, 13, 15)$

$F_1 = A'BD' + AB'C + AD + B'D$

AB \ CD	00	01	11	10
00		1	1	
01	1			1
11		1	1	
10		1	1	1

$F_2 = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 12, 14)$

$F_2 = D' + A'B$

$= A'B + D'$ #

AB \ CD	00	01	11	10
00	1			1
01	1	1	1	1
11	1			1
10	1			1

3. For the circuit shown in Fig. 4.26 (Section 4.11)

(a) Write the Boolean functions for the four outputs in terms of the inputs variables.

$Y_0 = A_0 S'E' + B_0 S E'$

$Y_1 = A_1 S'E' + B_1 S E'$

$Y_2 = A_2 S'E' + B_2 S E'$

$Y_3 = A_3 S'E' + B_3 S E'$

4. Design a Combinational circuit with three inputs and one output.

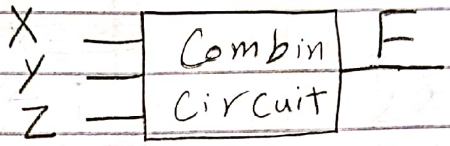
(b) The output is 1 when the binary value of the inputs is an even number?

inputs			output	
X	Y	Z	F	
0	0	0	0	
0	0	1	0	
0	1	0	1	← 2
0	1	1	0	
1	0	0	1	← 4
1	0	1	0	
1	1	0	1	← 6
1	1	1	0	

$F = \Sigma(2,4,6)$

$F = xz' + yz'$

X \ YZ	00	01	11	10
0	0	1	3	2 1
1	4 1	5	7	6 1



6. A majority circuit is combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The outpaut is zero otherwise.

(b) Write and verify a verilog gate-leve model ?

8. Design a Code Converter that Converts a decimal digit from:

(b) The 8, 4, −2, −1 Code to Gray Code?

inputs → a b c d   outputs → w x y z

$\boxed{1}$ Truth Table

D	a	b	c	d		w	x	y	z
0	0	0	0	0	0	0	0	0	0
1	0	1	1	1	7	0	1	0	0
2	0	1	1	0	6	0	1	0	0
3	0	1	0	1	5	0	1	1	1
4	0	1	0	0	4	0	1	1	0
5	1	0	1	1	11	1	1	1	0
6	1	0	1	0	10	1	1	1	1
7	1	0	0	1	9	1	1	0	1
8	1	0	0	0	8	1	1	0	0
9	1	1	1	1	15	1	0	0	0

don't care's $= \Sigma(1,2,3,12,13,14)$

$\boxed{2}$

$W = \Sigma(8,9,10,11,15) + d$

ab \ cd	00	01	11	10
00	^{0}	^{1} X	^{3} X	^{2} X
01	^{4}	^{5}	^{7}	^{6}
11	^{12} X	^{13} X	^{15} 1	^{14} X
10	^{8} 1	^{9} 1	^{11} 1	^{10} 1

$W = a$

$Z = \Sigma(5,9,10) + d$

ab \ cd	00	01	11	10
00	^{0}	^{1} X	^{3} X	^{2} X
01	^{4}	^{5} 1	^{7}	^{6}
11	^{12} X	^{13} X	^{15}	^{14} X
10	^{8}	^{9} 1	^{11}	^{10} 1

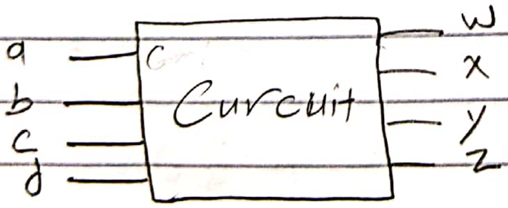
$Z = acd' + c'd$

$X = \Sigma(4,5,6,7,8,9,10,11,15) + d$

ab \ cd	00	01	11	10
00	^{0}	^{1} X	^{3} X	^{2} X
01	^{4} 1	^{5} 1	^{7} 1	^{6} 1
11	^{12} X	^{13} X	^{15} 1	^{14} X
10	^{8} 1	^{9} 1	^{11} 1	^{10} 1

$X = b + a$

Block diagram



$Y = \Sigma(4,5,10,11) + d$

ab \ cd	00	01	11	10
00	^{0}	^{1} X	^{3} X	^{2} X
01	^{4} 1	^{5} 1	^{7}	^{6}
11	^{12} X	^{13} X	^{15}	^{14} X
10	^{8}	^{9}	^{11} 1	^{10} 1

$Y = bc' + b'c$
$= b \oplus c$

9 An ABCD-to-seven-segment decoder — converts ~~a digital~~ decimal digit in BCD to an appropriate code .....

The seven outputs of decoder (a, b, c, d, e, f, g)

1- Using Truth table.

2- K_map.

3- To design the BCD-to-seven-segment decoder using a minimum number of gates.

Dec	inputs A	B	C	D	outputs a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

$d = \Sigma(10, 11, 12, 13, 14, 15)$

$a = \Sigma(0, 2, 3, 5, 6, 7, 8, 9) + d$

AB \ CD	00	01	11	10
00	1		1	1
01		1	1	1
11	X	X	X	X
10	1	1	X	X

$a = C + BD + AB' + B'D'$

$= AB' + \underbrace{BD + B'D'}_{(B \oplus D)'} + C$

$b = \Sigma(0, 1, 2, 3, 4, \cancel{5}, 8, 9) + d$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1		1	
11	X	X	X	X
10	1		X	X

$b = A'B' + \underbrace{C'D' + CD}_{(C \oplus D)'}$

$C = \Sigma(0, 1, 3, 4, 5, 6, 7, 8, 9) + d$

AB \ CD	00	01	11	10
00	1	1	1	
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$C = C' + D + B + A$

$= A + B + D + C'$

$d = \Sigma(0, 2, 3, 5, 6, 8, 9) + d$

AB \ CD	00	01	11	10
00	1		1	1
01		1		1
11	X	X	X	X
10	1	1	X	X

$d = BC'D + A + CD' + B'D'$

$= A + BC'D + CD' + B'D'$

Scanned with CamScanner

$e = \Sigma(0,2,6,8) + d$

AB \ CD	00	01	11	10
00	[0] 1	[1]	[3]	[2] 1
01	[4]	[5]	[7]	[6] 1
11	[12] X	[13] X	[15] X	[14] X
10	[8] 1	[9]	[11] X	[10] X

$e = B'D' + CD'$

$f = \Sigma(0,4,5,6,8,9) + d$

AB \ CD	00	01	11	10
00	[0] 1	[1]	[3]	[2]
01	[4] 1	[5] 1	[7]	[6] 1
11	[12] X	[13] X	[15] X	[14] X
10	[8] 1	[9] 1	[11] X	[10] X

$f = BD' + BC' + C'D' + A$

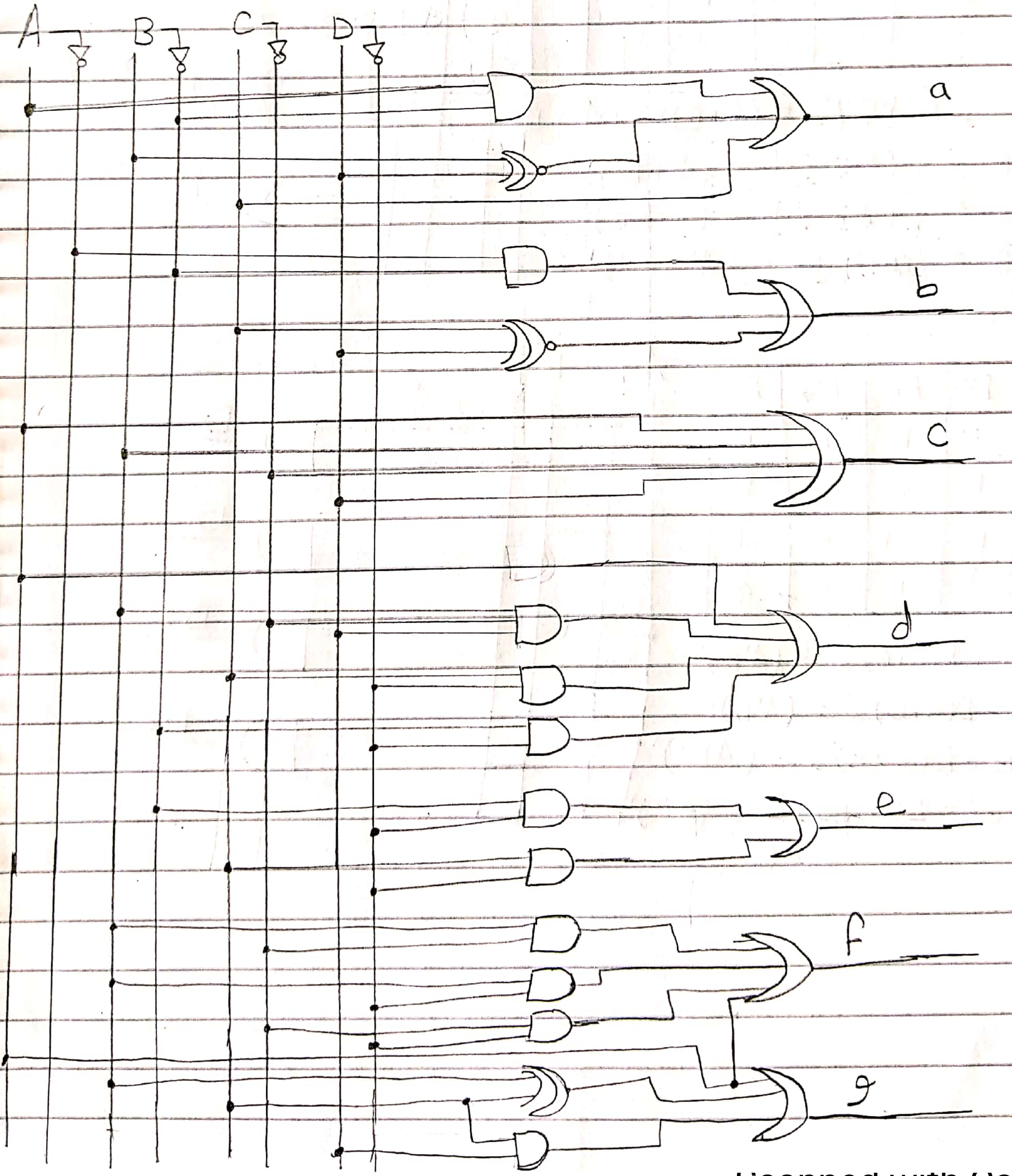
$= A + BC' + BD' + C'D'$

$g = \Sigma(2,3,4,5,6,8,9) + d$

AB \ CD	00	01	11	10
00	[0]	[1]	[3] 1	[2] 1
01	[4] 1	[5] 1	[7]	[6] 1
11	[12] X	[13] X	[15] X	[14] X
10	[8] 1	[9] 1	[11] X	[10] X

$g = BC' + A + B'C + CD$

$= A + \underbrace{B'C + BC'}_{(B \oplus C)} + CD$



11- Using four half-adders:

(b) Design a four-bit Combinational decrementer ?

a_3	a_2	a_1	a_0	
1	1	1	1	+

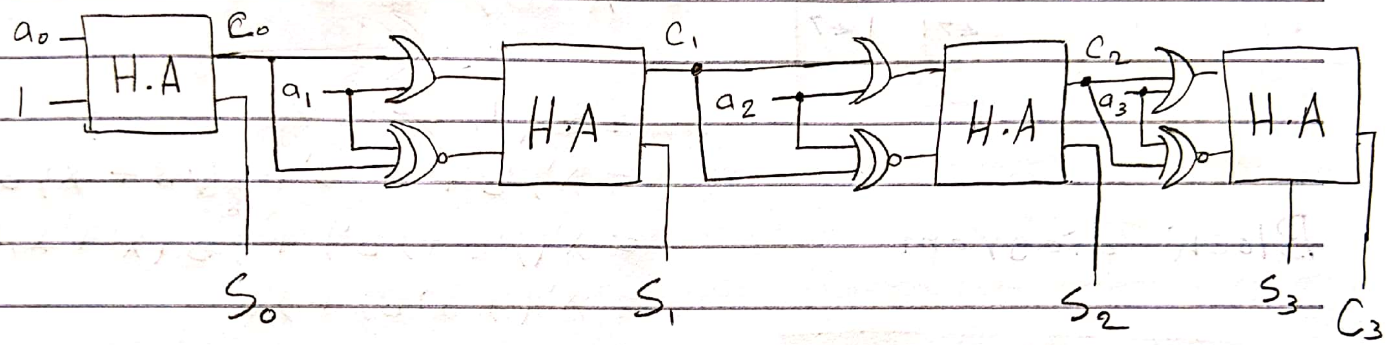
C_3 S_3 S_2 S_1 S_0

a_0	C_0	1	A	B
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

$A = a + C$

$B = a'c' + aC$

$= (a \oplus C)'$

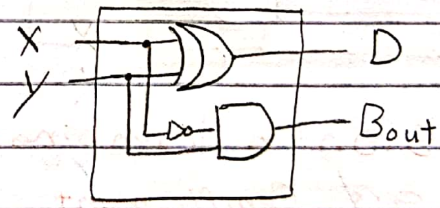


12- Design a ~~half~~ full-subtractor ciruit ~~wi~~ with inputs X and Y and outputs Diff & B_{out} :-

X	Y	D	B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$D = X'Y + XY' = X \oplus Y$

$B_{out} = X'Y$



(b) Design a full-Subtractor Circuit with inputs X, Y B_{in} and ~~out~~ two outputs Diff and B_{out}.

Scanned with CamScanner

Truth table

X	y	Bin	Diff	Bout
0	0	0	0	0
0	0	1	1 ←1	1 ←1
0	1	0	1 ←2	1 ←2
0	1	1	0	1 ←3
1	0	0	1 ←4	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1 ←7	1 ←7

Functions

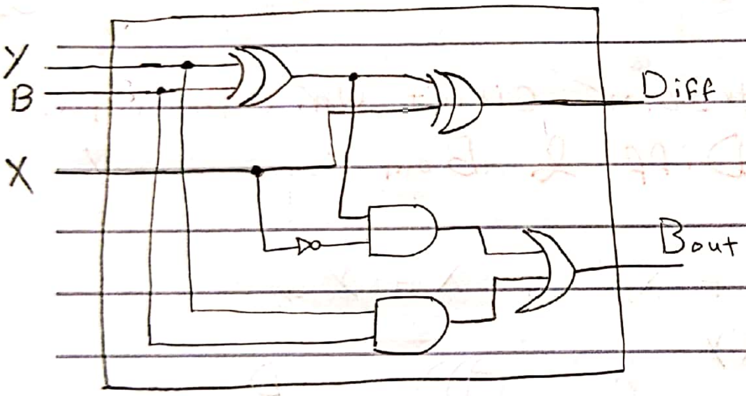
$Diff = \Sigma(1, 2, 4, 7)$

X \ yB	00	01	11	10
0		1		1
1	1		1	

$$Diff = Xy'B' + X'y'B + XyB + X'yB'$$
$$= y'(XB' + X'B) + y(XB + X'B')$$
$$= y'(X \oplus B) + y\overline{(X \oplus B)}$$
$$= X \oplus y \oplus B$$

$$B_{out} = \Sigma(1, 2, 3, 7)$$
$$= X'y'B + X'yB' + X'yB + XyB$$
$$= X'(y'B + yB') + yB(X' + X)$$
$$= X'(y \oplus B) + yB$$

Block diagram



18- Design a Combinational Circuit that generates the 9's Complement of (a) BCD digit

Dec	BCD	9's Complement
0	0001	→ 8
1	0010	→ 7
2	0011	→ 6
3	0100	→ 5
4	0101	→ 4
5	0110	→ 3
6	0111	→ 2
7	1000	→ 1
8	1001	→ 0
9		

18- Design a Combinational Circuit that generates the 9's Compl of a (a) BCD digit

Dec	BCD	9's Compl
0	0000	1001
1	0001	1000
2	0010	0111
3	0011	0110
4	0100	0101
5	0101	0100
6	0110	0011
7	0111	0010
8	1000	0001
9	1001	0000

(w, x, y, z)

$F_1 = \Sigma(0,1) + d = \Sigma(10,11,12,13,14,15)$

wx \ yz	00	01	11	10
00	1	1		
01				
11	X	X	X	X
10			X	X

$F_0 = w'x'y'$

$F_2 = \Sigma(2,3,4,5) + d$

wx \ yz	00	01	11	10
00			1	1
01	1	1		
11	X	X	X	X
10			X	X

$F_1 = xy' + x'y$
$= x \oplus y$

$F_3 = \Sigma(2,3,6,7) + d$

wx \ yz	00	01	11	10
00			1	1
01			1	1
11	X	X	X	X
10			X	X

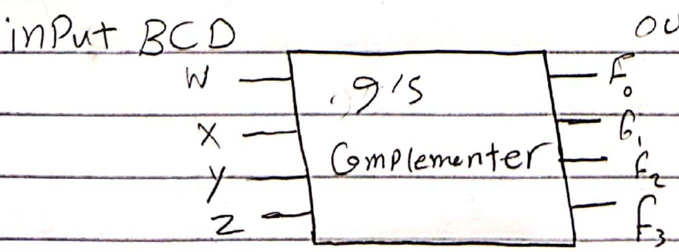
$F_2 = y$

$F_4 = \Sigma(0,2,4,6,8) + d$

wx \ yz	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1		X	X

$F_3 = z'$

Combinational Circuit



21. Design a Combinational Circuit that Compares two 4-bit numbers to check if they are equal.

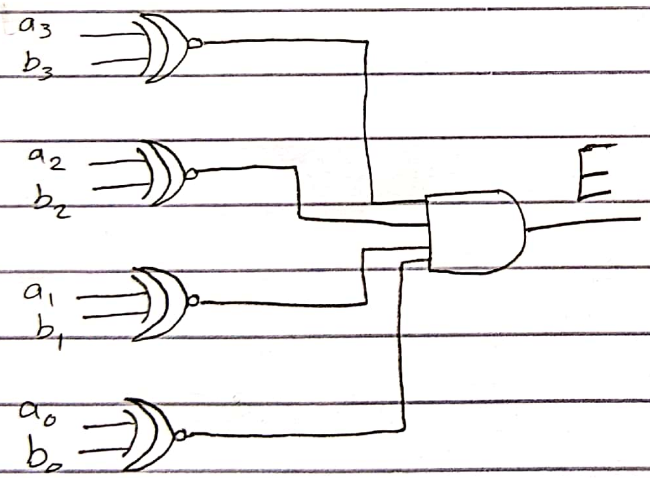
Output = 1 if the two numbers are equal
= 0 otherwise.

1st no ⇒ A a_3 a_2 a_1 a_0
2nd no ⇒ B b_3 b_2 b_1 b_0

Truth Table of 2-bit Com

a_3	b_3	Equal
0	0	1
0	1	0
1	0	0
1	1	1

$E = a_3' b_3' + a_3 b_3$
$= (a_3 \oplus b_3)'$



Scanned with CamScanner