Exercise Five-P2

**4.23** Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NAND

gates only. Include an enable input.

**4.24** Design a BCD-to-decimal decoder using the unused combinations of the BCD code as

don’t-care conditions.

**4.25** Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components.

**4.26** Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.

**4.27** A combinational circuit is specified by the following three Boolean functions:

*F*1(*A*, *B*, *C*) = Σ(1, 4, 6)

*F*21*A*, *B*, *C*2 = Σ(3, 5)

*F*3(*A*, *B*, *C*) = Σ(2, 4, 6, 7)

Implement the circuit with a decoder constructed with NAND gates (similar to Fig. 4.19 )

and NAND or AND gates connected to the decoder outputs. Use a block diagram for the

decoder. Minimize the number of inputs in the external gates.

**4.28** Using a decoder and external gates, design the combinational circuit defined by the

following three Boolean functions:

(a) *F*1 = *x*’*yz*’ + *xz* (b) *F*1 = (*y*’+ *x*)*z*

*F*2 = *xy*’*z*’ + *x*’*y F*2 = *y*’*z*’ + *x*’*y* + *yz*’

*F*3 = *x*’*y*’*z*’ + *xy F*3 = (*x* + *y)z*

**4.31** Construct a 16 X 1 multiplexer with two 8 X1 and one 2 X1 multiplexers. Use block diagrams.

**4.32** Implement the following Boolean function with a multiplexer:

(a) *F*(*A*, *B*, *C*, *D*) = Σm(0, 2, 5, 8, 10, 14)

(b) *F*(*A*, *B*, *C*, *D*) =Π M(2, 6, 11)

**4.33** Implement a full adder with two 4 X 1 multiplexers.

**4.34** An 8 X 1 multiplexer has inputs *A* , *B* , and *C* connected to the selection inputs *S*2 , *S*1 , and

*S*0 , respectively. The data inputs *I* 0 through *I*7 are as follows:

(a)*I* 1 =*I* 2 = *I* 7 =0; *I* 3 = *I* 5= 1; *I* 0 = *I* 4 = *D* ; and *I* 6 = *D* ’.

(b) *I* 1 =*I* 2 = 0; *I* 3 = *I* 7 = 1; *I* 4 = *I* 5 = *D* ; and *I* 0 =*I* 6 = *D* ’.

Determine the Boolean function that the multiplexer implements.