**Exercise Six**

**5.1** The following *D* latch of is constructed with NOR gates for the *SR* latch part and two AND gates for the control select and an inverter. Consider the following three other ways for obtaining a *D* latch. In each case, draw the logic diagram and verify the circuit operation.

(a) Use four NAND gates and an inverter.

(b) Use NOR gates for all four gates. Inverters may be needed.

(c) Use four NAND gates only (without an inverter). This can be done by connecting

the output of the upper gate in Fig. 5.6 (the gate that goes to the *SR* latch) to the input

of the lower gate (instead of the inverter output).

**5.2** Construct a *JK* flip-flop using a *D* flip-flop, a two-to-one-line multiplexer, and an inverter.

**5.3** Show that the characteristic equation for the complement output of a *JK* flip-flop is

*Q* ’\* = *J* ‘*Q* ‘ + *KQ*

**5.4** A *PN* flip-flop has four operations: clear to 0, no change, complement, and set to 1, when

inputs *P* and *N* are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.

(b) **\*** Derive the characteristic equation.

(c) Tabulate the excitation table.

(d) Show how the *PN* flip-flop can be converted to a *D* flip-flop.

**5.5** Explain the differences among a truth table, a state table, a characteristic table, and an

excitation table. Also, explain the difference among a Boolean equation, a state equation,

a characteristic equation, and a flip-flop input equation.

**5.6** A sequential circuit with two *D* flip-flops *A* and *B*, two inputs, *x* and *y*; and one output *z*

is specified by the following next-state and output equations:

***A*\*= *xy*’ + *xB***

***B\** = *xA* + *xB*’**

***z* = *A***

(a) Draw the logic diagram of the circuit.

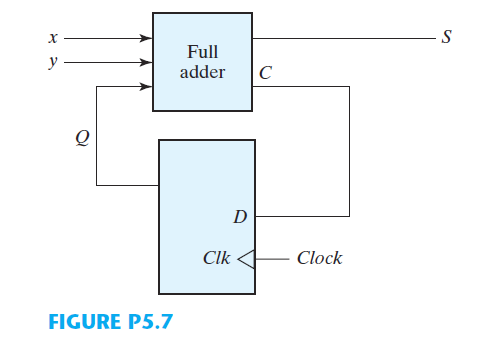
(b) List the state table for the sequential circuit.

(c) Draw the corresponding state diagram.

**5.7** A sequential circuit has one flip-flop *Q*, two inputs *x* and *y*, and one output *S*. It consists

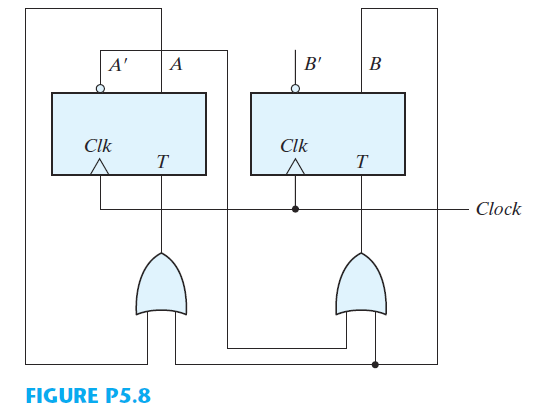
of a full-adder circuit connected to a *D* flip-flop, as shown in Fig. P5.7 . Derive the state

table and state diagram of the sequential circuit.



**5.8** Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8 .

Explain the function that the circuit performs.

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**5.9** A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x*. The circuit is described

by the following flip-flop input equations:

*JA* = *x KA* = *B*

*JB* = *x KB* = *A*’

(a) Derive the state equations *A\** and *B\** by substituting the input equations for the *J* and *K* variables.

(b) Draw the state diagram of the circuit.

**5.10** A sequential circuit has two *JK* flip-flops *A* and *B*, two inputs *x* and *y,* and one output *z* .

The flip-flop input equations and circuit output equation are

*JA* = *Bx* + *B* ‘*y*’ , *KA* = *B* ‘*xy*’

*JB* = *A*’*x , KB* = *A* + *xy*’

*z* = *Ax*’*y*’ + *Bx*’*y*’

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table.

(c) Derive the state equations for *A* and *B*.

**5.15** List a state table for the *JK* flip-flop using *Q* as the present and next state and *J* and *K* as

inputs. Design the sequential circuit specified by the state table and show that it is equivalent

to Fig. 5.12 (a).