Optimizing HW/SW Partition of a Complex Embedded Systems

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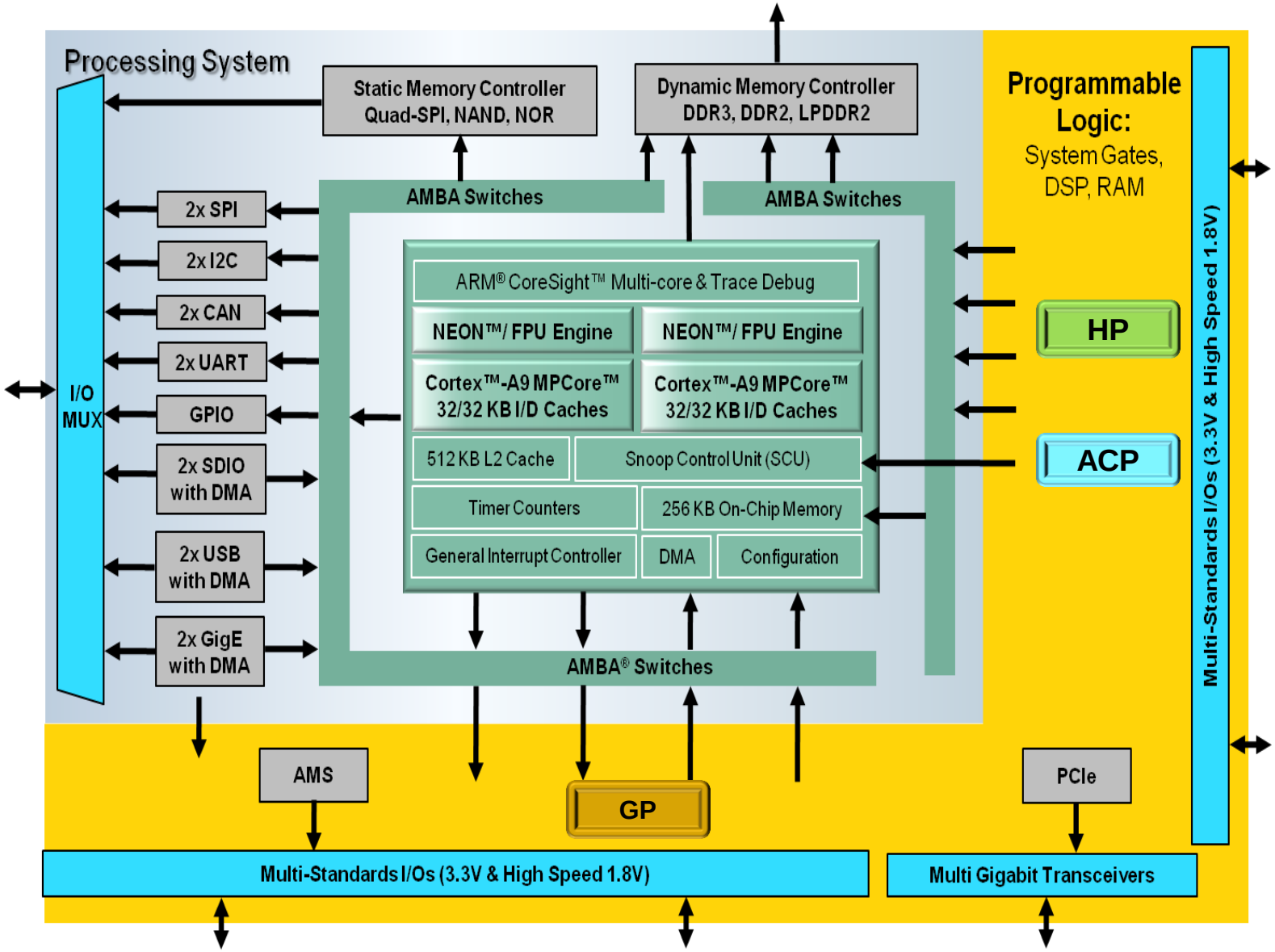
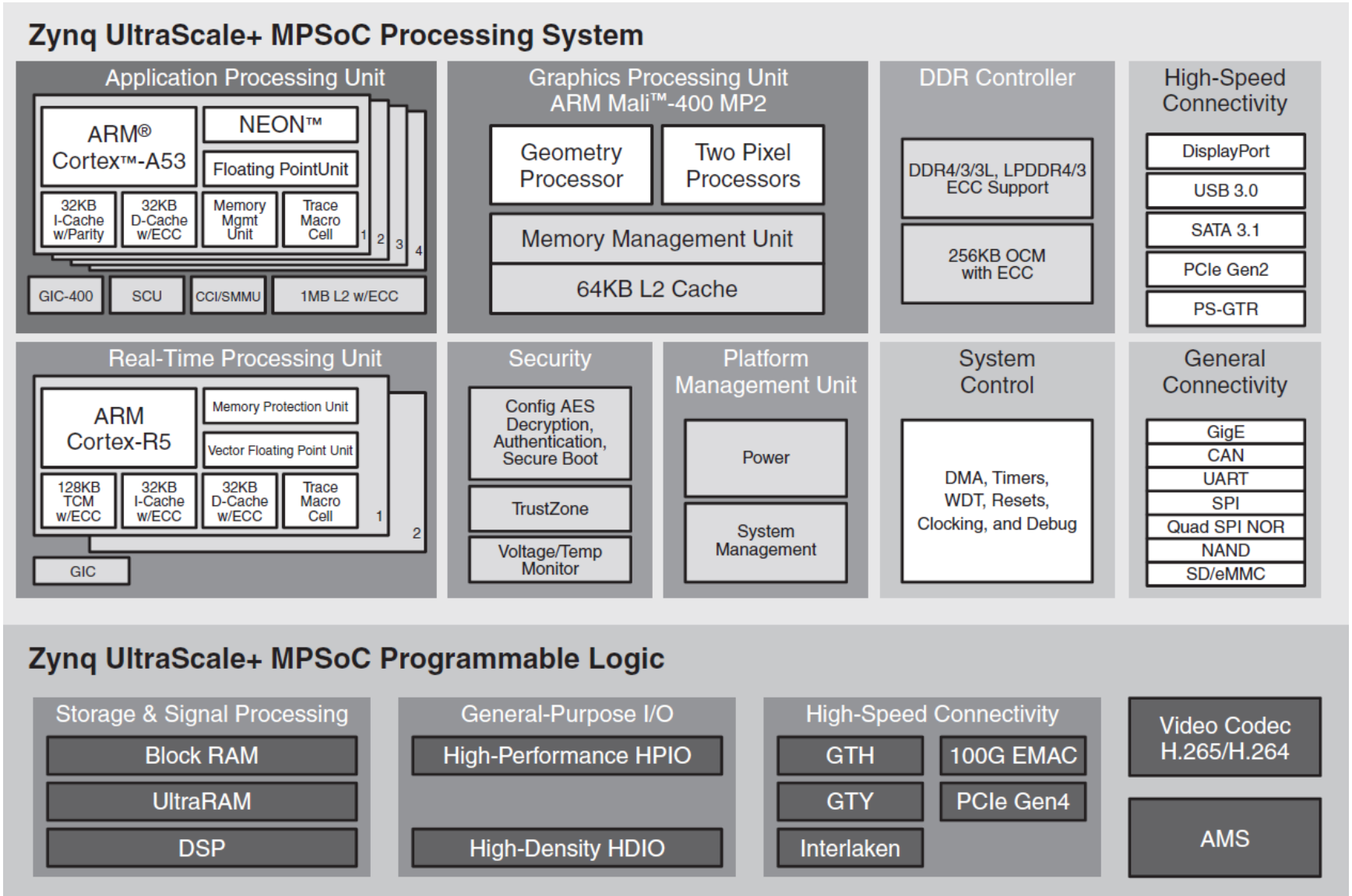
SDSoC™ Environment

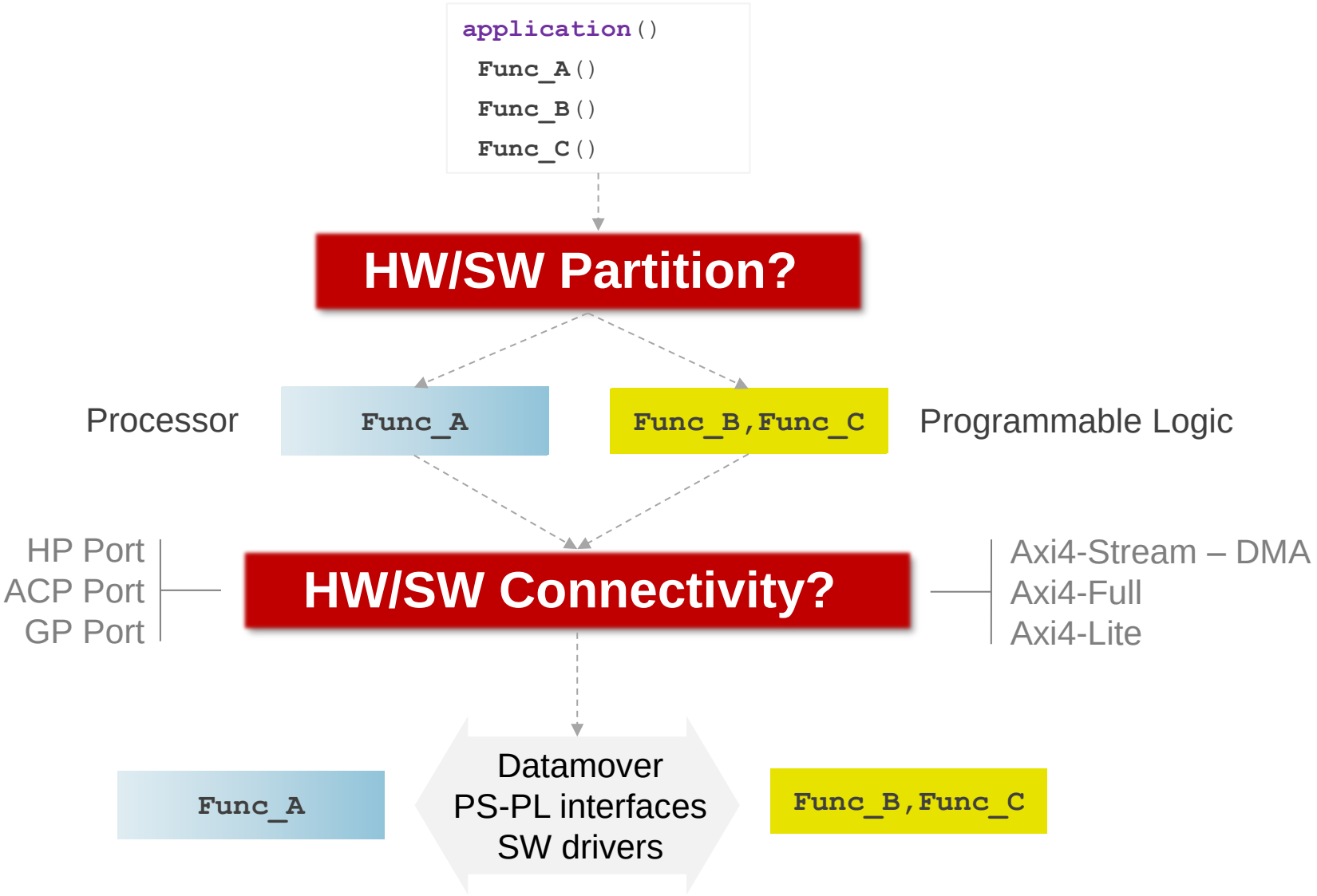
Zynq-7000 All Programmable SoC



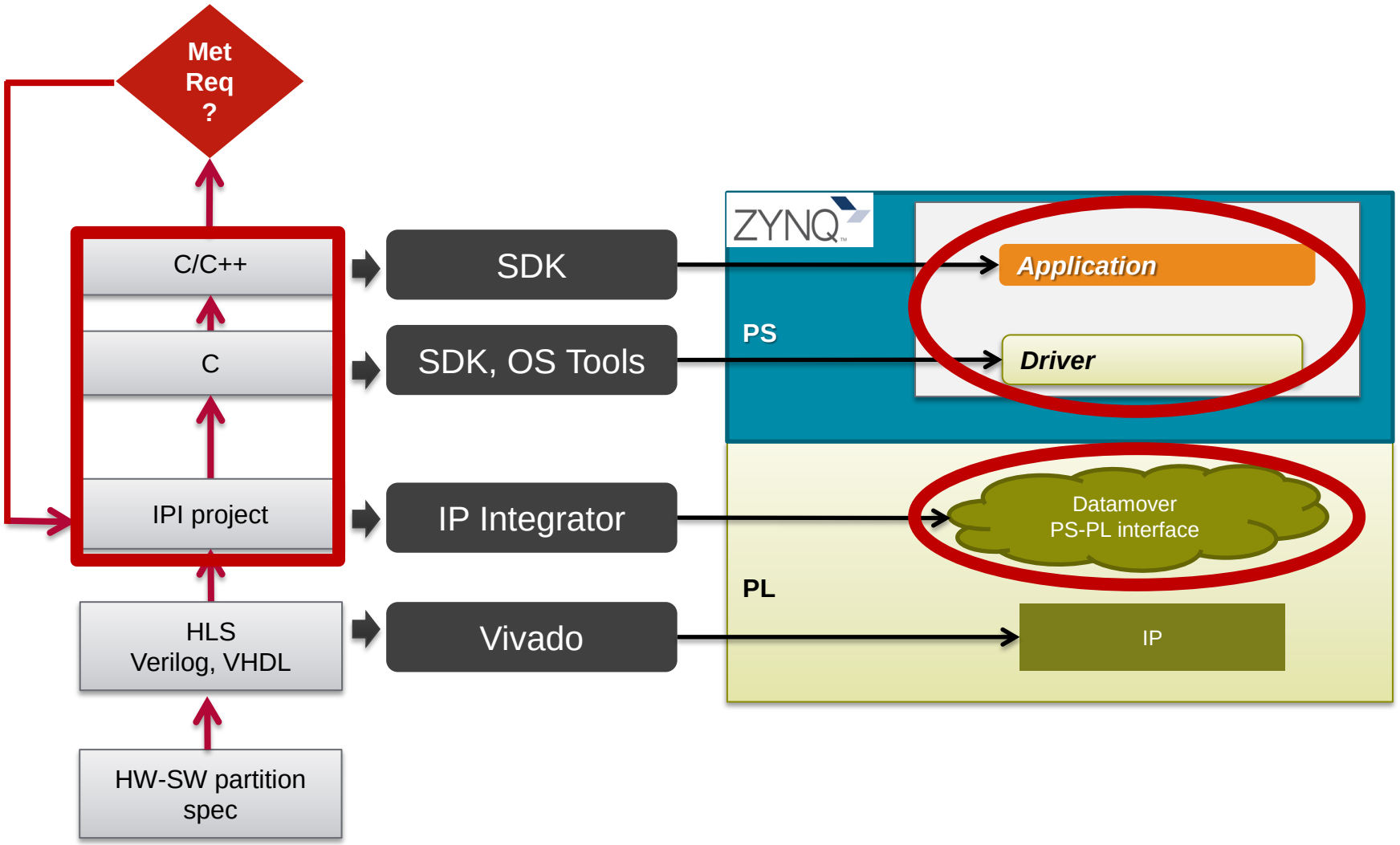
Zynq UltraScale+ MPSoC



HW/SW Optimization Challenges

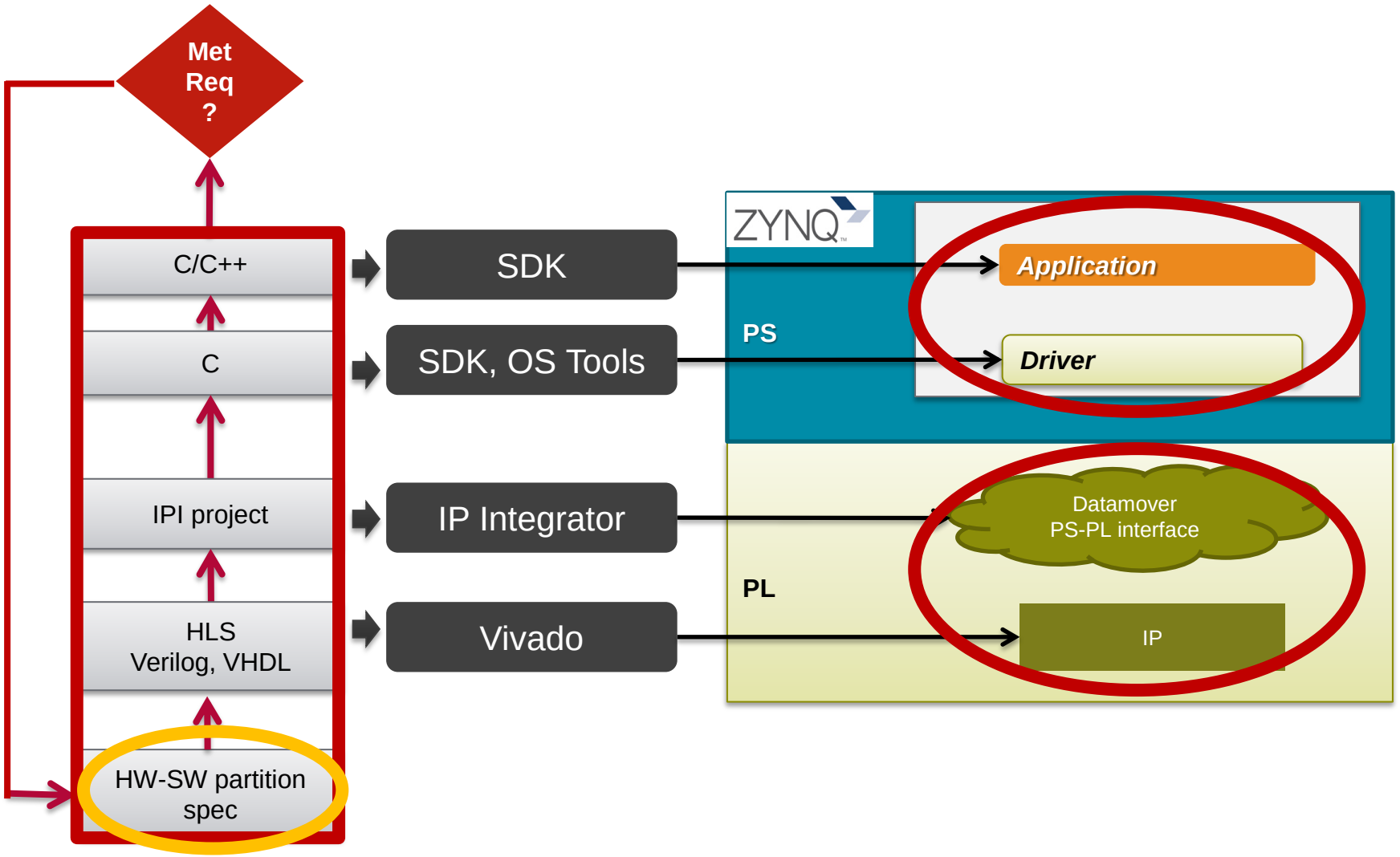


Before SDSoC: Connectivity Exploration



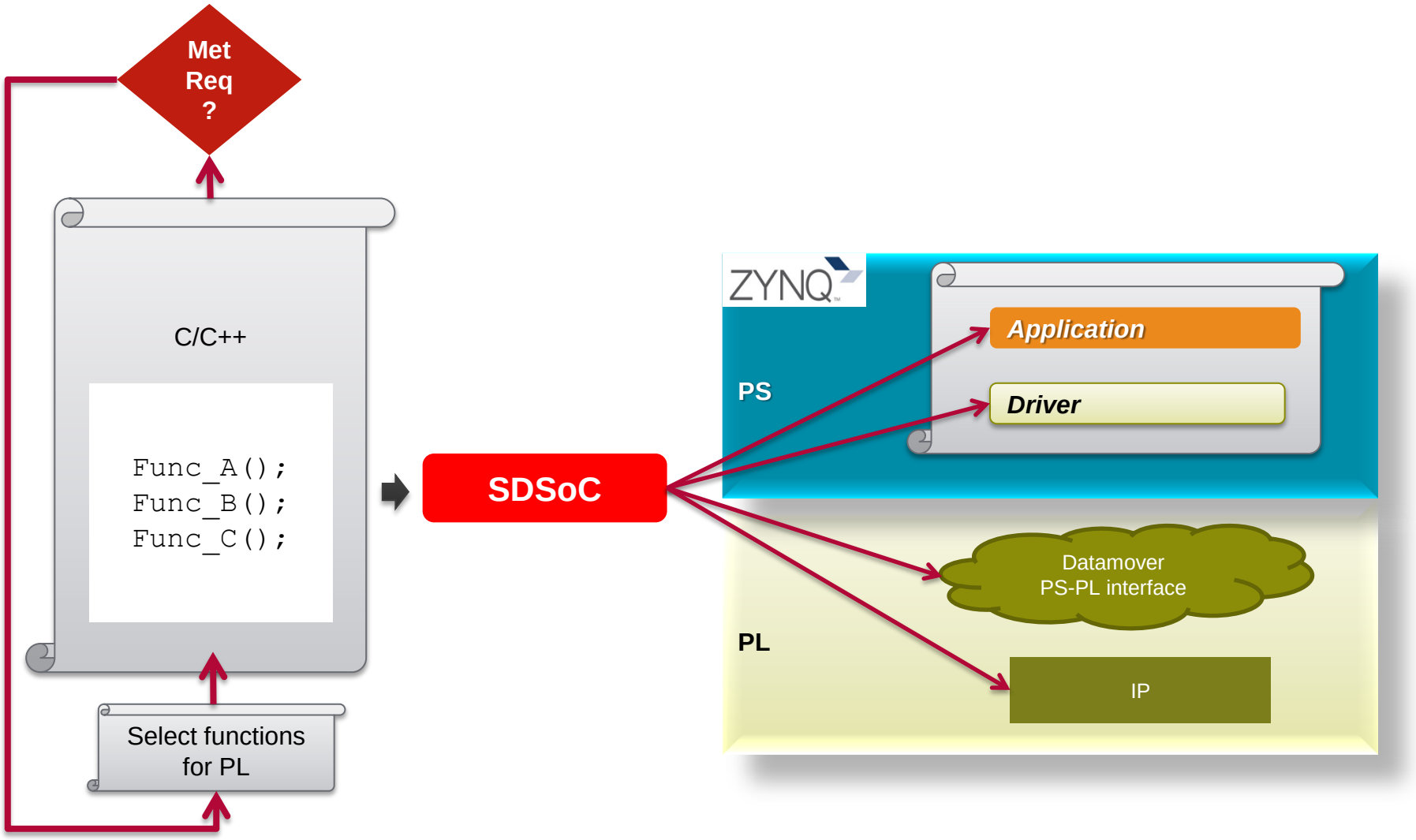
Need to Modify Multiple Levels of Design Entry

Before SDSoC: HW/SW Partition Exploration



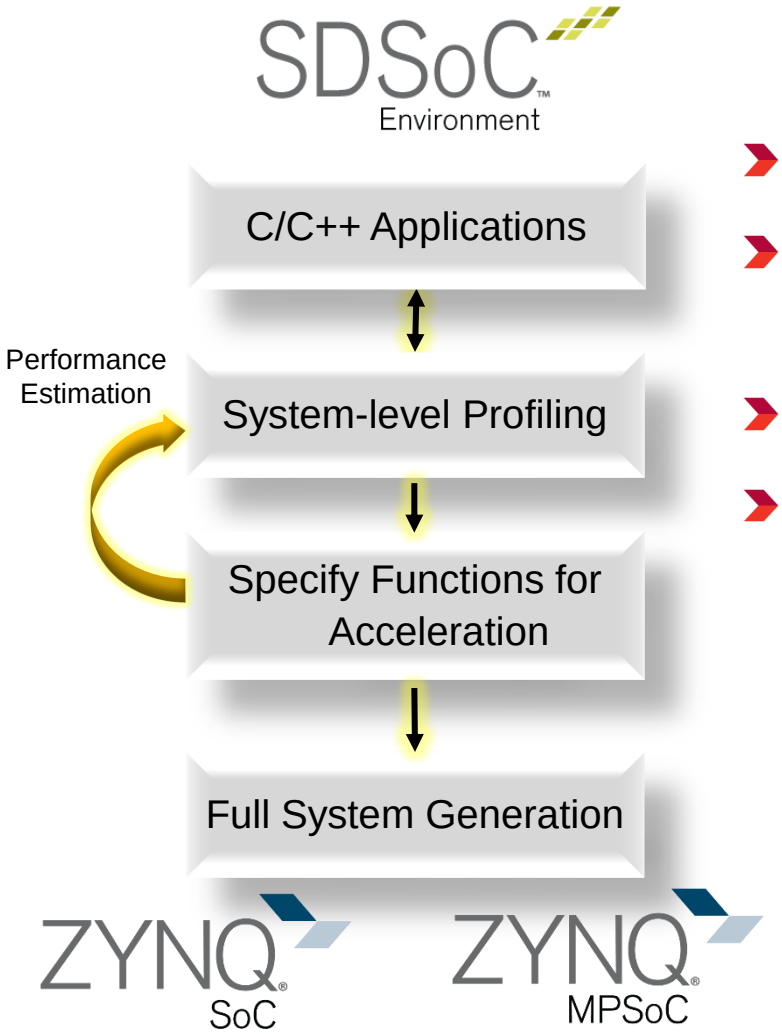
Involves Multiple Disciplines to Explore Architecture

SDSoC: Automatic System Generation

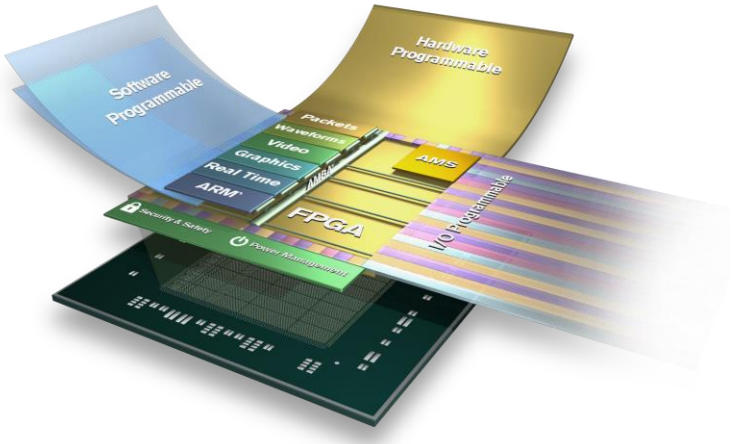


C/C++ Applications to System in hours

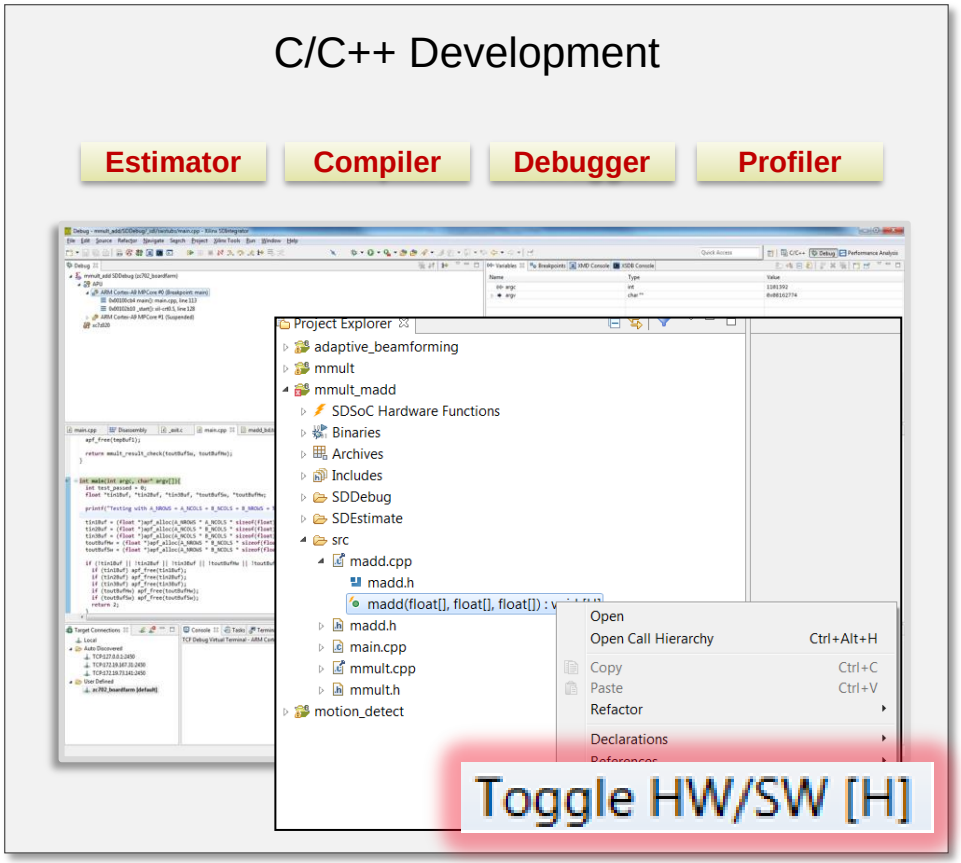
SDSoC: HW Acceleration from C/C++ Applications



- **Move C/C++ functions to hardware**
- **Full system generation including driver and hardware connectivity**
- **System-level debug and profile**
- **Rapid HW partitioning and exploration**

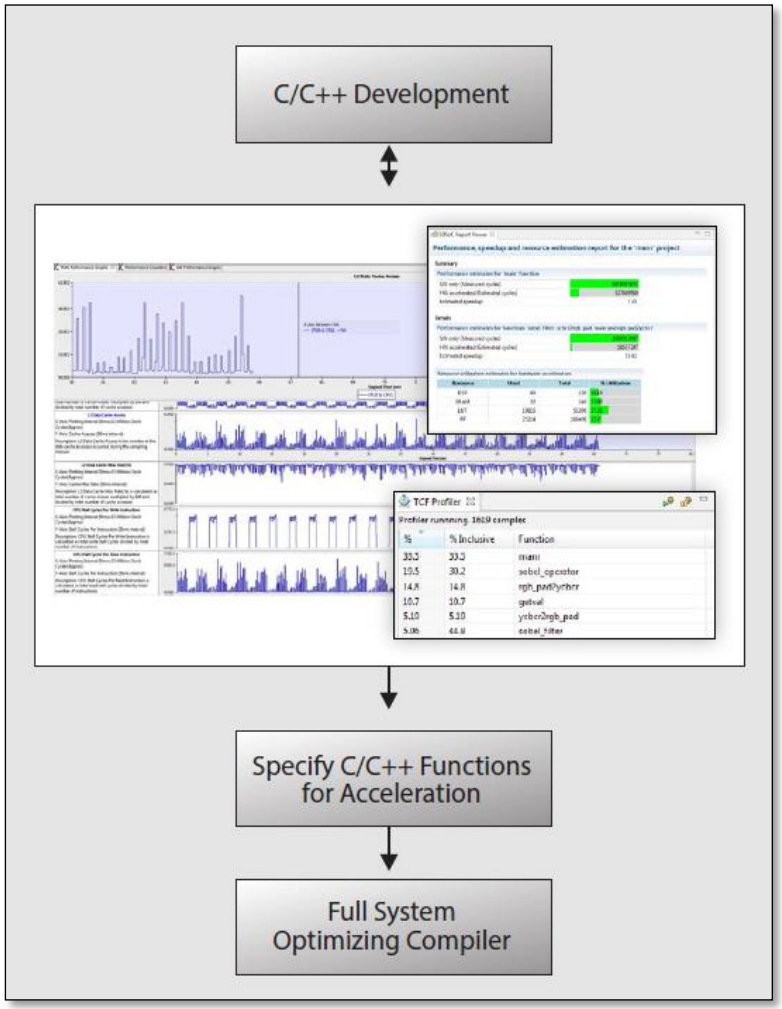


SDSoC: Embedded C/C++ Applications Programming Experience



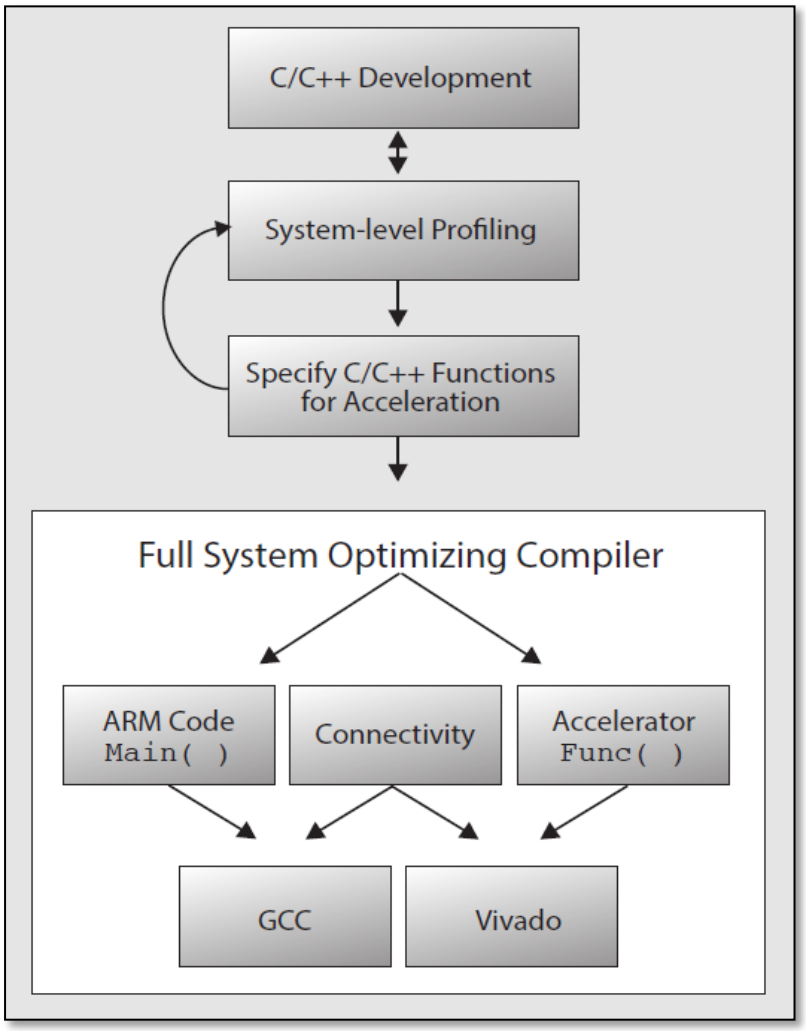
- **Easy to use Eclipse IDE**
- **One click to accelerate functions in Programmable Logic (PL)**
- **Optimized libraries**
  - Xilinx, ARM and Partners
  - DSP, Video, fixed point, linear algebra, BLAS, OpenCV
- **Support for Linux, FreeRTOS and baremetal**
  - Additional OS support in future releases

SDSoC: System Level Profiling



- **Rapid system performance estimation**
  - Full system estimation (programmable logic, data communication, processing system)
  - Reports SW/HW cycle level performance and hardware utilization
- **Automated performance measurement**
  - Runtime measurement by instrumentation of cache, memory, and bus utilization

SDSoC: Full System Optimizing Compiler



- **Rapid software configurable application acceleration using C/C++**
  - Automated function acceleration in programmable logic
  - Up to 100X increase in performance vs. software
  - System optimized for latency, bandwidth, and hardware utilization

Automated Generation of System Connectivity

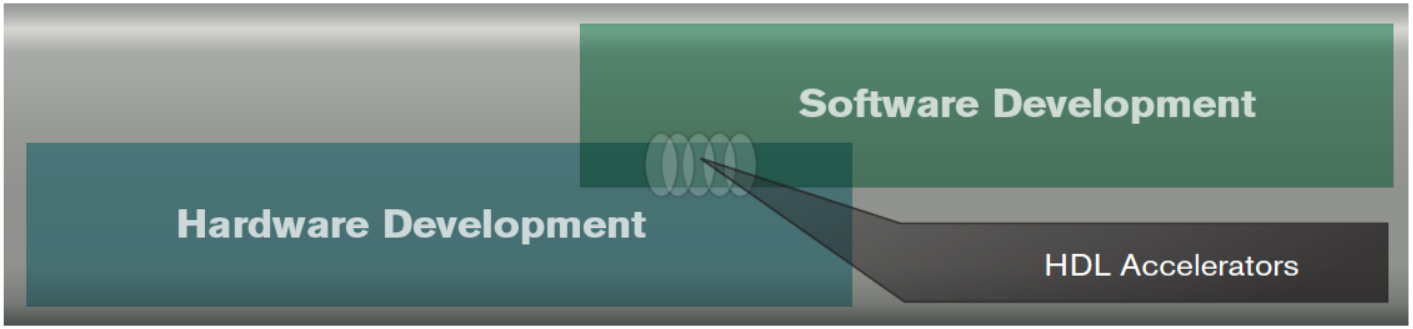
	PS-PL Interface				
Find the lowest latency DataMover		ACP	HP cache	HP non-cache	GP
	SW only	180,957	181,009	365,766	
	Simple DMA	27,023	38,705	26,797	
	SGDMA	30,804	43,225	30,818	
	Processor Direct	45,868	81,941	46,057	
	FIFO				427,878

32X32 floating point matrix multiply (latency in processor cycles)

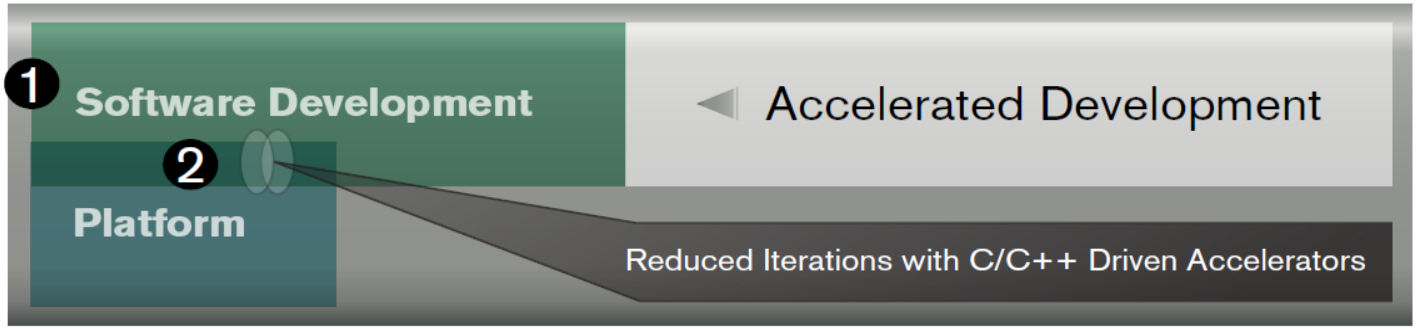
- **Explore system performance and power**
  - Rapidly configure, generate macro and micro architectures
  - Explore optimal interconnect and memory interfaces
  - Automatic insertion of AXI-Performance Monitor (APM) to obtain detailed cache/port/memory performance data
- **Shorten development time over traditional Hardware/Software flows**

SDSoC: Productivity Advantage

Traditional Development Schedule



Software Defined Development Schedule

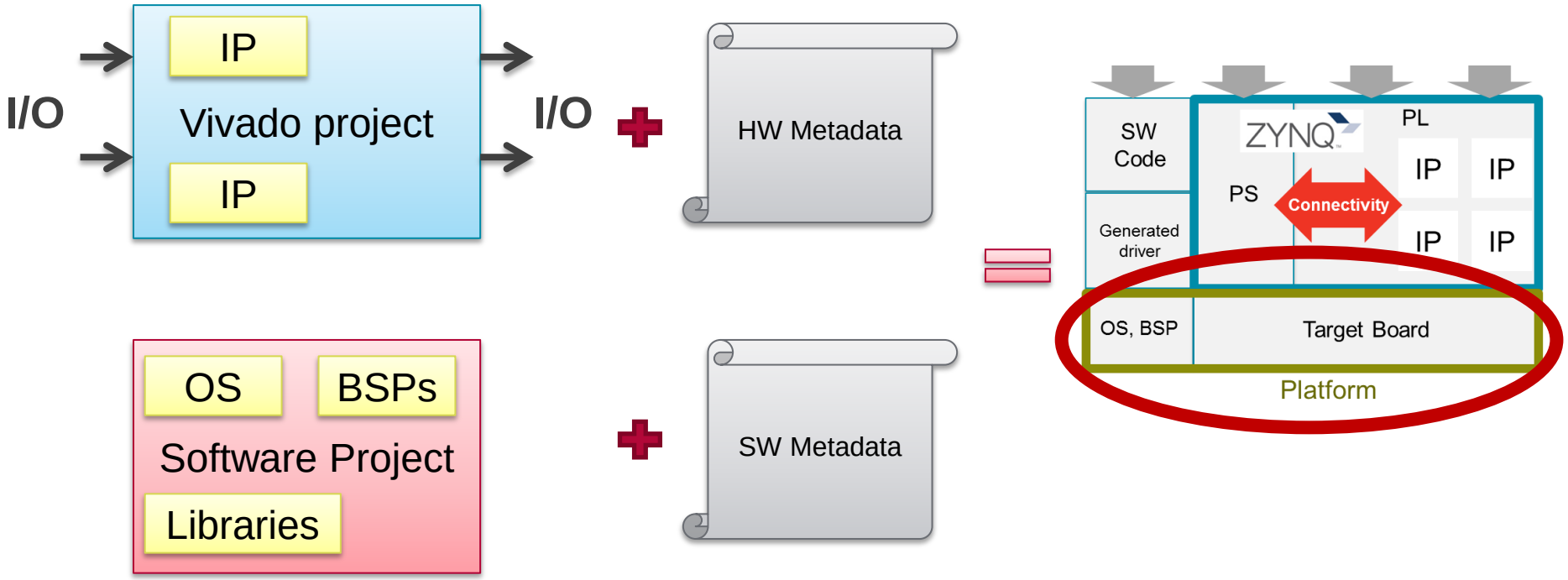


1. Software development starts immediately, 3rd party and end user platforms
2. SDSoC's ASSP-like development, system-level profiling and full system optimizing compiler empowers software developers to accelerate C/C++ functions

SDSoC: Supported Development Platforms

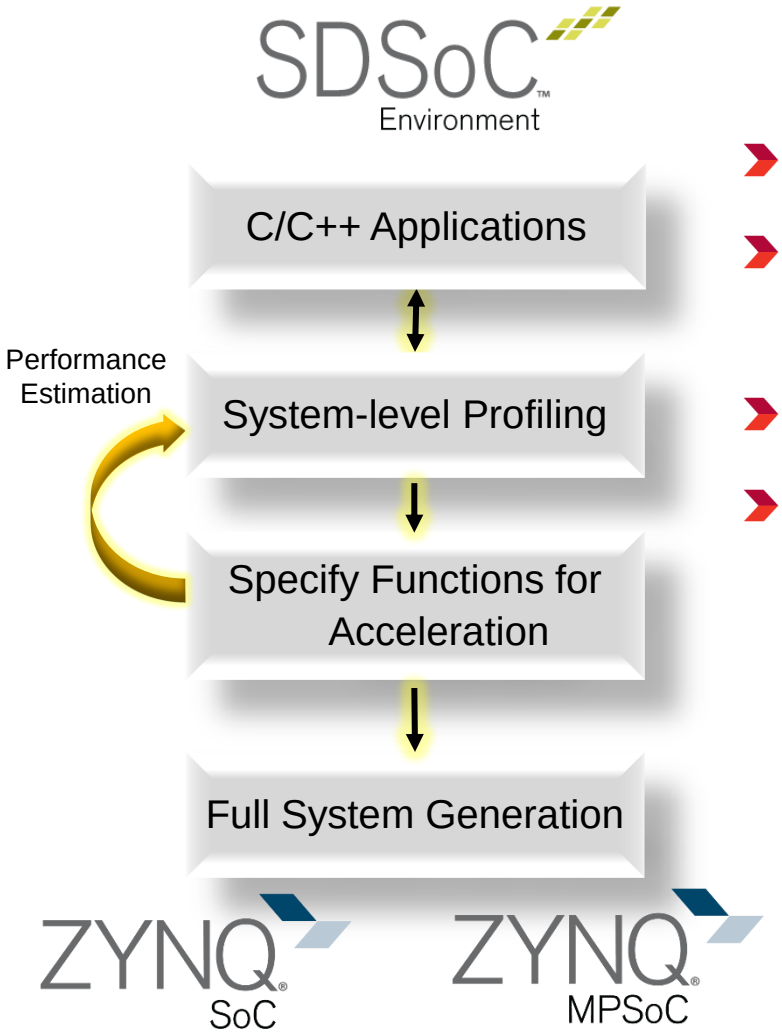
- **Start today with:**
  - Xilinx development platforms: ZC702 & ZC706,
  - Alliance Member platforms: Zedboard, MicroZed, ZYBO, Zynq SDR, ZC702+HDMI IO, SVDK, any many more
  - Visit http://www.xilinx.com/products/design-tools/software-zone/sdsoc.html#boardskits
- Customer platform flow supported today (UG1146)

Custom Platform Creation



- **Target customer's own board for production design with SDSoC**
- **Add metadata to existing Vivado project and existing Software projects (OS, BSPs and libraries)**

Summary



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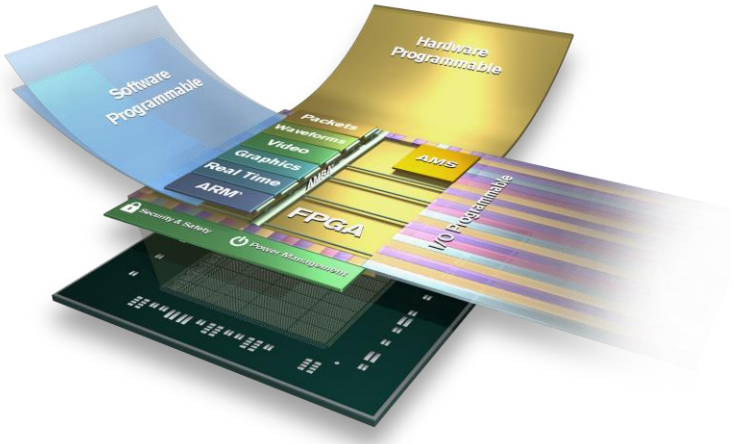
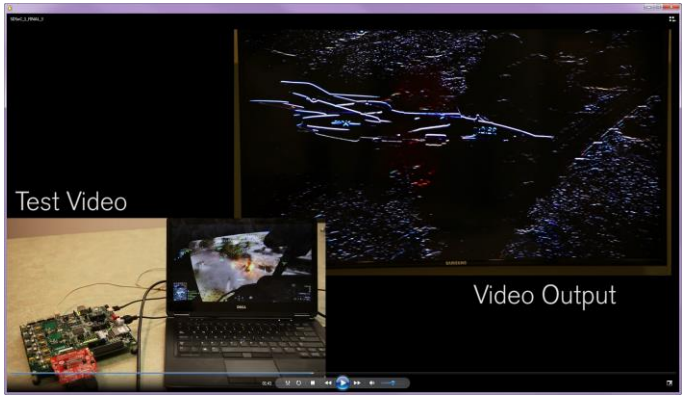


Learn More About SDSoC



- **Xilinx.com/sdsoc**
  - 10 Videos
  - 3 User Guides
  - Backgrounder
  - Worldwide ATP Classes
  - Self-guided labs (part of UG1028)