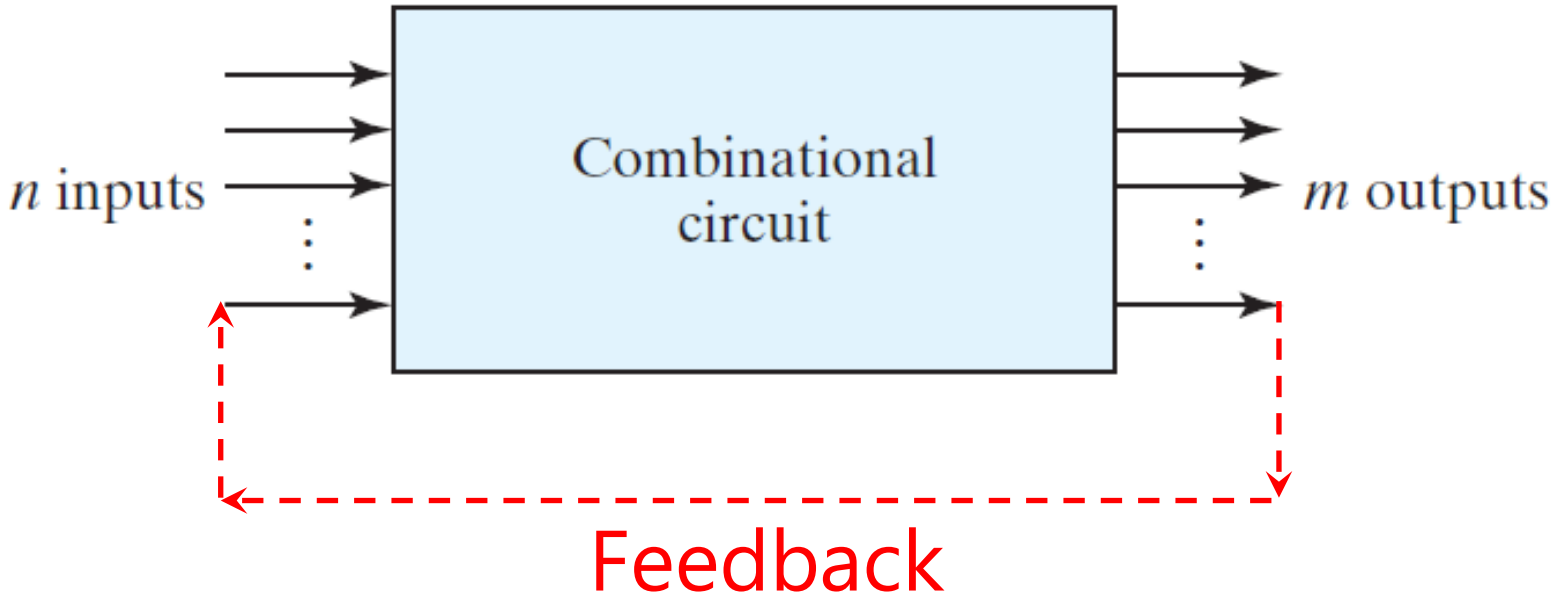
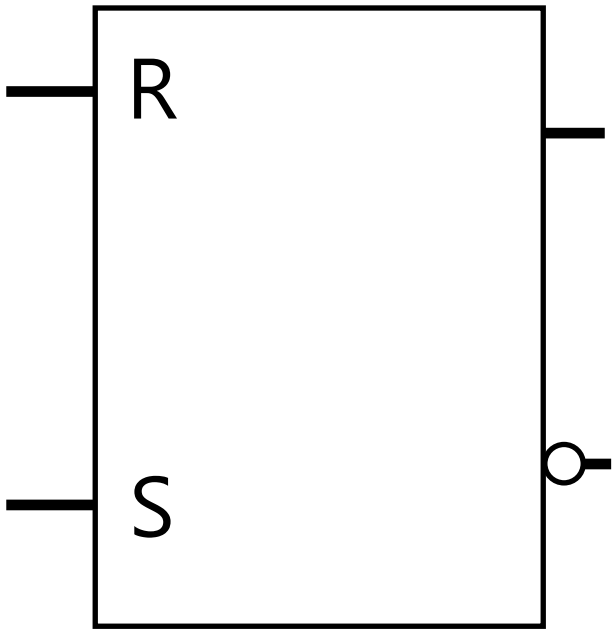
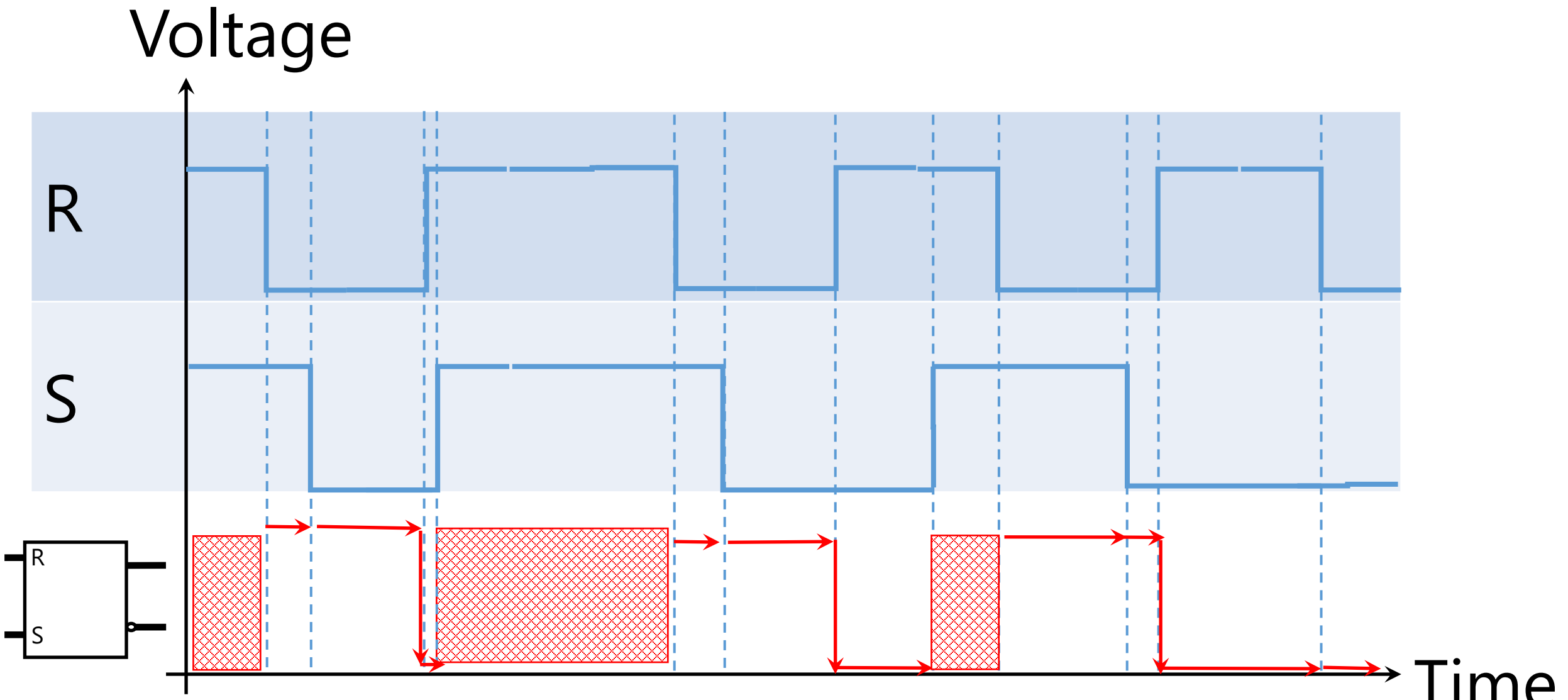
Sequential Logic

Sequential Logic





S	R	Q	Q′
0	0	Q_t	Q'_t
0	1	0	1
1	0	1	0
1	1	X	X

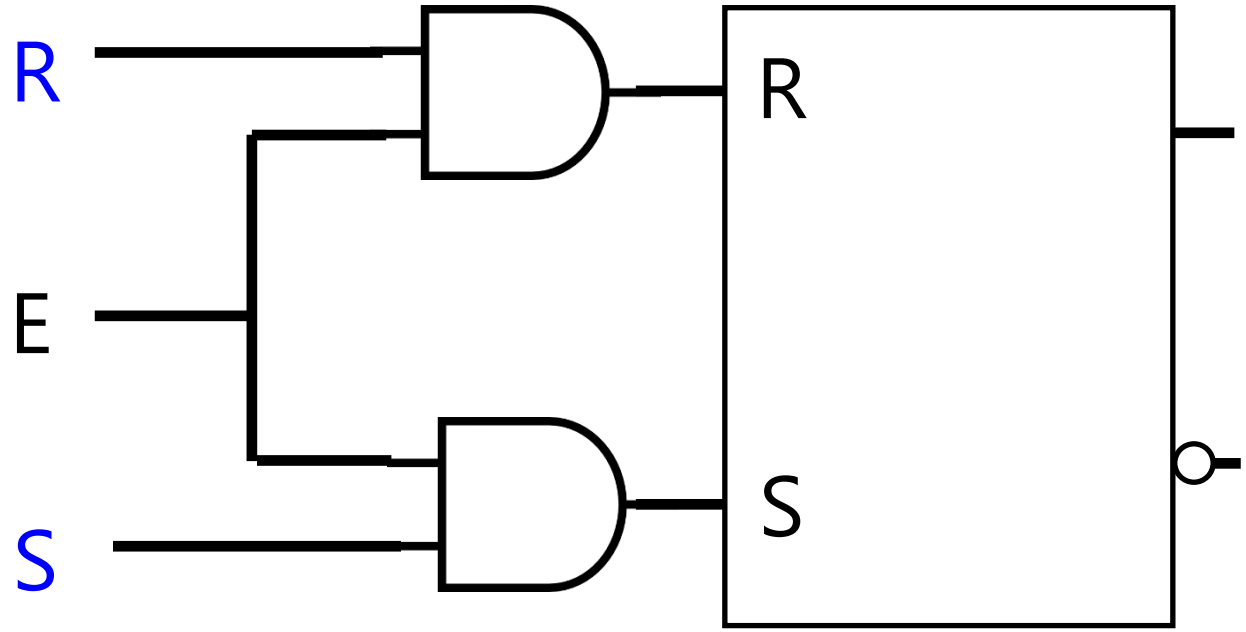

Voltage
R
S
R
S
Time

S and R control how the state changes.

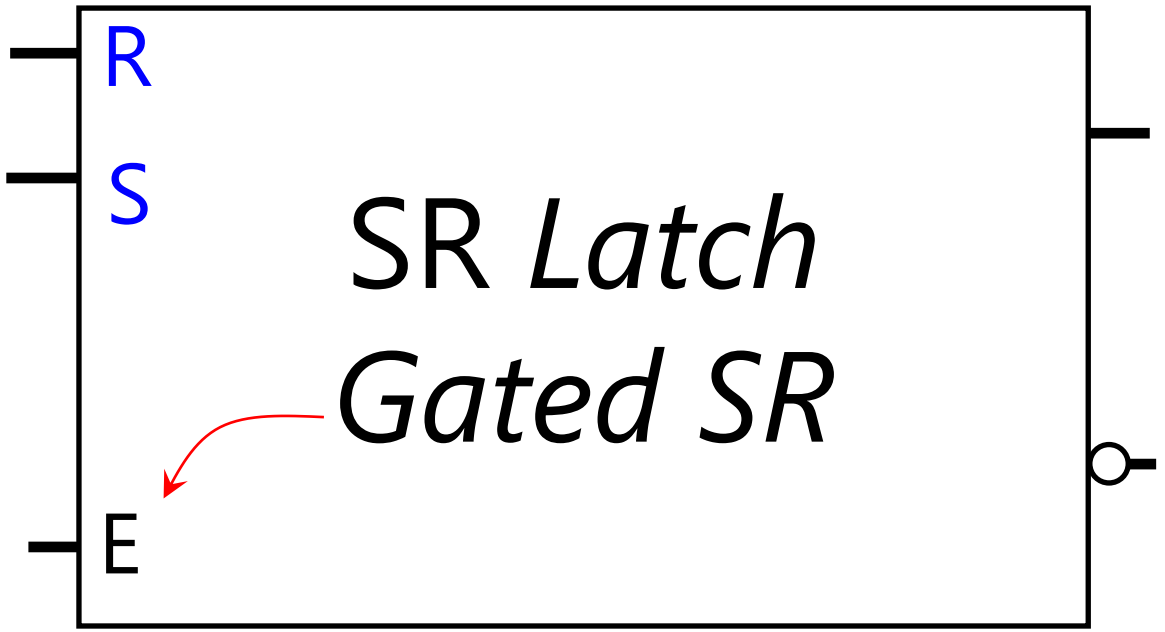
Put a gate/latch on when change applies

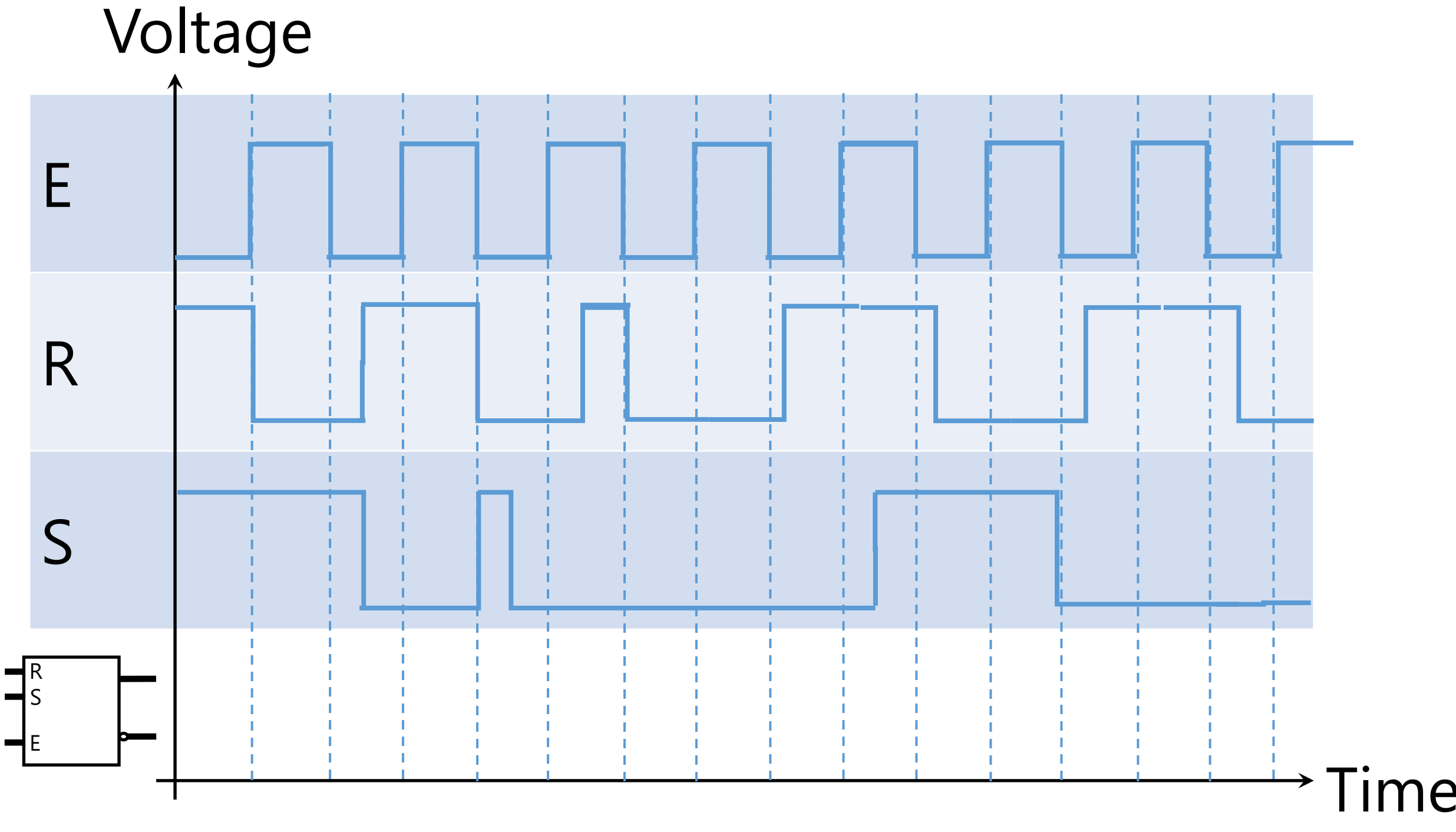
SR w/ enable input

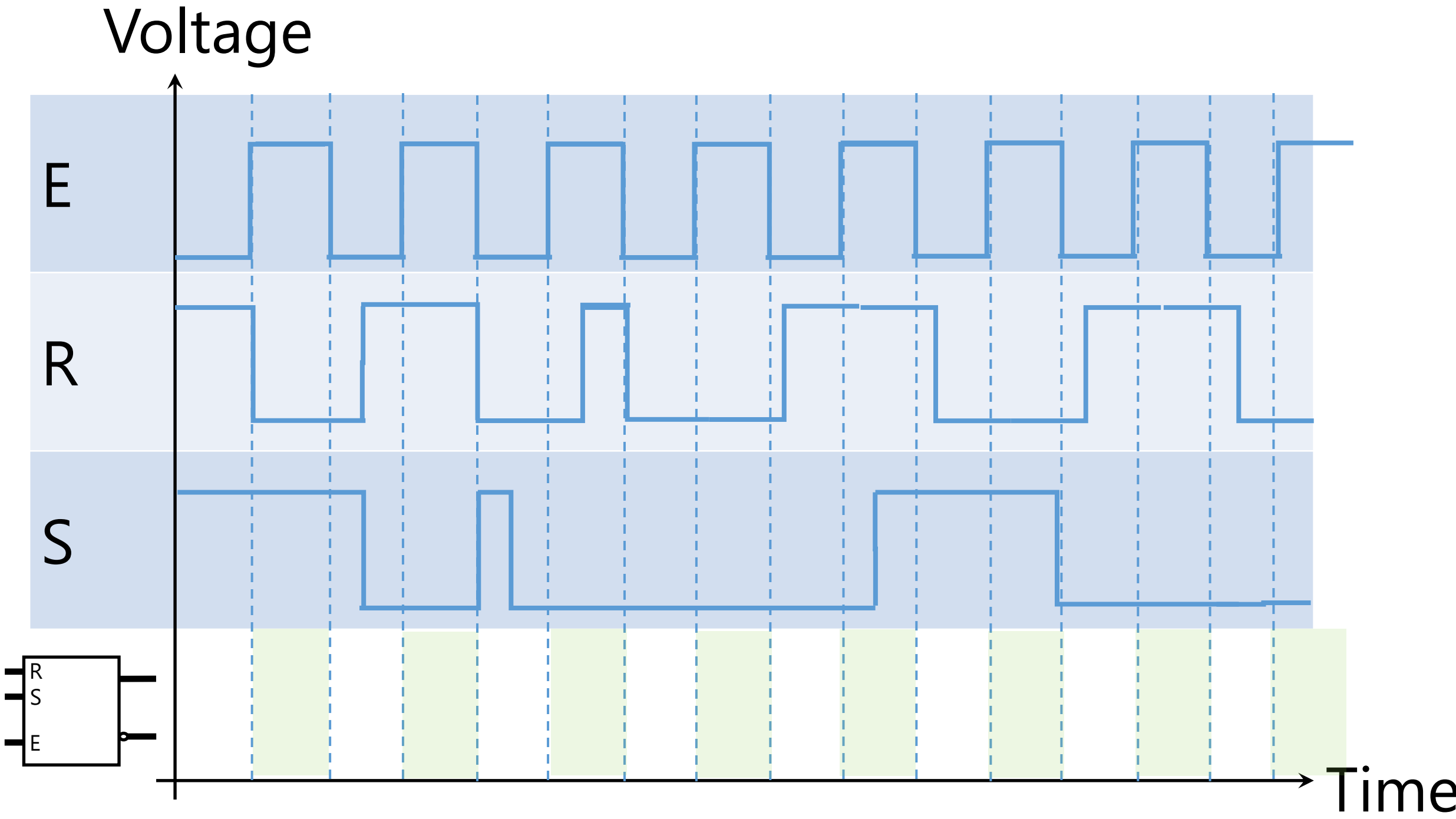
SR *Latch*

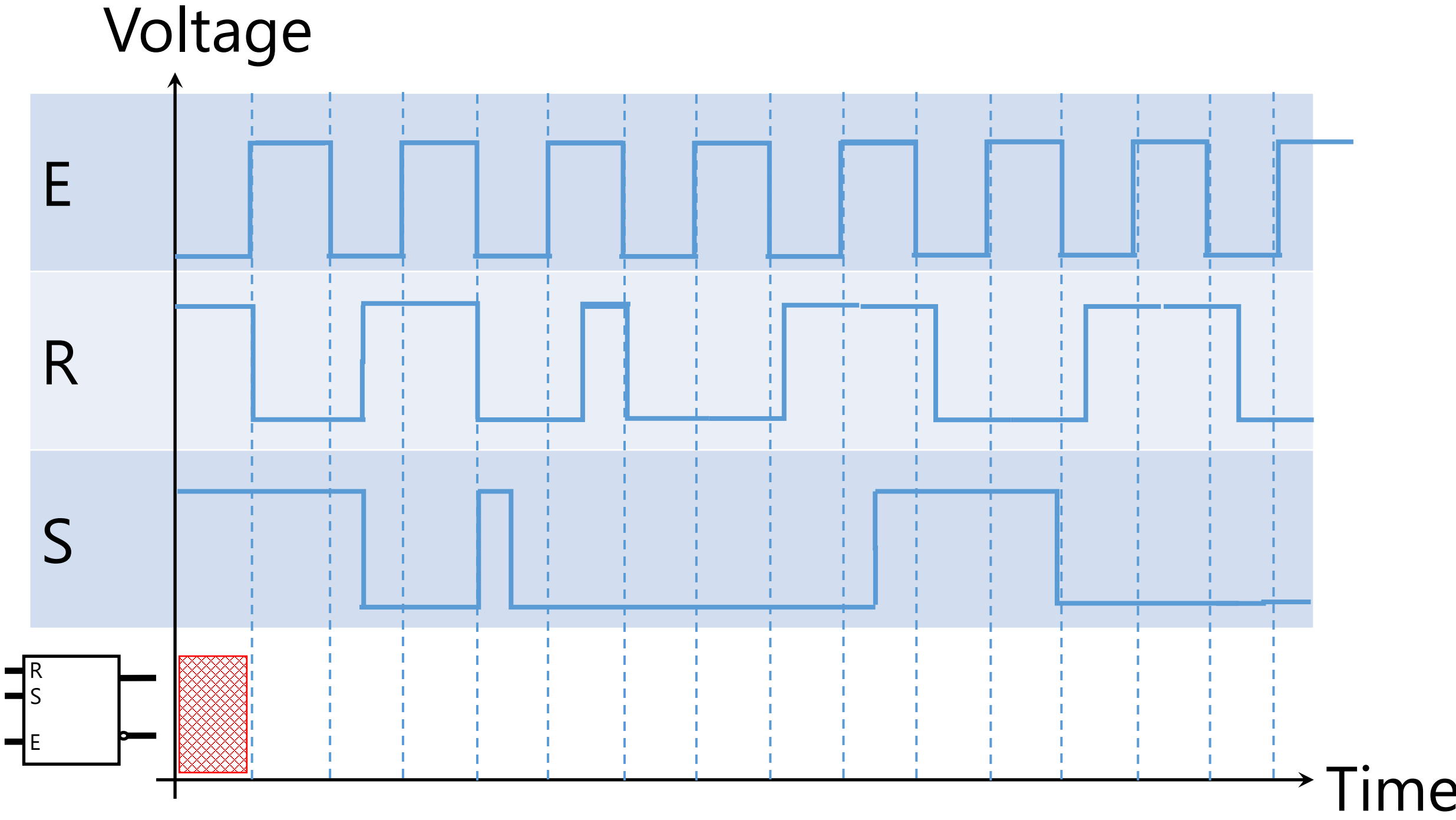


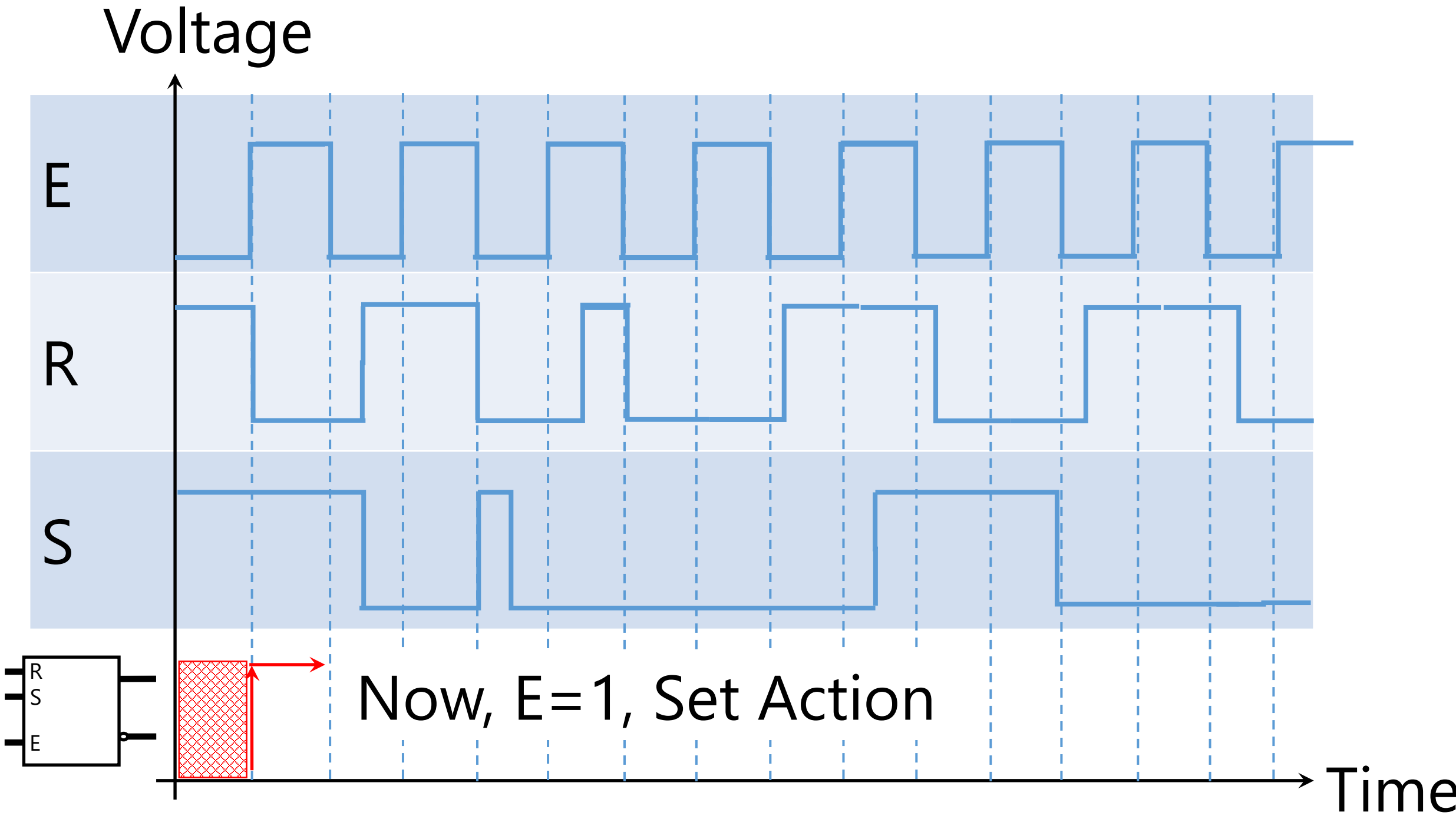
E	S	R	S	R	Q	Q′
0	X	X	0	0	Q_t	Q'_t
1	0	0	0	0	Q_t	Q'_t
1	0	1	0	1	0	1
1	1	0	1	0	1	0
1	1	1	1	1	X	X

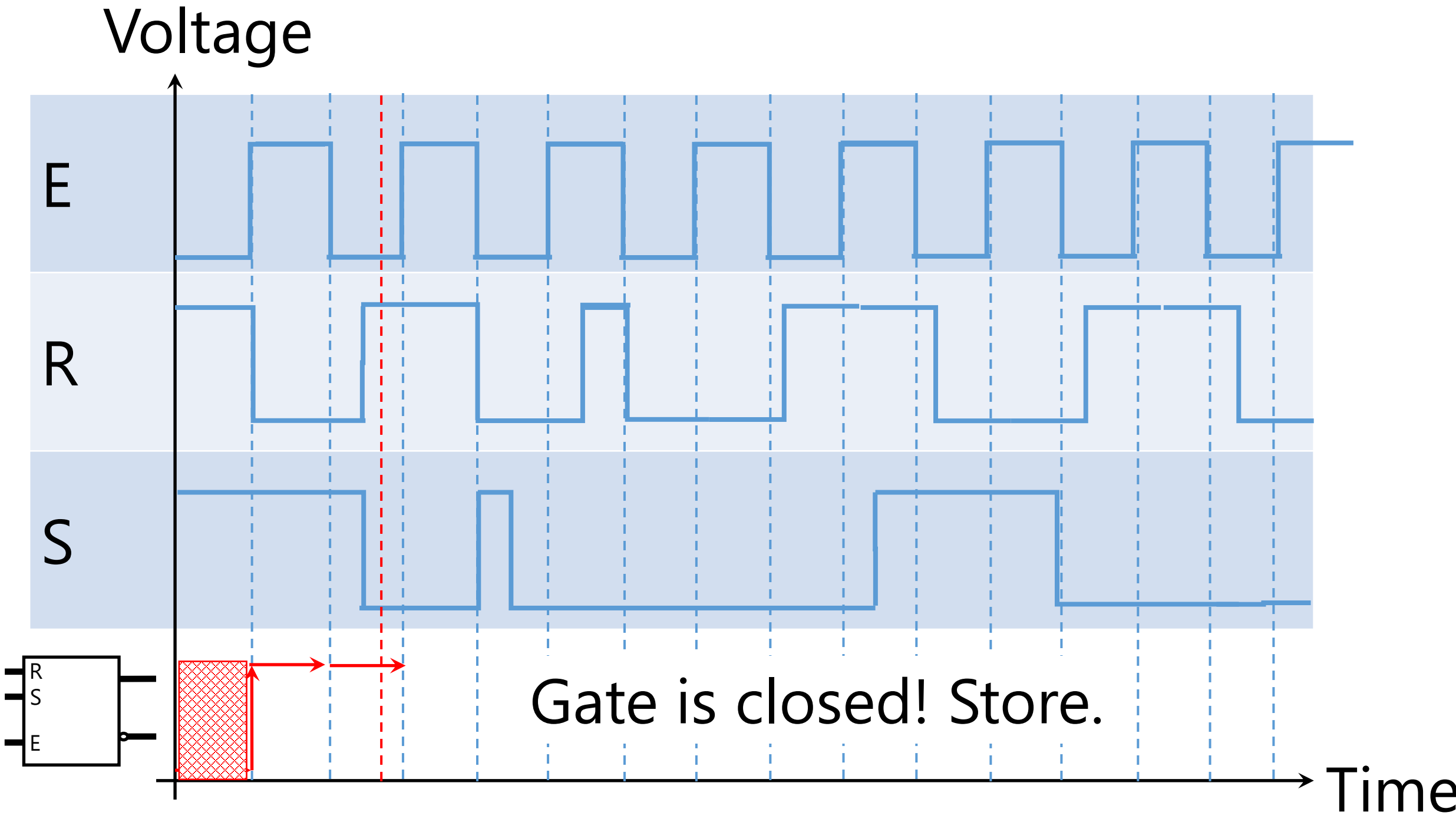

R
S
E
SR Latch
Gated SR

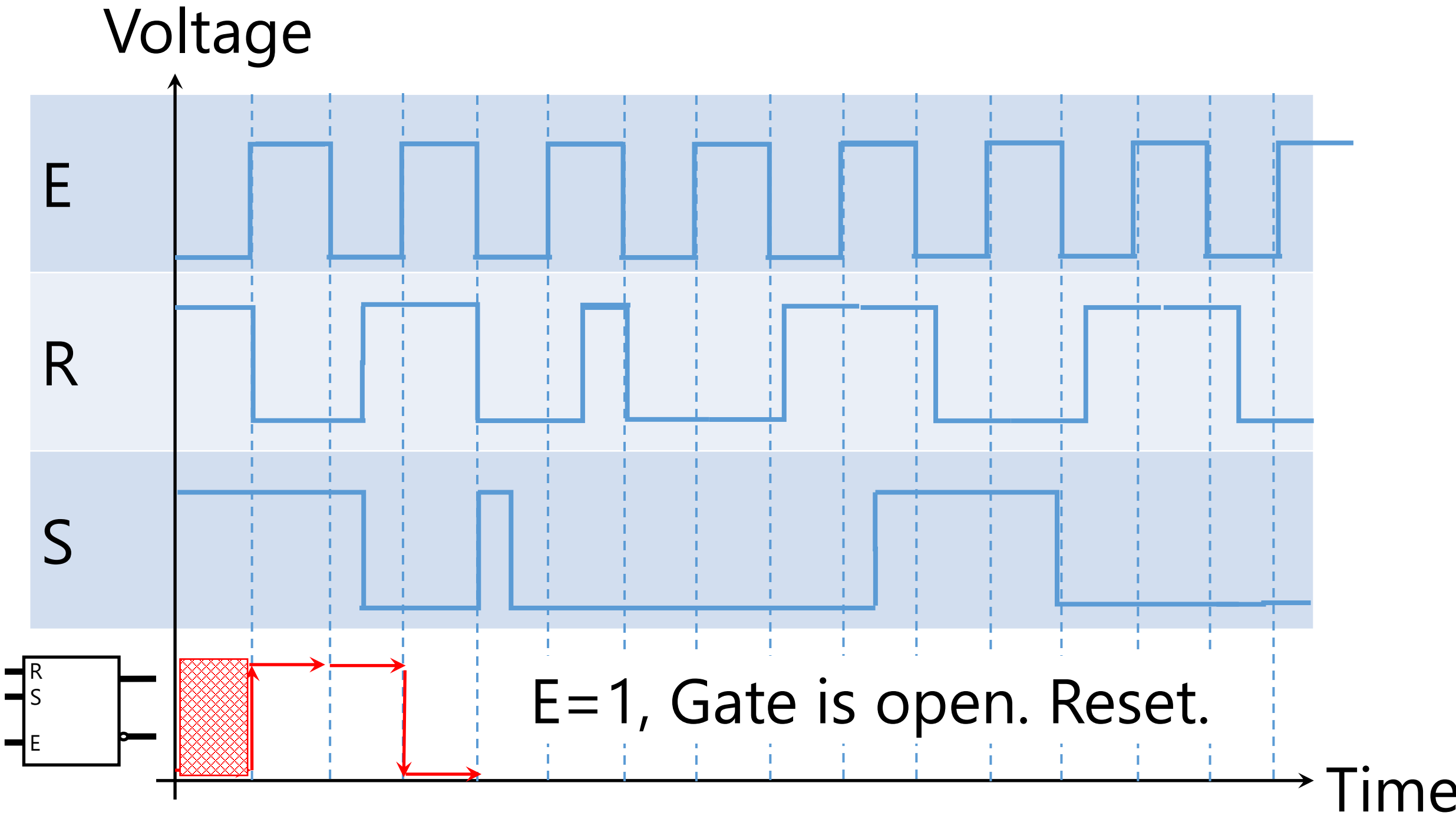

Voltage
E
R
S
R
S
E
Time

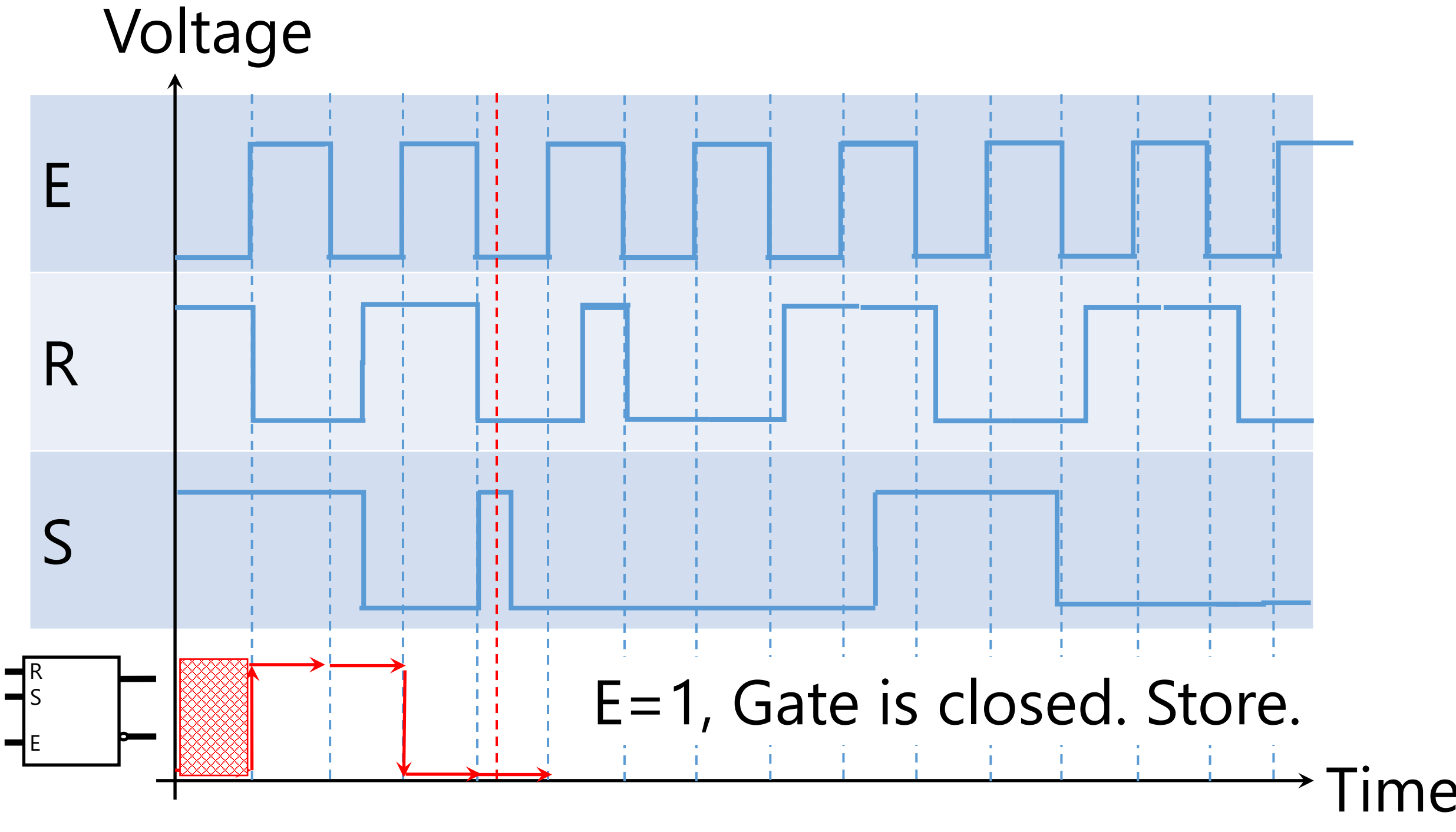

Voltage
E
R
S
R
S
E
Time


Voltage
E
R
S
R
S
E
Time


Voltage
E
R
S
R
S
E
Now, E=1, Set Action
Time

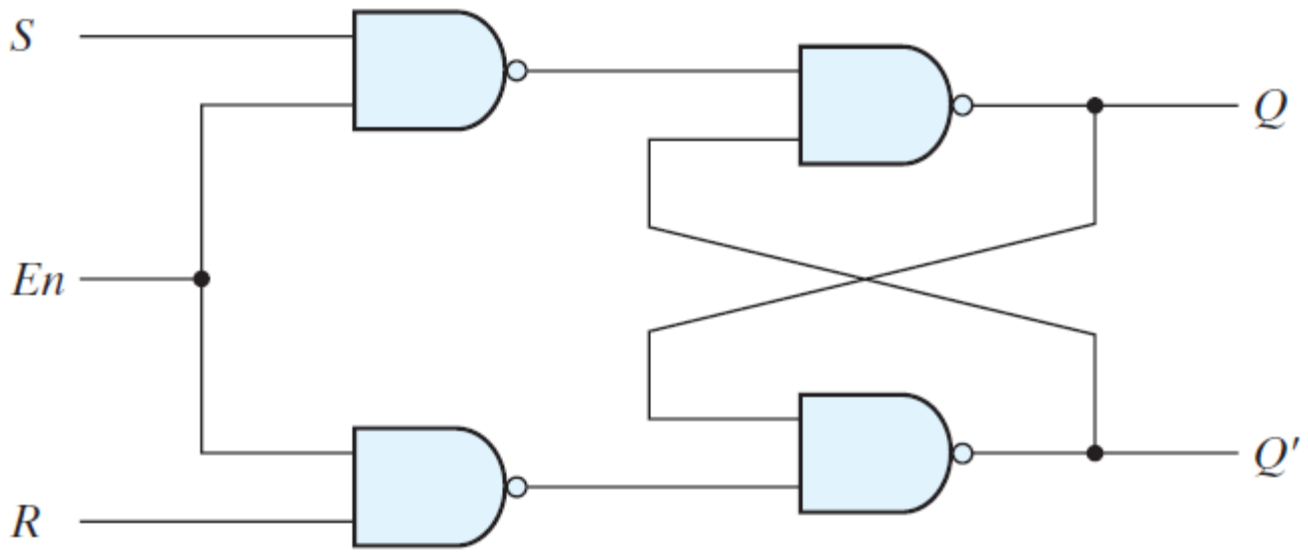

Voltage
E
R
S
R
S
E
Gate is closed! Store.
Time


Voltage
E
R
S
R
S
E
E=1, Gate is open. Reset.
Time


Voltage
E
R
S
R
S
E
E=1, Gate is closed. Store.
Time

SR *Latch*

NAND

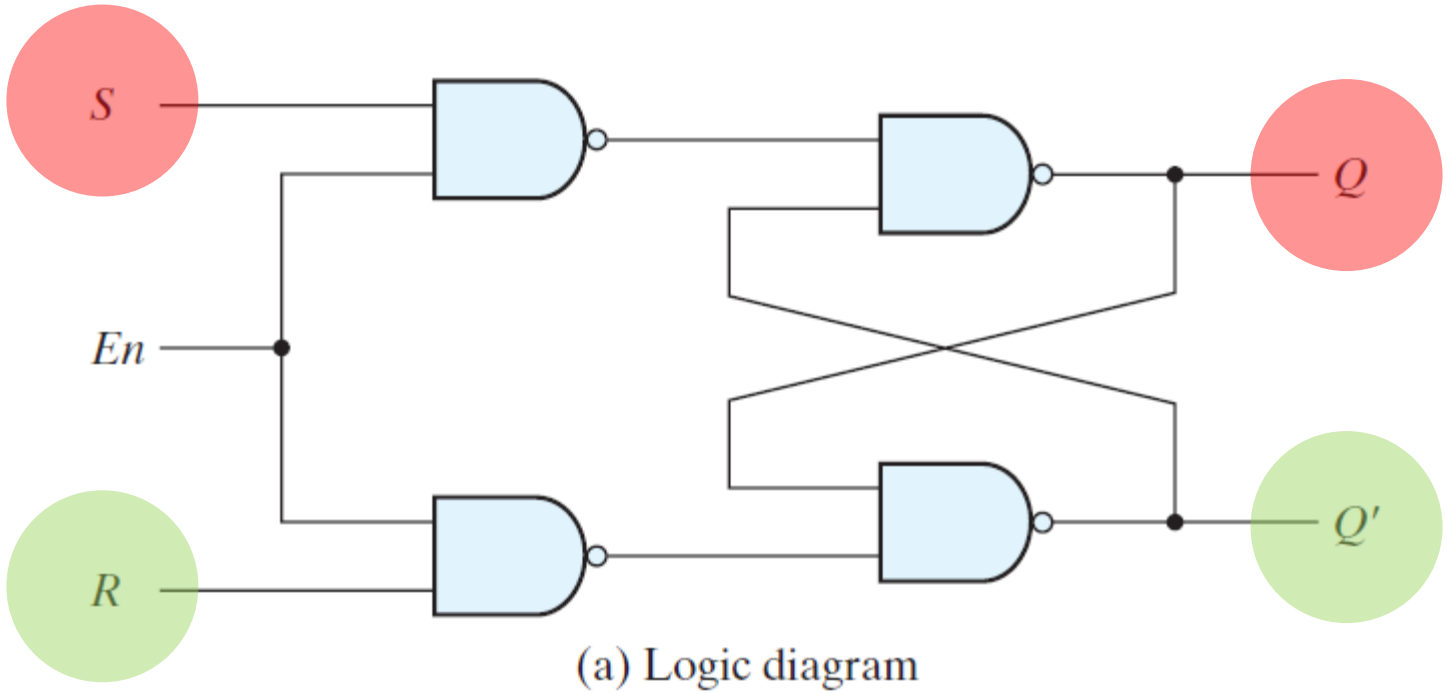


(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

FIGURE 5.5
SR latch with control input



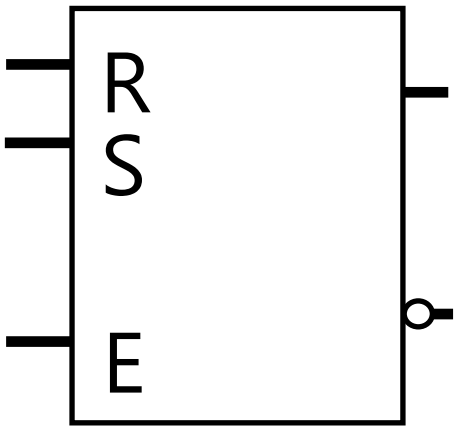
(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

FIGURE 5.5
SR latch with control input

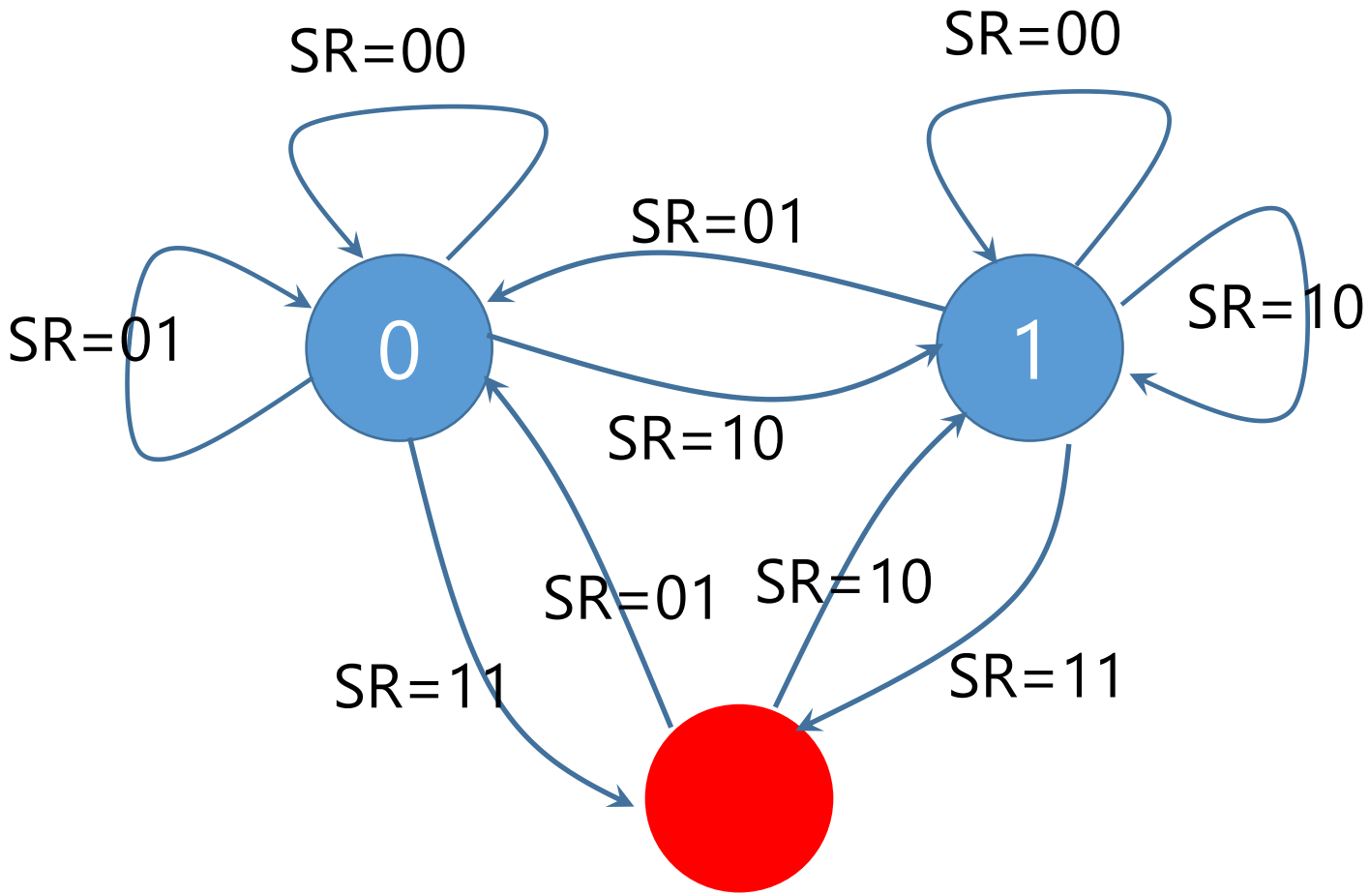
Block Diagram



Characteristic Table

S	R	Q
0	0	Q_t
0	1	0
1	0	1
1	1	X

State Transition Diagram

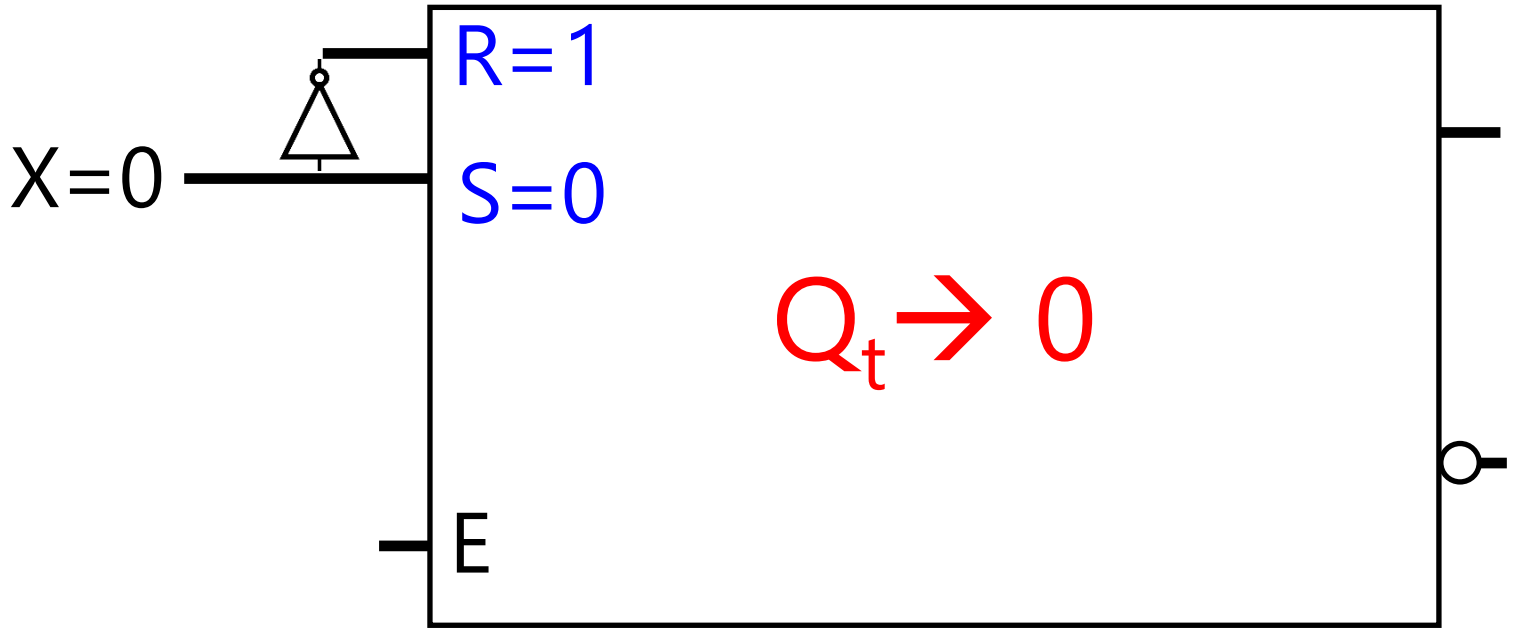


Other *Latches*

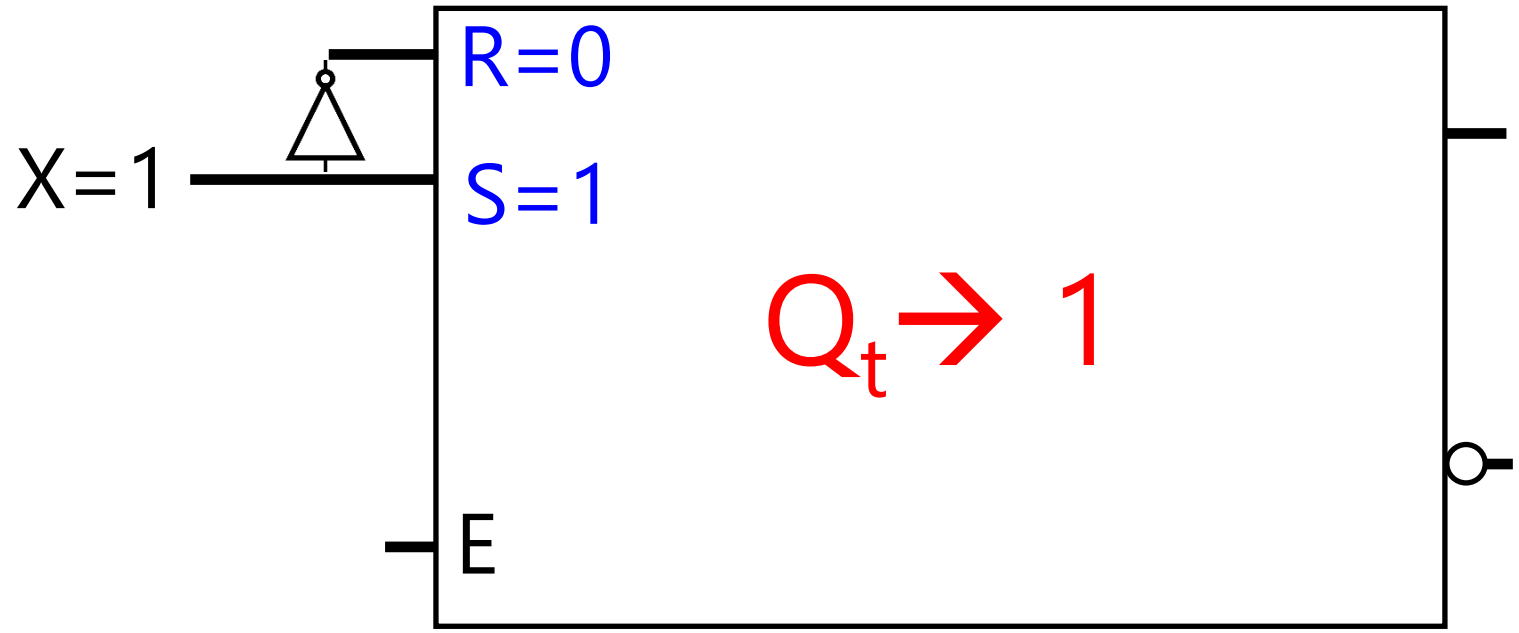
Let’s avoid the forbidden action! R≠S

R=S’ and S=R’

X	E	S	R	Q	Q′
0	0	x	x	Q_t	Q'_t
1	0	x	x	Q_t	Q'_t
0	1	0	1	0	1
1	1	1	0	1	0
Never happens		~~1~~	~~1~~	~~x~~	~~x~~



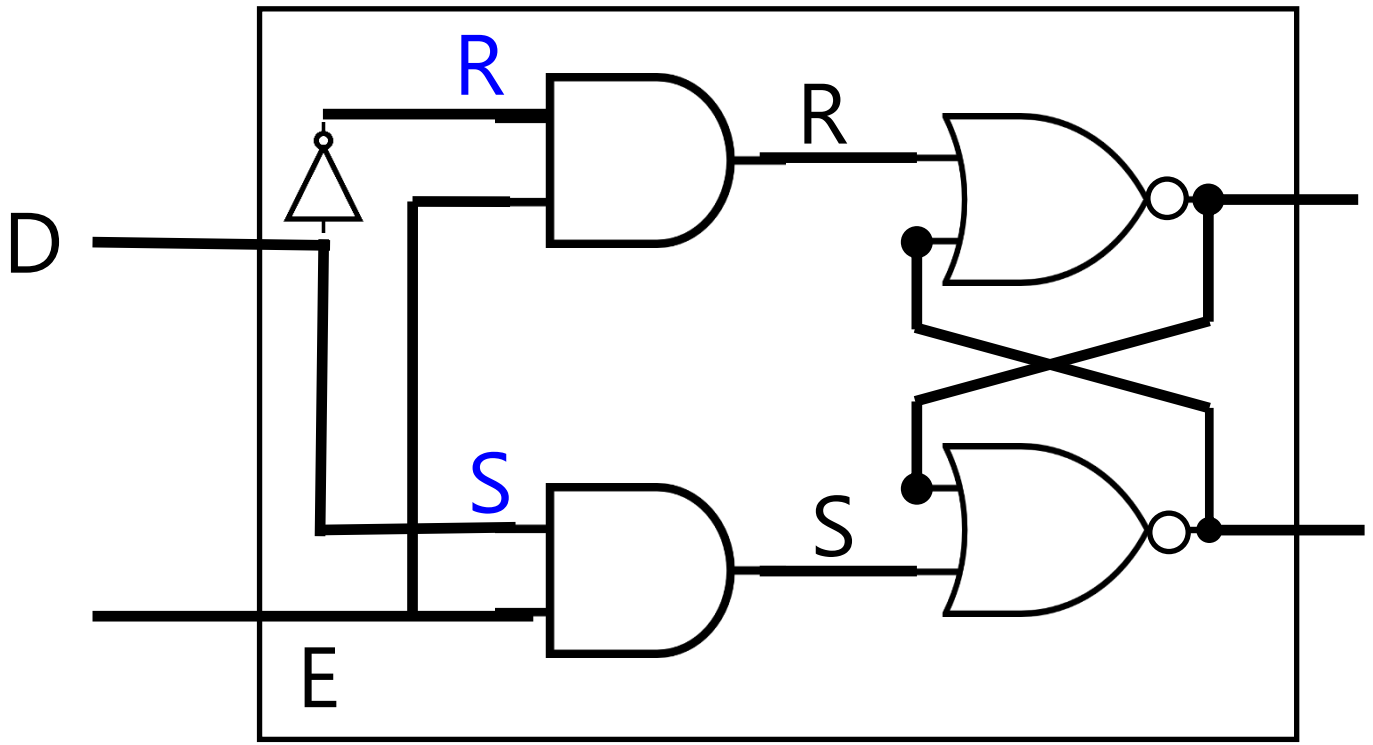
X	E	S	R	Q	Q′
0	0	x	x	Q_t	Q'_t
1	0	x	x	Q_t	Q'_t
0	1	0	1	0	1
1	1	1	0	1	0
Never happens		~~1~~	~~1~~	~~x~~	~~x~~



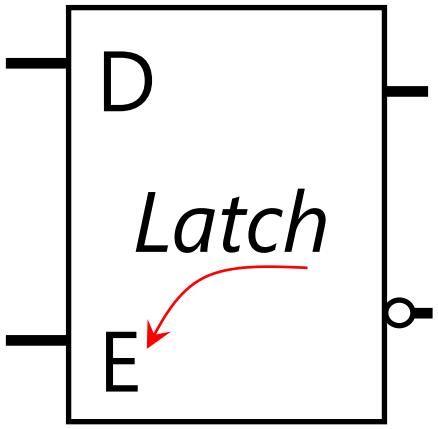
X	E	S	R	Q	Q′
0	0	x	x	Q_t	Q'_t
1	0	x	x	Q_t	Q'_t
0	1	0	1	0	1
1	1	1	0	1	0
Never happens		~~1~~	~~1~~	~~x~~	~~x~~

D	E	Q
0	0	Q_t
1	0	Q_t
0	1	0
1	1	1

D	Q
0	0
1	1


R
R
D
S
S
E

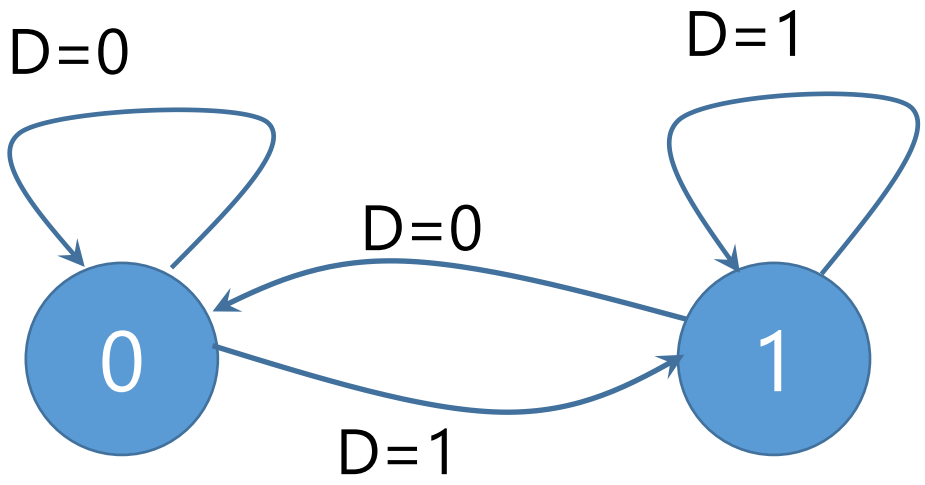
Block Diagram



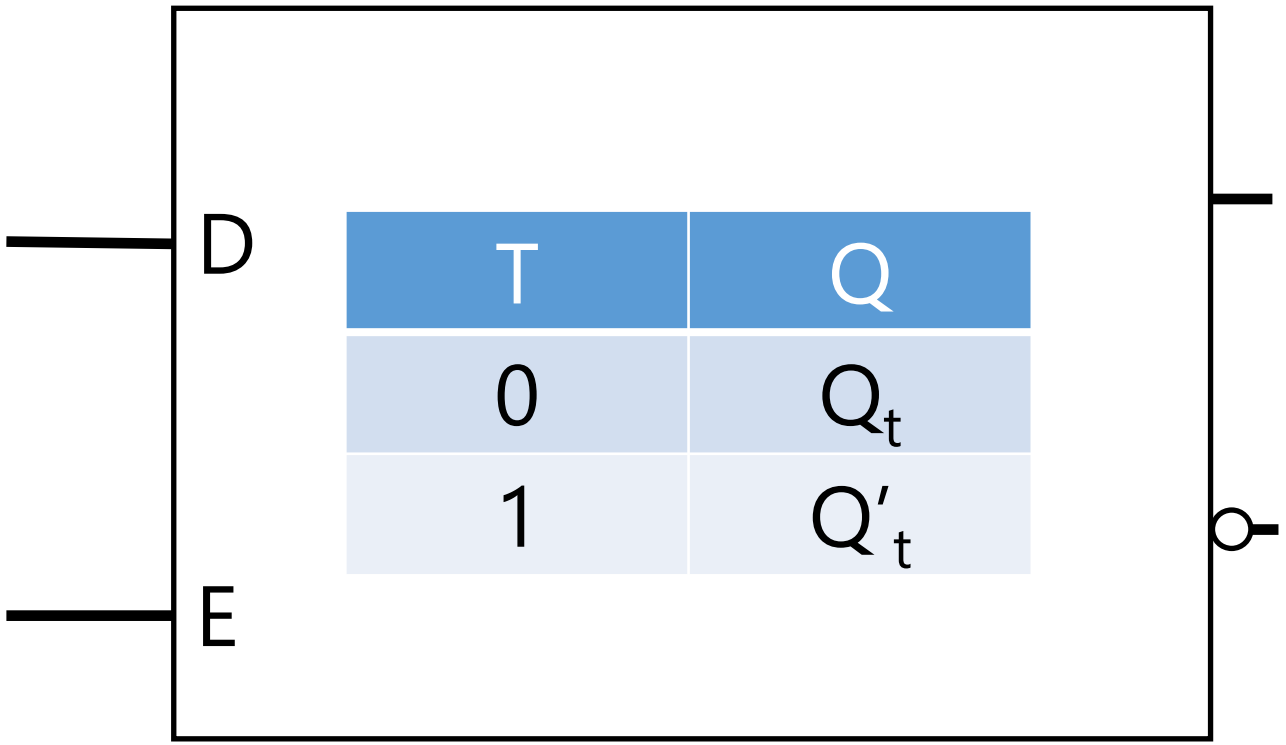
Characteristic Table

D	Q
0	0
1	1

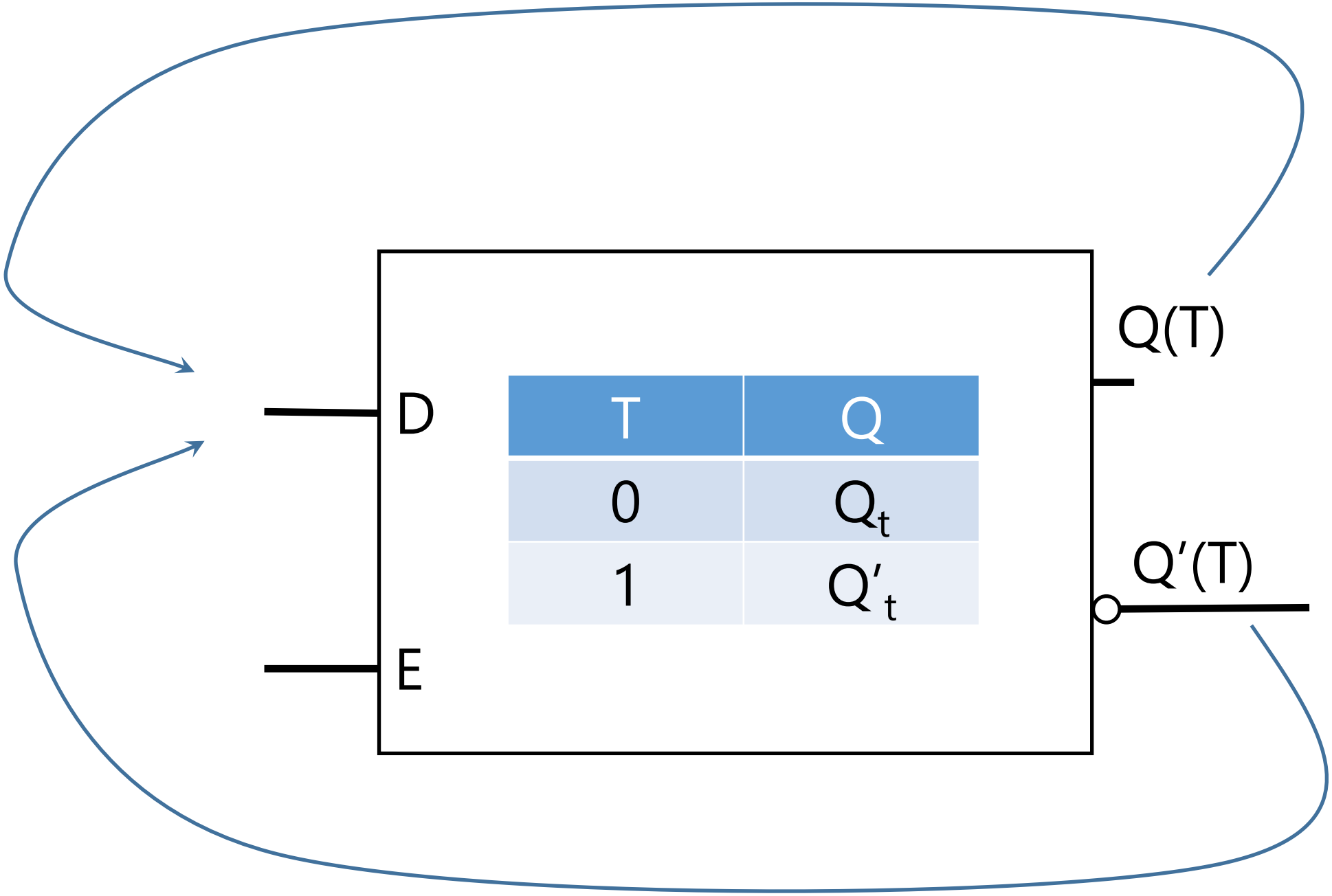
State Transition Diagram

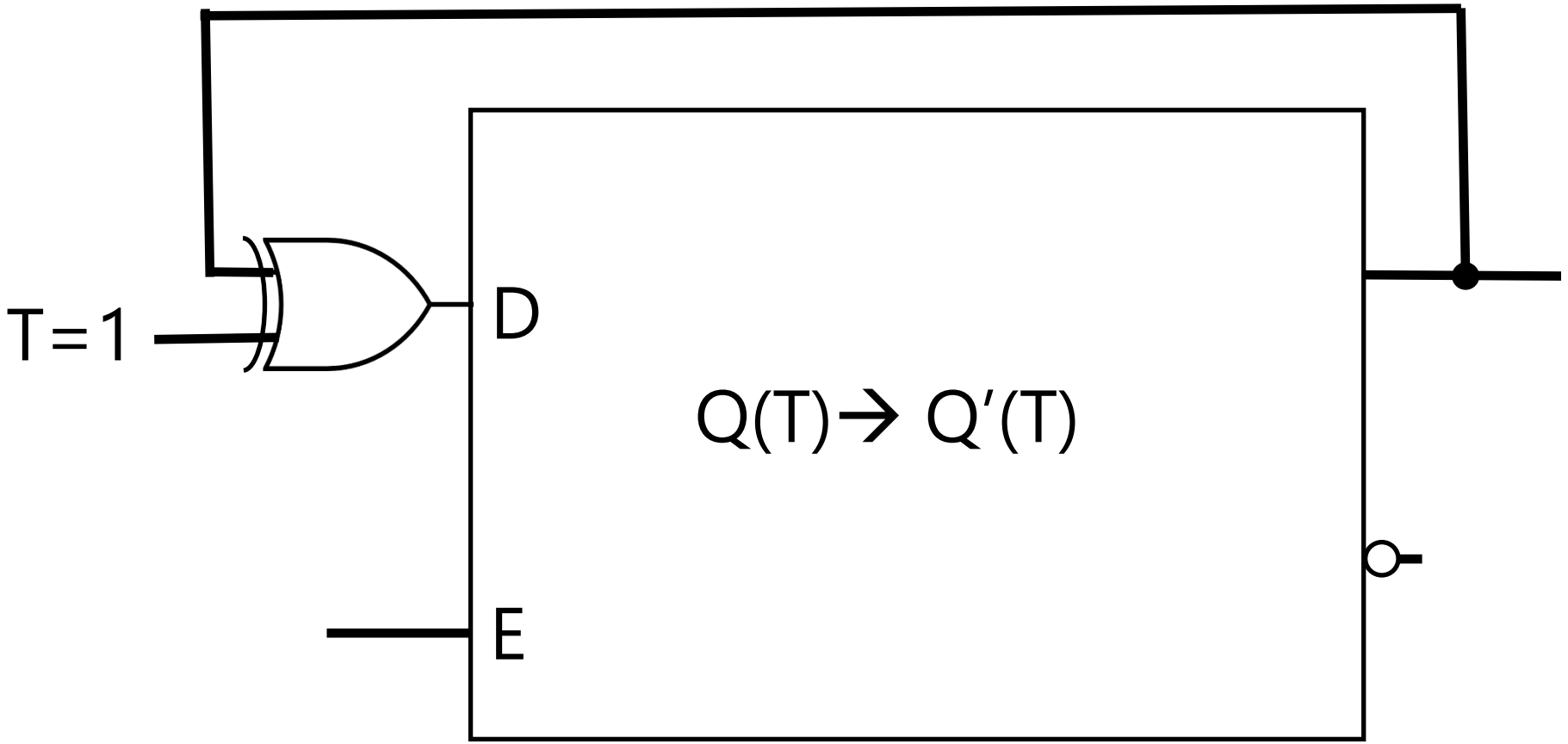


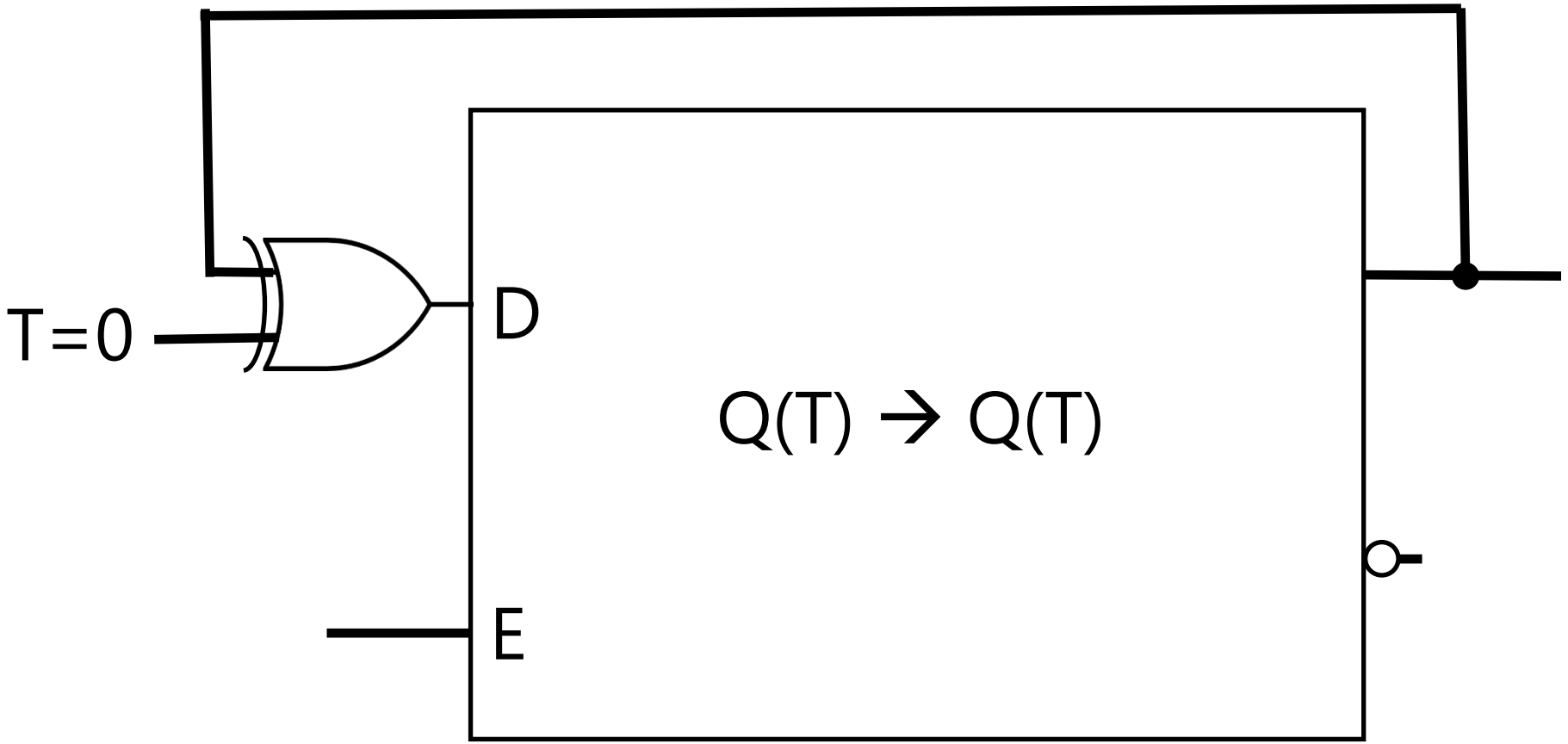
T *Latch*

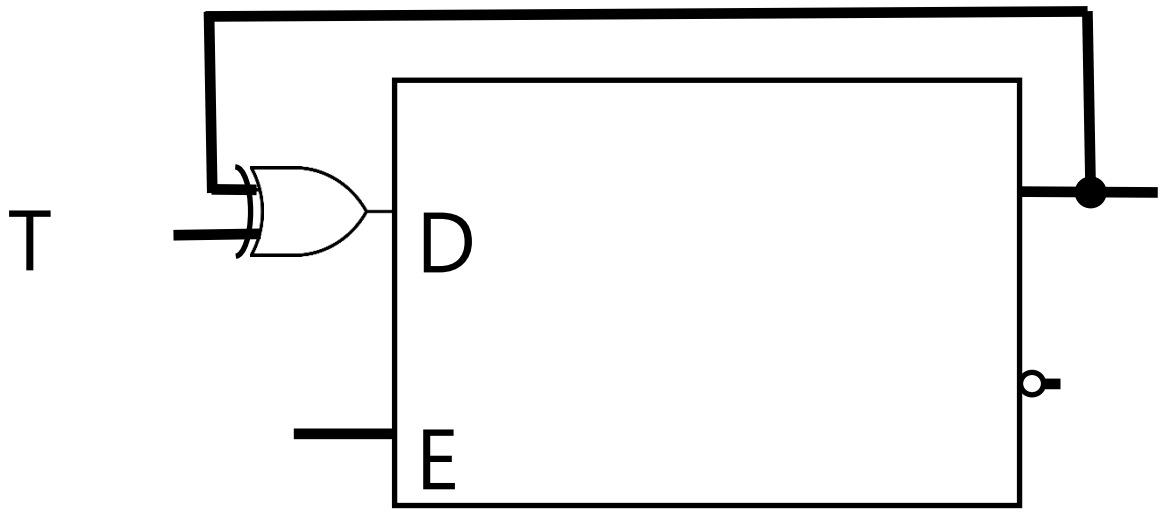


T	Q
0	Q_t
1	Q'_t


D
E
T
Q
0
Q_t
1
Q'_t
Q(T)
Q'(T)

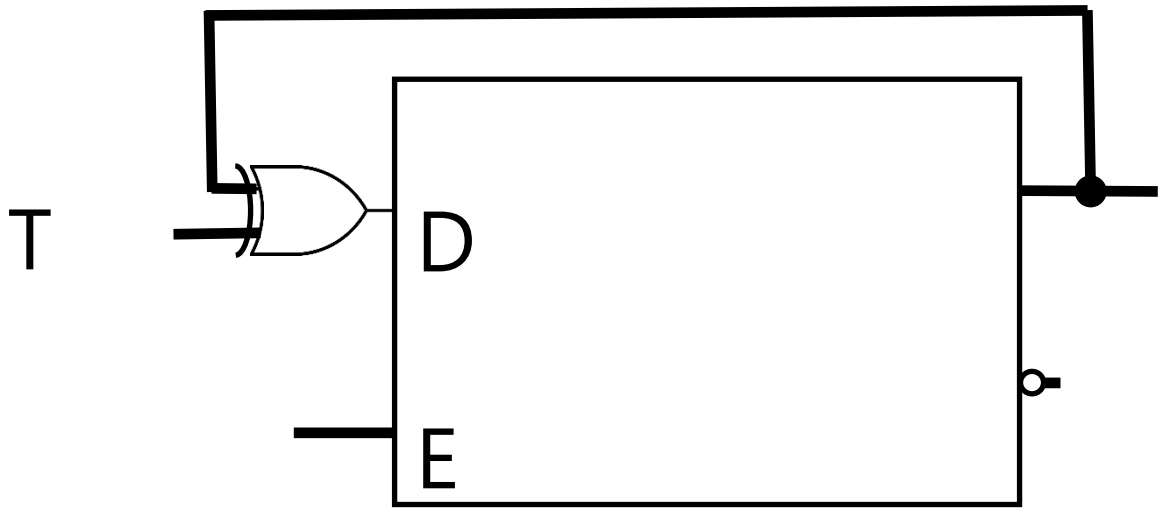

T=1
D
Q(T)→ Q’(T)
E


T=0
D
Q(T) → Q(T)
E



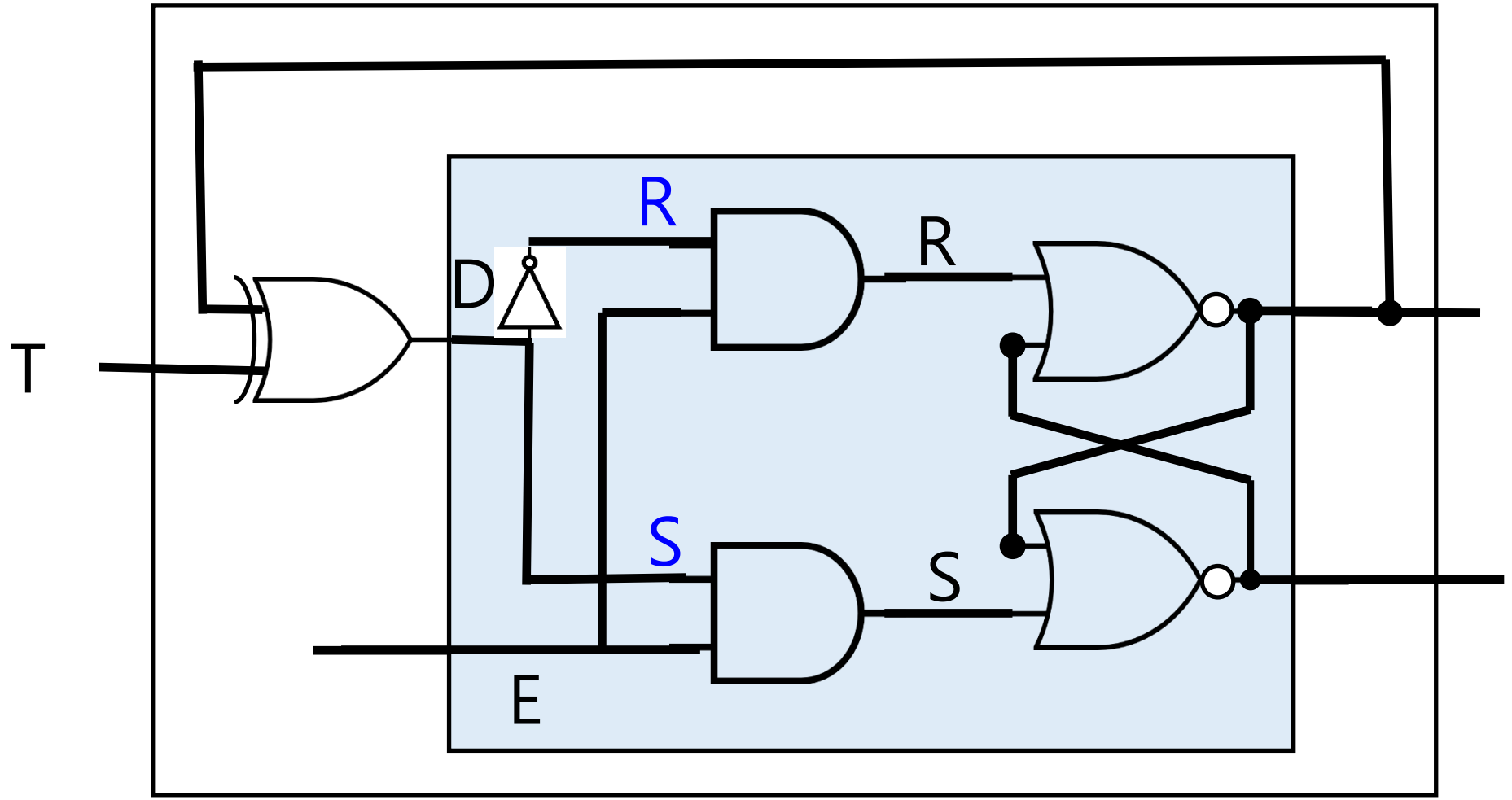
Store

T	D	Q
0	Q⊕0	Q
1	Q⊕1	Q’

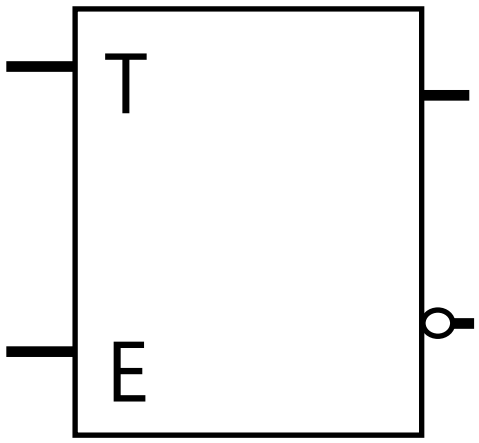


Complement

T	D	Q
0	Q⊕0	Q
1	Q⊕1	Q′


T
D
R
R
S
S
E

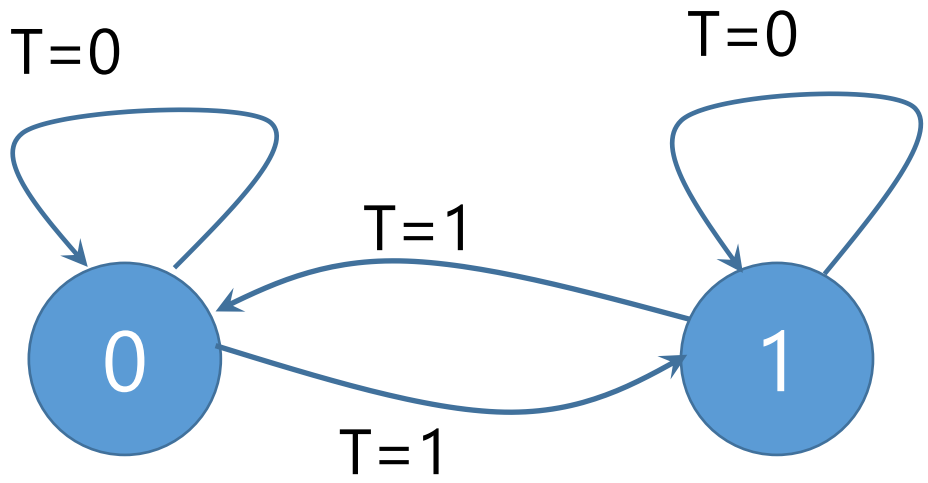
Block Diagram



Characteristic Table

T	Q
0	Q_t
1	Q'_t

State Transition Diagram



JK *Latch*

Jack St. Clair **Kilby**

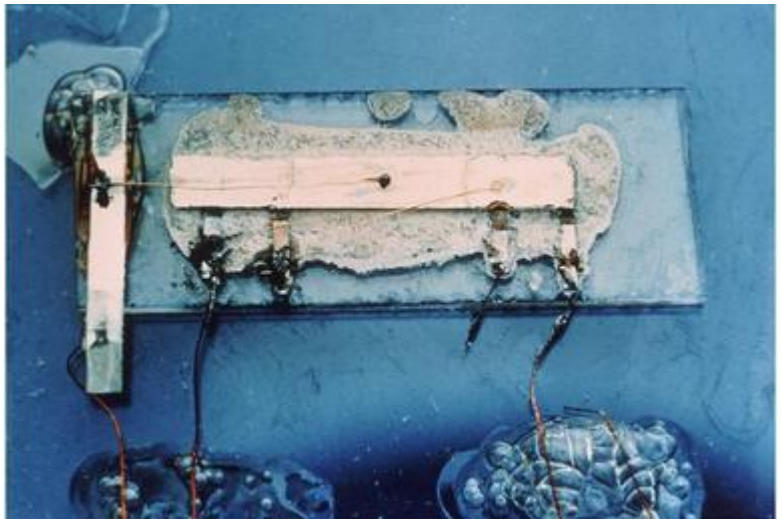
(Nov. 8, 1923 – June 20, 2005)

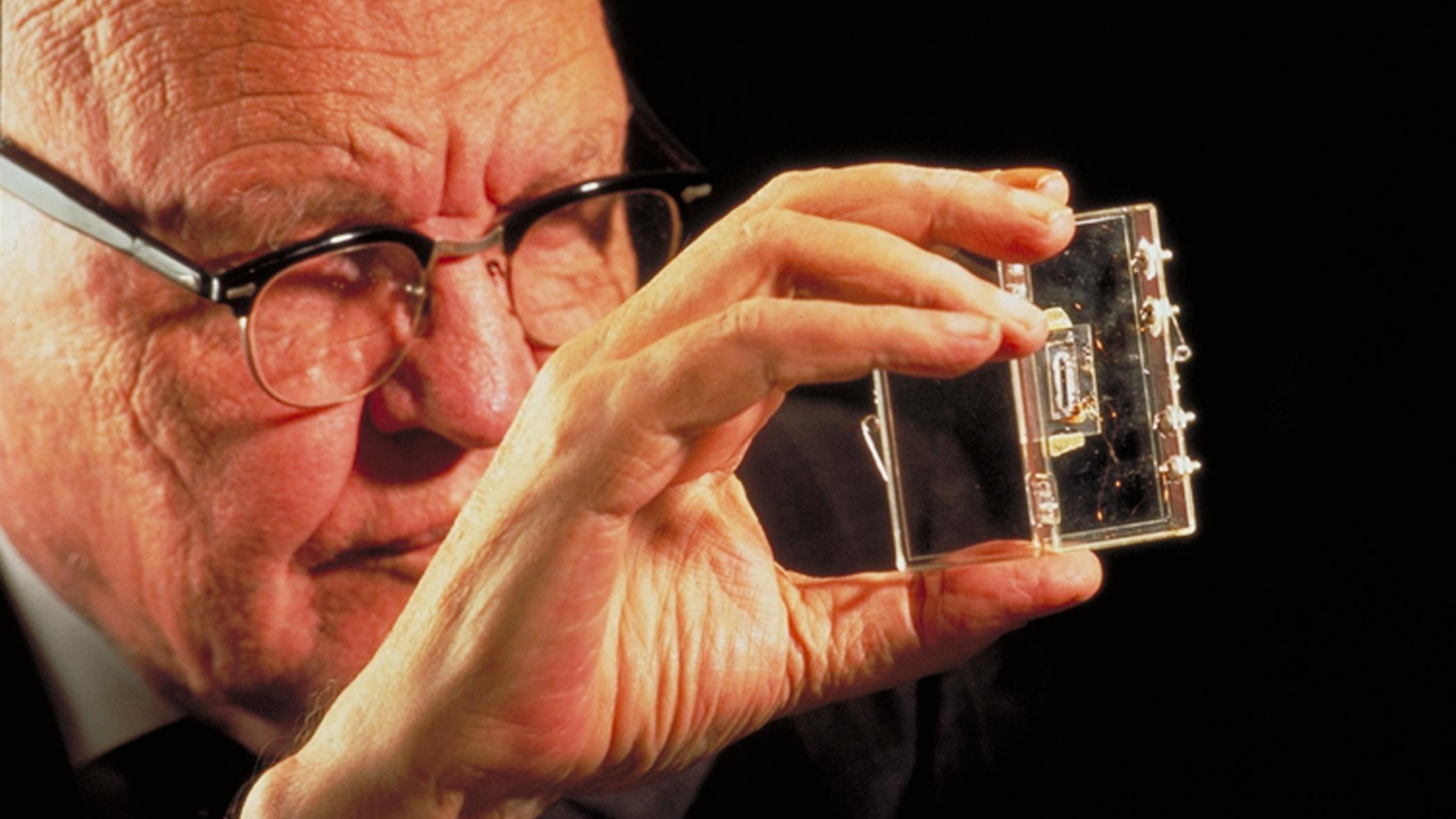
Electrical Engineer

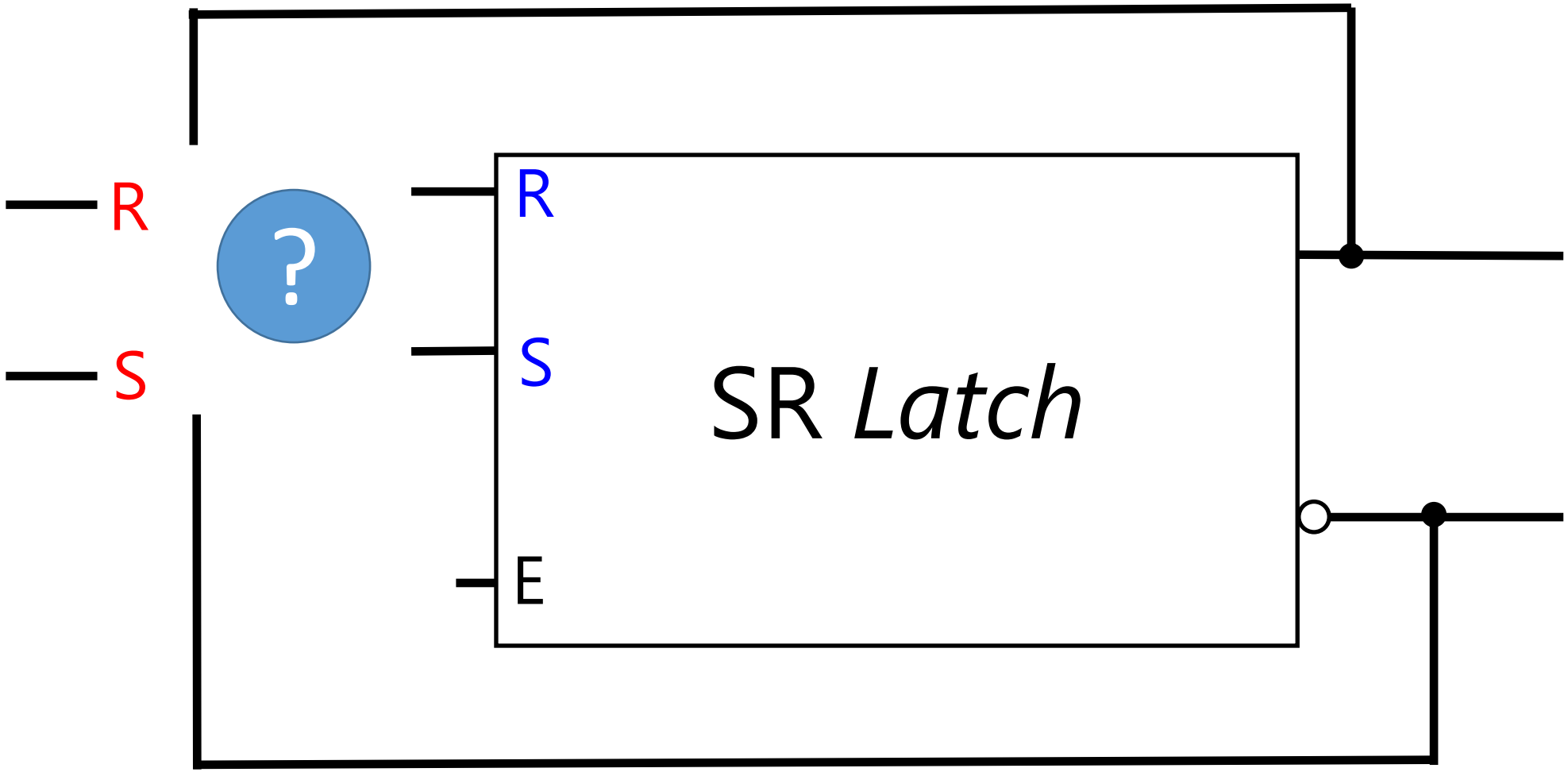
The 1st integrated circuit

1958

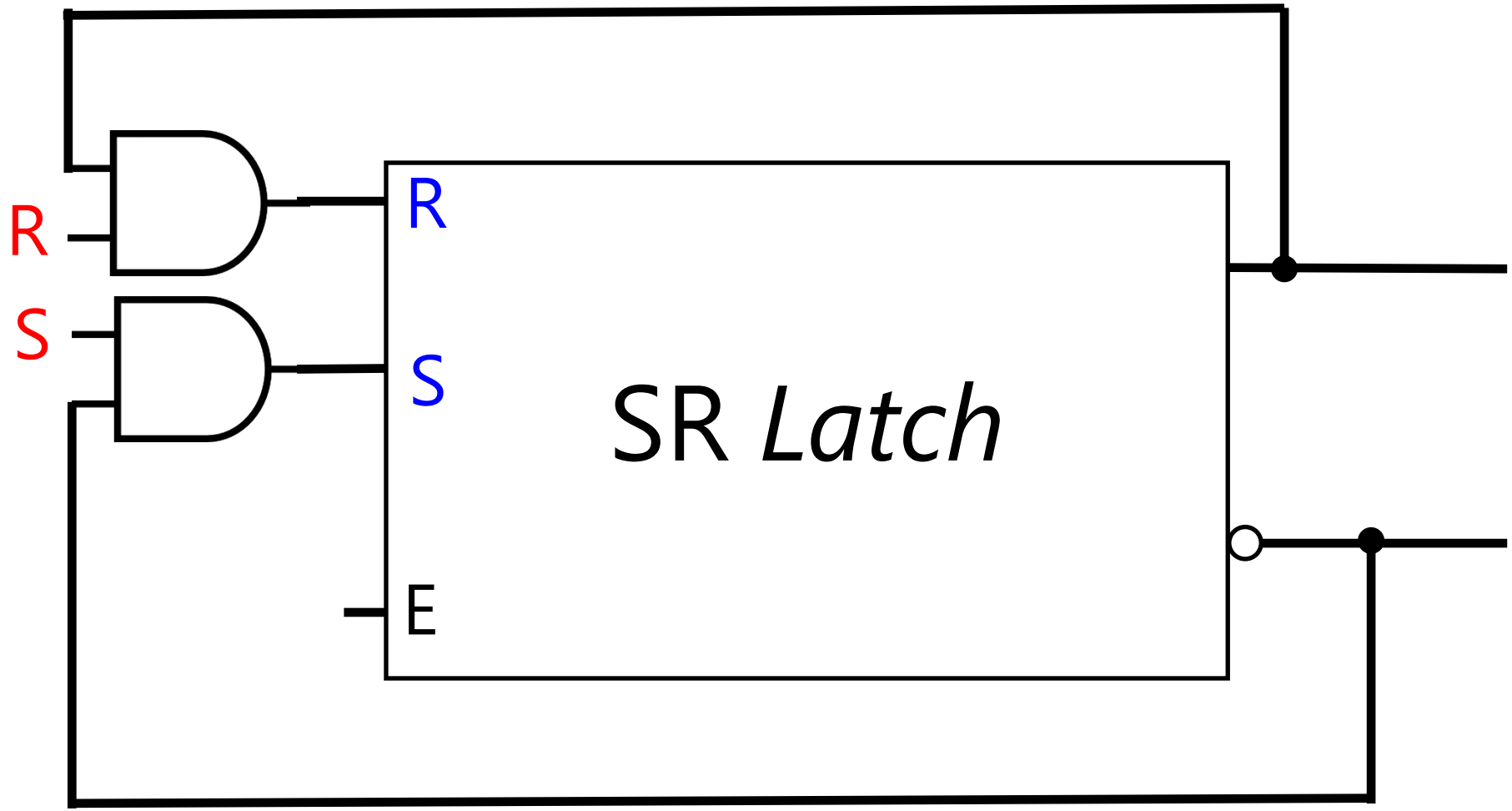
Nobel Prize in Physics, 2000

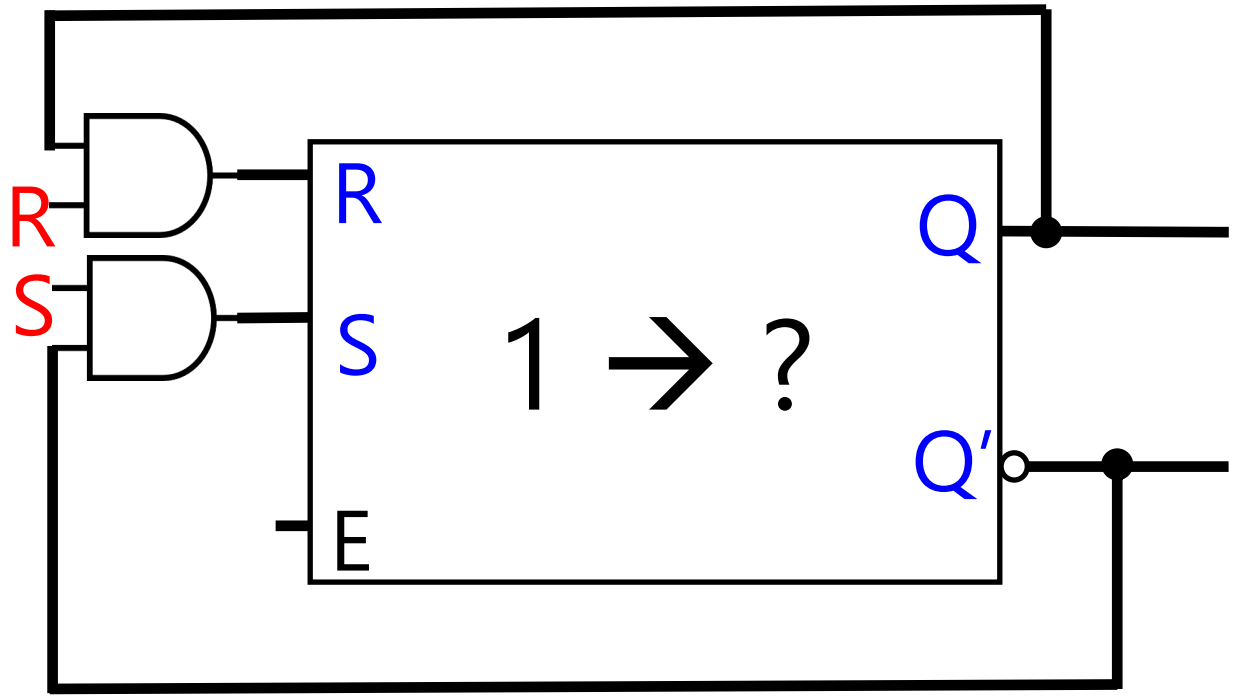




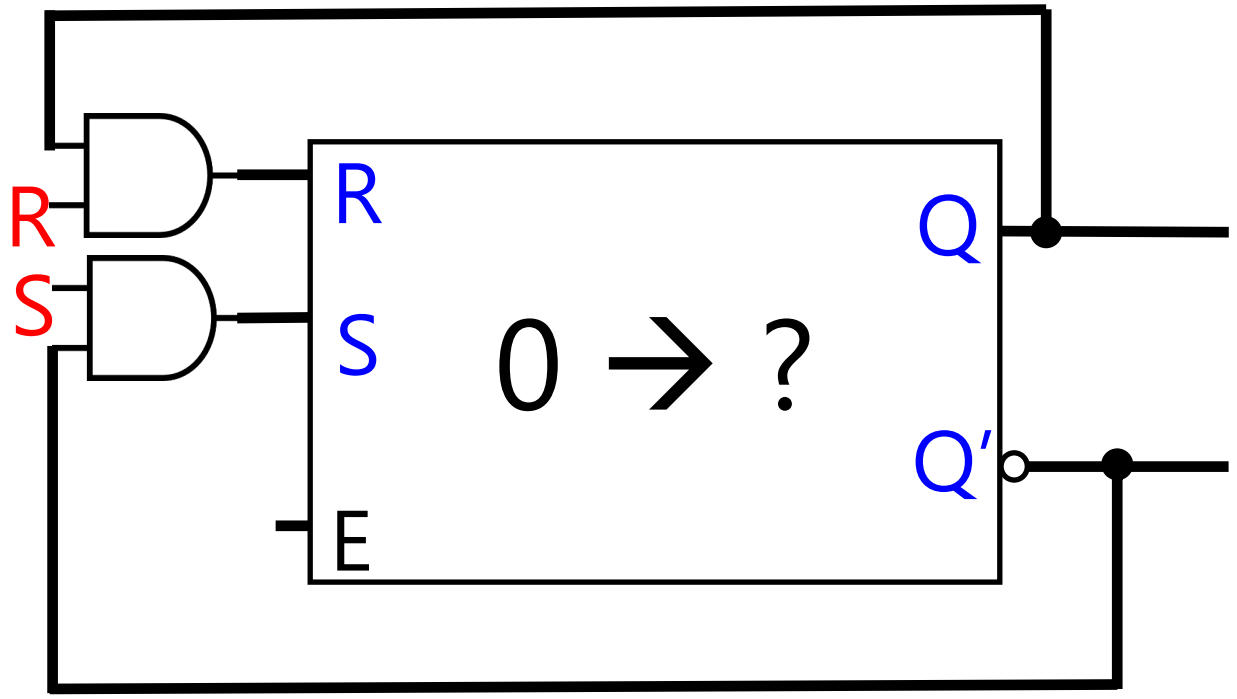


Although you have to guess, we'll see a design algorithm it ☺

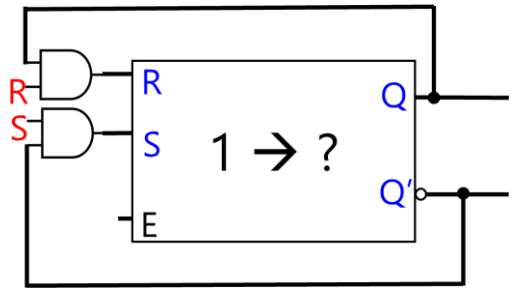

R
S
R
S
E
SR Latch



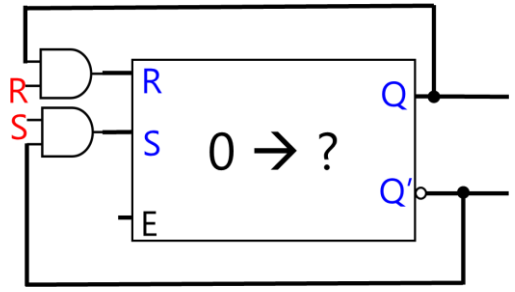
S	R	S	R	Q
0	0	0	0	Store=Q_t=1
0	1	0	1	Reset=0
1	0	0	0	Store=Q_t=1
1	1	0	1	Reset=0



S	R	S	R	Q
0	0	0	0	Store=Q_t=0
0	1	0	0	Store=Q_t=0
1	0	1	0	Set=1
1	1	1	0	Set=1



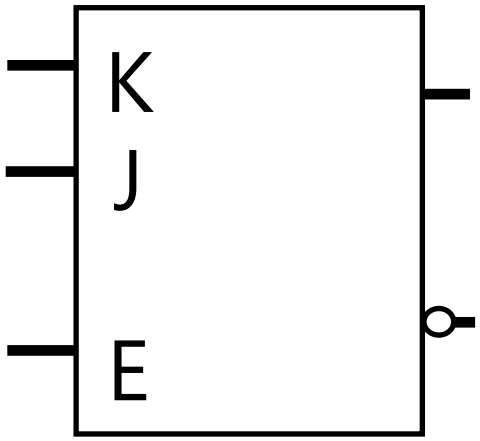
S	R	S	R	Q
0	0	0	0	Store=Q_t=1
0	1	0	1	Reset=0
1	0	0	0	Store=Q_t=1
1	1	0	1	Reset=0



S	R	S	R	Q
0	0	0	0	Store=Q_t=0
0	1	0	0	Store=Q_t=0
1	0	1	0	Set=1
1	1	1	0	Set=1

S=J	R=K	Q
0	0	Store=Q_t
0	1	Reset = 0
1	0	Set = 1
1	1	Comp. =Q'_t

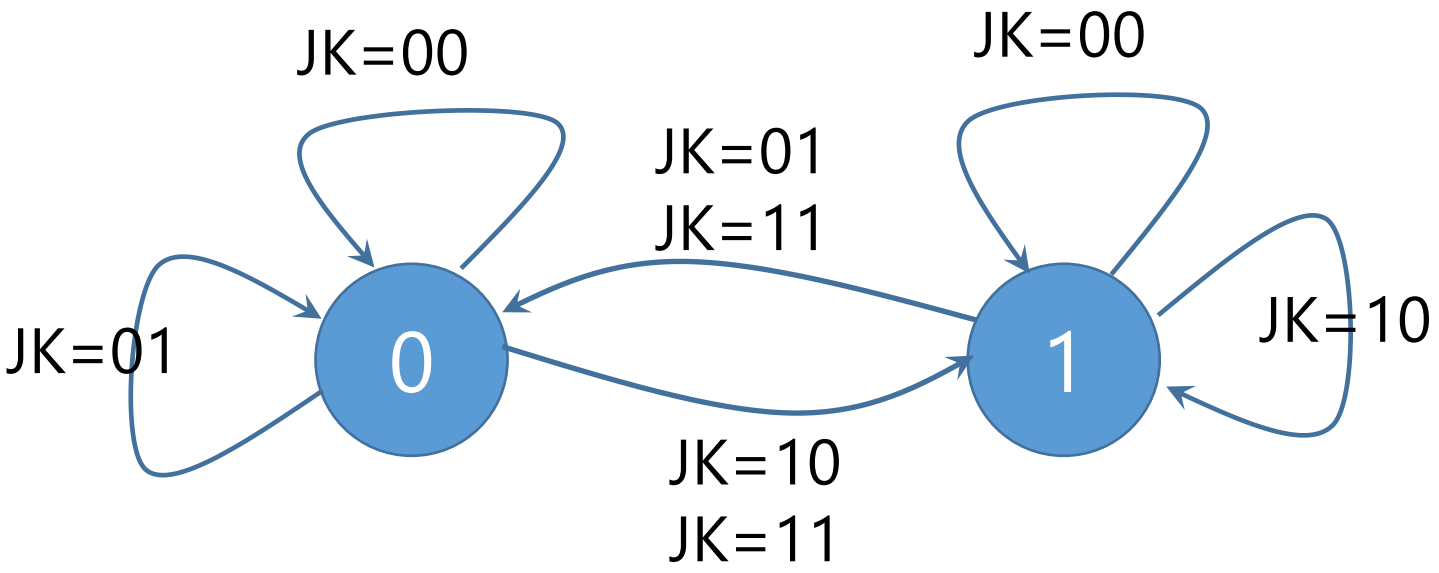
Block Diagram



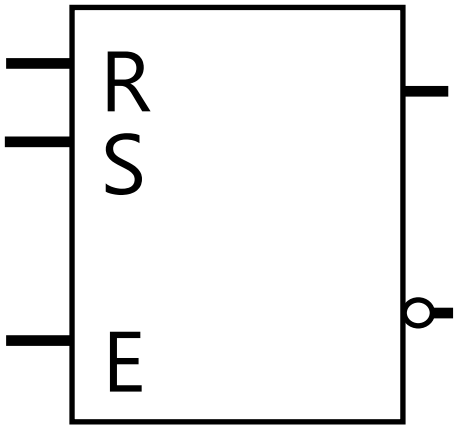
Characteristic Table

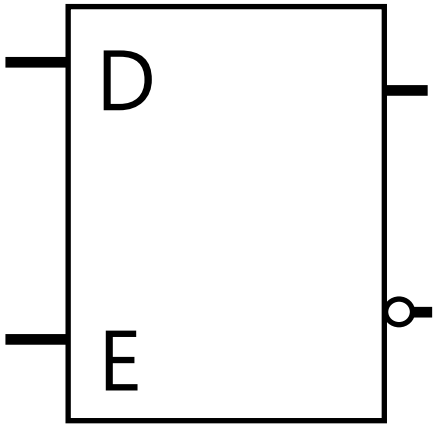
J	K	Q
0	0	Q_t
0	1	0
1	0	1
1	1	Q'_t

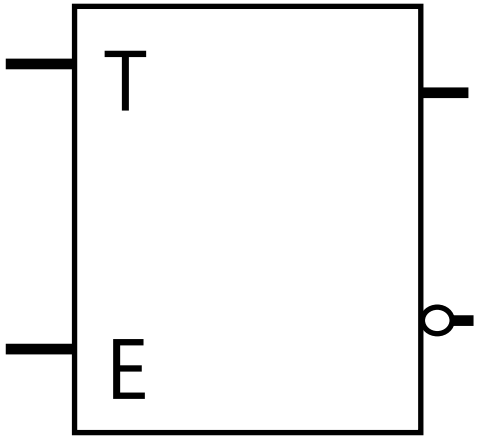
State Transition Diagram

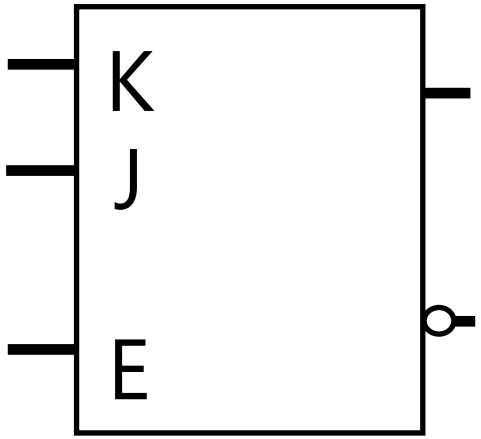


Recap









S	R	Q
0	0	Q_t
0	1	0
1	0	1
1	1	X

D	Q
0	0
1	1

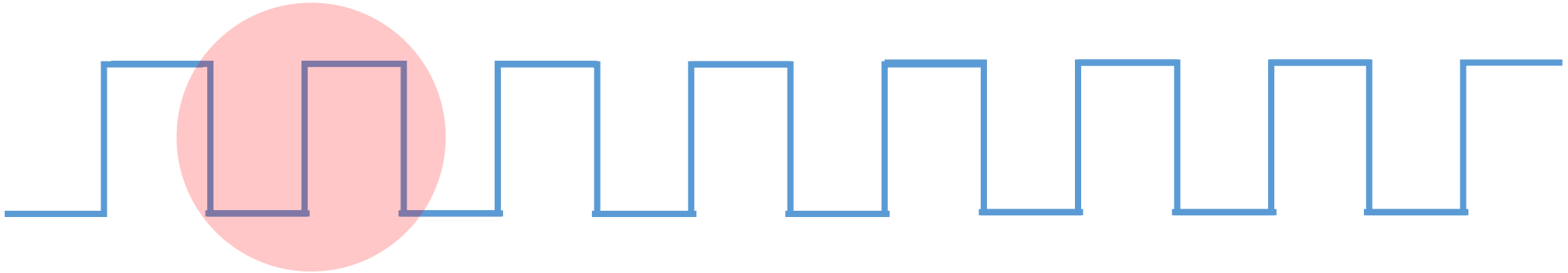
T	Q
0	Q_t
1	Q'_t

J	K	Q
0	0	Q_t
0	1	0
1	0	1
1	1	Q'_t

Clock

shortened as *clk*

timing device that generates a train of pulses



One period is called pulse!

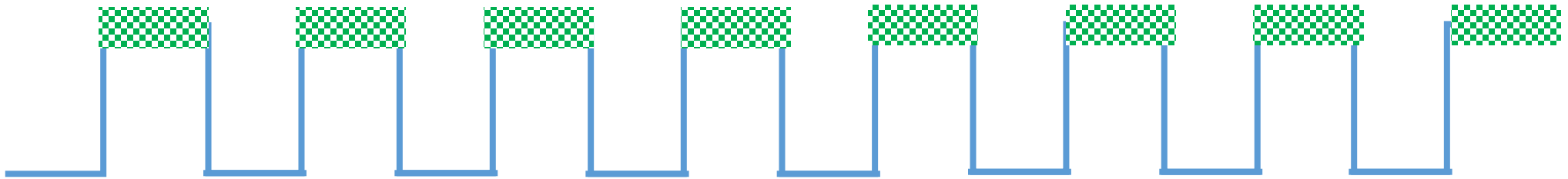
Clock

shortened as *clk*

Synchronize *all* the memory units *when* to work

Clock

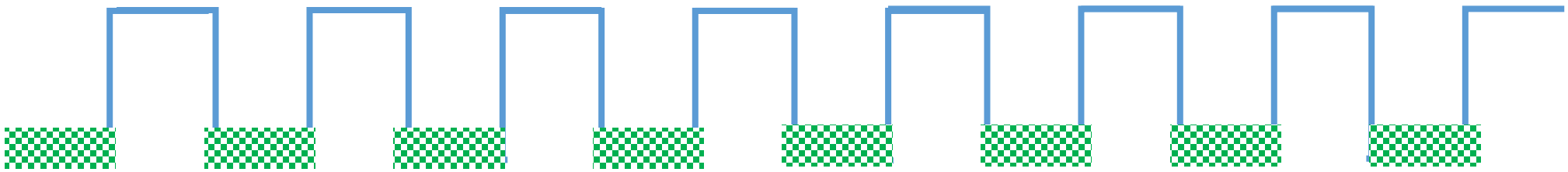
Positive Level (default)




R
S
E
SR Latch
Active High

Clock

Negative Level



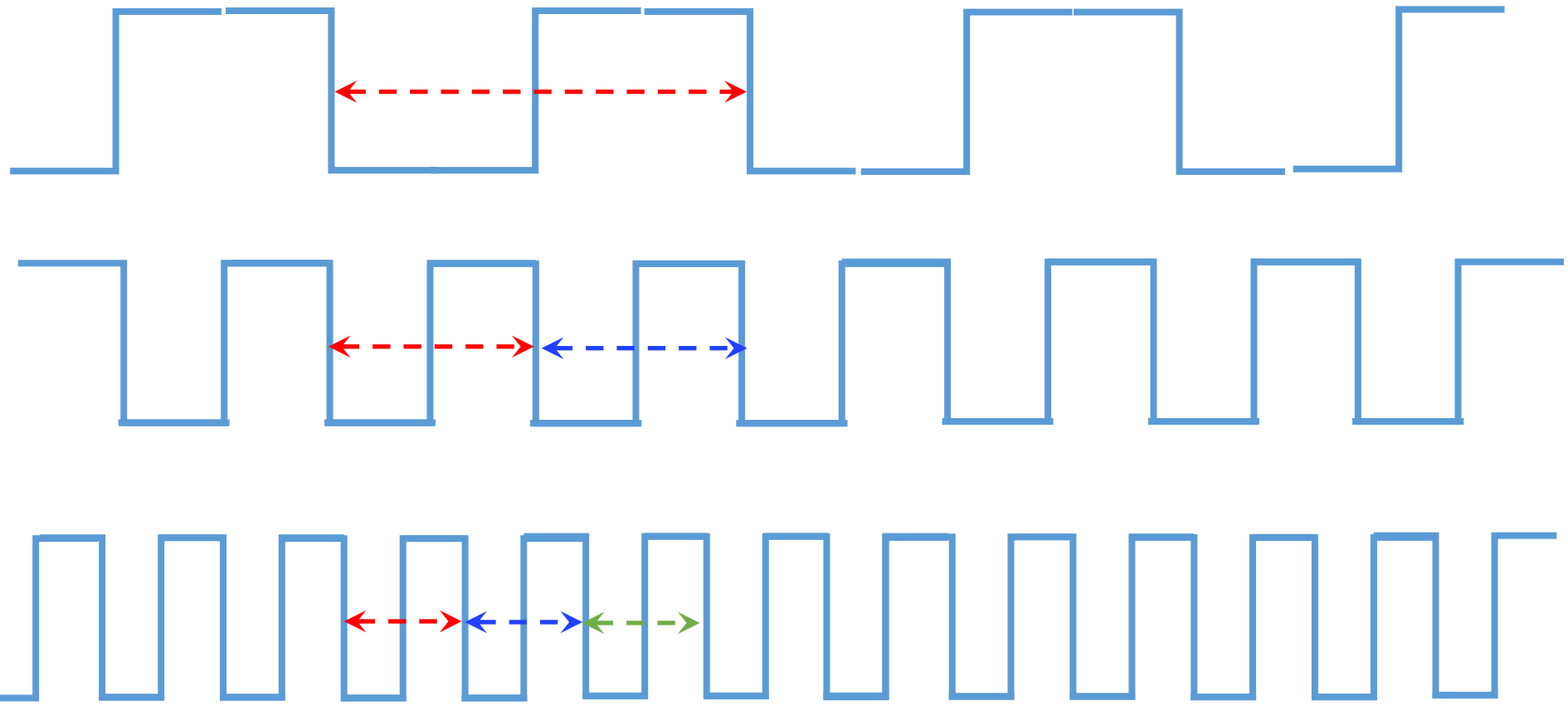

R
S
E
SR Latch
Active Low

Clock

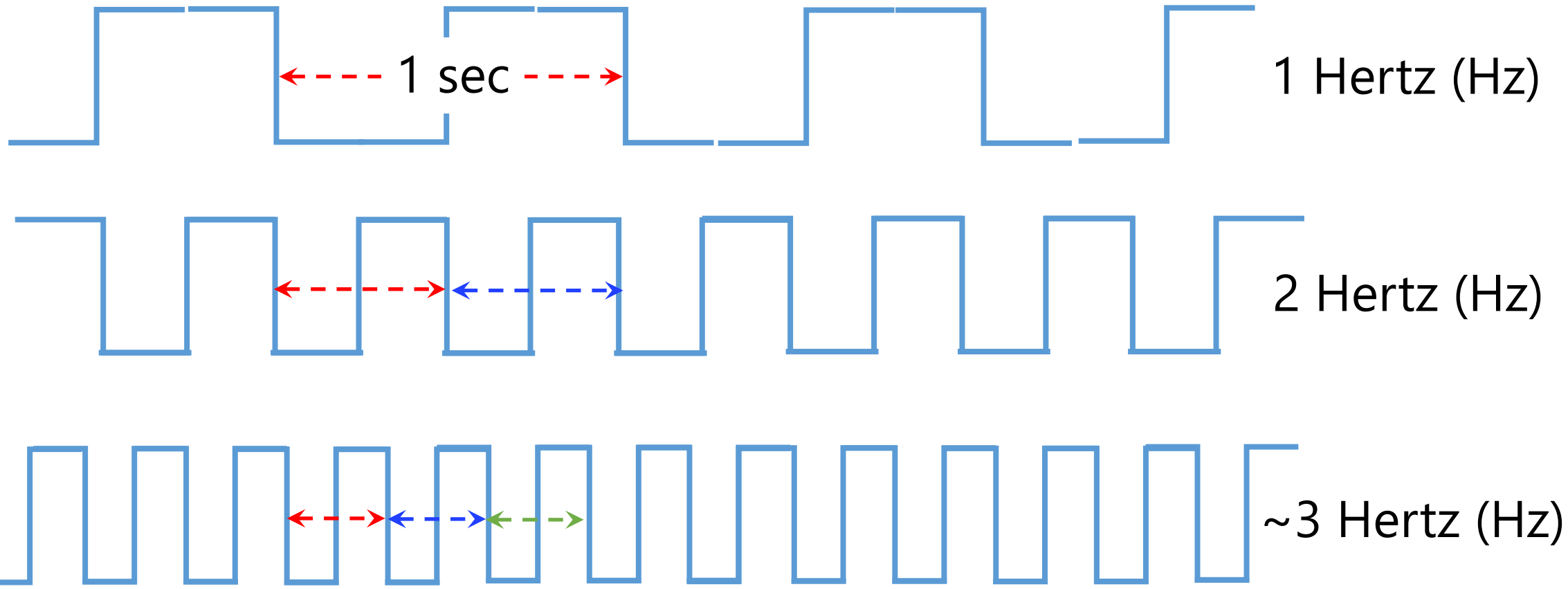
Frequency (Hz)

Heinrich Rudolf Hertz

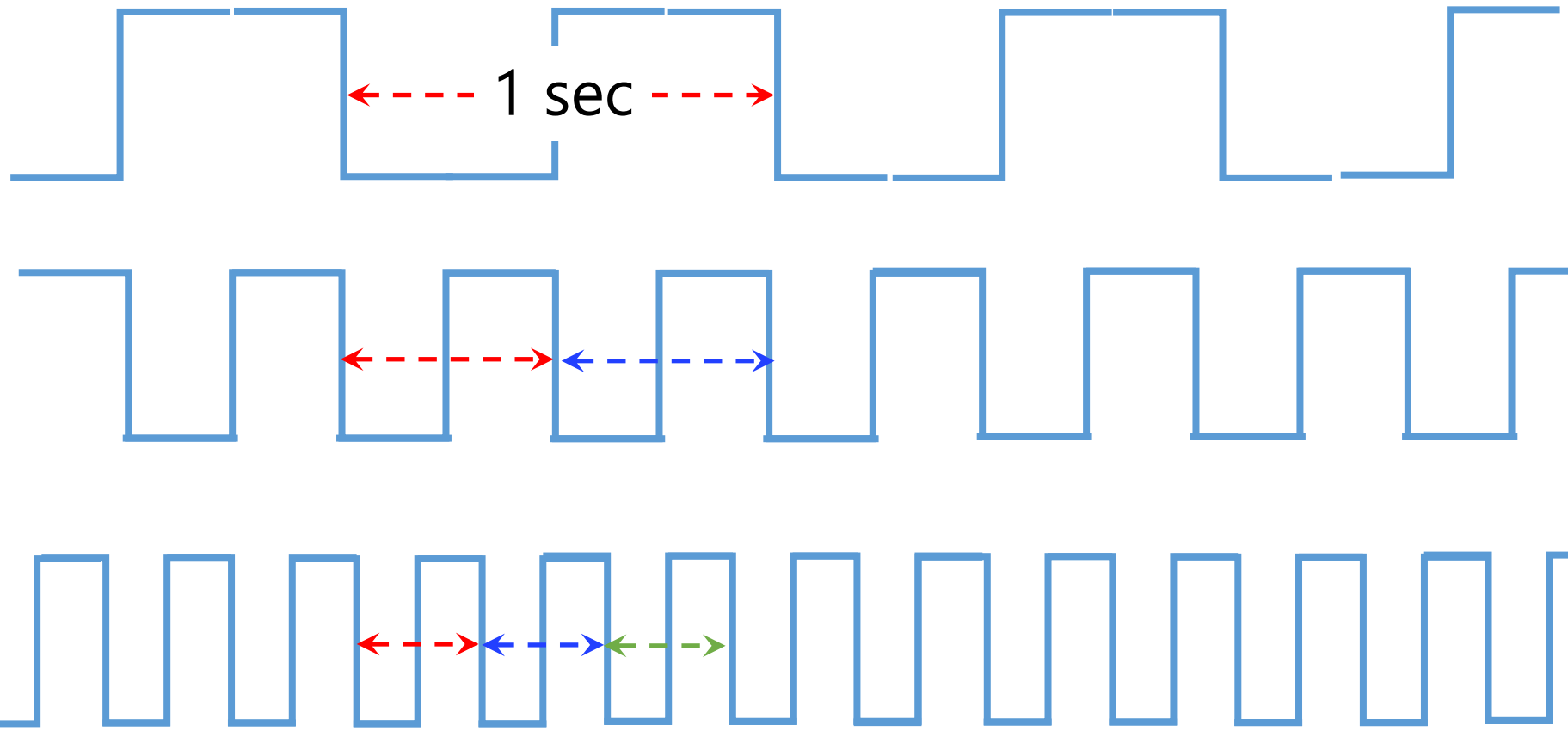
A Metric for Speed



How many pulse in 1 sec?



How many pulse in 1 sec?



How long is one pulse?
1/freq. (Hz)

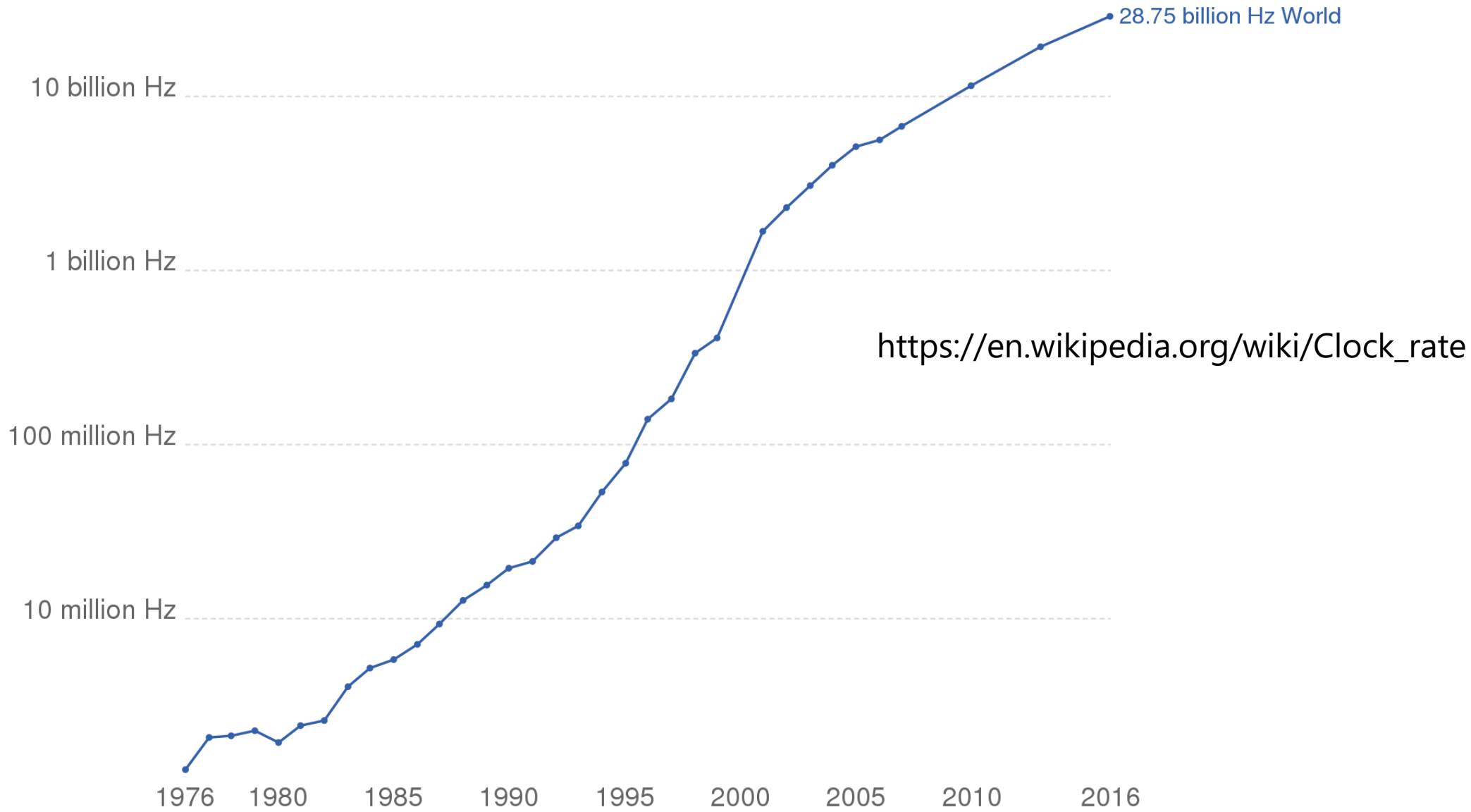
Intel® Xeon® Platinum 8380HL Processor (38.5M Cache, 2.90 GHz)

- 38.5 MB Cache
- 28 Cores
- 56 Threads
- 4.30 GHz Max Turbo Frequency

1,000,000,000 (one billion) Hz (hertz)
1,000,000,000 (one billion) pulse per sec!

Microprocessor clock speed

Microprocessor clock speed measures the number of pulses per second generated by an oscillator that sets the tempo for the processor. It is measured in hertz (pulses per second).



https://en.wikipedia.org/wiki/Clock_rate

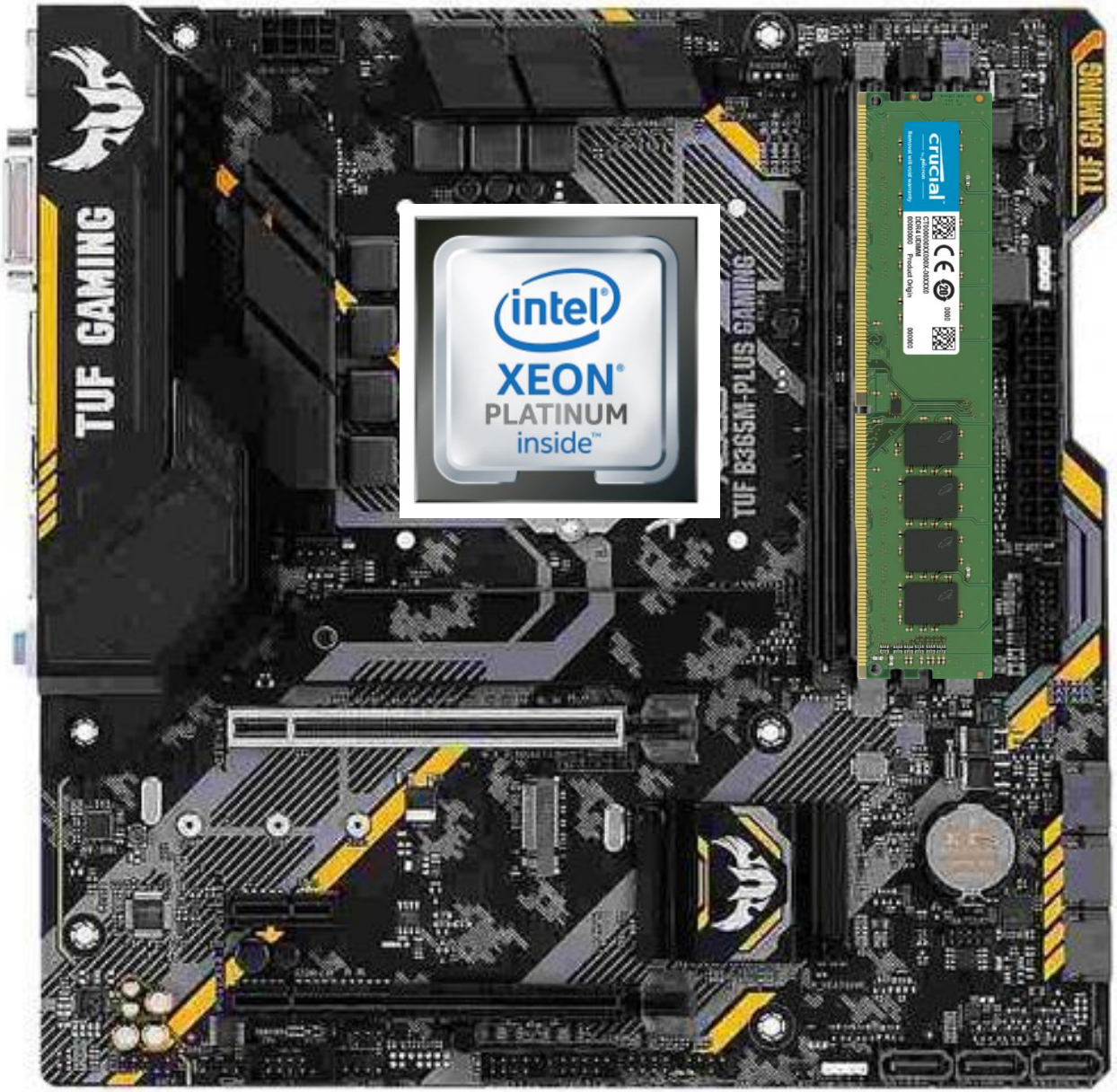
Source: Ray Kurzweil (2005, updated to 2016). The Singularity Is Near: When Humans Transcend Biology.

Speed - DDR4-2666

Warranty - Manufact

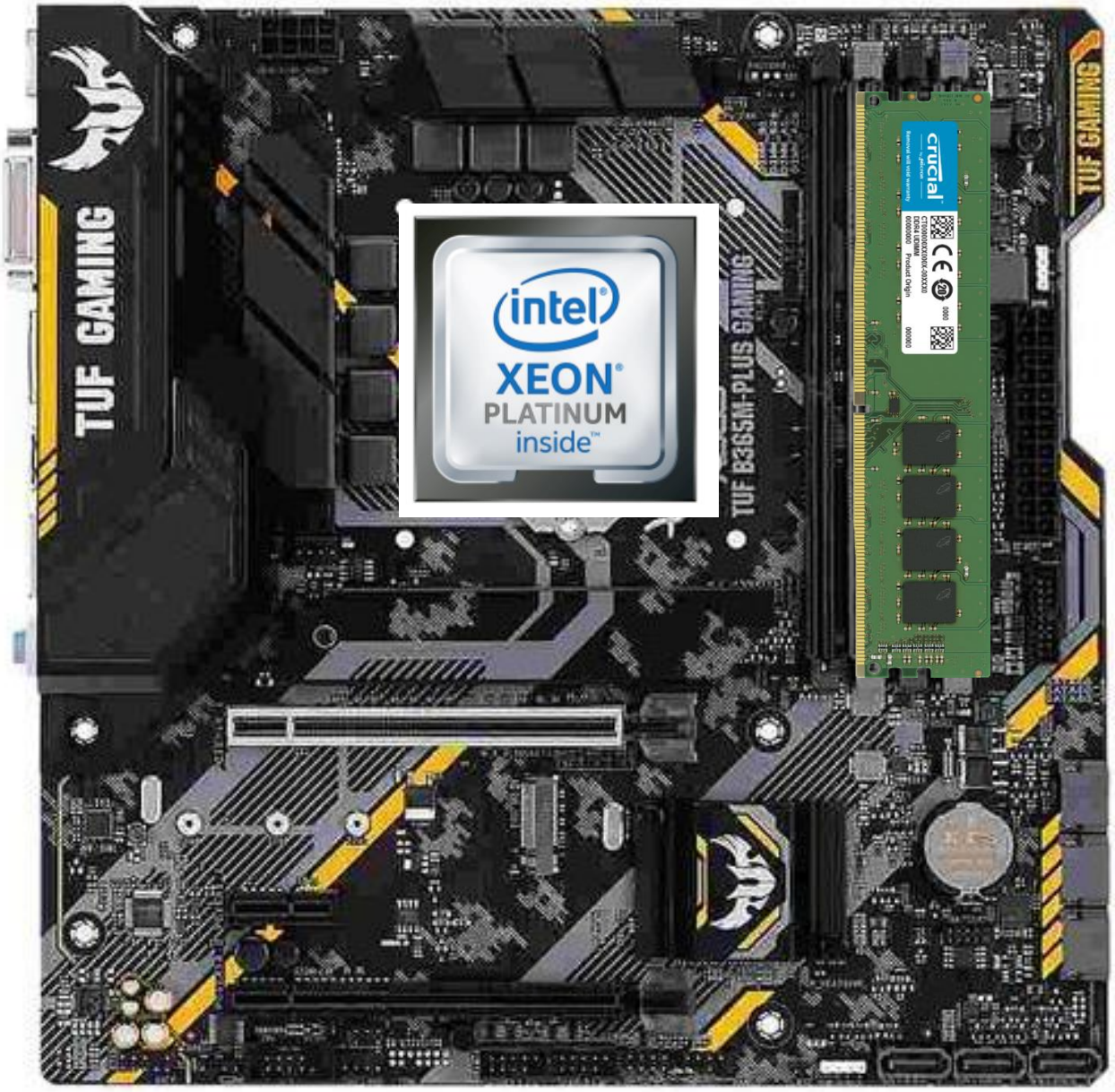
CAS latency - 19

The number of transfers per clock cycle times the clock frequency, expressed as MegaTransfers per second.



CPU: X Hz
Memory: Y Hz
Mainboard (BUS): Z Hz

Final Speed?

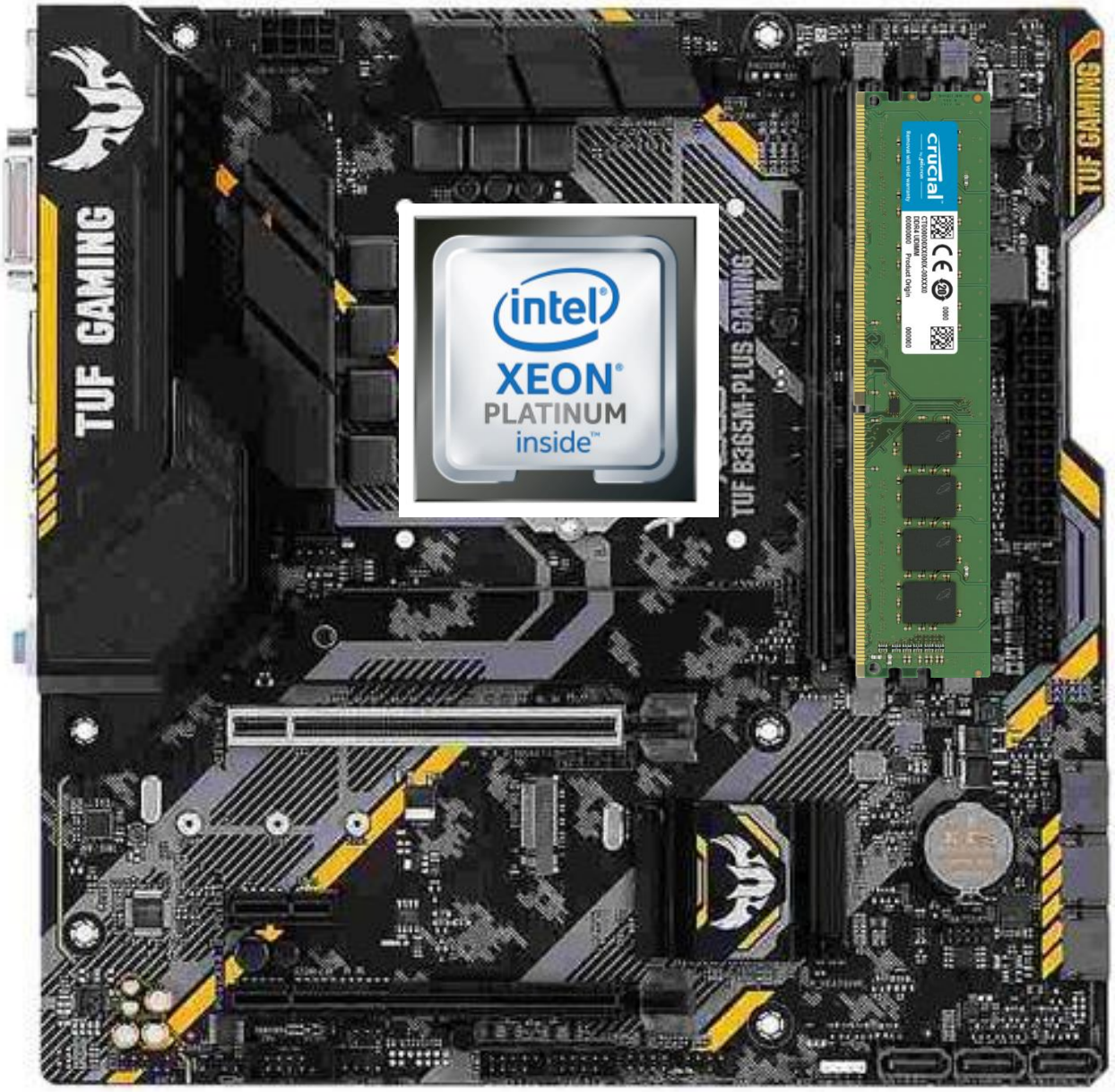


CPU: X Hz
Memory: Y Hz
Mainboard (BUS): Z Hz

At market:

X > Y = Z

X=2.9GHz
Y=Z= 2.6GHz



CPU: X Hz
Memory: Y Hz
Mainboard (BUS): Z Hz

Final Speed:

CPU internal: X
CPU external ←→ Memory
Y=Z= 2.6GHz

Overclock?

Flip-Flop