University of Windsor

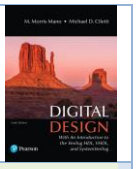
School of Computer Science
Faculty of Science

COMP-2650: Computer Architecture I: Digital Design
Winter 2021

Course Outline (Syllabus) v1.2	
Description[1]	Digital systems are indispensable and the foremost means of technology in today's everyday life that we refer to the present period as the *digital age*. Digital systems are used in communication, traffic control, spacecraft guidance, medical treatment, and many other enterprises. Today, a myriad of digital devices surrounds us, including digital telephones (Smart Phones), digital televisions (Smart TVs), digital cameras, and, of course, digital *computers.* Although these devices enable us to execute commands easily, they involve precise execution of a sequence of complex internal instructions underneath at the hardware level indeed. This course, *COMP-2650: Computer Architecture I: Digital Design*, provides a first introduction to the design of digital circuits and computer architecture following a bottom-up approach, from basic logic gates to circuits like adders, decoders, flip-flops, registers to be then combined into more complex units such as memory and processors as well as a whole computer system. Topics covered include number systems, switching algebra, logic gates, circuit minimization, combinational circuit, read-only memory, random-access memory, programmable logic, synchronous and asynchronous sequential circuits, latches, flip-flops, registers, counters, register transfer language, and CPU architecture overview. This course is followed by a complementary course *COMP-2660: Computer Architecture II: Microprocessor Programming,* where more in-depth topics such as memory segmentation are covered. It is essential to understand how a modern computer works underneath, from the bottom up, to develop efficient programs by knowing the followings: ○ Physical memory layout when using data types, e.g., (un)signed numbers and floating-point, and data structures like arrays, linked lists, and hash tables, ○ Boolean algebra and applying logical operation, ○ How CPU oscillates the program's statements and commands. And at the end of the day, everything runs on hardware*!*
Learning Outcome	Blackboard → COMP2650-1-R-2021W: Computer Architecture I: Digital Design → Learning Outcome
Course Type	Required
Program Level	COMP 2
Prerequisite	COMP-1400: Introduction to Algorithms and Programming
Required for	COMP-2660: Computer Architecture II: Microprocessor Programming COMP-3150: Database Management Systems COMP-3300: Operating Systems Fundamentals COMP-3500: Introduction to Multimedia Systems COMP-3670: Computer Networks
Instructional Hour	3:00 lecture + 01:20 laboratory, each week.
Lecture	Tuesday & Thursday, 10:00AM - 11:20AM, Blackboard Collaborate Ultra → Classroom
Office Hour	Tuesday & Thursday, 11:30AM - 12:30AM, Blackboard Collaborate Ultra → Office
Homepage	blackboard.uwindsor.ca → COMP2650-1-R-2021W: Computer Architecture I: Digital Design
Instructor	Name: Hossein Fani Email: hfani@uwindsor.ca[2] Page: hfani.myweb.cs.uwindsor.ca Office: 5111 Lambton Tower 

[1] This course is based on schematic design only and Hardware Description Language (HDL) is not covered. The selected programming language is C.

[2] Wishing to contact the instructor via email about the course, please use [uwinid]@uwindsor.ca and indicate full name, studentid, a course title.

Book	Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog, 6/E M. Morris R. Mano, Michael D. Ciletti ISBN-10: 0134549899, ISBN-13: 9780134549897 ©2018 Pearson	
Marking Scheme	**Weekly Lecture Assignments (Lecs)**	20%
	Weekly Lab Assignments (Labs)[3]	20%
	Midterm Exam	30%
	Final Exam	30%
	Discussion Board (Bonus+)	5%
Remarks	The written reports will be assessed not only on their academic merit but also on the student's communication skills as exhibited through the reports. To achieve a passing grade, the students must achieve at least 50% of the entire marking scheme. The fraction mark is rounded to ceiling. The students earn final course grades as per the Senate policy for Grading and Calculation of Averages and Grading Key.	
Theoretical[4]	**Lec01B: Meet and Greet** Course Outline.	Jan. 07
	Lec02A: Number Systems I Binary, Octal, and Hexa Numbers. Number-base Conversions. **Lec02B: Number Systems II** Complements of Numbers. Signed Numbers. Binary Codes.	Jan. 12 Jan. 14
	Lec03A: Digital Systems Binary Systems. *Jan. 20 Last Day Academic Add/Drop* **Lec03B: Boolean and Switching Algebra** Axiomatic Definition, Basic Theorems, and Properties of Boolean Algebra.	Jan. 19 Jan. 21
	Lec04A: Logic (Digital) Gates Boolean Functions. Digital Logic Gates. **Lec04B: Canonical Forms** Canonical Forms. Universal Gate (s)	Jan. 26 Jan. 28
	Lec05A: Gate-Level Minimization I Algebraic Manipulation. Standard Forms. *Feb. 03 Financial Drop Date* **Lec05B: Gate-Level Minimization II** The Map Method. Don't Care Conditions.	Feb. 02 Feb. 04
	Lec06A: Combinational Logic I Analysis. Design. Two-Level Design AND-OR, OR-AND. **Lec06B: Combinational Logic II** Two-Level Design NAND, NOR. Binary Code Convertors.	Feb. 09 Feb. 11
	Lec07: Reading Week: No Class	Feb. 13 – 21
	Lec08A: Midterm Exam **Lec08B: Combinational Logic III** Adders. Subtractors. Multipliers.	Feb. 23 Feb. 25
	Lec09A: Combinational Logic IV Decoders. Encoders. **Lec09B: Combinational Logic V** Multiplexers. Demultiplexers.	Mar. 02 *Midterm Exam Grade Release* Mar. 04
	Lec10A: Sequential Logic Sequential Circuits. Latches. **Lec10B: Synchronous Sequential Logic I** Clocked Sequential Circuits. Flip-Flops	Mar. 09 Mar. 11
	Lec11A: Synchronous Sequential Logic II Analysis: State Diagram, Timing Diagram, State Table. *Mar. 17 Last Day Voluntarily Withdraw* **Lec11B: Synchronous Sequential Logic III** Design: State Diagram, Timing Diagram, State Table.	Mar. 16 Mar. 18
	Lec12A: Synchronous Sequential Logic IV Registers and Counters. Shift Registers. **Lec12B: Asynchronous Sequential Logic V** Ripple Counters.	Mar. 23 Mar. 25

[3] More on Labs can be found in the Laboratory Guide available in Blackboard → COMP2650-1-R-2021W: Computer Architecture I: Digital Design → Labs

[4] This is a preliminary schedule. The material and depth and order of presentation are subject to change at the discretion of the instructor and student pace.

	Lec13A: Computer Systems I Memory. RAM. ROM **Lec13B: Computer Systems II** Processor	Mar. 30 Apr. 01
	Lec14A: Programmable Logic	Apr. 06 *Apr. 07 Last Day: Winter 2021 Classes*
	Lec15: Final Exam Date and Time to be Announced.	Apr. 12 – 22
Laboratory[5]	Section 53, Wednesday 04:00 PM - 05:20 PM, Blackboard Collaborate Ultra → Labroom	
	Section 52, Wednesday 05:30 PM - 06:50 PM, Blackboard Collaborate Ultra → Labroom	
	Section 51, Wednesday 07:00 PM - 08:20 PM, Blackboard Collaborate Ultra → Labroom	
	Section 54, Wednesday 08:30 PM - 09:50 PM, Blackboard Collaborate Ultra → Labroom	
Attendance	Encouraged but not mandatory due to time zone accommodation in the COVID-19 pandemic era. Lecture recordings with captions along with presentation slides will be made available.	

Notes to Students:

1. **Equity, Diversity, and Inclusiveness (EDI):** This course, along with all its components such as lab sections are, without question, safe places for students of all races, genders, sexes, ages, sexual orientations, religions, disabilities, and socioeconomic statuses. Disrespectful attitude, sarcastic comments, offensive language, or language that could be translated as offensive and/or marginalize anyone are absolutely unacceptable. Immediate actions will be taken by the instructor to protect the safety and comfort of the students. An ethnically rich and diverse multi-cultural world should be celebrated in the classroom. The instructor, too, must treat every student equally and with the respect and compassion that all students deserve. Furthermore, UWindsor is committed to combatting sexual misconduct. All members are required to report any instances of sexual misconduct, including harassment and sexual violence, to the Sexual Misconduct Response & Prevention Office so that the victim may be provided appropriate resources and support options.

2. **Student Accessibility Services:** Students who have special needs due to legitimate medical reasons should notify the Student Accessibility Services and the instructor at the beginning of the course and before any assessment.

3. **Weekly Lab and Lecture Assignment:** Assignments are of two types of i) lecture assignments (Lecs) and ii) lab assignments (Labs). Labs are explained in the laboratory guide for each week and are mainly programming assignments in C. However, lecture assignments are based on the content of lectures each week and are primarily problem-solving exercises.
   - Lab instructors are available at lab sections to explain and help the student in both types of assignments.
   - Assignments are expected to be submitted on the assigned due date and time.
   - Late submission is not accepted and receive zero (left unmarked!) unless a verifiable reason with appropriate documentation is provided.
   - The students should follow the submission procedure for each assignment. Failure to follow the procedure (e.g., incorrect, unreadable, and missing file attachments as instructed) heavily penalizes the submission.
   - Each assignment must be done *individually*.
   - The last 7 calendar days prior to, and including, the last day of classes are free from any procedures for which a mark will be assigned.
   - For any issue regarding the submissions, students should foremost communicate with their lab instructor based on the lab section they registered:
     - Request for another submission,
     - Accept late submission for a verifiable reason,
     - Review and appeal on markings, and etc.

     If not resolved, students reach out to the course instructor.

4. **Midterm Exam:** Should a student miss a midterm exam, with appropriate documentation and verifiable reason, the weight of the missed midterm exam will be moved to the final exam. The results of the midterm exam will be released to students at least 2 days prior to the voluntary withdrawal deadline as per the Senate Bylaw 54: Undergraduate Academic Evaluation Procedures.

[5] There is no lab session in the first and last weeks of the course as well as the reading week. For more information refer to Laboratory Guide v1.0.

5. **Final Exam:** Students who miss a final exam for a verifiable reason and with appropriate documentation will be given a make-up exam prior to the submission of final course grades that carries the same weight and measure the same knowledge.
6. **Make-up of the Make-up:** There will be *no* make-up of the make-up exam, and the final grade will be assigned based on overall work.

7. **Required Documentation for Missing Exam:** Medical or compassionate documents for the missing of an exam must be submitted within 1 week of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

8. **Accommodation for Religious or Spiritual Observance:** Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than 2 weeks prior to the conflict in question (in the case of final examinations within two weeks of the release of the examination schedule). In extenuating circumstances, this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Timely requests will prevent difficulties in arranging constructive accommodations.

9. **Academic Accommodation:** A student who has 3 or more major in-term evaluations scheduled or due within 24 hours may apply, no later than the end of the first quarter of classes, to seek an appropriate accommodation such as a due date extension, alternative assignment, or rescheduled exam.

10. **Appeal:** Students have the right to review the exams and assignments marking within 1 week of their release.

11. **Bonus:** Students are encouraged to initiate course-related topics and participate in discussions in forums in Discussion Board available in *COMP2650-1-R-2021W: Computer Architecture I: Digital Design → Discussion Board*. Motivating bonus points of +5% have been allocated in the marking schema.

12. **Policies, Bylaws, and Procedures:** Students are required to adhere to all relevant policies, bylaws, and procedures at the University of Windsor, including, but not limited to, the student code of conduct, academic integrity, student academic and non-academic conduct. Failure to follow the policies, bylaws, and procedures are subject to disciplinary procedures as set out under, but not limited to, the Senate Bylaw 31: Academic Integrity and Procedures for Addressing Student Non-Academic Misconduct. Regarding plagiarism, the Blackboard's SafeAssign will be used for some or all student assignments or equivalent at the instructor's discretion. Plagiarized submissions or equivalent (e.g., exams), i.e., submissions with the same or minor modifications, left unmarked. Should you need to record the lectures, please follow the Senate Policy on Recording Lectures.

13. **Communication:** Students are required to obtain and maintain a University of Windsor e-mail account, [uwindid]@uwindsor.ca, for timely communications with the instructor. The course homepage on the Blackboard, *COMP2650-1-R-2021W: Computer Architecture I: Digital Design*, is the main notification center for the course announcements and repository for the course material and resources. Blackboard Collaborate Ultra at *COMP2650-1-R-2021W: Computer Architecture I: Digital Design → Classroom* is the official place for the lectures and office hours with the instructor. In Microsoft Teams, the team *COMP2650-1-R-2021W* is provided for emergency cases and backup plans only.

14. **Change Notification:** Any changes in the course outline, exam dates, marking, or evaluation will be discussed in class at least 1 week prior to being implemented.

15. **Student Evaluation of Teaching (SET):** The Student Evaluation of Teaching (SET) will be conducted during the last 2 weeks of the classes.

16. **Online Experience:** Participants in online lectures and lab sections include an instructor, a moderator, and students. Students are able to share camera or send messages but cannot share audio unless they Raise Hand, and the moderator or the instructor allows them. The moderator also supervises private messages. Students are encouraged to let the moderator and/or the instructor know of any connection issues asap regarding the quality of presentation in terms of audio and video (e.g., slides).

17. **Feeling Overwhelmed?** Should face obstacles and experience difficulties that affect her academic performance, students can reach out to the following service centers as well as other on- and off-campus resources listed here www.uwindsor.ca/wellness:
    - Student Health Services
    - Student Counselling Centre
    - Peer Support Centre