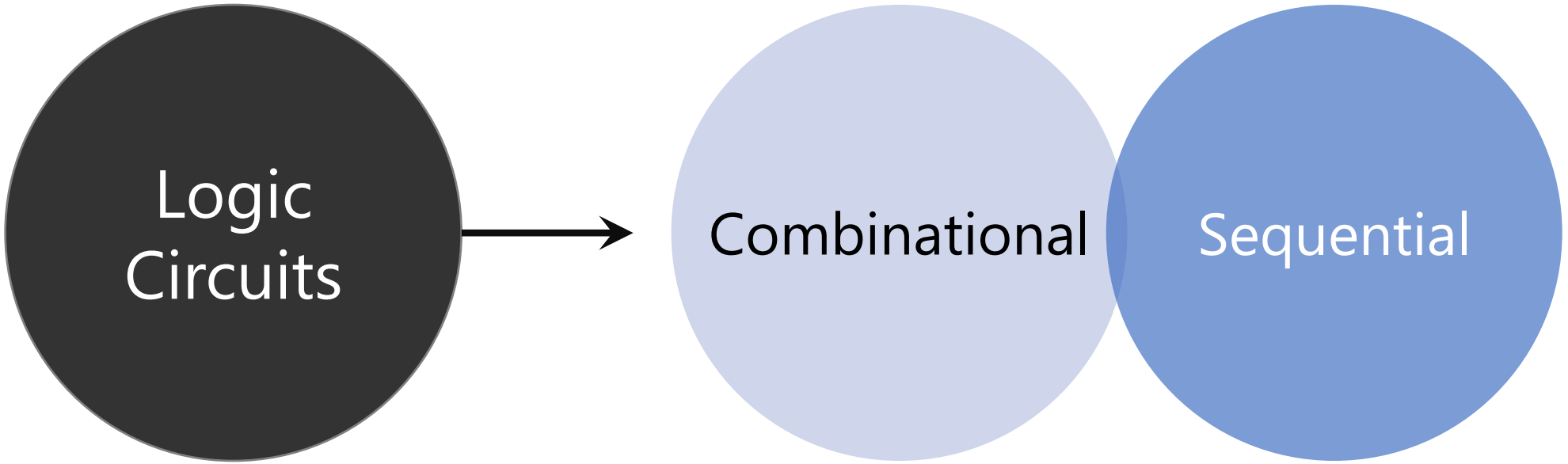

Logic
Circuits
Combinational
Sequential

Chapter 4 Combinational Logic

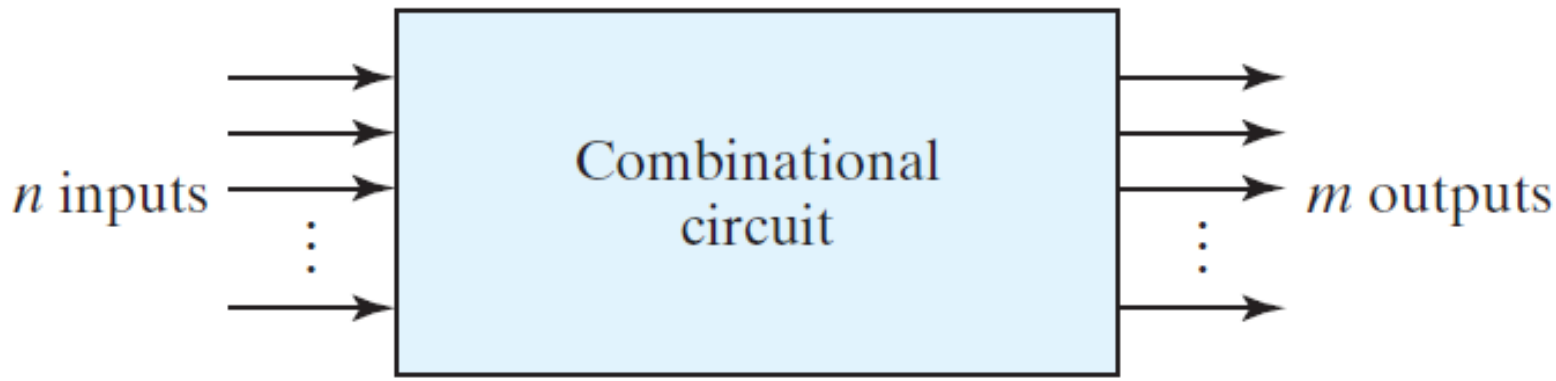


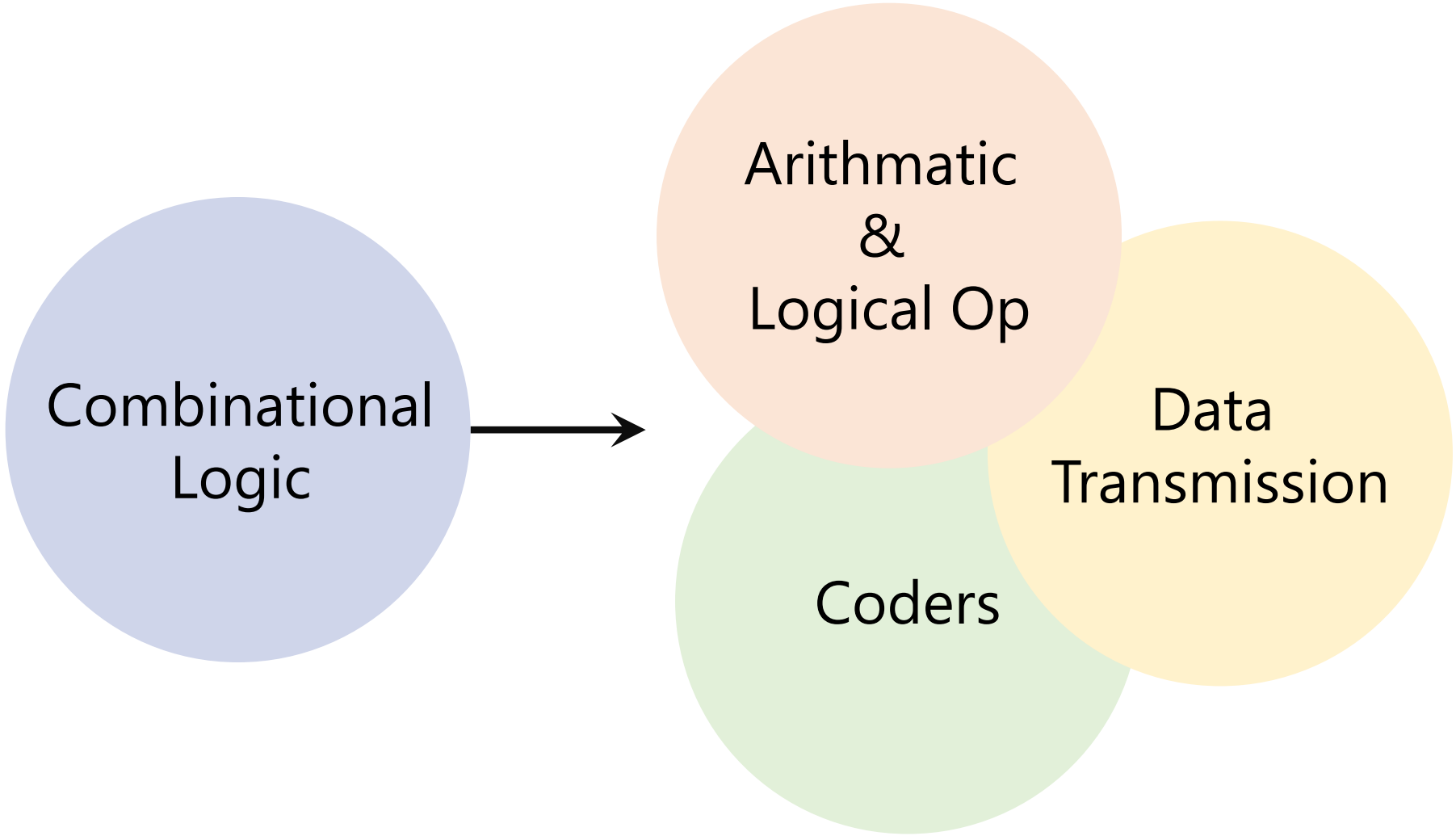
FIGURE 4.1
Block diagram of combinational circuit

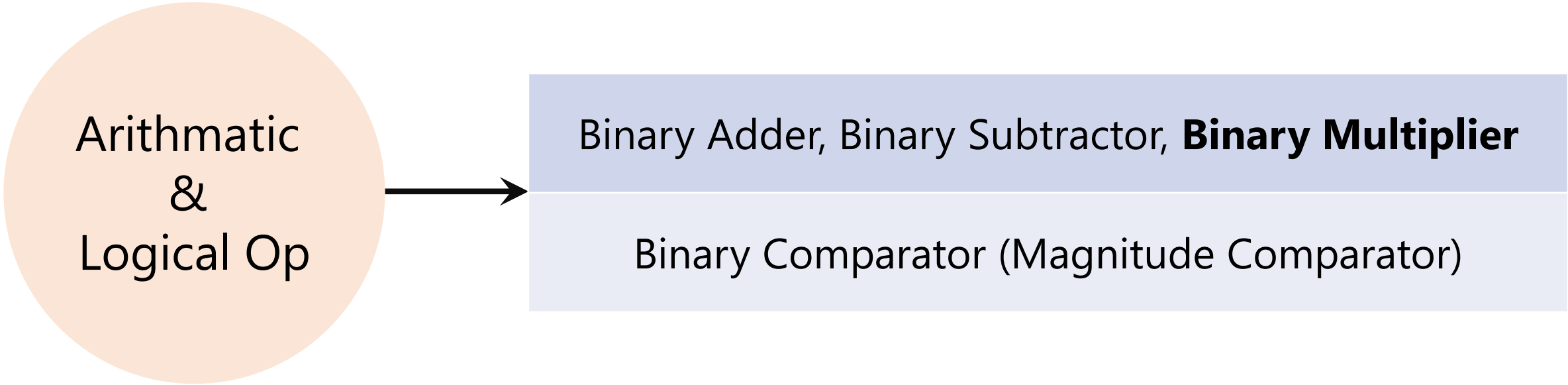
Combinational Logic

aka. Combinational Circuit

Combination of logic gates on the present inputs → the outputs *at any time*!

A combinational circuit performs an operation that can be specified logically by a set of Boolean functions.


Combinational
Logic
Arithmatic
&
Logical Op
Data
Transmission
Coders

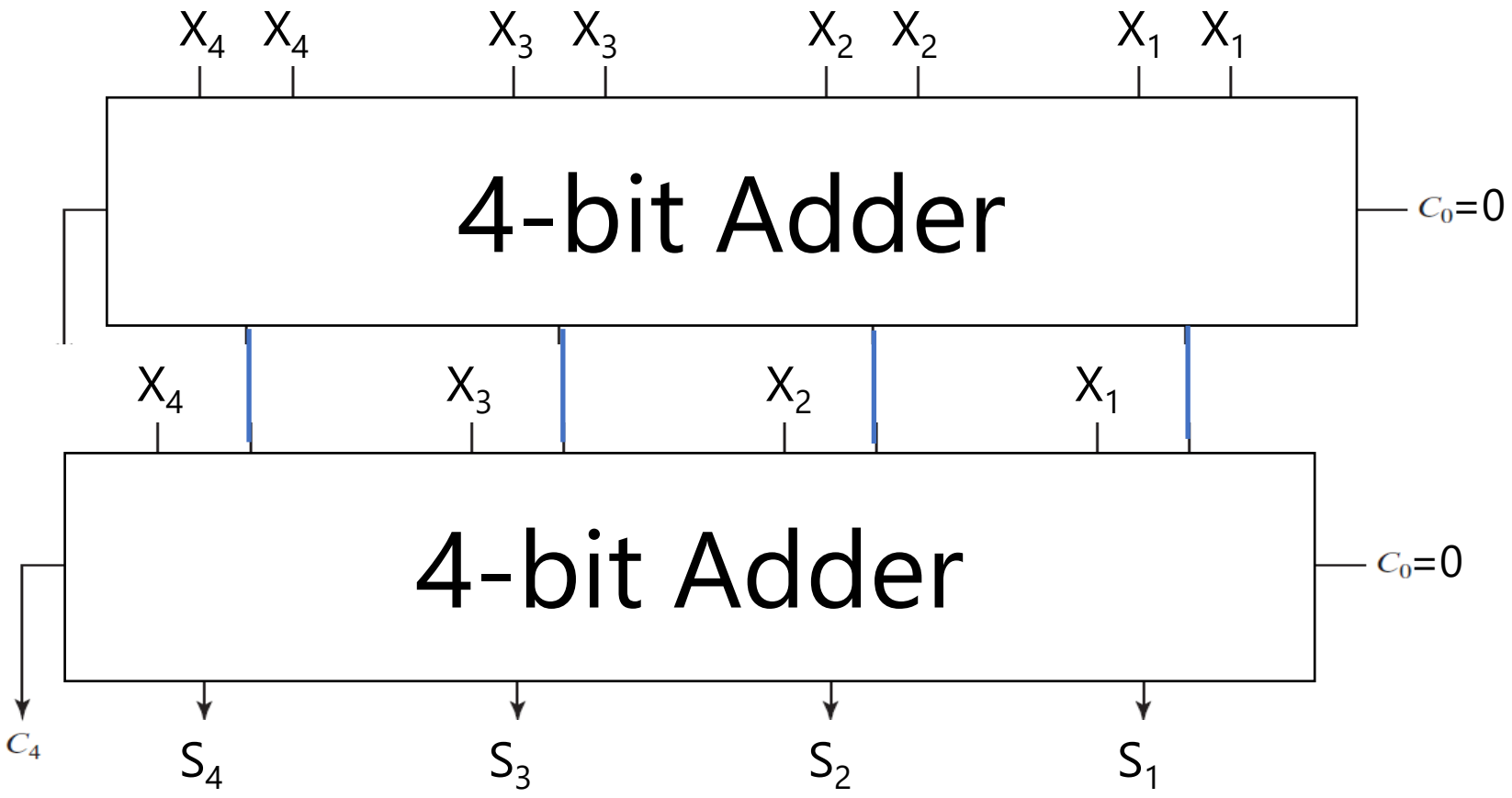

Arithmatic
&
Logical Op
Binary Adder, Binary Subtractor, **Binary Multiplier**
Binary Comparator (Magnitude Comparator)

Binary Multiplier

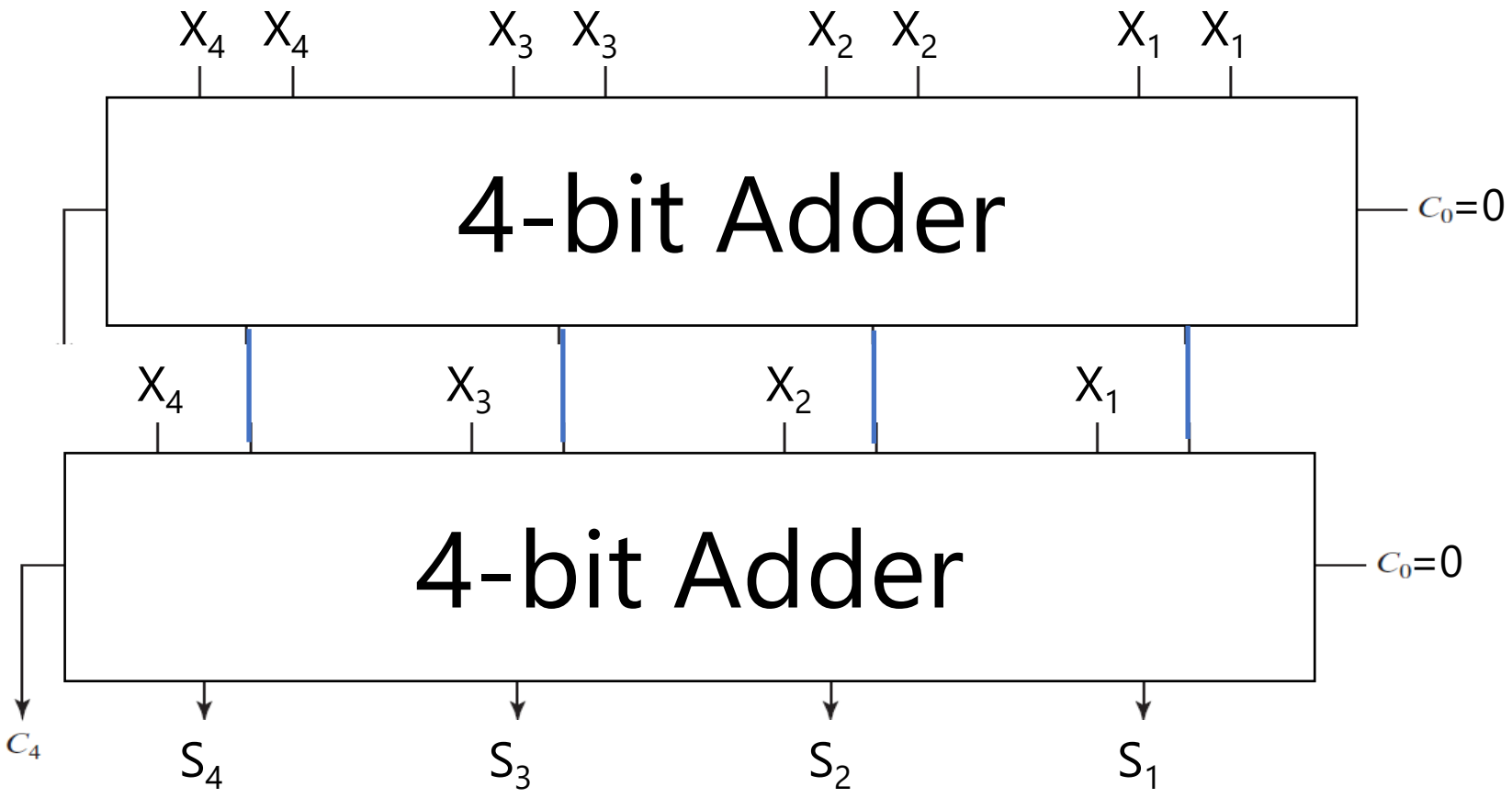
Unsigned

n-bit X + n-bit X + … + n-bit X

m-bit Y times!

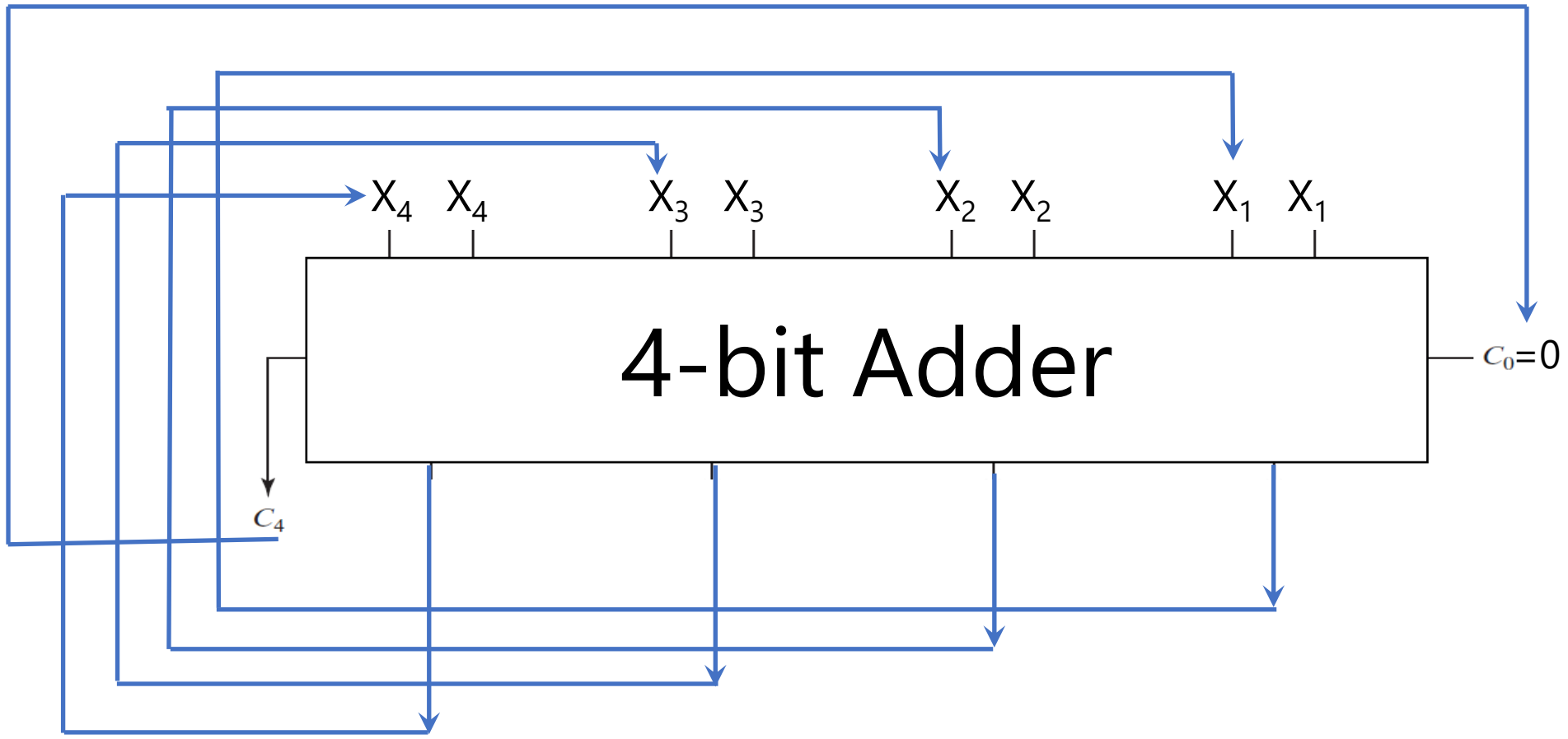


$$X \times (11)_2 = X+X+X$$



$$X \times (11)_2 = X+X+X$$

If you change Y, you have to change circuit!!



X × Y = X+…+X → When to stop?

Feedback → Sequential Logic

Binary Multiplier

Unsigned

$$\times \frac{X_4X_3X_2X_1}{Y_1} \over M_4M_3M_2M_1$$

$$\times \frac{X_4X_3X_2X_1}{Y_1} \over M_1 = Y_1X_1$$

$$\times \frac{X_4X_3X_2X_1}{Y_1}$$

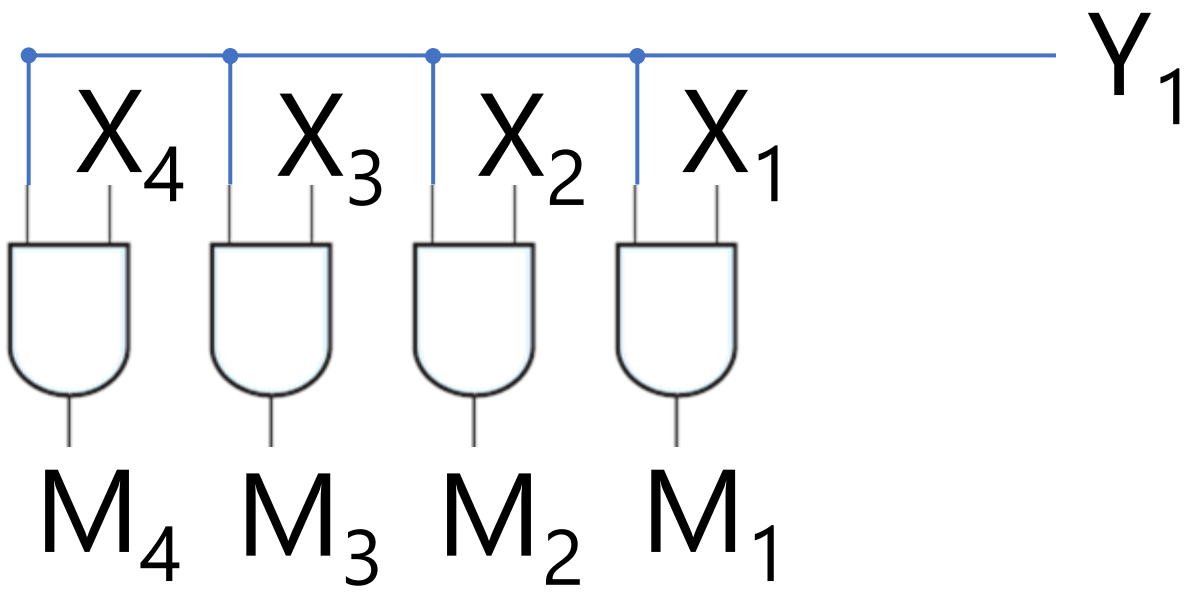
$$M_2=Y_1X_2$$

$$\times \frac{X_4 X_3 X_2 X_1}{Y_1}$$

$$M_3 = Y_1 X_3$$

$$\times \frac{X_4X_3X_2X_1}{Y_1}$$

$$M_4 = Y_1X_4$$

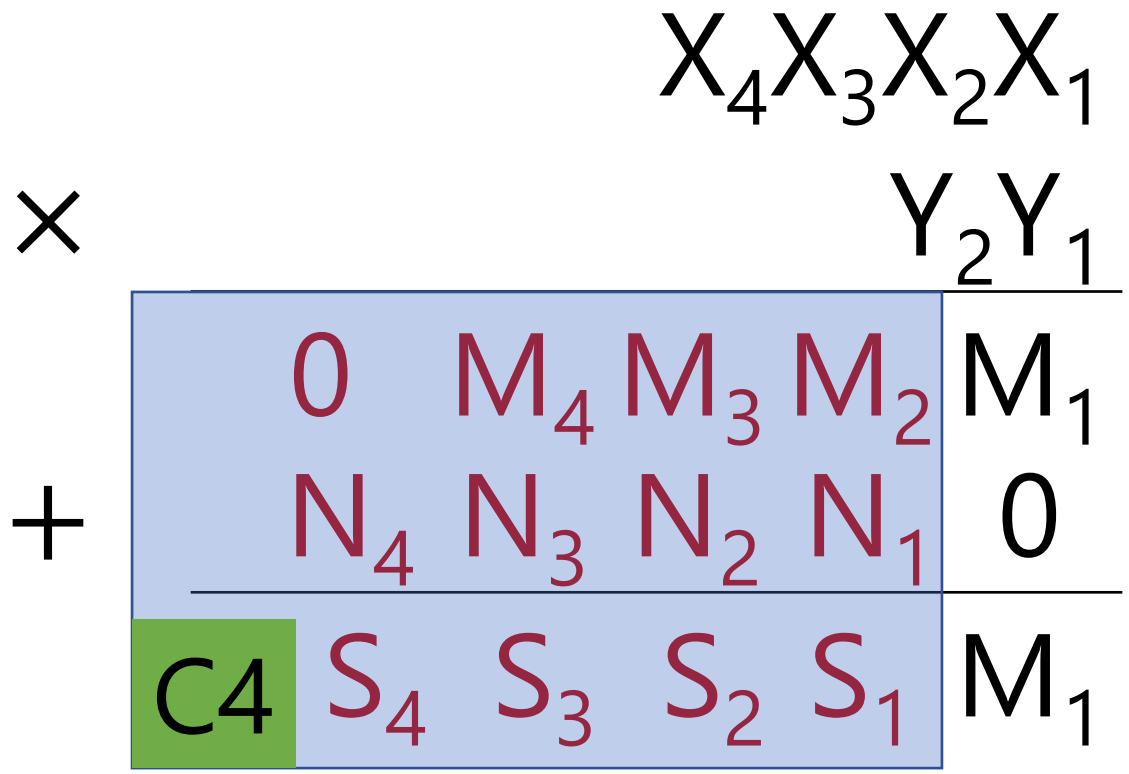

Y1
X4
X3
X2
X1
M4
M3
M2
M1

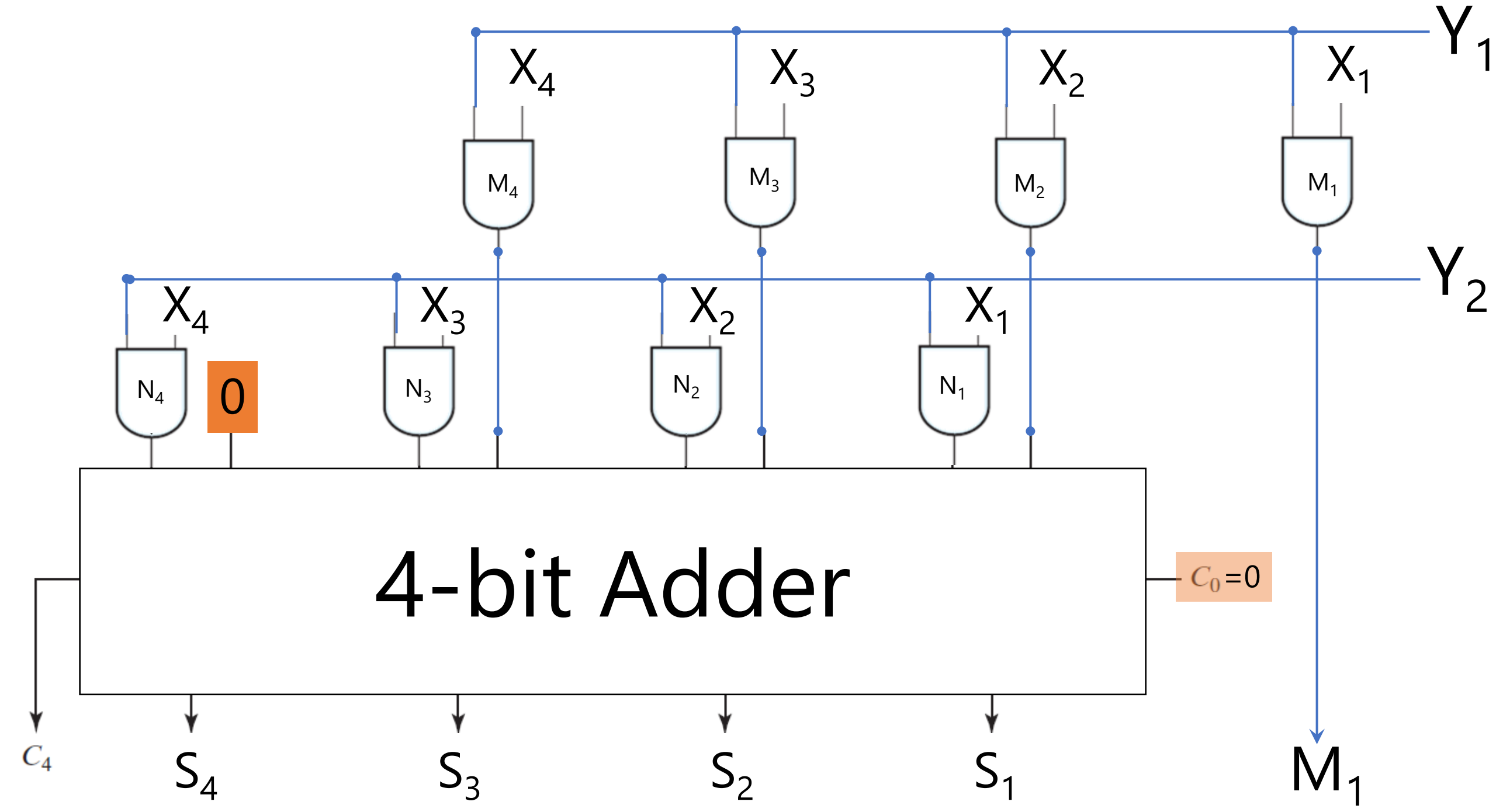
$$\times \quad \frac{X_4X_3X_2X_1}{Y_2Y_1} \qquad M_4\,M_3\,M_2\,M_1$$

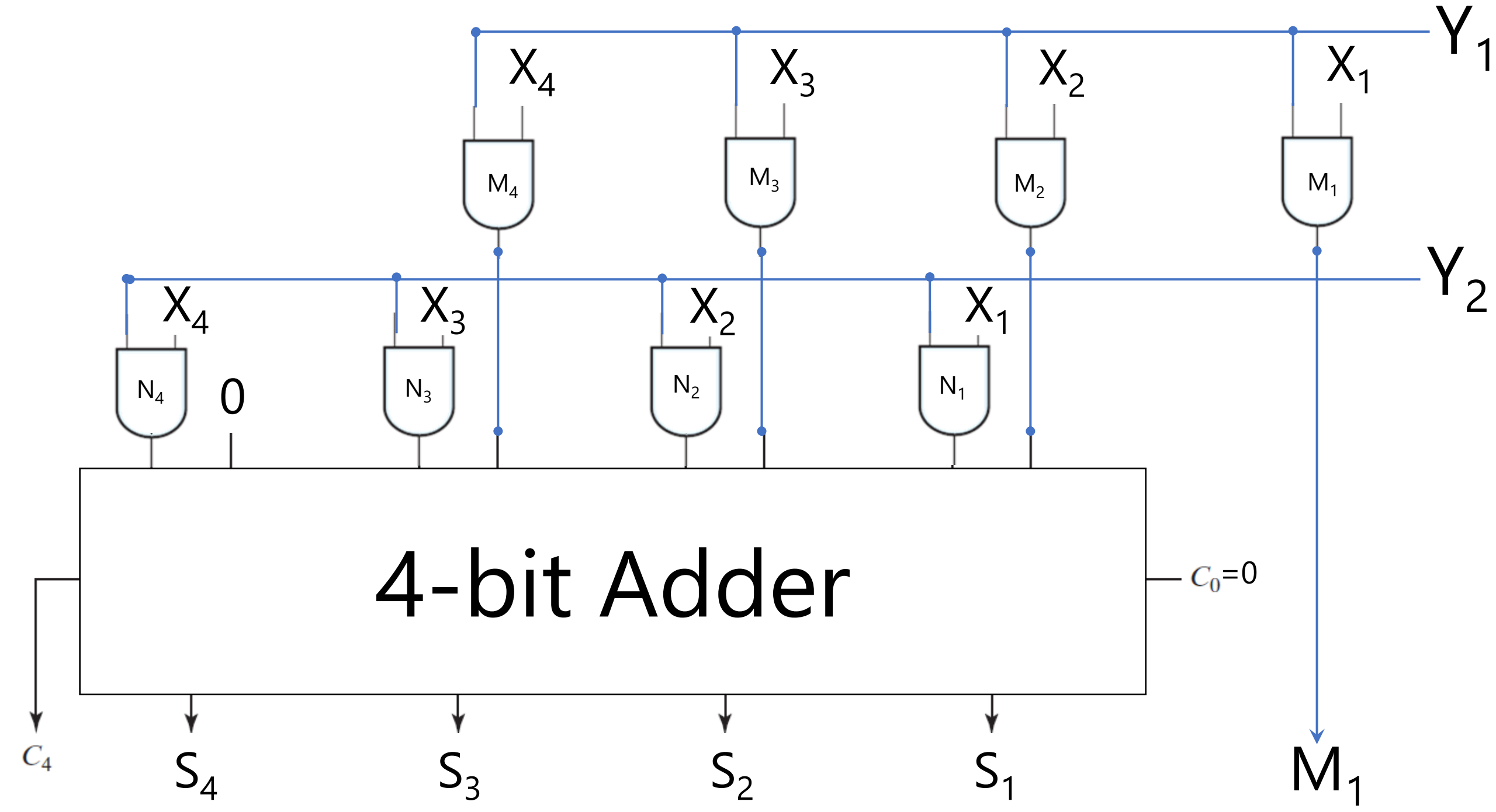
$$
\begin{array}{rr}
 & X_4X_3X_2X_1 \\
\times & \qquad Y_2Y_1 \\
\hline
 & M_4\,M_3\,M_2\,M_1 \\
 & N_4\;N_3\;N_2\;N_1\;\;0
\end{array}
$$

$$
\begin{array}{rr}
 & X_4 X_3 X_2 X_1 \\
\times & \quad Y_2 Y_1 \\
\hline
 & M_4\ M_3\ M_2\ M_1 \\
+ & N_4\ N_3\ N_2\ N_1\ 0 \\
\hline
\end{array}
$$

$$
\begin{array}{rr}
 & X_4X_3X_2X_1 \\
\times & Y_2Y_1 \\
\hline
 & 0\ M_4\ M_3\ M_2\ M_1 \\
+ & N_4\ N_3\ N_2\ N_1\ 0 \\
\hline
C4 & S_4\ S_3\ S_2\ S_1\ M_1
\end{array}
$$


$X_4X_3X_2X_1$
×
Y_2Y_1
0 M_4 M_3 M_2 M_1
+
N_4 N_3 N_2 N_1 0
C4 S_4 S_3 S_2 S_1 M_1

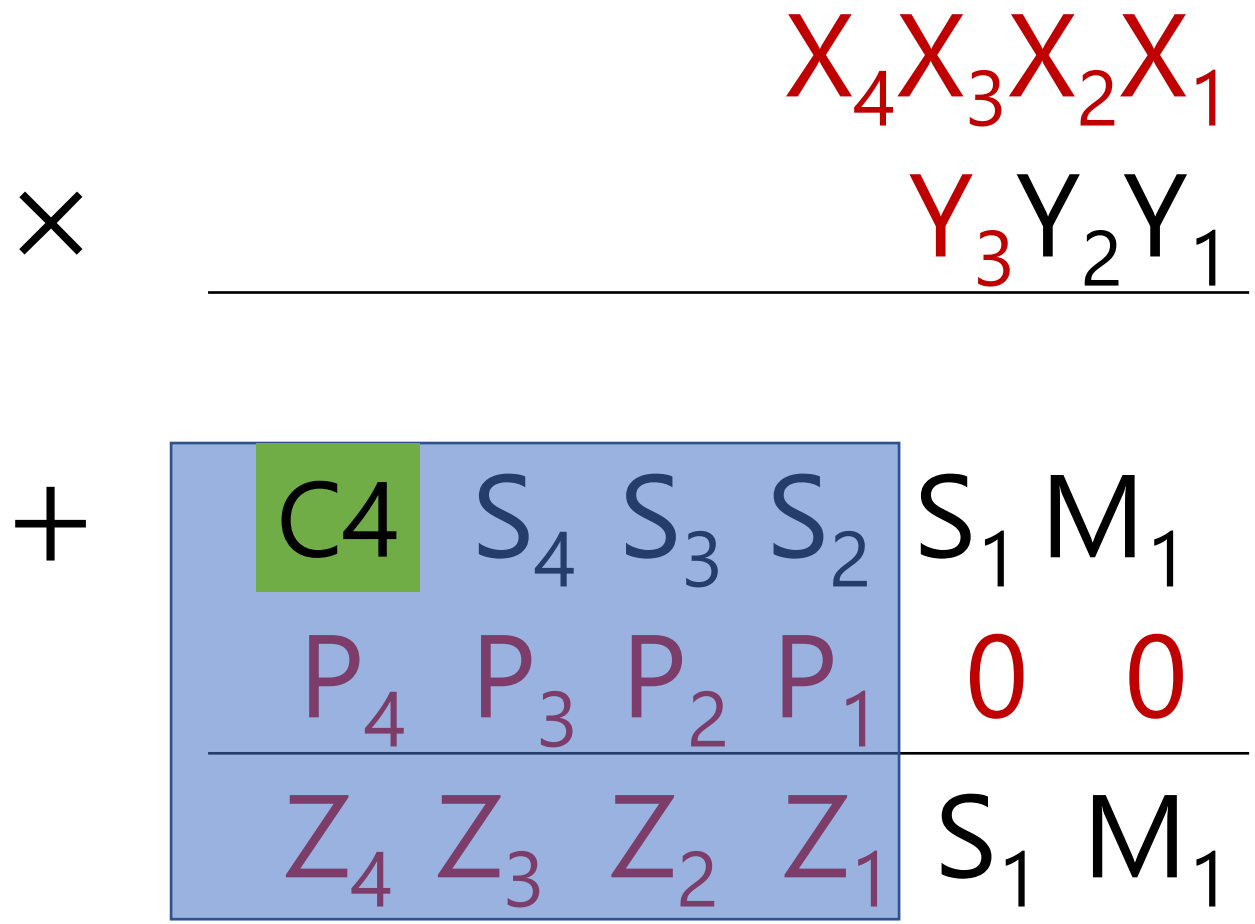

Y1
X4
X3
X2
X1
M4
M3
M2
M1
Y2
X4
X3
X2
X1
N4
0
N3
N2
N1
4-bit Adder
C0=0
C4
S4
S3
S2
S1
M1

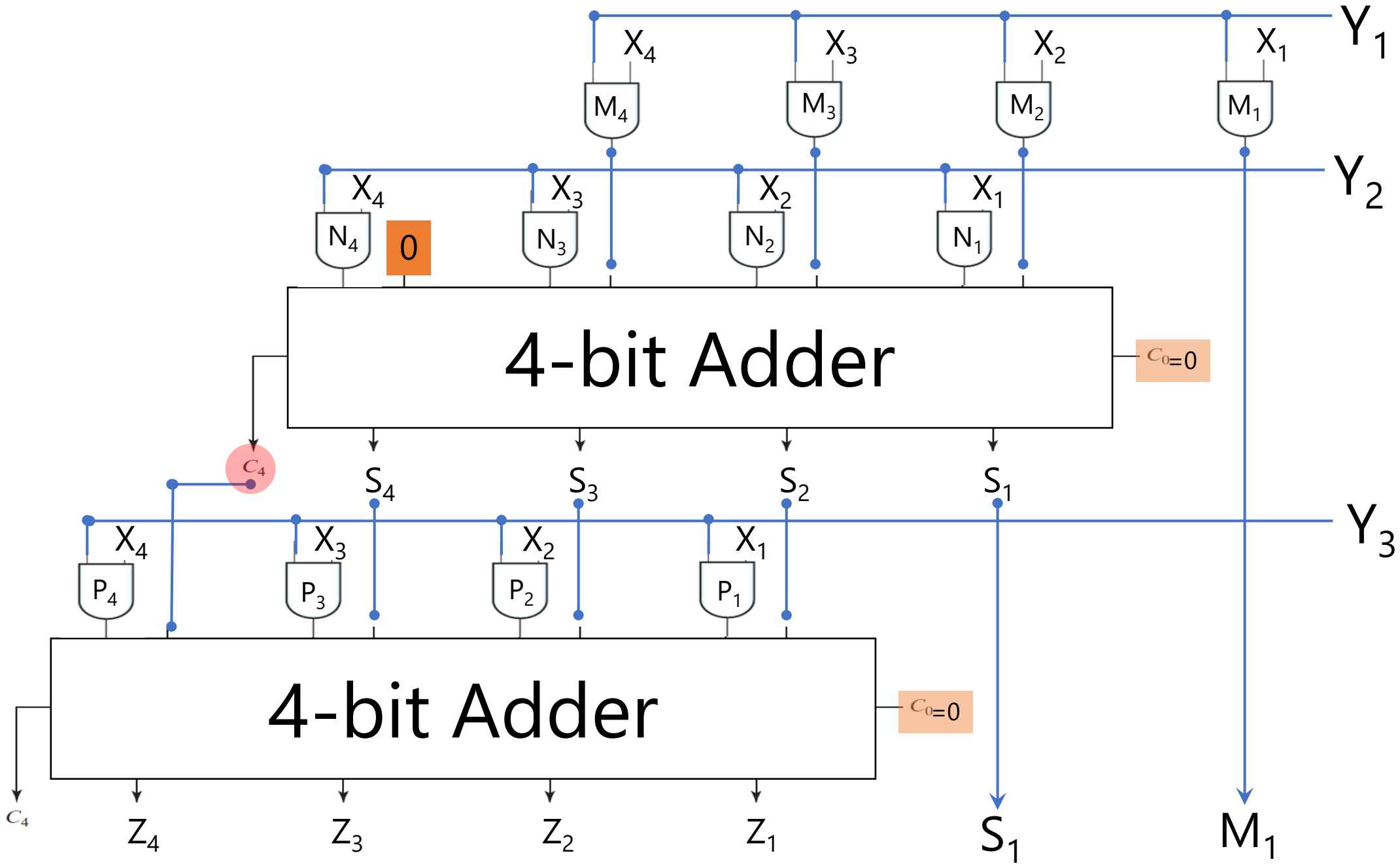

Y1
X4
X3
X2
X1
M4
M3
M2
M1
Y2
X4
X3
X2
X1
N4
0
N3
N2
N1
4-bit Adder
C0=0
C4
S4
S3
S2
S1
M1

$$
\begin{array}{rr}
 & X_4X_3X_2X_1 \\
\times & Y_3Y_2Y_1 \\
\hline
 & M_4\,M_3\,M_2\,M_1 \\
+ & N_4\,N_3\,N_2\,N_1\,0 \\
 & P_4\,P_3\,P_2\,P_1\,0\,0 \\
\hline
\end{array}
$$

$$
\begin{array}{rr}
 & X_4X_3X_2X_1 \\
\times & Y_3Y_2Y_1 \\
\hline
+ & C4\ S_4\ S_3\ S_2\ S_1\ M_1 \\
 & P_4\ P_3\ P_2\ P_1\ 0\ 0 \\
\hline
\end{array}
$$

$$
\begin{array}{rr}
 & X_4 X_3 X_2 X_1 \\
\times & Y_3 Y_2 Y_1 \\
\hline
+ & C4\ S_4\ S_3\ S_2\ S_1\ M_1 \\
 & P_4\ P_3\ P_2\ P_1\ 0\ 0 \\
\hline
 & Z_4\ Z_3\ Z_2\ Z_1\ S_1\ M_1
\end{array}
$$


$X_4X_3X_2X_1$
×
$Y_3Y_2Y_1$
+
C4 S_4 S_3 S_2 S_1 M_1
P_4 P_3 P_2 P_1 0 0
Z_4 Z_3 Z_2 Z_1 S_1 M_1


Y1
X4
X3
X2
X1
M4
M3
M2
M1
Y2
X4
X3
X2
X1
N4
0
N3
N2
N1
4-bit Adder
C0=0
C4
S4
S3
S2
S1
Y3
X4
X3
X2
X1
P4
P3
P2
P1
4-bit Adder
C0=0
C4
Z4
Z3
Z2
Z1
S1
M1

Binary Multiplier

Unsigned

n-bit X × m-bit Y

→ how many output bit?

Binary Multiplier

Unsigned

n-bit X × m-bit Y

→ how many ANDs?

Binary Multiplier

Unsigned

n-bit X × m-bit Y

→ how many k-bit adders?

Binary Multiplier

Unsigned

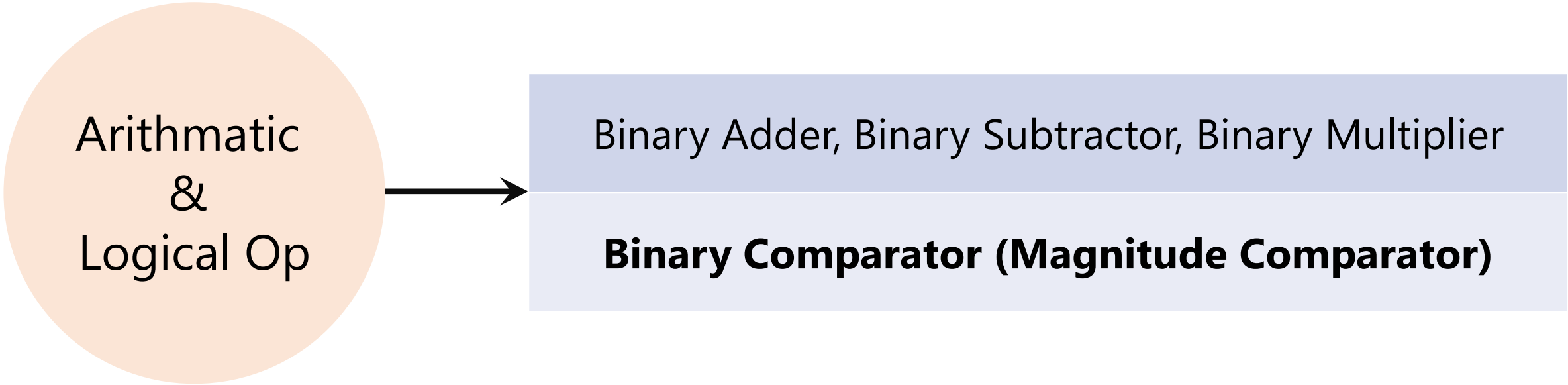
n-bit X × m-bit Y

→ what is k in k-bit adders?

Binary Multiplier

Signed?

n-bit X × m-bit Y


Arithmatic
&
Logical Op
Binary Adder, Binary Subtractor, Binary Multiplier
Binary Comparator (Magnitude Comparator)

Binary Comparator

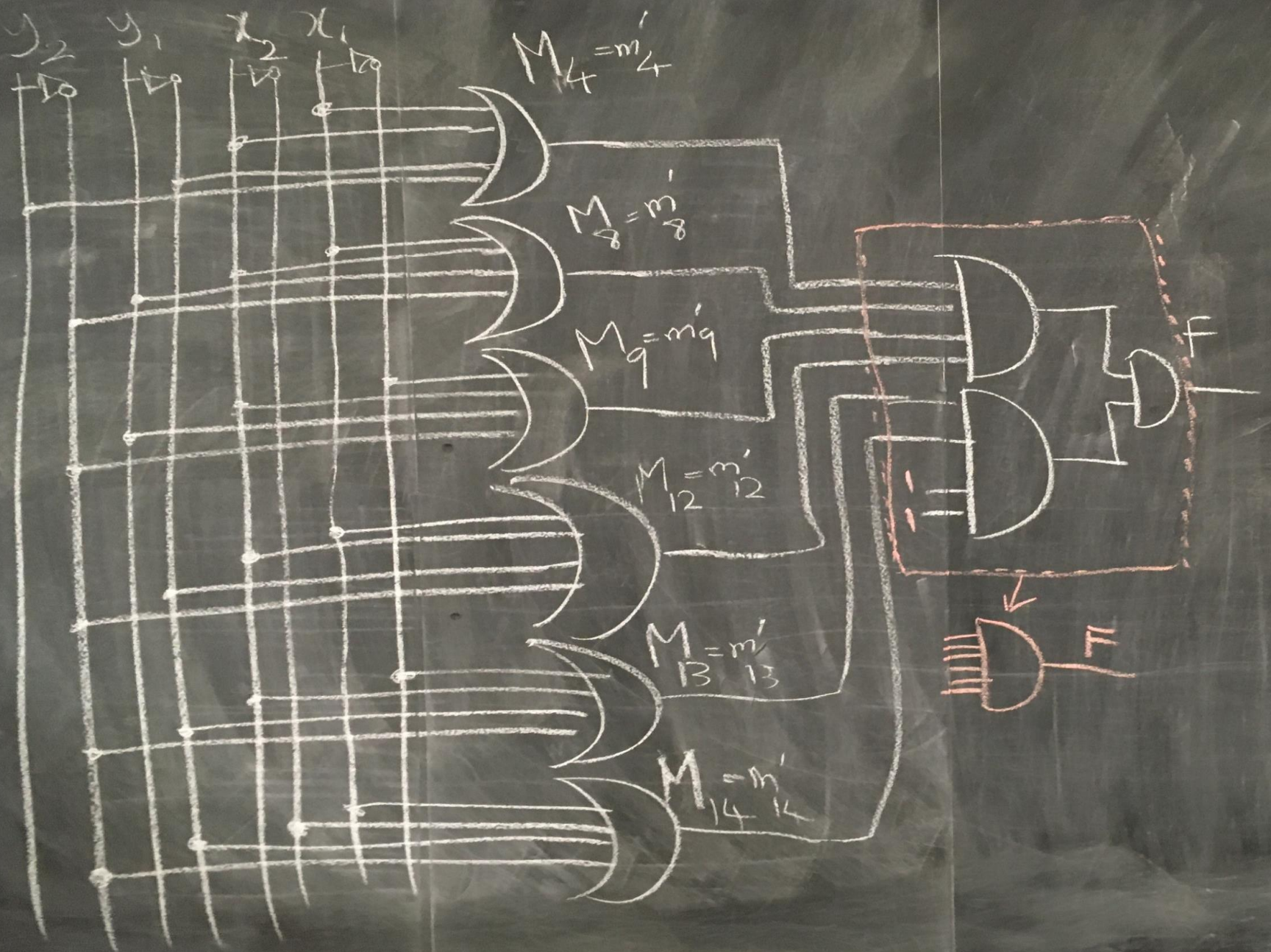
Unsigned

X > Y X==Y X < Y

Given two unsigned numbers x and y, design a logic circuit to see

$$x \geq^{?} y$$

Y2	Y1	X2	X1	F(Y2,Y1,X2,X1)=Σ m(0,1,2,3,5,6,7,10,11,15)	F(Y2,Y1,X2,X1)=Π M(4,8,9,12,13,14)
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	1	1



$$F = \prod M(4,8,9,12,13,14)$$

$$= M_4 M_8 M_9 M_{12} M_{13} M_{14}$$

$$= m'_4 m'_8 m'_9 m'_{12} m'_{13} m'_{14}$$

$(y'_2 y'_1 x'_2 x'_1)'$ $m'_4 \rightarrow y_2 + y'_1 + x_2 + x_1$

$(y_2 y'_1 x'_2 x'_1)'$ $m'_8 \rightarrow y'_2 + y_1 + x_2 + x_1$

$(y_2 y'_1 x_2 x'_1)'$ $m'_9 \rightarrow y'_2 + y_1 + x_2 + x'_1$

$(y_2 y'_1 x_2 x_1)'$ $m'_{12} \rightarrow y'_2 + y'_1 + x_2 + x'_1$

$(y_2 y_1 x'_2 x_1)'$ $m'_{13} \rightarrow y'_2 + y'_1 + x_2 + x'_1$

$(y_2 y_1 x_2 x'_1)'$ $m'_{14} \rightarrow y'_2 + y'_1 + x'_2 + x_1$

Given two unsigned numbers x and y, design a logic circuit to see

$$x > y\ ; x == y\ ;\ x < y$$

Y2	Y1	X2	X1	F_1= (X > Y)	F_2= (X==Y)	F_3= (X < Y)
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Y2	Y1	X2	X1	F_1= (X > Y)	F_2= (X==Y)	F_3= (X < Y)
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1		0
0	0	1	1	1		0
0	1	0	0	0		1
0	1	0	1	0		0
0	1	1	0	1		0
0	1	1	1	1		0
1	0	0	0	0		1
1	0	0	1	0		1
1	0	1	0	0		0
1	0	1	1	1		0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

If X and Y
3, 4, 5, …
bits?!

Binary Subtractor

Binary Subtractor

Unsigned by Hossein's Way!

$$
\begin{array}{rl}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
- & 0\ Y_3Y_2Y_1 \\
\hline
C4 & S_4S_3S_2S_1
\end{array}
$$

$$
\begin{array}{rr}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
- & 0\ Y_3Y_2Y_1 \\
\hline
C4 & S_4S_3S_2S_1
\end{array}
$$

$$
\begin{array}{rr}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
+ & 2\text{'s-comp}(0\ Y_3Y_2Y_1) \\
\hline
C4 & S_4S_3S_2S_1
\end{array}
$$

$$
\begin{array}{rr}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
+ & 2\text{'s-comp}(0\ Y_3Y_2Y_1) \\
\hline
 & C4 \quad S_4S_3S_2S_1
\end{array}
$$

If S'_4 then $X \geq Y$

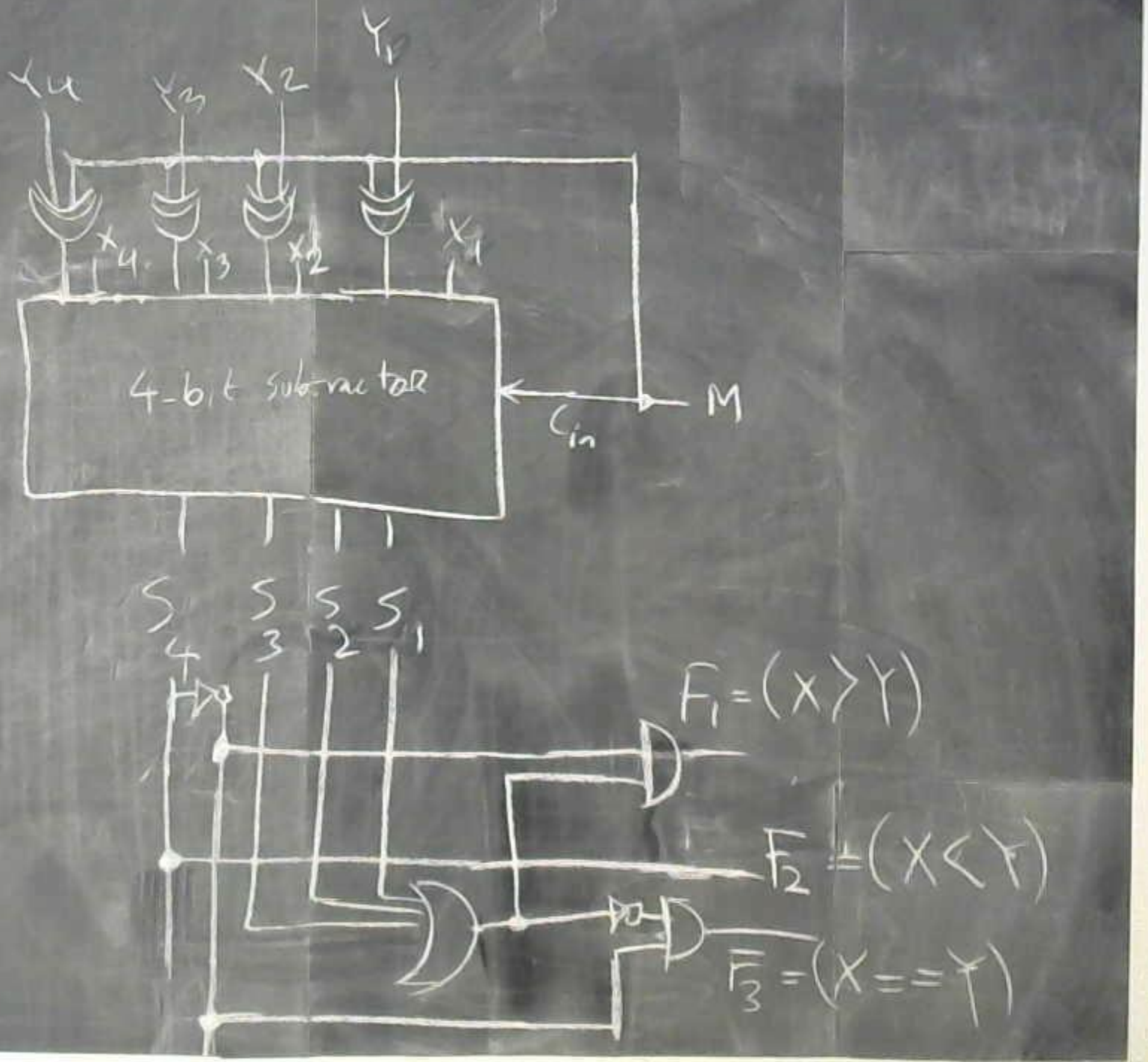
If S'_4 AND $(S_3+S_2+S_1)=1$ then $X > Y$

$$
\begin{array}{rr}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
+ & 2\text{'s-comp}(0\ Y_3Y_2Y_1) \\
\hline
 & C4 \quad S_4S_3S_2S_1
\end{array}
$$

If S_4 then $X < Y$

$$
\begin{array}{rr}
 & C_3C_2C_1C_0 \\
 & 0\ X_3X_2X_1 \\
+ & 2\text{'s-comp}(0\ Y_3Y_2Y_1) \\
\hline
 C4 & S_4S_3S_2S_1
\end{array}
$$

If S'_4 AND $(S_3+S_2+S_1)'=1$ then X == Y

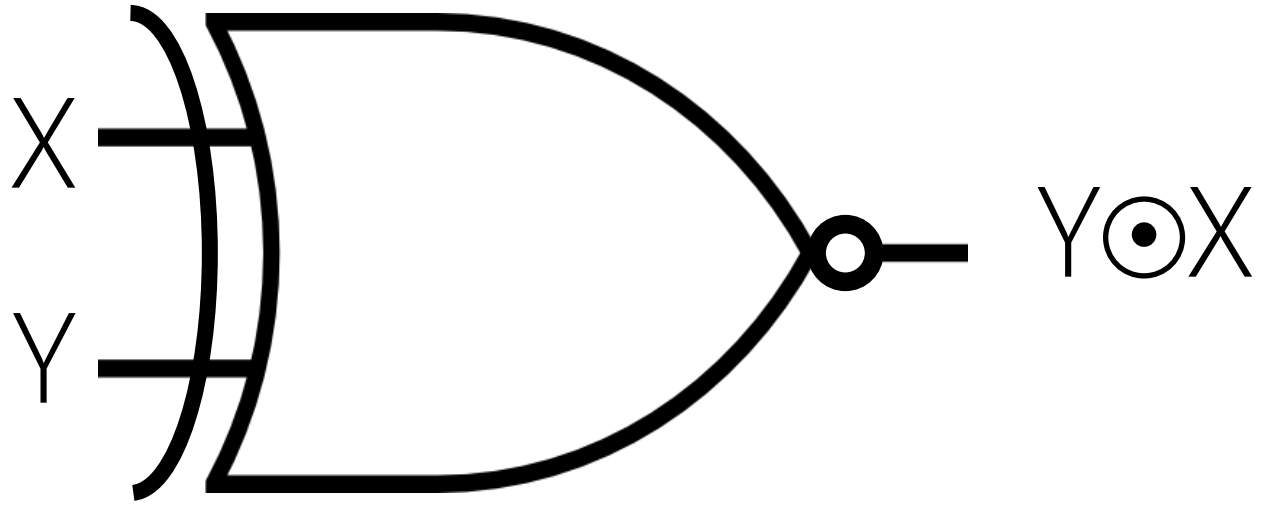

Y4
Y3
Y2
Y1
X4
X3
X2
X1
4-bit subtractor
Cin
M
S4
S3
S2
S1
F1 = (X > Y)
F2 = (X < Y)
F3 = (X == Y)

XNOR

Equality Gate

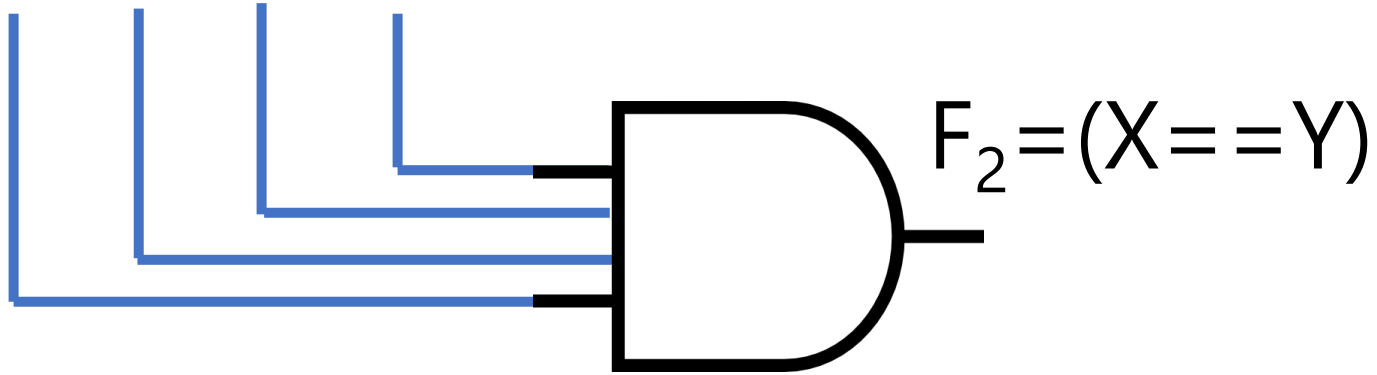
NOT Exclusive-OR (XNOR)

W04



Y	X	F = F(Y,X) = Y'X'+YX = m_0+m_3
0	0	1
0	1	0
1	0	0
1	1	1

$$\begin{array}{r} X_4X_3X_2X_1 \\ \odot \quad Y_4Y_3Y_2Y_1 \\ \hline 1 \quad 1 \quad 1 \quad 1 \end{array}$$



$$X_4 = 1\ X_3 X_2 X_1$$

$$Y_4 = 0\ Y_3 Y_2 Y_1$$

$$X_4 Y'_4 \rightarrow X > Y$$

$$X_4 = 0\ X_3 X_2 X_1$$

$$Y_4 = 1\ Y_3 Y_2 Y_1$$

$$X'_4 Y_4 \rightarrow X < Y$$

$$\begin{array}{r} X_4\ X_3 X_2 X_1 \\ Y_4\ Y_3 Y_2 Y_1 \\ \hline X_4 \odot Y_4 = 1 \end{array}$$

$$X_4\ X_3=1\ X_2X_1$$

$$Y_4\ Y_3=0\ Y_2Y_1$$

$$X_4 \odot Y_4 = 1$$

$$X'_3Y_3 \rightarrow X > Y$$

$$X_4\ X_3=0\ X_2X_1$$

$$Y_4\ Y_3=1\ Y_2Y_1$$

$$X_4 \odot Y_4 = 1$$

$$X_3Y'_3 \rightarrow X < Y$$

$$F1=(X>Y)= X_4Y'_4+$$
$$(X_4\odot Y_4)X_3Y'_3+$$
$$(X_4\odot Y_4)(X_3\odot Y_3)X_2Y'_2+$$
$$(X_4\odot Y_4)(X_3\odot Y_3)(X_2\odot Y_2)X_1Y'_1$$

$$F1=(X<Y)= X'_4Y_4+$$
$$(X_4\odot Y_4)X'_3Y_3+$$
$$(X_4\odot Y_4)(X_3\odot Y_3)X'_2Y_2+$$
$$(X_4\odot Y_4)(X_3\odot Y_3)(X_2\odot Y_2)X'_1Y_1$$

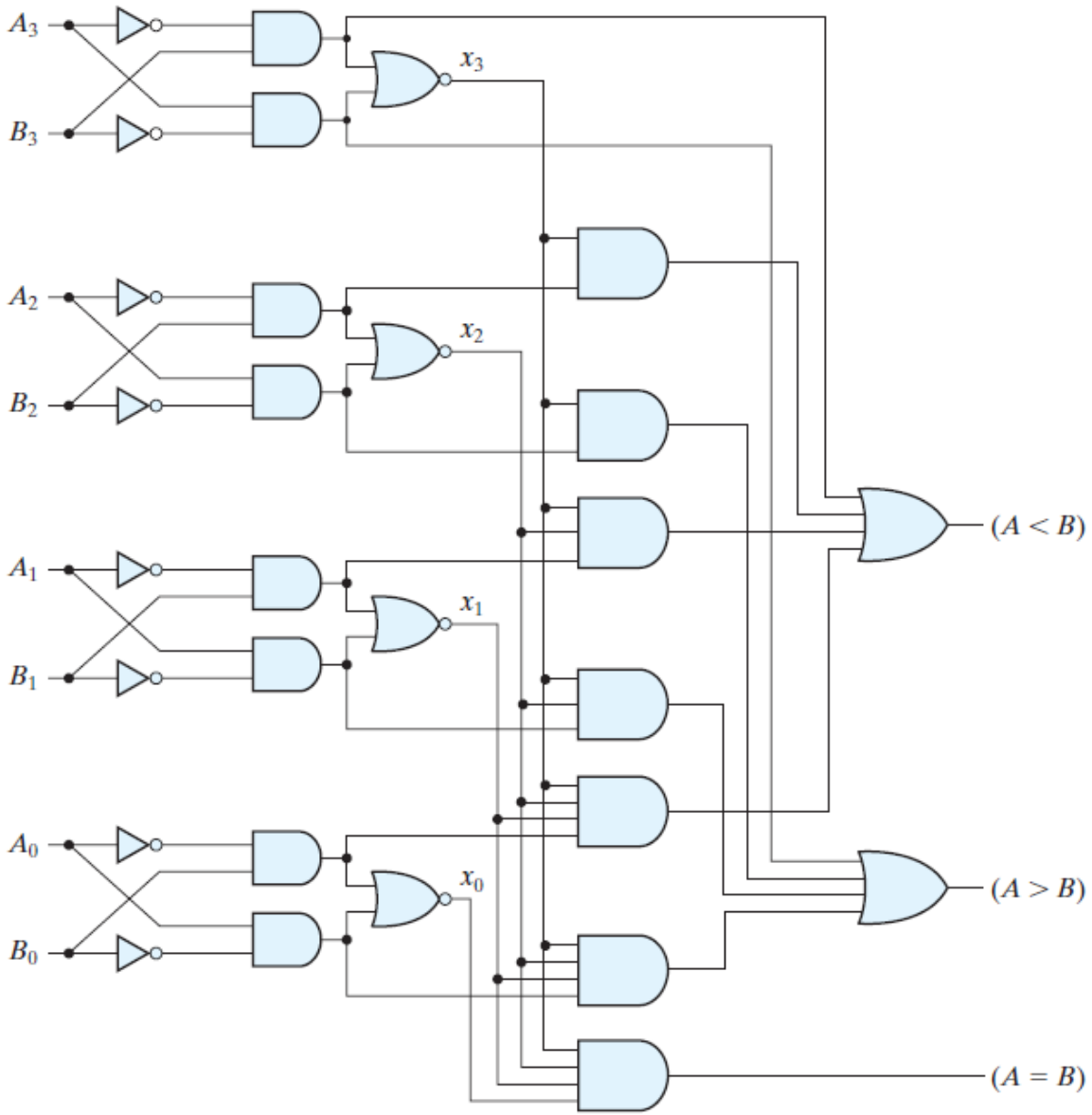


FIGURE 4.17
Four-bit magnitude comparator

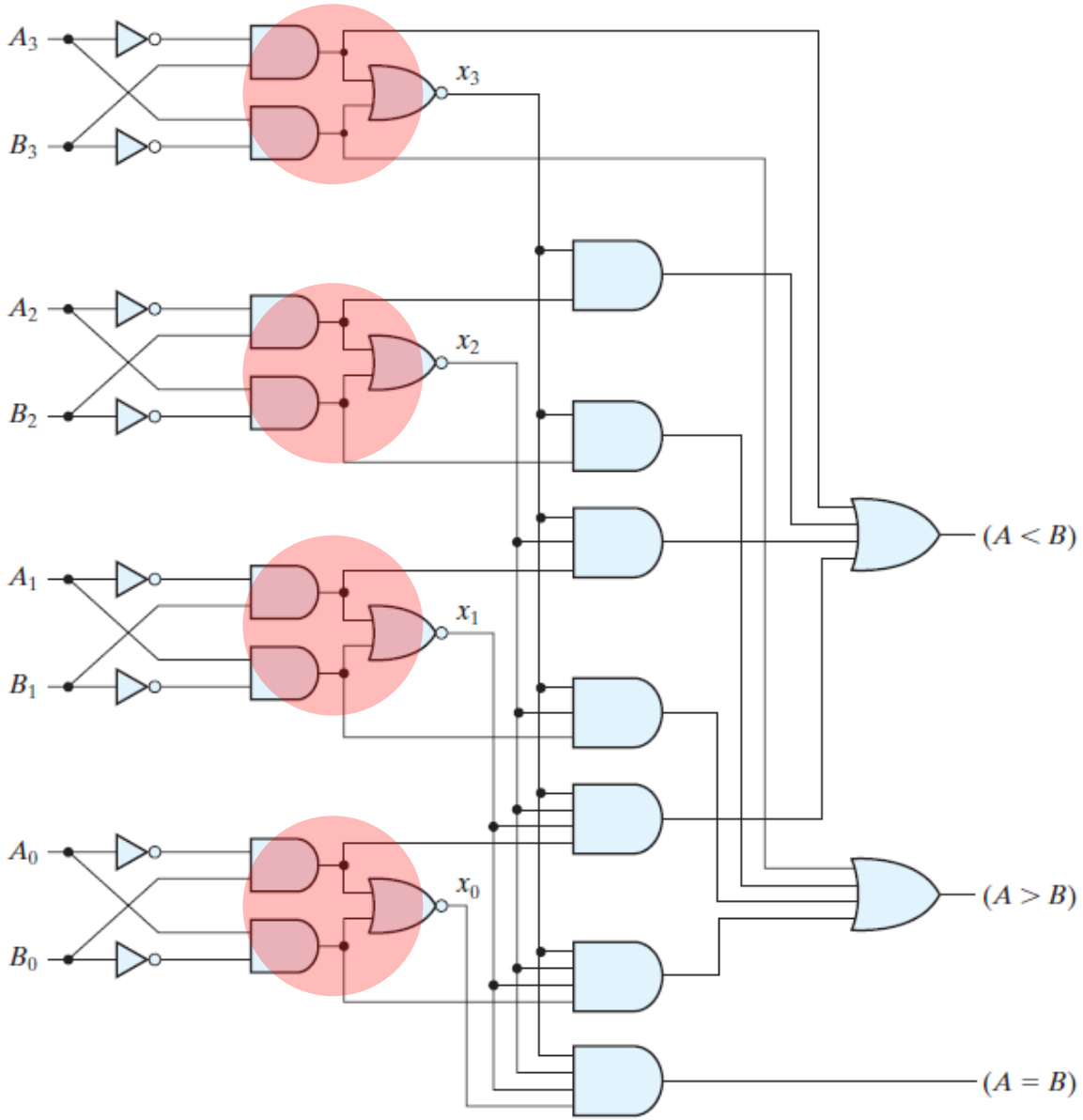
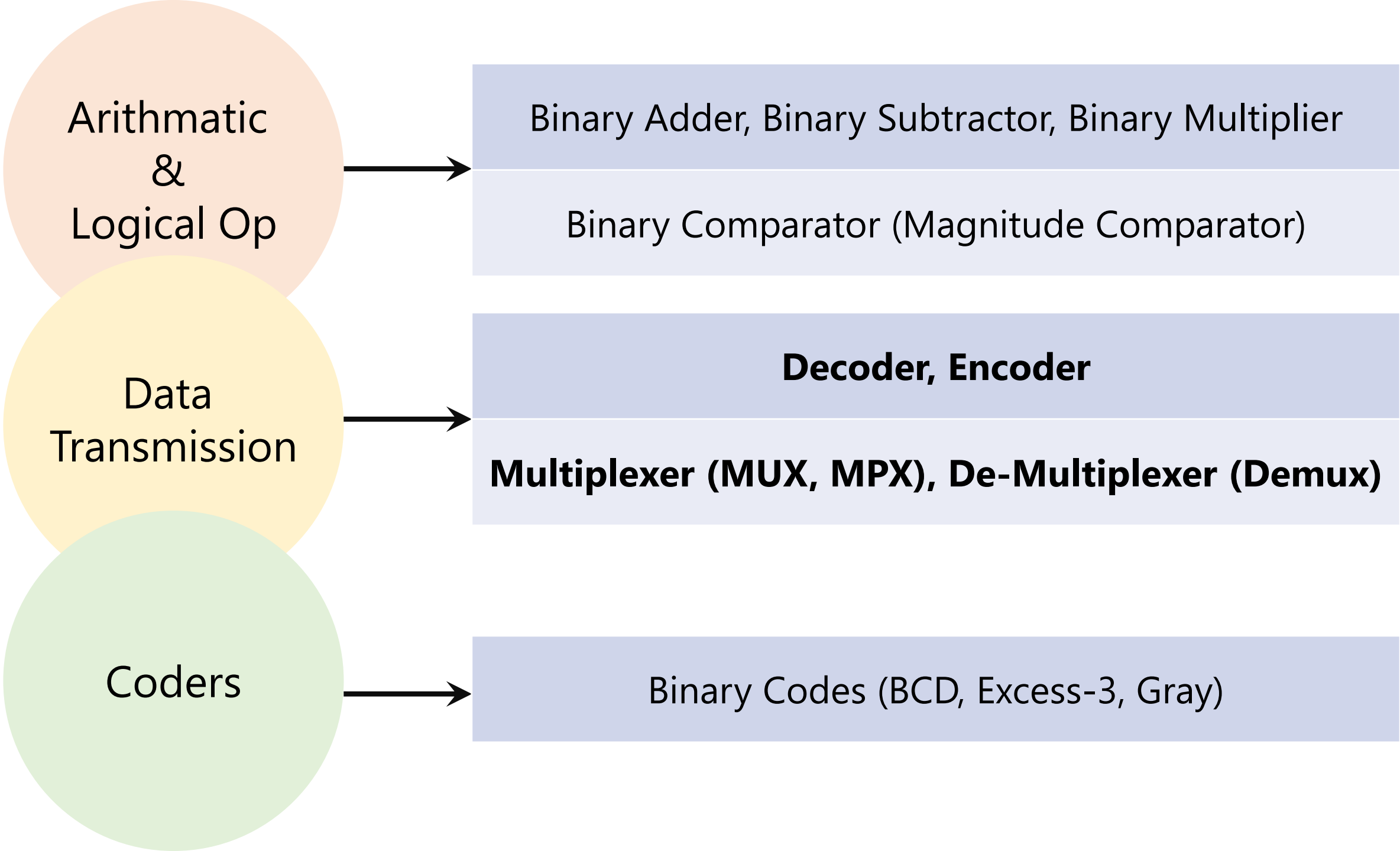


FIGURE 4.17
Four-bit magnitude comparator


Arithmatic
&
Logical Op
Binary Adder, Binary Subtractor, Binary Multiplier
Binary Comparator (Magnitude Comparator)
Data
Transmission
Decoder, Encoder
Multiplexer (MUX, MPX), De-Multiplexer (Demux)
Coders
Binary Codes (BCD, Excess-3, Gray)

Binary Decoder

Binary Code Decoder
Display Decoder

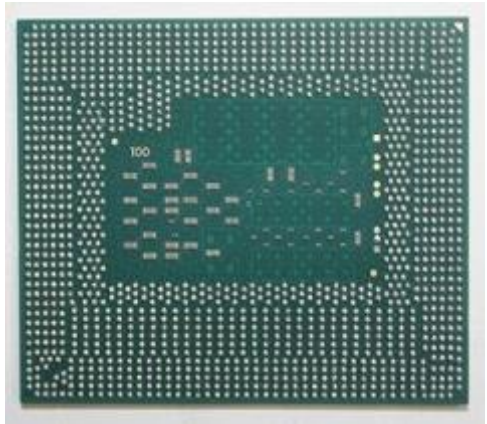
Decoder
Decode Binary to 1-hot

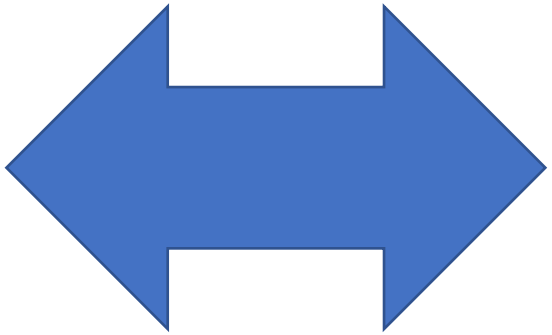
1-hot: a vector of bits with a single 1 and all the others 0

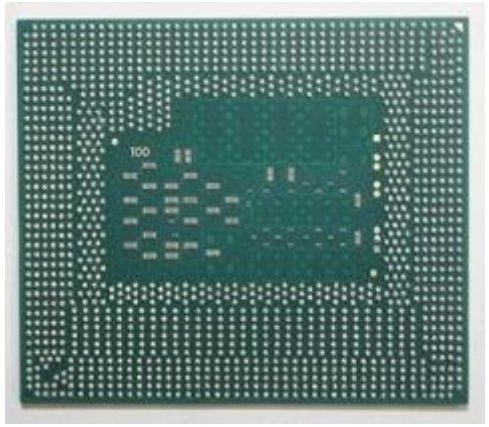
[0010000000]

[0000000100]

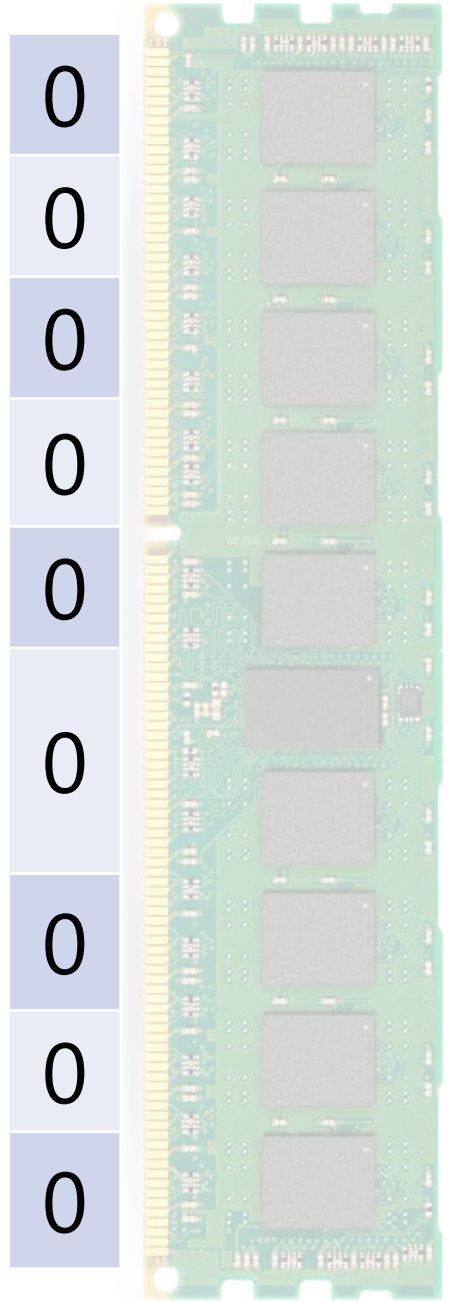
~~[0010010000]~~

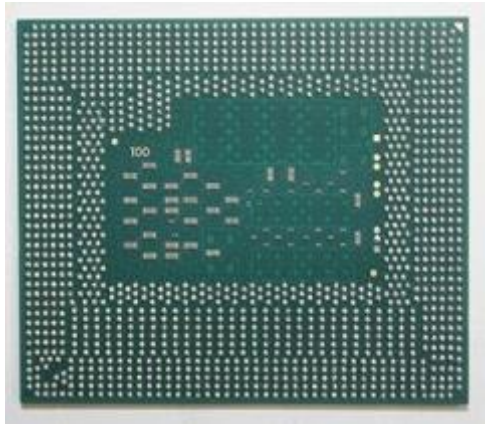






Address





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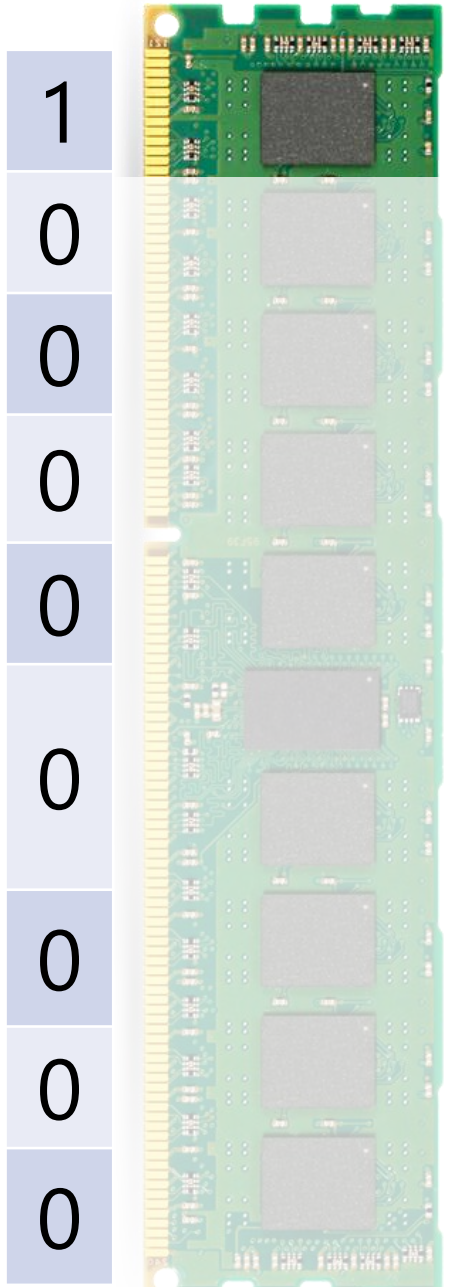

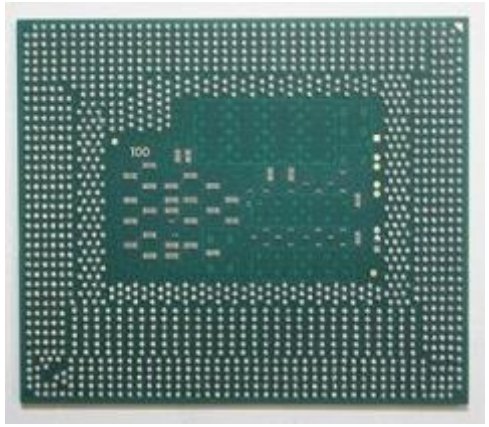

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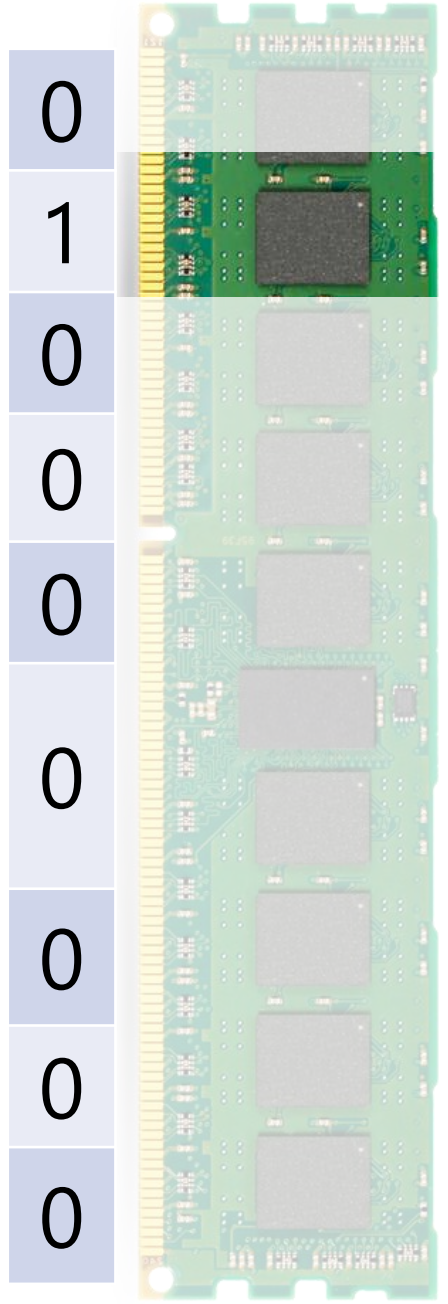

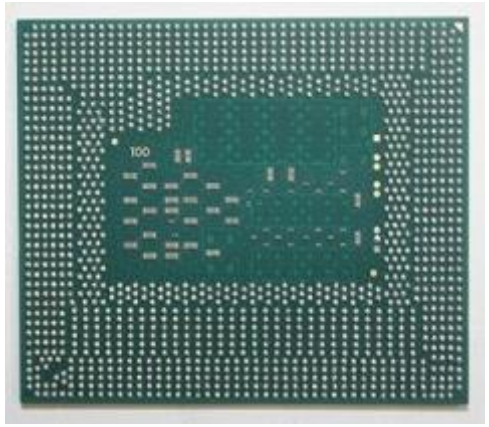

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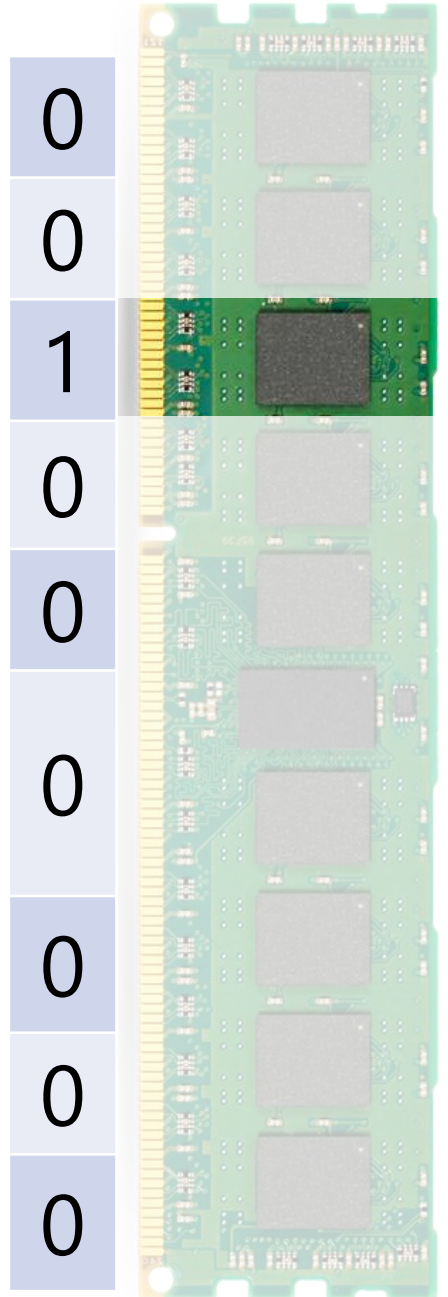
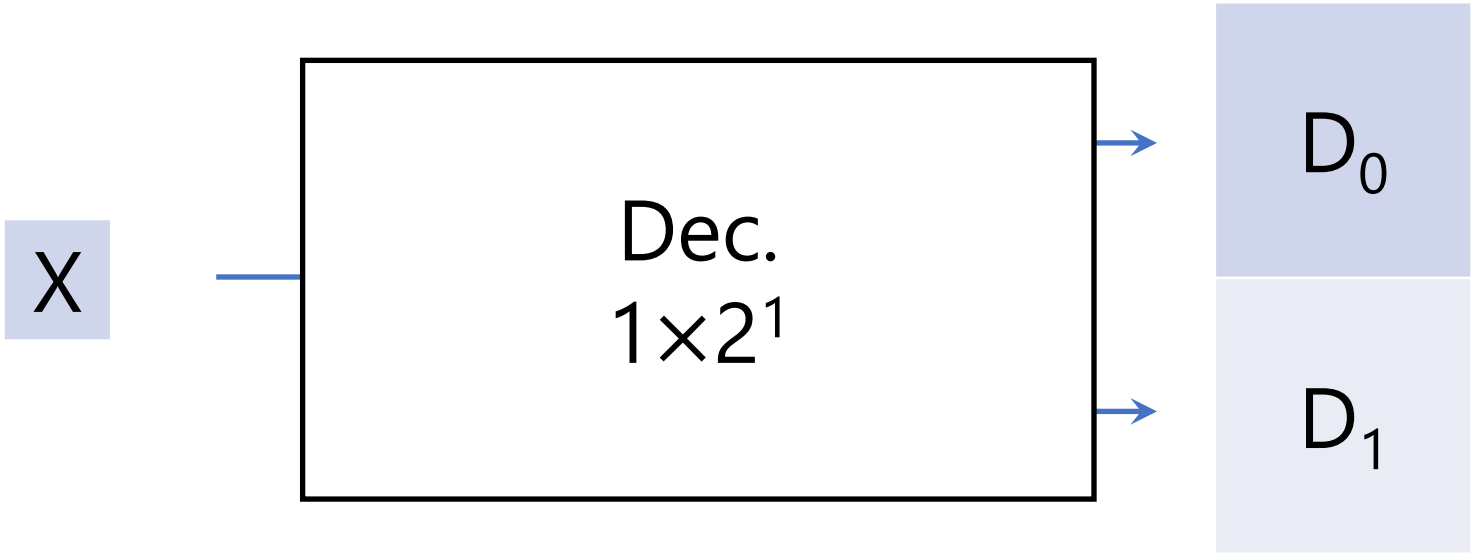



X
D_0
D_1

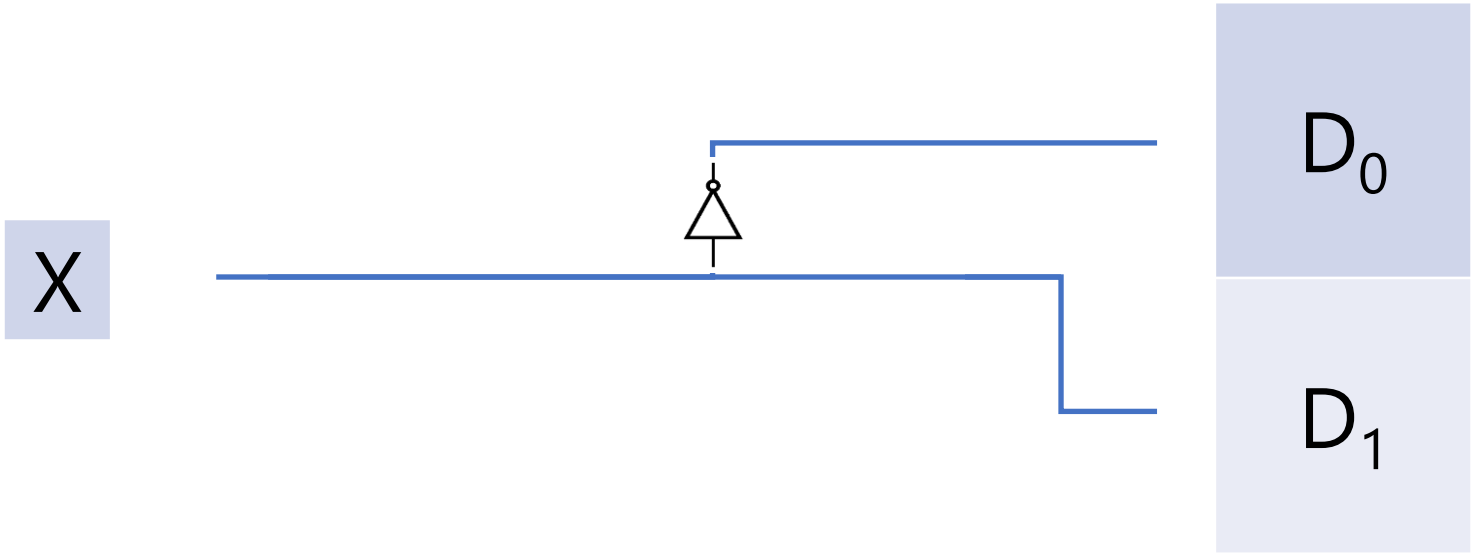

0
$D_0=1$
$D_1=0$

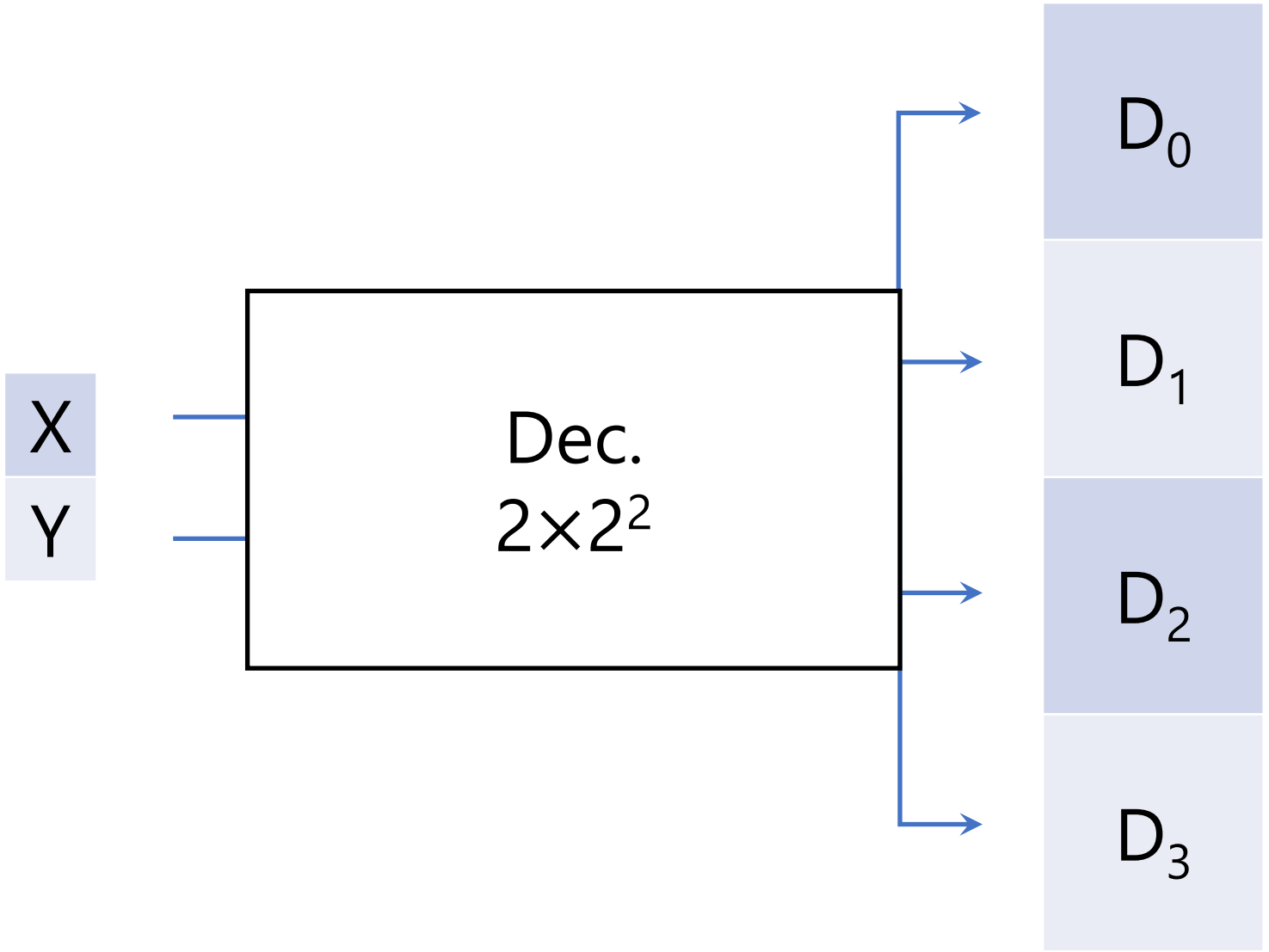

1
$D_0=0$
$D_1=1$

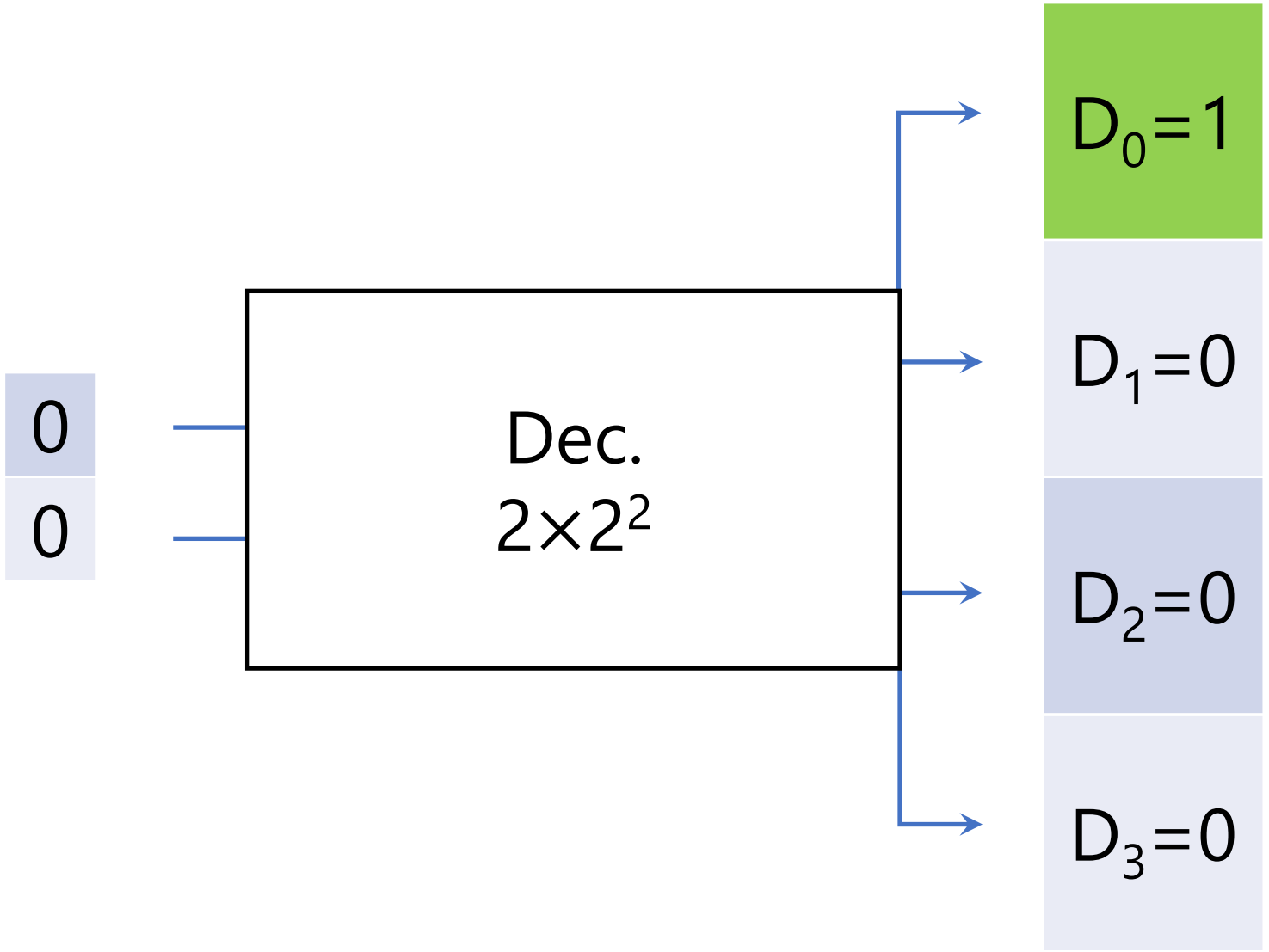

X
Dec.
1×2¹
D0
D1

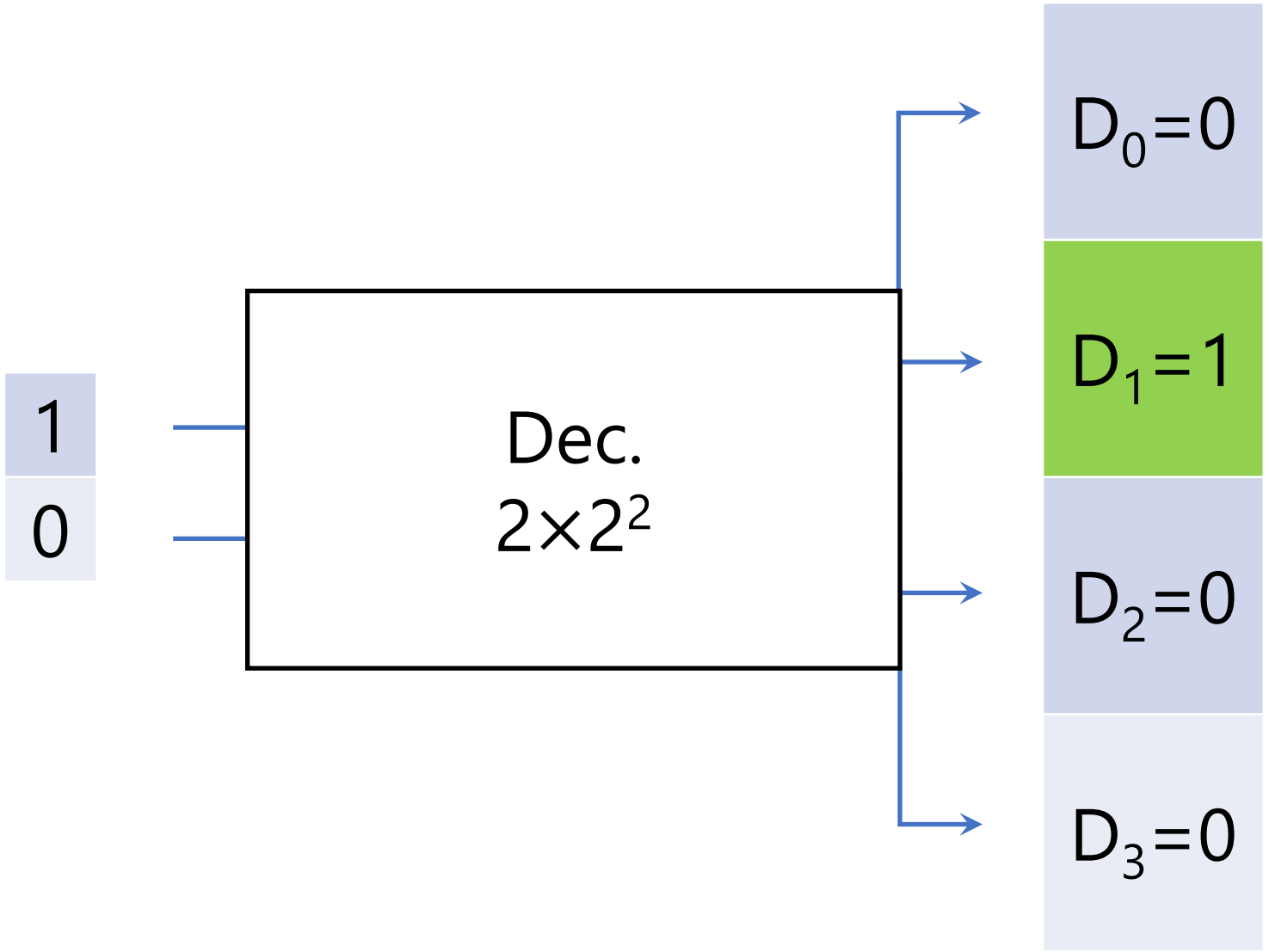
X	D_0	D_1
0	1	0
1	0	1

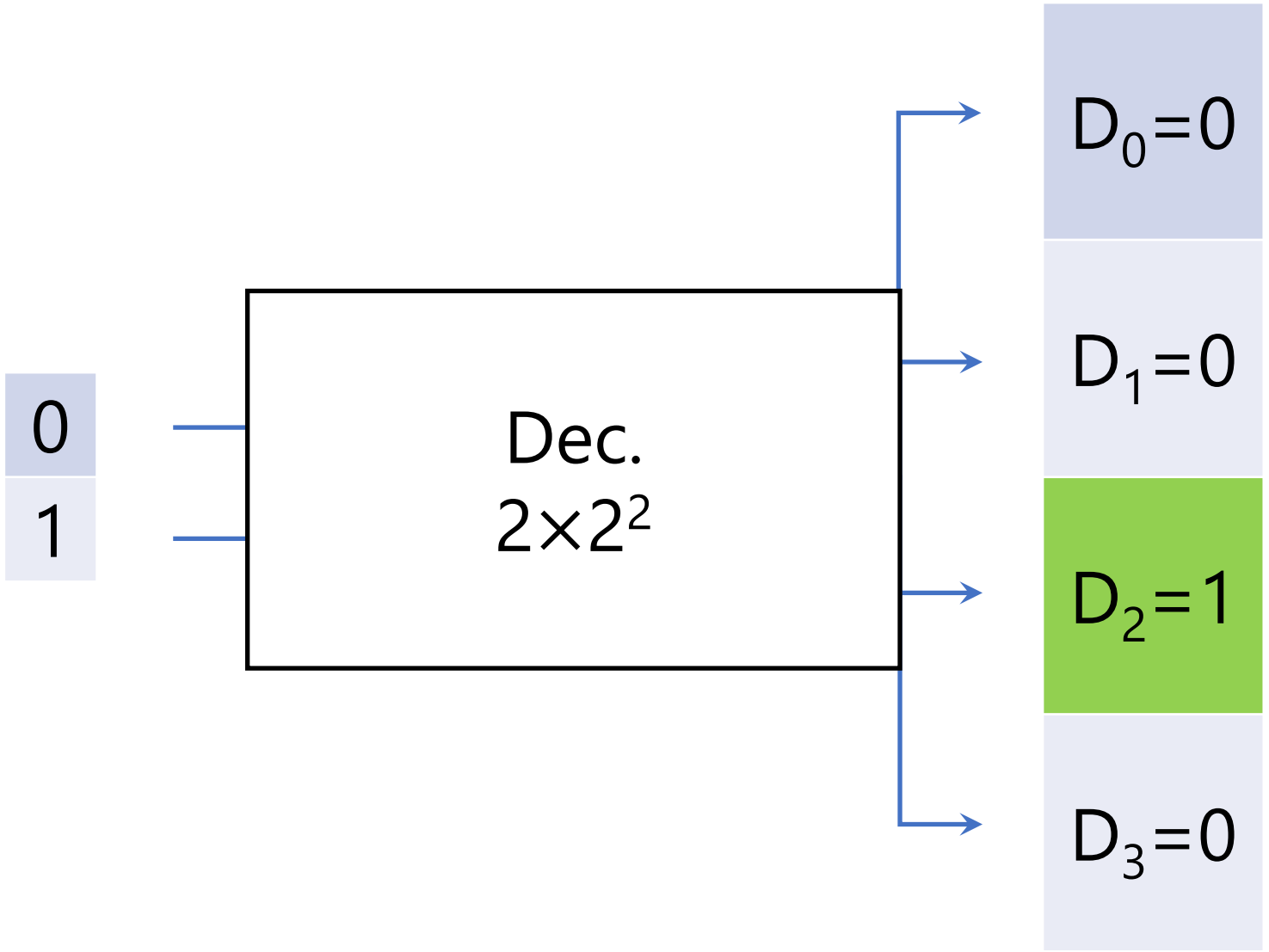
X	$D_0 = m_0$	$D_1 = m_1$
0	1	0
1	0	1

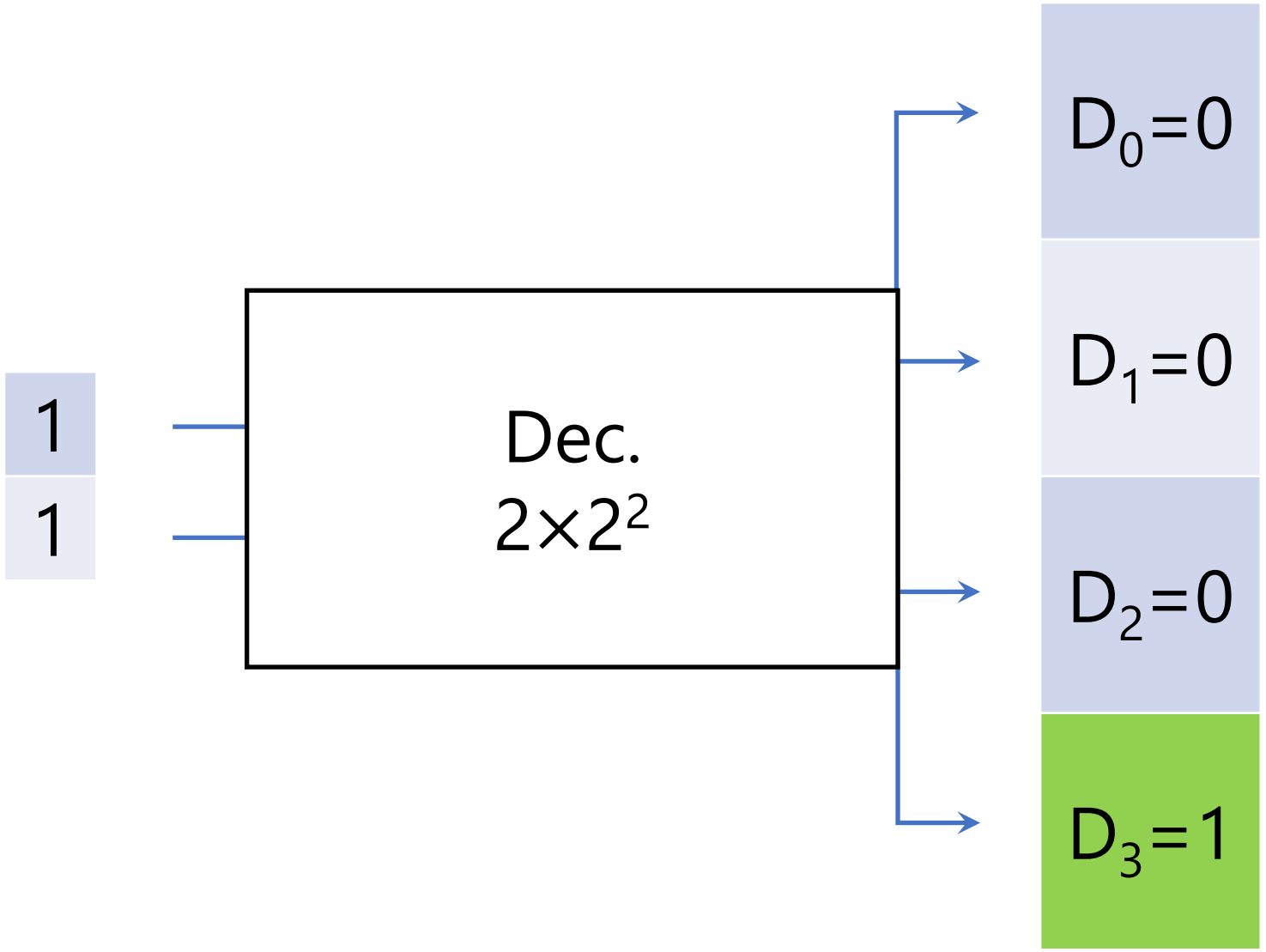

X
D_0
D_1


X
Y
Dec.
2×2²
D0
D1
D2
D3


0
0
Dec.
2×2²
D0=1
D1=0
D2=0
D3=0


1
0
Dec.
2×2²
D0=0
D1=1
D2=0
D3=0


0
1
Dec.
2×2²
D0=0
D1=0
D2=1
D3=0


1
1
Dec.
2×2²
D0=0
D1=0
D2=0
D3=1

Y	X	$D_0=m_0$	$D_1=m_1$	$D_2=m_2$	$D_3=m_3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

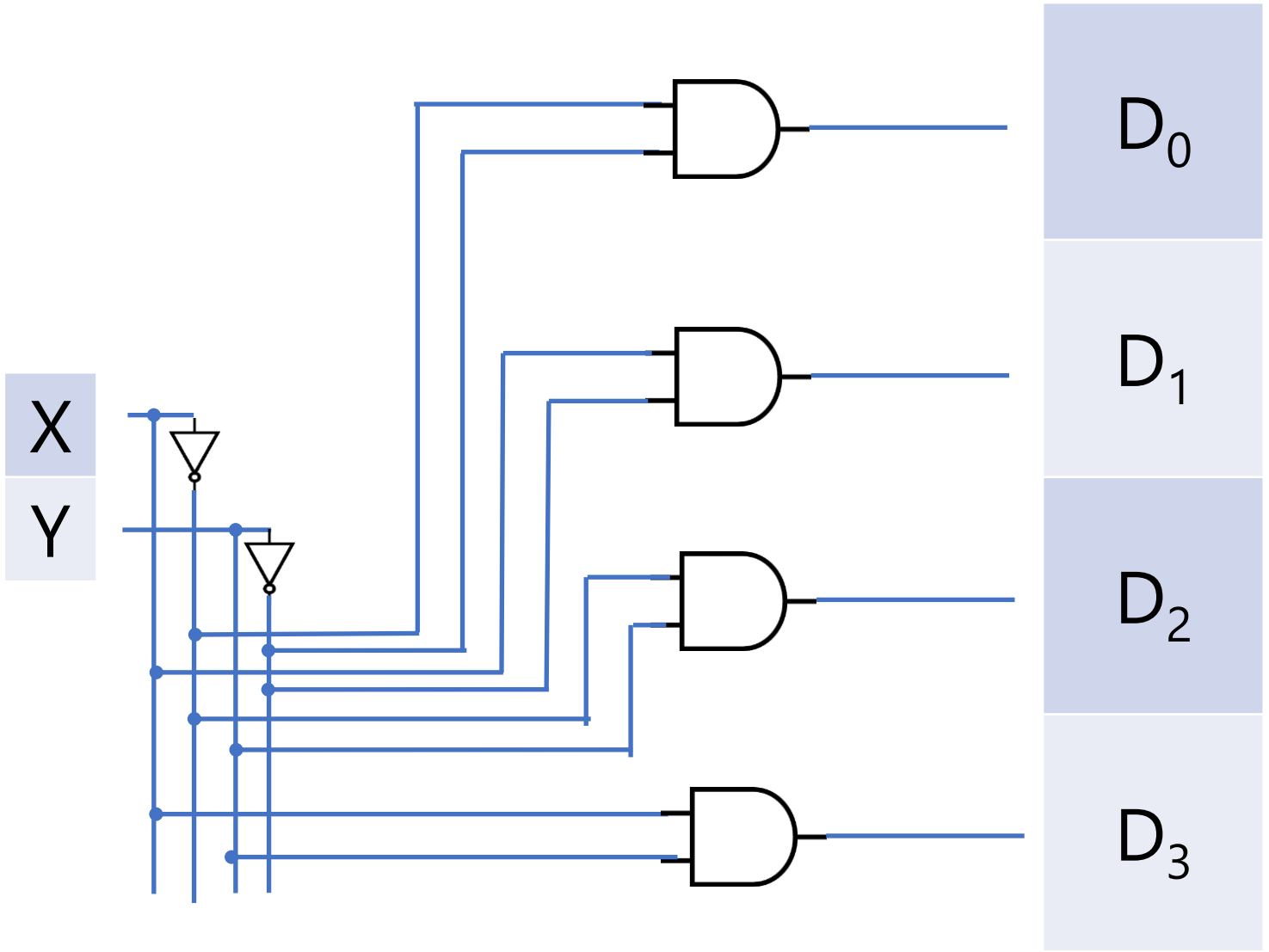

X
Y
D0
D1
D2
D3

Table 4.6
Truth Table of a Three-to-Eight-Line Decoder

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

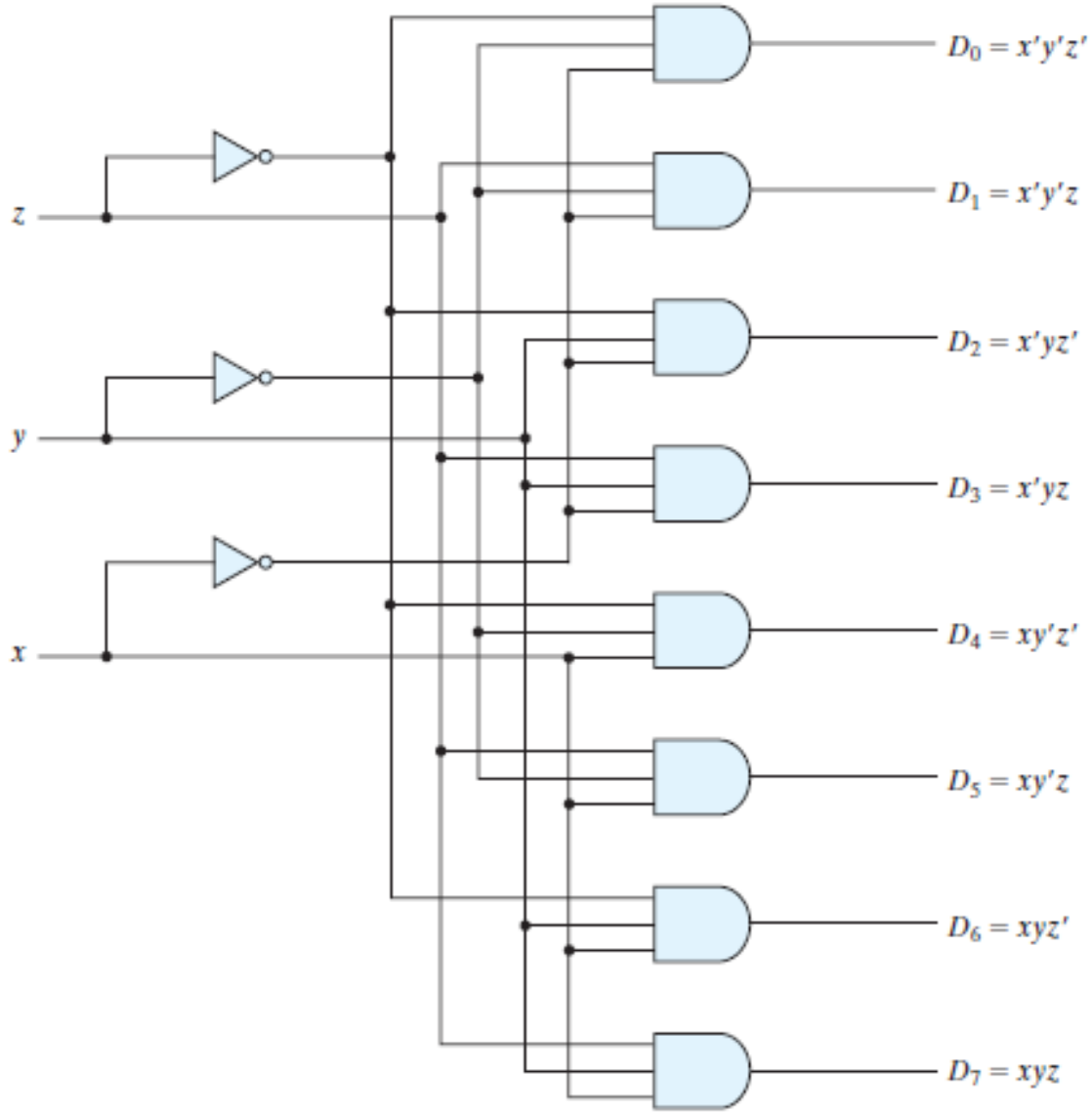


FIGURE 4.18
Three-to-eight-line decoder