

Assignment#	Date	Title	Due Date	Grade Release Date
Lec 09	Week 09	Calculator	March 23, 2022, Wednesday 4 AM EDT	March. 28, 2022

The objectives of the lecture (weekly) assignments are to practice on topics covered in the lectures as well as improve the student's critical thinking and problem-solving skills in ad hoc topics that are closely related but not covered in the lectures. Lecture assignments also help students with research skills, including the ability to access, retrieve, and evaluate information (information literacy.)

### Deliverables

You should answer 2 of the below questions based on your preference using an editor like MS Word, Notepad, and the likes or pen in papers. In the latter case, you have to write and scan the papers clearly and merge them into a single file. In the end, you have to submit all your answers in one **single pdf** file **lec09\_UWinID.pdf** containing the question ids for the answer. Please note that if your answers cannot be read, you will lose marks. Please follow the naming convention as you lose marks otherwise. Instead of UWinID, use your own UWindsor account name, e.g., mine is hfani@uwindsor.ca, so my submission would be: lec09\_hfani.pdf

### Lecture Assignments

**(Select Only 2 Questions based on your preference)**

1. Design a half-subtractor circuit with inputs  $x$  and  $y$  and outputs  $D$  (Difference) and  $B_{out}$  (Output Borrow). The circuit subtracts the bits  $x - y$  and places the difference in  $D$  and the borrow in  $B_{out}$ .
2. Design a full-subtractor (1-bit subtractor) circuit with three inputs  $x$ ,  $y$ ,  $B_p$  in and two outputs  $D$  and  $B_{out}$ . The circuit subtracts  $x - y - B_p$ , where  $B_p$  in is the input borrow from previous subtraction,  $B_{out}$  is the output borrow, and  $D$  is the difference.
3. Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND or OR gates have a propagation delay of 5 ns. What is the total propagation delay time in the 4-bit adder?
4. Design a full-adder (1-bit adder) using 1 half-adder and combination of other Boolean gates.
5. Design a full-adder (1-bit adder) using 2 half-adders and combination of other Boolean gates.
6. Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.
7. Design a *signed*  $n$ -bit multiplier.