University of Windsor
Faculty of Science
School of Computer Science

COMP-2650
Computer Architecture I: Digital Design
Winter 2022

Assignment#	Date	Title	Due Date	Grade Release Date
Lec 12	Week 12	**Sequential Logic**	April 13, 2022, Wednesday 4 AM EDT	April 18, 2022

The objectives of the lecture (weekly) assignments are to practice on topics covered in the lectures as well as improve the student's critical thinking and problem-solving skills in ad hoc topics that are closely related but not covered in the lectures. Lecture assignments also help students with research skills, including the ability to access, retrieve, and evaluate information (information literacy.)

Deliverables

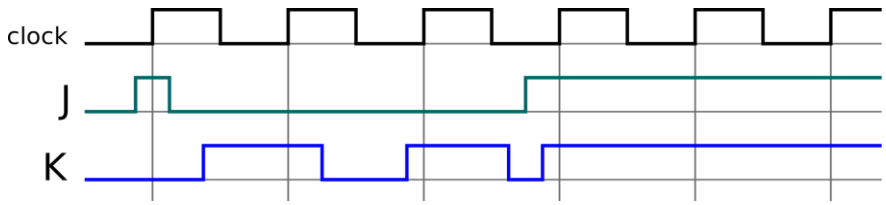
You should answer 2 of the below questions based on your preference using an editor like MS Word, Notepad, and the likes or pen in papers. In the latter case, you have to write and scan the papers clearly and merge them into a single file. In the end, you have to submit all your answers in one single pdf file `lec12_UWinID.pdf` containing the question ids for the answer. Please note that if your answers cannot be read, you will lose marks. Please follow the naming convention as you lose marks otherwise. Instead of UWinID, use your own UWindsor account name, e.g., mine is hfani@uwindsor.ca, so my submission would be: `lec12_hfani.pdf`

Lecture Assignments

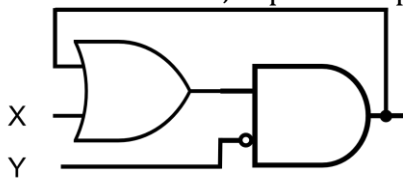
(select only 2 questions based on your preference)

1. Timing Diagram is a diagram that shows the state of a sequential logic within time dimension. Complete the following diagram for Q (main output) for the following cases:

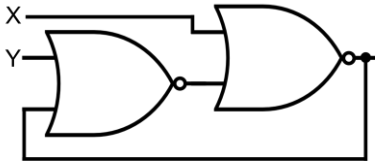
   a. Active high JK latch
   b. Active low JK latch
   c. Positive edge JK
   d. Negative edge JK
   e. Dual-edge JK



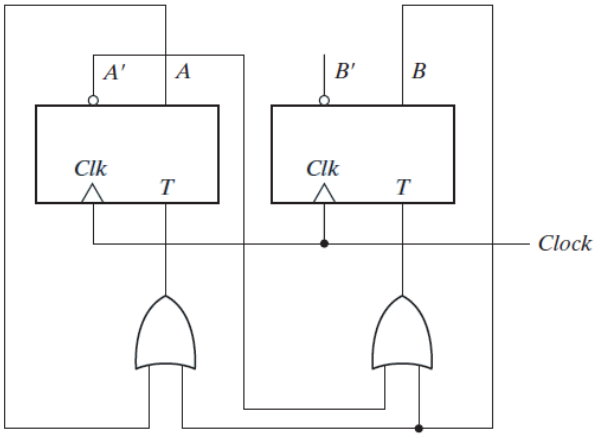
2. Analyze the following design based on different values of X and Y and determine whether it can store a bit of information. If yes, form the characteristic table and show each of the set, reset, store, and complement actions if available. Otherwise, explain the problem with the design.



3. Analyze the following design based on different values of X and Y and determine whether it can store a bit of information. If yes, form the characteristic table and show each of the set, reset, store, and complement actions if available. Otherwise, explain the problem with the design.



4. Derive the state table and the state diagram of the sequential circuit shown below. Explain the function that the circuit performs.



5. Design gated T using gated JK. "Gated" is another name for "latch".

6. Design JK flip-flop using gated JKs (latches).

7. Design SR flip-flop using gated SRs (latches).

8. Design T flip-flop using gated Ts (latches).

9. Flip-Flops that are triggered on both the rising (positive edge) and the falling (negative edge) edge of the clock are called *dual*-edge-triggered flip-flops. Such a flip-flop may be built using two single-edge-triggered flip-flops. Design a dual-edge-triggered for D latch.