University of Windsor

School of Computer Science
Faculty of Science

COMP-2650: Computer Architecture I: Digital Design
Fall 2020

Date	Duration	Title	Due Date	Grade Release Date
Dec 18, 2020	200 minutes	**Final Exam**	Dec. 18, 2020 Midnight AoE	Dec. 25, 2020

Questions

You must show your work and all steps for every question!

Question 1: [10 marks: 2 marks each]
Explain the following terms in two or three sentences.

a. Closure Property
b. Duality
c. Don't Care Condition
d. Latch versus Flip-Flop
e. Moore model

Question 2: [10 marks]
Simplify F=∑(0,2,4,6,8,13,15)+d(10,11,12,13,14) in the form of product of sums using 4-variable K-map.

Question 3: [5 marks: 2.5 marks each]
In a binary multiplier that multiplies an *n*-bit (first number) by *m*-bit (second number) binary numbers,

a. How many *k*-bit adders are needed?
b. How many ANDs, external to the *k*-bit adders are needed?

Question 4: [10 marks]
Design F = ∑(0,2,4,6,8,9,15) using *only one of the options* below:

a. 8-to-1 MUX to get the full marks.
b. 16-to-1 MUX to get half marks.

Question 5: [20 marks]
Design BCD to Aiken encoder.

- **[4 marks]** Truth table
- **[12 marks]** minimization
- **[4 marks]** logic circuit.

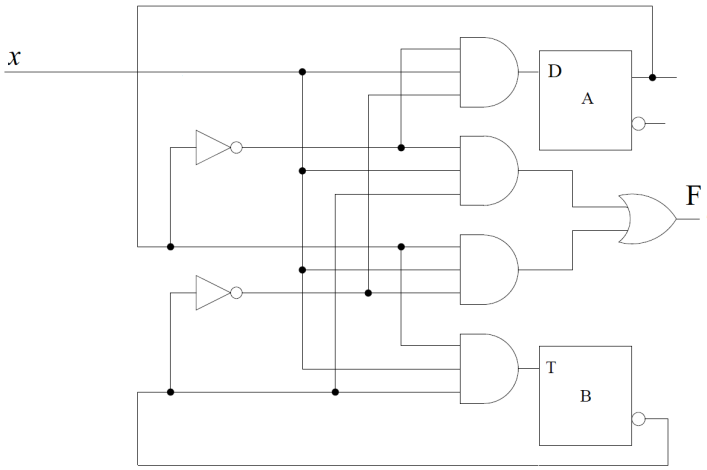
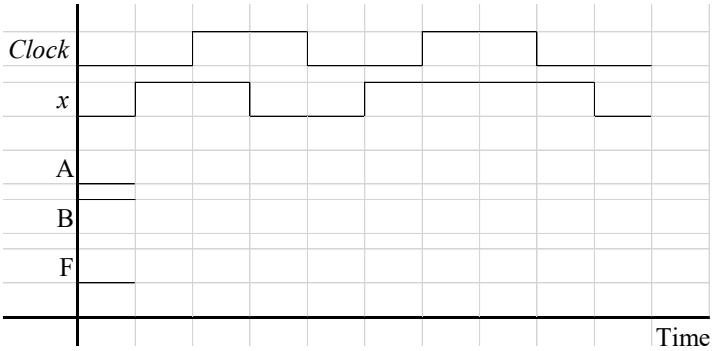


Figure 1. This circuit is needed for Questions 6 and 7. It has one binary input *x*, one binary output F, one T and one D memory units. The memory units are either latches or flip-flops, depending on the question. They are working in *positive* logic.

Question 6: [10 marks: 5 marks each]
Given the circuit in Figure 1 in *positive* logic, complete the timing diagram if the memory units are:

a. Latches.
b. Flip-flops.



Question 7: [10 marks]
Assuming the memory units in the circuit in Figure 1 are flip-flops:

a. **[4 marks]** Draw the state (transition) diagram. (*hints: there would be 4 nodes based on different combinations of BA: 00, 01, 10, 11. From each node there would be two output directed edges based on whether x is 0 or 1. Also, either the edges or nodes need to be labeled by the value of F.)*
b. **[4 marks]** Derive the state table.
c. **[2 marks]** Is the circuit based on the Mealy or Moore model? Justify your answer.

Question 8: [20 marks]
Using D-FFs, design a 3-bit register [C,B,A] with a single input control *x*. If *x*=0, the register shifts the value of the memory units to the *right*. If *x*=1, the register shifts them to the *left*. In shift right, 0 enters C. In shift left, 0 enters A. For instance: *x*=0: 011 → 001, *x*=1: 011 → 110.

a. **[5 marks]** Draw the state diagram of the circuit
b. **[5 marks]** Derive the state table
c. **[10 marks]** Draw the *minimized* logic diagram of the circuit

Question 9: [5 marks]
Given *n*-bit address bus and *m*-bit data bus, how many flip-flops are needed to reach the max memory capacity? Justify your answer.