

**School of Computer Science**

**Faculty of Science**

**COMP-2650: Computer Architecture I: Digital Design**

**Fall 2020**

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| Date | Duration | Title | Due Date | Grade Release Date |
| Dec 18, 2020 | 200 minutes | **Final Exam** | Dec. 18, 2020 Midnight [AoE](https://www.timeanddate.com/time/zones/aoe) | Dec. 25, 2020 |

**Questions**

You must show your work and all steps for every question!

**Question 1: [10 marks: 2 mark each]**

Explain the following terms in two or three sentences.

* 1. Distributivity
  2. Duality
  3. Don’t Care Condition
  4. Latch versus Flip-Flop
  5. Mealy model

**Question 2: [10 marks]**

Simplify F=∑(1,3,5,7,8)+d(10,12,13,14,15) in the form of product of sums using 4-variable K-map.

**Question 3: [5 marks: 2.5 marks each]**

In a binary multiplier that multiplies an *n*-bit (first number) by *m*-bit (second number) binary numbers,

1. How many *k*-bit adders are needed?
2. How many bits would be in the output including the last carry?

**Question 4: [10 marks]**

Design F = ∑(1,2,5,7,8,10,15) using *only one of the options* below:

1. 8-to-1 MUX to get the full marks.
2. 16-to-1 MUX to get half marks.

**Question 5: [20 marks]**

Design BCD to Aiken encoder.

* **[4 marks]** Truth table
* **[12 marks]** minimization
* **[4 marks]** logic circuit.

**Diagram, engineering drawing

Description automatically generated**

**Figure 1.** This circuit is needed for Questions 6 and 7. It has one binary input *x*, one binary output F, one T and one D memory units. The memory units are either latches or flip-flops, depending on the question. They are working in *positive* logic.

**Question 6: [10 marks: 5 marks each]**

Given the circuit in Figure 1 in *positive* logic, complete the timing diagram if the memory units are:

1. Latches.
2. Flip-flops.



**Question 7: [10 marks]**

Assuming the memory units in the circuit in Figure 1 are flip-flops:

1. **[4 marks]** Draw the state (transition) diagram. (*hints: there would be 4 nodes based on different combinations of AB: 00, 01, 10, 11. From each node there would be two output directed edges based on whether x is 0 or 1. Also, either the edges or nodes need to be labeled by the value of F.)*
2. **[4 marks]** Derive the state table.
3. **[2 marks]** Is the circuit based on the Mealy or Moore model? Justify your answer.

**Question 8: [20 marks]**

Using D-FFs, design a 3-bit register [C,B,A] with a single input control x. If *x*=1, the register shifts the value of the memory units to the *right*. If *x*=0, the register shifts them to the *left*. In shift right, 0 enters C. In shift left, 0 enters A. For instance: *x*=1: 011 🡪 001, *x*=0: 011 🡪 110.

1. **[5 marks]** Draw the state diagram of the circuit
2. **[5 marks]** Derive the state table
3. **[10 marks]** Draw the *minimized* logic diagram of the circuit

**Question 9: [5 marks]**

Given *m*-bit address bus and *n*-bit data bus, how many flip-flops are needed to reach the max memory capacity? Justify your answer.