i.MX6 SMART DEVICE SYSTEM

MCIMX6DL-SDP

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GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum
2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.
3. Interrupted lines coded with the same letter or letter combinations are electrically connected.
4. Device type number is for reference only. The number varies with the manufacturer.
5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

Revision History

Rev. Code	Date	Description
X1	11/02/2011	
A	12/15/2011	
AX1		
B	02/17/12	
B1	04/11/12	
B2	05/04/12	
B3	05/25/12	
B4	07/18/12	
B5		
C1		
C2	11/09/12	- Moved Ferrite Beads L10 and L17 to pads for L25 and L26. Camera Analog Voltage supply moved to VGEN3. - Added notes for 24MHz crystal and USB layout design. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 1% resistors due to lead time availability issues.
C3	02/20/13	- Changed BT500 Battery Holder to new manufacturer due to parts availability. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 0.5% resistors due to parts availability. - Changed R97 and R106 pull up resistors to 4.7 Ohm. - Changed R19 pull up resistor to 10K Ohm.

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Multimedia Application Division,
Wireless & Mobile System Group

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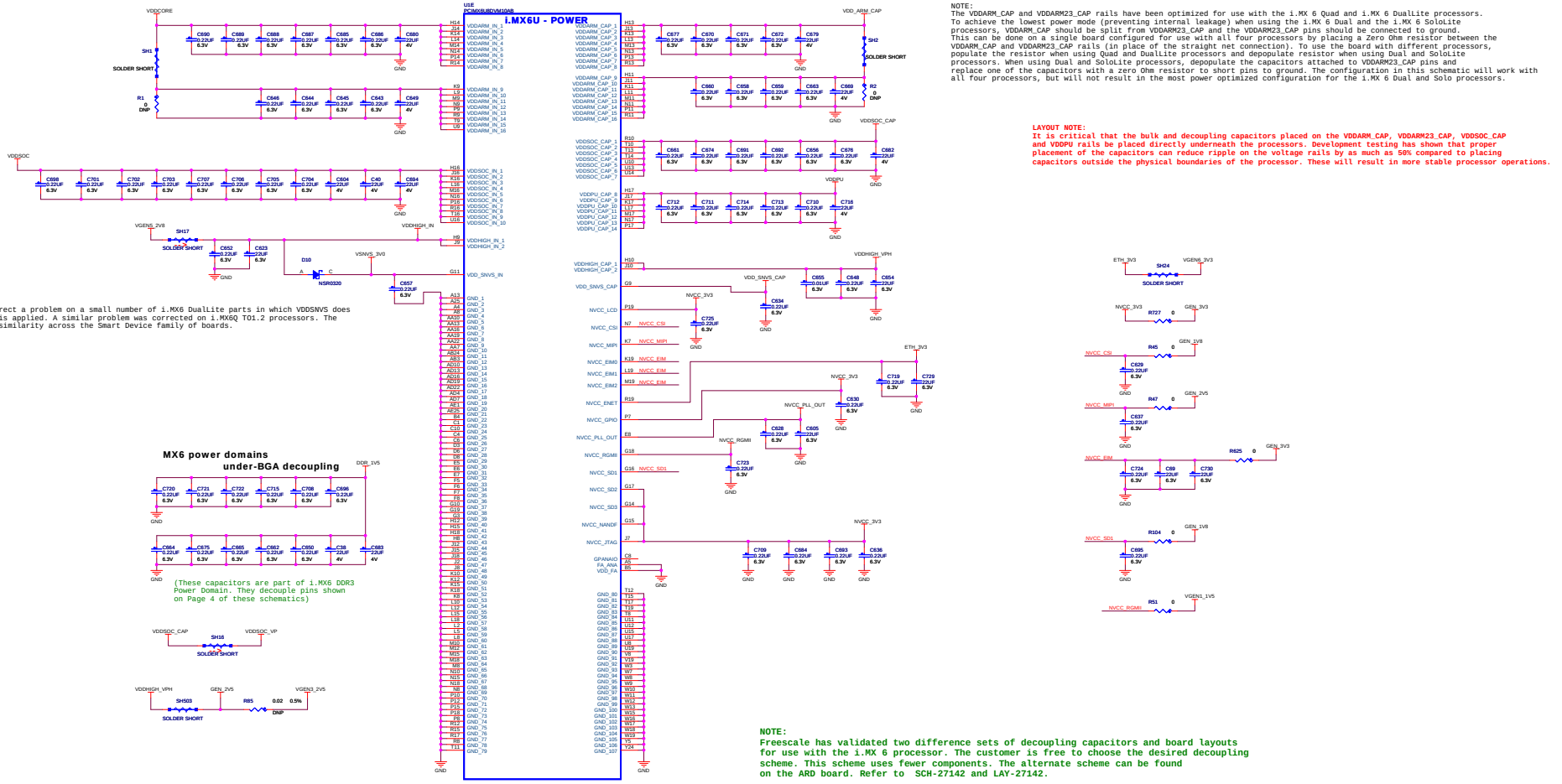
ICAP Classification: FCP: ____ FIUO: ____ PUBI: X

Designer: Mark Middleton	Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM
Drawn by: Mark Middleton	Page Title: TITLE PAGE
Approved: <Approver>	Size: D; Document Number: SOURCE:SCH-27417 PDF:SPF-27417; Rev: C3
	Date: Tuesday, July 02, 2013; Sheet 1 of 25



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

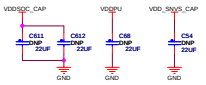
LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

VDDARMxx_xx Power Connections

	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
SH1	Shorted	Open	Shorted	Shorted
SH2	Shorted	Open	Shorted	Shorted
R1	Open	Shorted	Open	Open
R2	Open	Shorted	Open	Open

Extra Bulk Capacitors



NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

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ICAP Classification:	FCP: FUO: PUB: X
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM
Page Title:	CPU POWER
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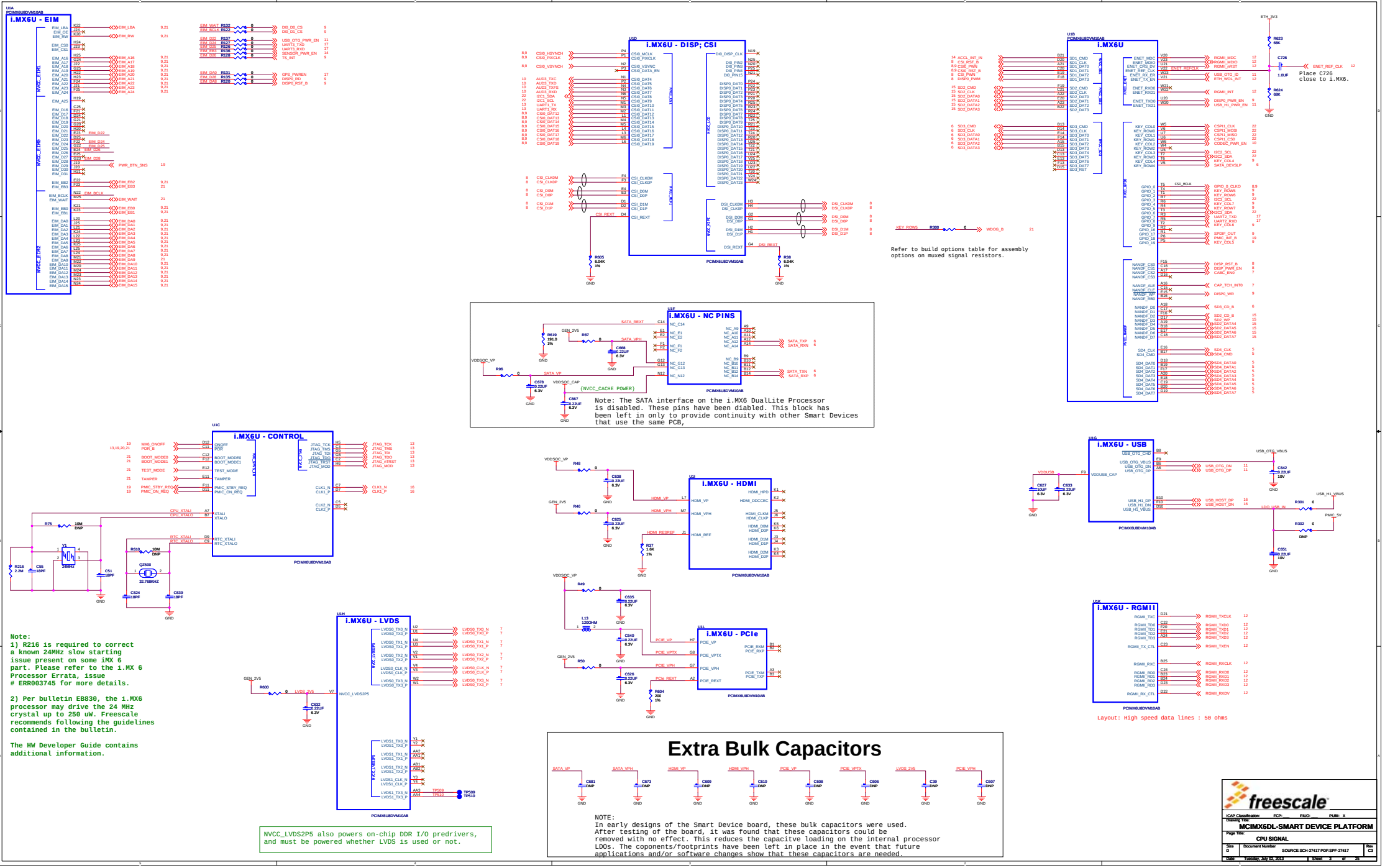
i.MX6U - EIM
i.MX6U - DISP; CSI
i.MX6U - NC PINS
i.MX6U - CONTROL
i.MX6U - HDMI
i.MX6U - USB
i.MX6U - PCIe
i.MX6U - LVDS
i.MX6U - RGMII
i.MX6U
Refer to build options table for assembly options on muxed signal resistors.
Note: The SATA interface on the i.MX6 Dualite Processor is disabled. These pins have been diabled. This block has been left in only to provide continuity with other Smart Devices that use the same PCB,
Place C726 close to i.MX6.
Layout: High speed data lines : 50 ohms
Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.
The HW Developer Guide contains additional information.
NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.
Extra Bulk Capacitors
NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.
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MCIMX6DL-SMART DEVICE PLATFORM
CPU SIGNAL
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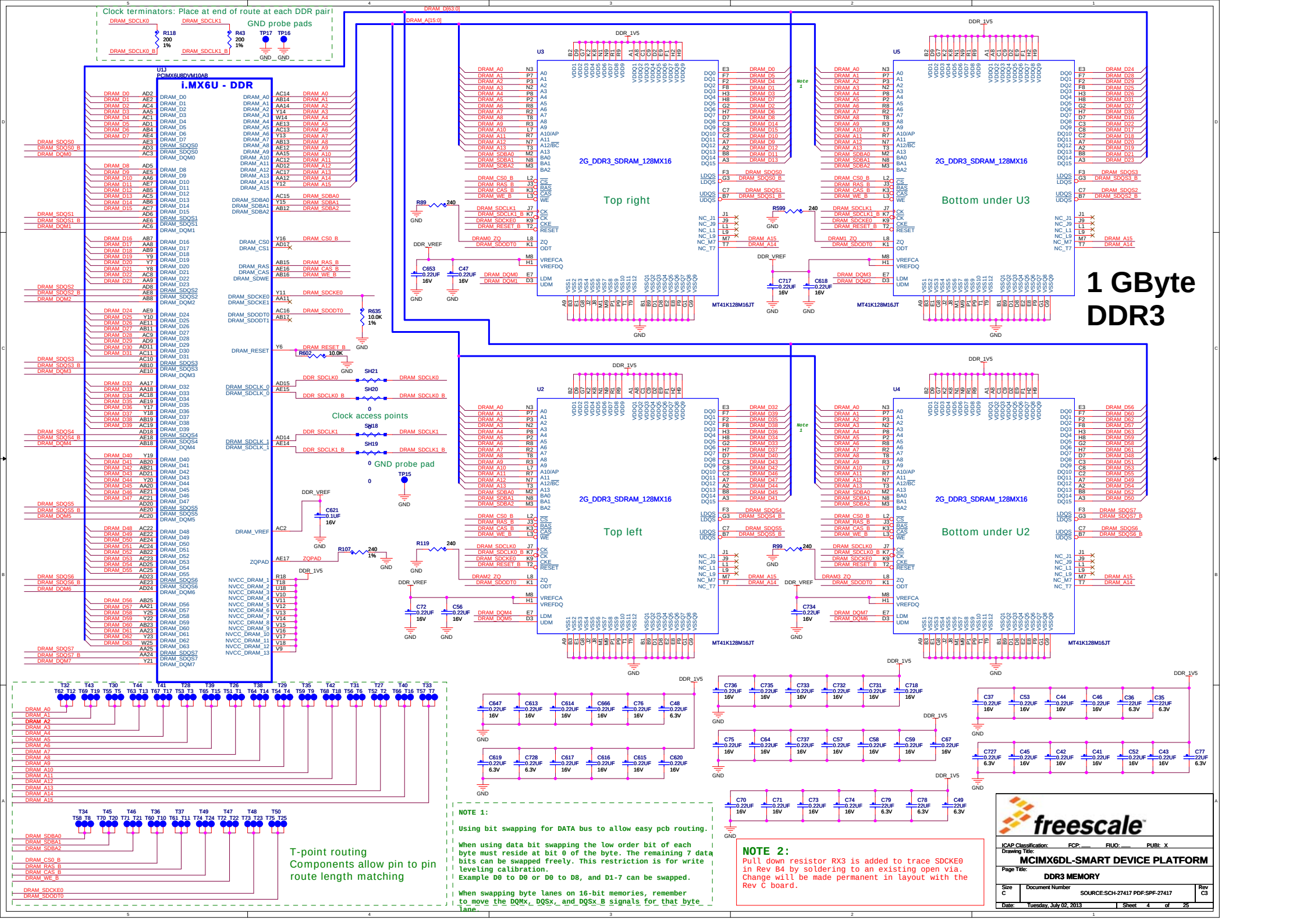
Clock terminators: Place at end of route at each DDR pair
GND probe pads
i.MX6U - DDR
U1J
MCIMX6U8DVM10AB
2G_DDR3_SDRAM_128MX16
MT41K128M16JT
Top right
Bottom under U3
Top left
Bottom under U2
1 GByte DDR3
Clock access points
GND probe pad
T-point routing
Components allow pin to pin route length matching
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
NOTE 2:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.
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PUBI: X
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MCIMX6DL-SMART DEVICE PLATFORM
Page Title:
DDR3 MEMORY
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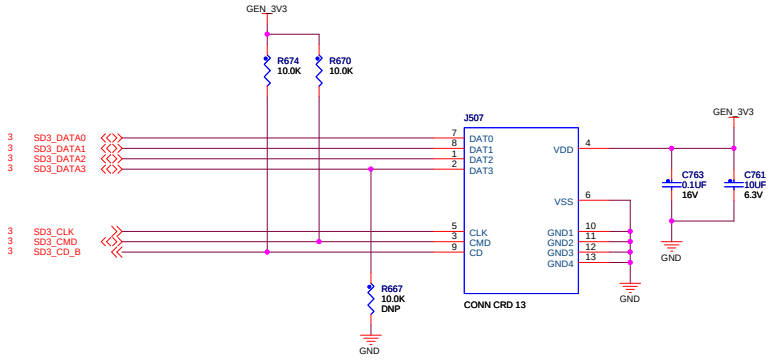
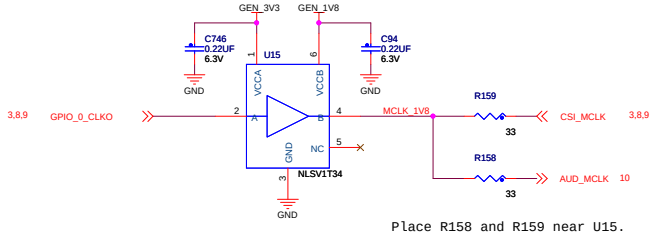
SD CARD SOCKET





Place R158 and R159 near U15.
Acts as source termination.

Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

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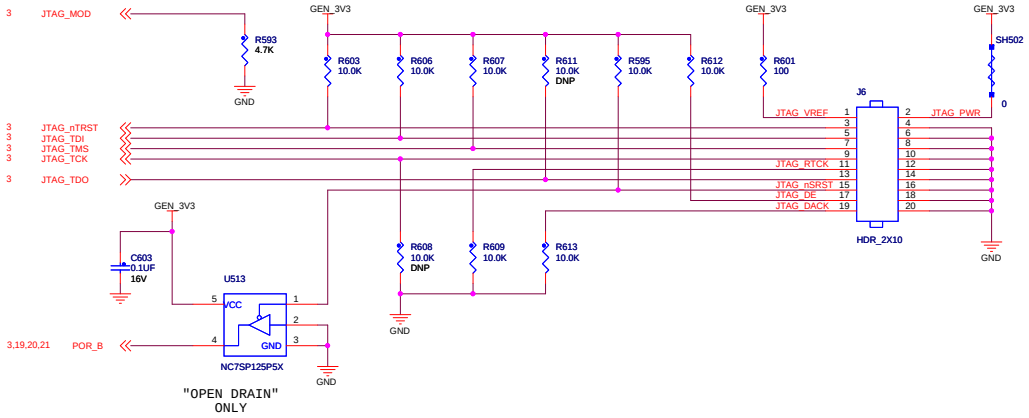
JTAG



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Page Title:	JTAG, DEBUG		
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PMIC LDO Outputs

PMIC Switched Outputs

PMIC Powered-ON LED indicator

PMIC Control

POWER

OPTIONAL: PMIC Power On Circuit

Note:
Bulk capacitors on VGEN1-6 are all 4.7uF for BOM consolidation purposes. Freescale recommended guidance for minimum capacitance on VGEN1, VGEN3, VGEN5, VGEN6 is 2.2uF.

NOTE:
R632 is provided for testing an alternate gating source for PMIC_5V power. The circuit has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

VDDOTP -
Connect TP14 to 8 volts to program PMIC OTP fuses

Default state:
I2C Address:0X08
PWRON:Level sensitive

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Note:
PMPF0100 Pass1.0 through Pass1.2 are subject to boot issues if power is removed from the board and reapplied within ~ 2 minutes.
PMPF0100 Pass2.0 will correct this issue. For more details, see the PMPF0100 ERRATA, Issue #ER19

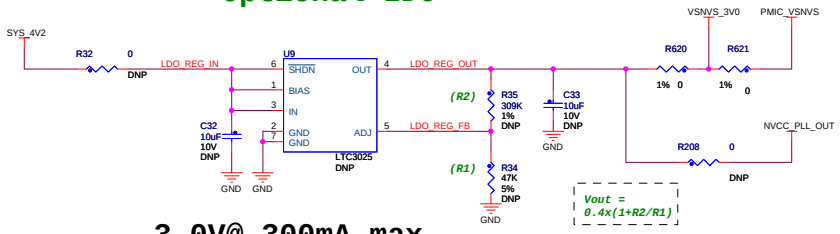
Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A	1.375	1	2155	1001	
SW1B					
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A	1.5	3	1500	760	
SW3B					
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:				4454	

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
		HDMI			
	AUX_5V	SATA	MAX8815	1000	
		LVDS0			
		CAN			
3.3	GEN_3V3	EMMC	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
		SENSORS			
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
		TOUCH			
		GPS			
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
		ACC			
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS	PF0100 VGEN1	100	
		mPCIe			
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

Optional LDO



3.0V@ 300mA max

U9 is no longer required for PF0100 VSNVS issue, but may be desired for NVCC_PLL_VOUT.
It is being left in a depopulated condition. If the LDO is needed, R34 and R35 should be populated as follows:
For VSNVS (3.0V): R34 = 47K, R35 = 309K
For NVCC_PLL_OUT (1.1V): R34 = 47K, R35 = 82.5K

NOTE FOR VDDHIGH_IN LOADING ON VGEN5:
VDDHIGH was placed on VGEN5 early in the design as a compromise solution for a board designed primarily for software development. Validation of the i.MX6 processor has shown that operations at elevated temperatures may cause VDDHIGH_IN to require much more current than VGEN5 can supply. It is recommended for robust designs potentially operating at more extreme temperatures for VDDHIGH to be supplied from a power rail that can supply 250 mA or more.
This allows for datasheet maximum of 125 mA for internal VDDHIGH_IN loads plus 125 mA for external PHY IO loads.

The optional LDO U9 shown on this page could be reconfigured to supply both VDDHIGH_IN and VDD_SNVS_IN loads to meet the additional current requirments

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Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM
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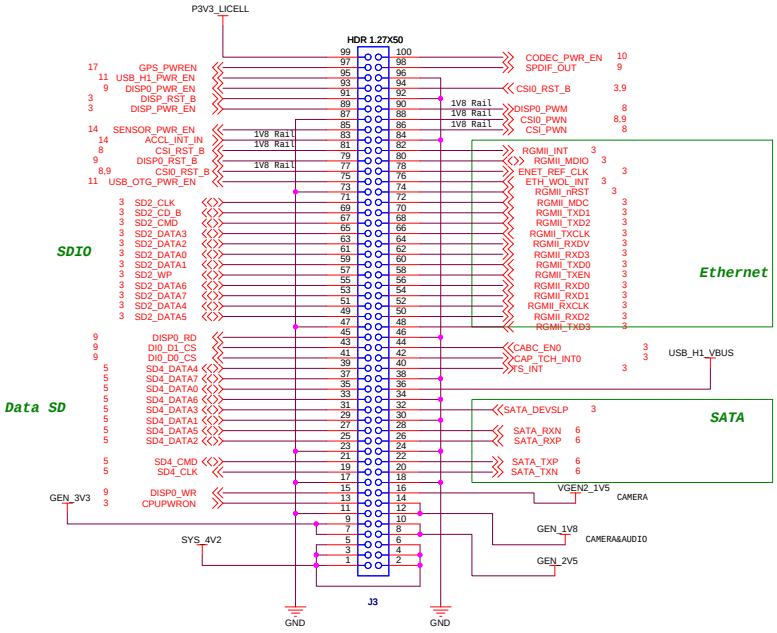
BOARD-TO-BOARD CONNECTION

Mating connector on Base Board

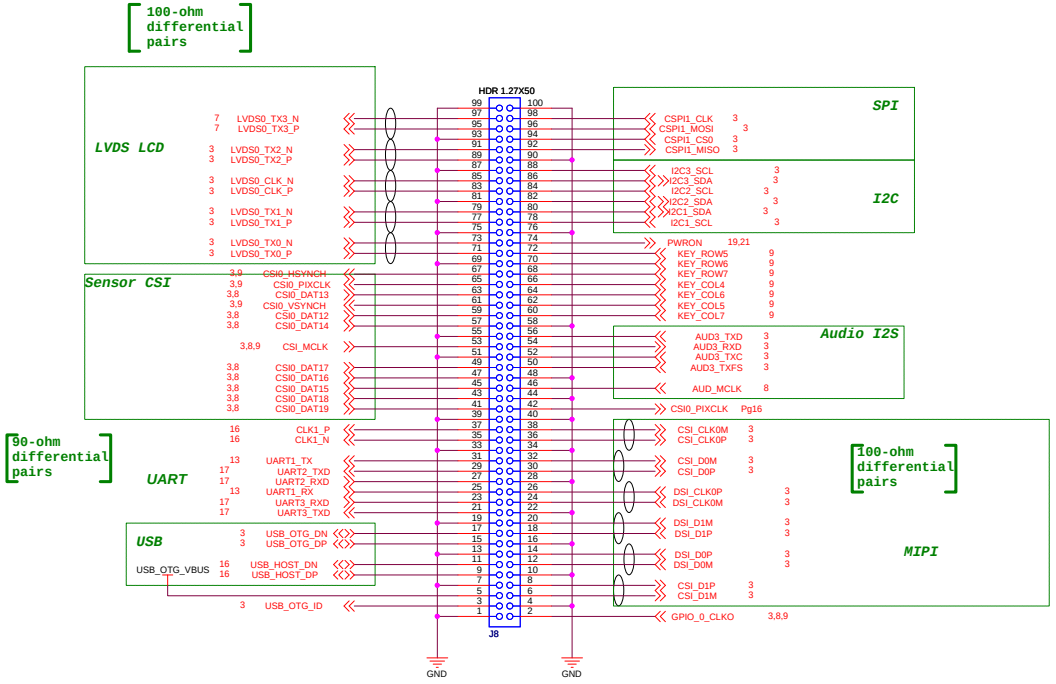
PWM

>4.8V match PF0100
1 to 4 A typical

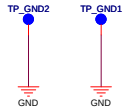


100-ohm differential pairs

90-ohm differential pairs



Ground Test Points



NOTES:

1 If not Android, can be used as GPIO on Main Board. Main Board schematic cross-reference table does not apply to MX6.

2 Could be used as spare GPIO if SPI NOR is not needed.

3 Could be used as spare open-drain GPIO if not needed for local CAN PHY wake up.

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Drawing Title: MCIMX6DLAICPU1

Page Title: Card Edge Fingers

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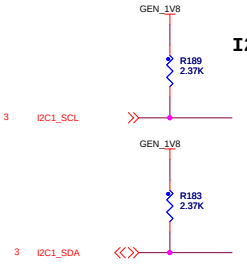
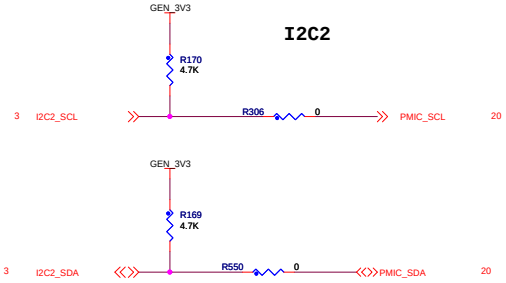
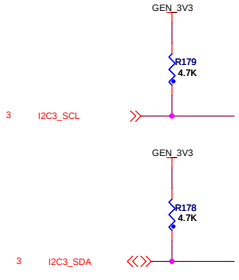


I2C1

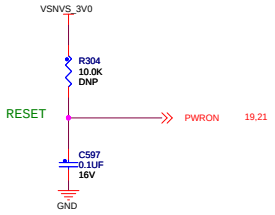
NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.



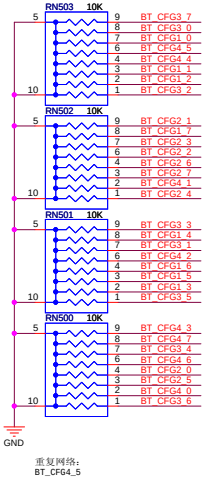
I2C2



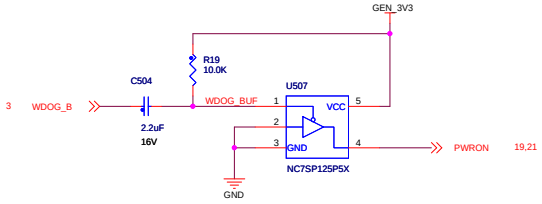
I2C3

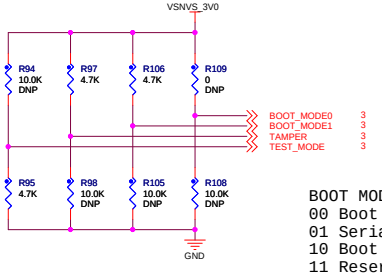


NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.



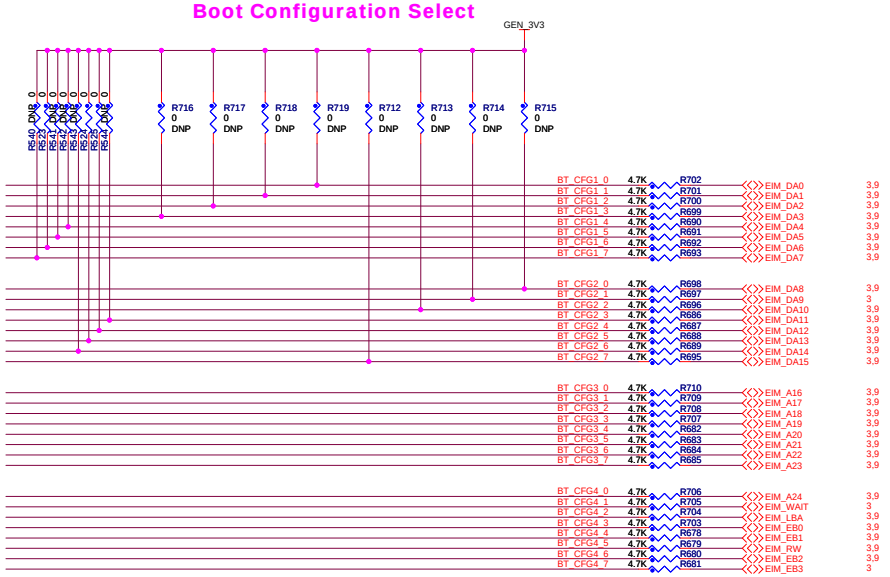
重复网络:
BT_CFG4_5





BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

Boot Configuration Select



NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0

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