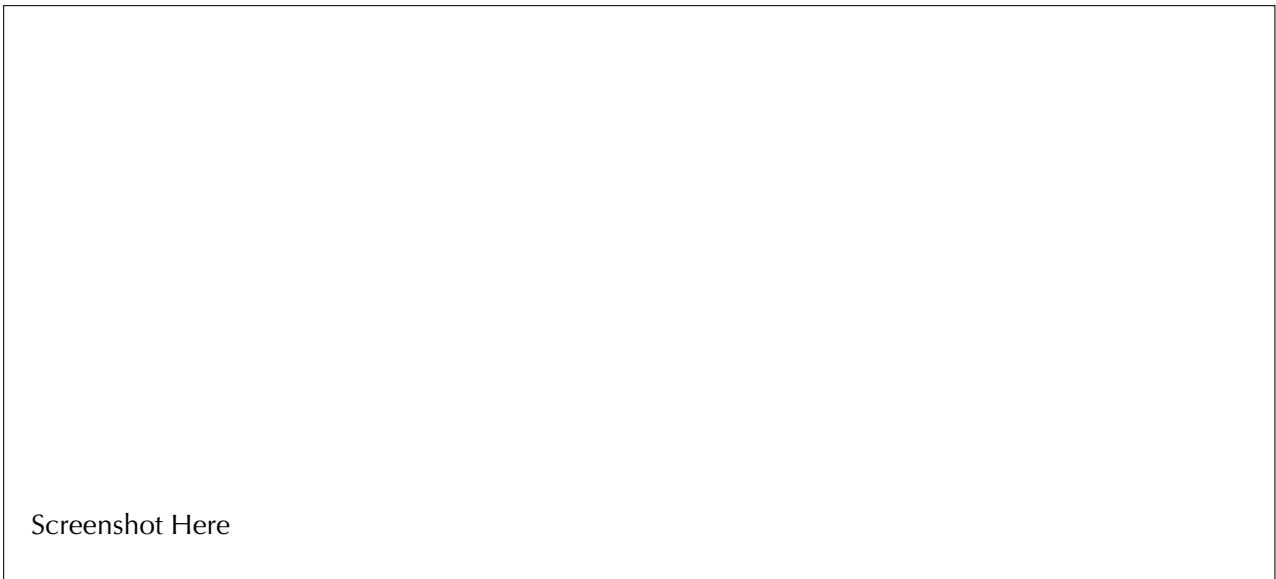| First name	
Last name	
Collaborator	
Pledge	

1 Reading a Register File

In this part, we will test if reading register file works for all four registers.

(1) First of all, manually set up register values. Click on the grey box in each register, and type two digits of hexadecimal to set the data stored in that register. You can pick any value you like, but the four registers should not have any equal values;

(2) Open timing diagram from the menu bar, and start simulation. You should be able to see the clock ticking;

(3) Change the value of `ReadReg1` from `00b`, `01b`, `10b`, to `11b`. For each of the value, you should be able to see the change on `RegData1`. After changing all four values, take a screenshot of **both** the timing diagram and the circuit. The diagram should show that the value of `RegData1` has been changed four times. They also should change immediately after the change of `ReadReg1`;

Screenshot Here

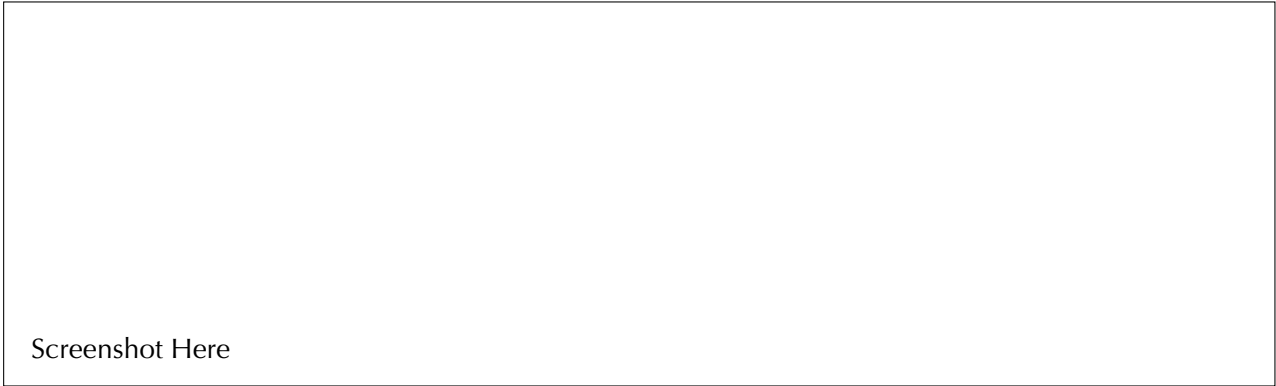(4) Repeat the above step for `ReadReg2` .

Screenshot Here

2   Writing a Register File

In this part, we will test if writing register file works for all four registers.

(1) First of all, reset the circuit (Menu bar ▶Simulate ▶Reset simulation). **Make sure** all four registers now have values of `0` ;

(2) Set control signal `RegWrite` to `1` , and change `RegDataW` to any non-zero number you like;

(3) Open timing diagram from the menu bar, and start simulation. You should be able to see the clock ticking;

(4) Change the value of `WriteReg` from `00b` to `11b` . **Be careful:** because writing register is sequential, and so the data will only be updated at rising edge, make sure you wait long enough to change `WriteReg` ;

(5) At the end, you should be able to see all four registers have been updated to the same value. Please provide a screenshot below. **Note:** it has to be timing diagram showing the values – not the grey boxes in the registers;

Screenshot Here
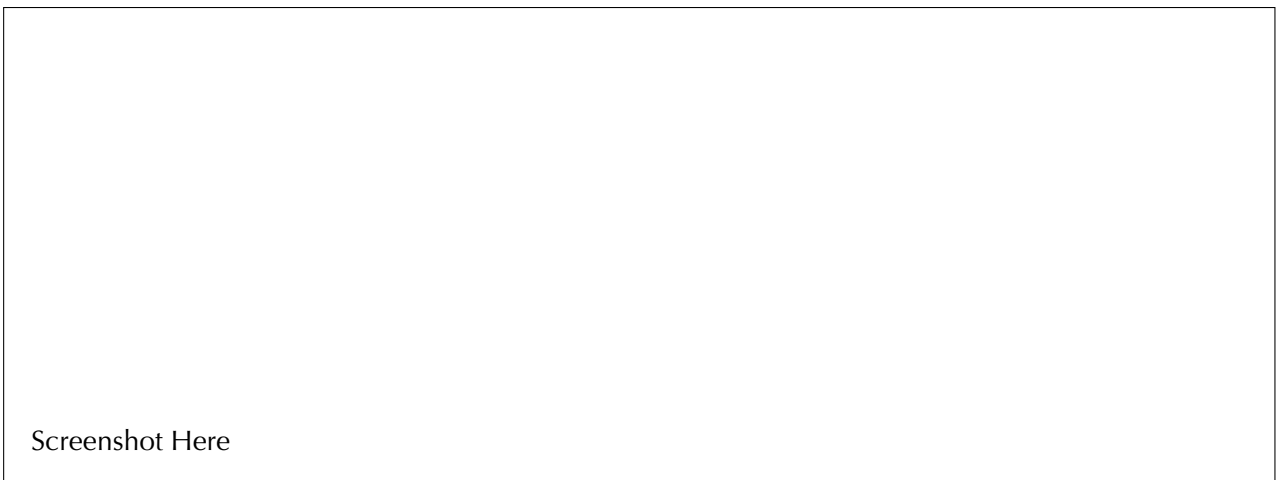
(6) Now, **pause** the simulation, and change `RegDataW` to `0`, and set control signal `RegWrite` to `0`. Set `WriteReg` back to `00b`;

(7) Restart the simulation, and again change the value of `WriteReg` from `00b` to `11b`. Also be aware of the timing of these changes;

(8) At the end, you should not observe any value change of all four registers. Please provide a screenshot of the timing diagram below:

Screenshot Here

The End ✋