

ZCU102 Evaluation Board

User Guide

UG1182 (v1.6) June 12, 2019



Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|------------|---------|---|
| 06/12/2019 | 1.6 | Chapter 3, Board Component Descriptions . Replaced Table 3-7 . Updated HDMI Video Output in Chapter 3 . Updated Figure 3-23 . Updated Table 3-30 for pin B1. Added HDMI Video Input section. Enhanced Figure A-1 . |
| 01/11/2019 | 1.5 | Changed DDR4 72-bit to DDR4 64-bit in Figure 1-1 and PS-Side: DDR4 SODIMM Socket in Chapter 3 . Removed ECC from Board Features . Updated Table 2-1 , callout 2, with DDR4 SODIMM and updated the Micron part number (MTA4ATF51264HZ-2G6E1). Updated Markings . |
| 10/04/2018 | 1.4 | <ul style="list-style-type: none">Updated Figure 2-1 and Figure 2-2.Added Electrostatic Discharge Caution in Chapter 2.Updated schematic number in Table 2-1.Updated SFP0-SFP3 functions in Table 2-3.Updated callout in Cooling Fan Connector in Chapter 3.Updated descriptions in PS-Side: DDR4 SODIMM Socket and PL-Side: DDR4 Component Memory in Chapter 3.Updated Ports 0 and 4 I2C address in Table 3-23.Added Note in SFP/SFP+ Connector in Chapter 3.Updated Bank info in SFP+ in Chapter 3.Updated I/O Standard for AE5 and AF5 in Table 3-52.Updated Appendix B, Xilinx Design Constraints.Updated Appendix C, Regulatory and Compliance Information.Updated XTP433 and XTP435 links and added DS925 and ZCU102 Design Hub link in Appendix D, Additional Resources and Legal Notices. |
| 08/02/2017 | 1.3 | Updated logic cell and CLB flip-flop resource count in Table 1-1 . Added Note 2 to Table 2-2 . Changed maximum PL internal supply voltage from 0.875V to 0.876V in Table 3-1 . Updated GTR_REF_CLK_USB3 frequency in Table 3-12 . Added I2C addresses to Table 3-23 and Table 3-24 . Clarified third paragraph under HDMI Clock Recovery in Chapter 3 . |
| 03/20/2017 | 1.2 | Added notes to Dimensions in Chapter 1 . Updated SW6 default switch setting in Table 2-2 and SD configuration setting in Table 2-4 . Clarified SW6[4:1] boot mode pin settings under Quad-SPI and SD in Chapter 2 . Changed "DDR SODIMM Memory J1" heading to "DDR Component Memory" in Table 3-4 . Changed PS_REF_CLK frequency from 33 MHz to 33.33 MHz in Table 3-12 . Changed "UART2_RTS_O_B" to "UART2_CTS_O_B" in Table 3-16 . Replaced Figure 3-16 . Changed "QSPI119 (LWR), U120 (UPR)" heading to "MSP430 U41" in Figure 3-17 . Clarified references to Figure 3-17 in Table 3-19 and Table 3-20 . Added addresses to titles in Table 3-21 and Table 3-22 and headings in Table 3-23 and Table 3-24 . Changed "22" to "L22" in Table 3-28 . Updated GTH connectivity for Quad 128, Quad 228, Quad 229, and Quad 23 under GTH Transceivers in Chapter 3 . Updated bank assignments in Figure 3-36 . Added callout 44 to Switches in Chapter 3 . Updated Xilinx websites in Appendix D, Additional Resources and Legal Notices . |

| Date | Version | Revision |
|------------|---------|---|
| 11/16/2016 | 1.1 | Updated device part number from XCZU9EG-2FFVB1156 to XCZU9EG-2FFVB1156I throughout document. Updated board photos (Figure 2-1 and Figure 2-2) to rev 1.0. Updated Table 2-1 and Table 2-3 . Updated Component Descriptions in Chapter 3 . Updated Appendix B, Xilinx Design Constraints . |
| 05/11/2016 | 1.0 | Initial Xilinx release - limited distribution. |

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Introduction

Overview

The ZCU102 is a general purpose evaluation board for rapid-prototyping based on the Zynq® UltraScale+™ XCZU9EG-2FFVB1156E MPSoC (multiprocessor system-on-chip). High speed DDR4 SODIMM and component memory interfaces, FMC expansion ports, multi-gigabit per second serial transceivers, a variety of peripheral interfaces, and FPGA logic for user customized designs provides a flexible prototyping platform.

Block Diagram

The ZCU102 board block diagram is shown in [Figure 1-1](#). Page numbers in the block diagram reference the corresponding page number(s) of schematic 0381701.

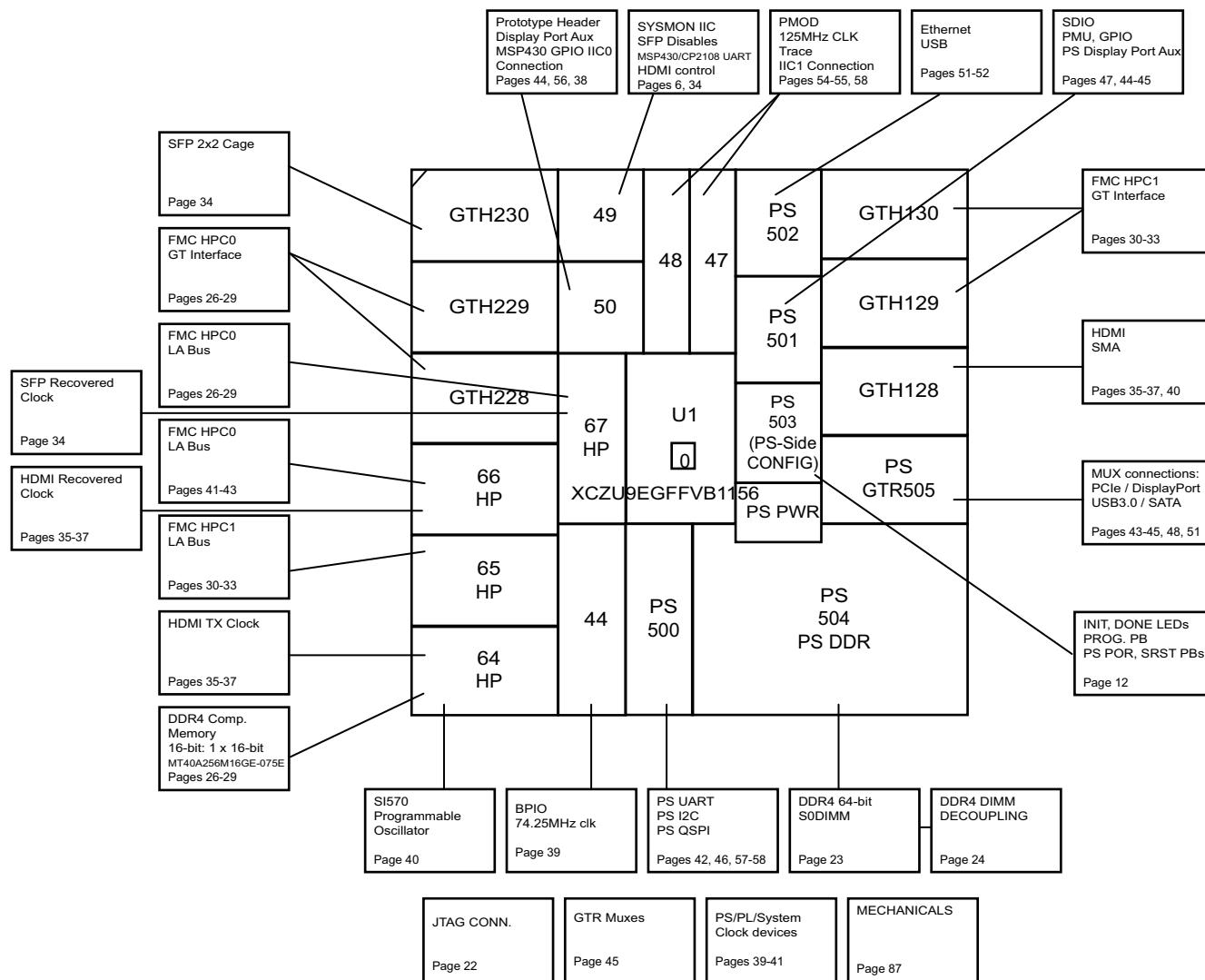


Figure 1-1: ZCU102 Evaluation Board Block Diagram

Board Features

The ZCU102 evaluation board features are listed here. Detailed information for each feature is provided in [Chapter 3, Board Component Descriptions](#).

- XCZU9EG-2FFVB1156E MPSoC
- PL V_{CCINT} for range in datasheet
- Form factor for PCIe Gen2x4 Host, Micro-ATX chassis footprint
- Configuration from QSPI
- Configuration from SD card
- Configuration over JTAG with PC4 header
- Configuration over JTAG with Arm 20-pin header
- Configuration over USB-to-JTAG Bridge
- Clocks (PL-system, PS_CLK, Programmable Clock, SMA, SMA_GT_REF, Ethernet, USB)
- PS DDR4 64-bit SODIMM
- PL DDR4 component (16-bit)
- PS GTR assignment
 - SATA
 - DisplayPort
 - USB3
 - PCIe Gen2x4 Root Port
- PL GTH assignment
 - FMC #1 (8 GTH) and FMC #2 (8 GTH) PL GT assignment
 - High-Definition Multimedia Interface (HDMI™) technology (3 GTH) PL GT assignment
 - SFP+ (4 GTH) PL GT assignment
 - SMA (1 GTH) PL GT assignment
- PL FMC HPC #1 Connectivity - Full LA Bus
- PL FMC HPC #2 Connectivity - Partial LA Bus
- PS MIO: QSPI
- PS MIO: Ethernet
- PS MIO: USB2 (same connector as USB3)

- PS MIO: SD
- PS MIO: CAN
- PS MIO: UART (using USB-to-UART bridge)
- PS MIO: second UART
- PS MIO: I2C shared across PS and PL
- PS/PL EMIO: Trace
- PL-side UART
- PL-side LEDs (8)
- PL-side DIP switch (8-position)
- PL-side pushbuttons (5)
- PS-side pushbutton (1)
- PS-side LED (1)
- System user switches (PROG, CPU Reset)
- PjTAG
- Security - PSBATT button battery backup
- SYSMON
- Operational switches (Power on/off, PROG, Boot mode)
- Operational status LEDs (power supply status, INIT, DONE, PG, JTAG status, DDR power good)
- Power Management

The ZCU102 evaluation board provides designers a rapid prototyping platform using the XCZU9EG-2FFVB1156E device. The ZU9EG contains many useful processor system (PS) hard block peripherals exposed through the Multi-use I/O (MIO) interface and a variety of FPGA programmable logic (PL), high-density (HD) and high-performance (HP) banks. [Table 1-1](#) lists a brief summary of the resources available within the ZU9EG. A feature set overview, description, and ordering information is provided in the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [\[Ref 1\]](#).

Table 1-1: Zynq UltraScale+ MPSoC ZCU9EG Features and Resources

| Feature | Resource Count |
|---------------------------------|----------------------------|
| HD banks | 5 banks, total of 120 pins |
| HP banks | 4 banks, total of 208 pins |
| MIO banks | 3 banks, total of 78 pins |
| PS-side GTR 6 Gb/s transceivers | 4 PS-GTRs |

Table 1-1: Zynq UltraScale+ MPSoC ZCU9EG Features and Resources (Cont'd)

| Feature | Resource Count |
|------------------------------------|----------------|
| PL-side GTH 16.3 Gb/s transceivers | 24 GTs |
| Logic cells | 599,550 |
| CLB flip-flops | 548,160 |
| Max. distributed RAM | 8.8 Mb |
| Total block RAM | 32.1 Mb |
| DSP slices | 2,520 |

Board Specifications

Dimensions

Width: 9.350 in. (23.749 cm)

Length: 9.600 in. (24.384 cm)

Thickness: 0.104 in. (0.2642 cm)

Notes:

- A 3D model of this board is not available.
- ZCU102 board documentation (xdc listing, schematics, layout files and board outline/fab drawings, etc.) is available on the web at www.xilinx.com/zcu102.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU102 board component locations. Each numbered component shown in Figure 2-1 is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic page numbers, and links to a detailed functional description of the components and board features in Chapter 3.



IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the latest revision of the board. (This user guide documents ZCU102 Rev. 1.0 and later.)*



IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions is not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic and xdc of the specific ZCU102 version of interest for such details.*

Electrostatic Discharge Caution

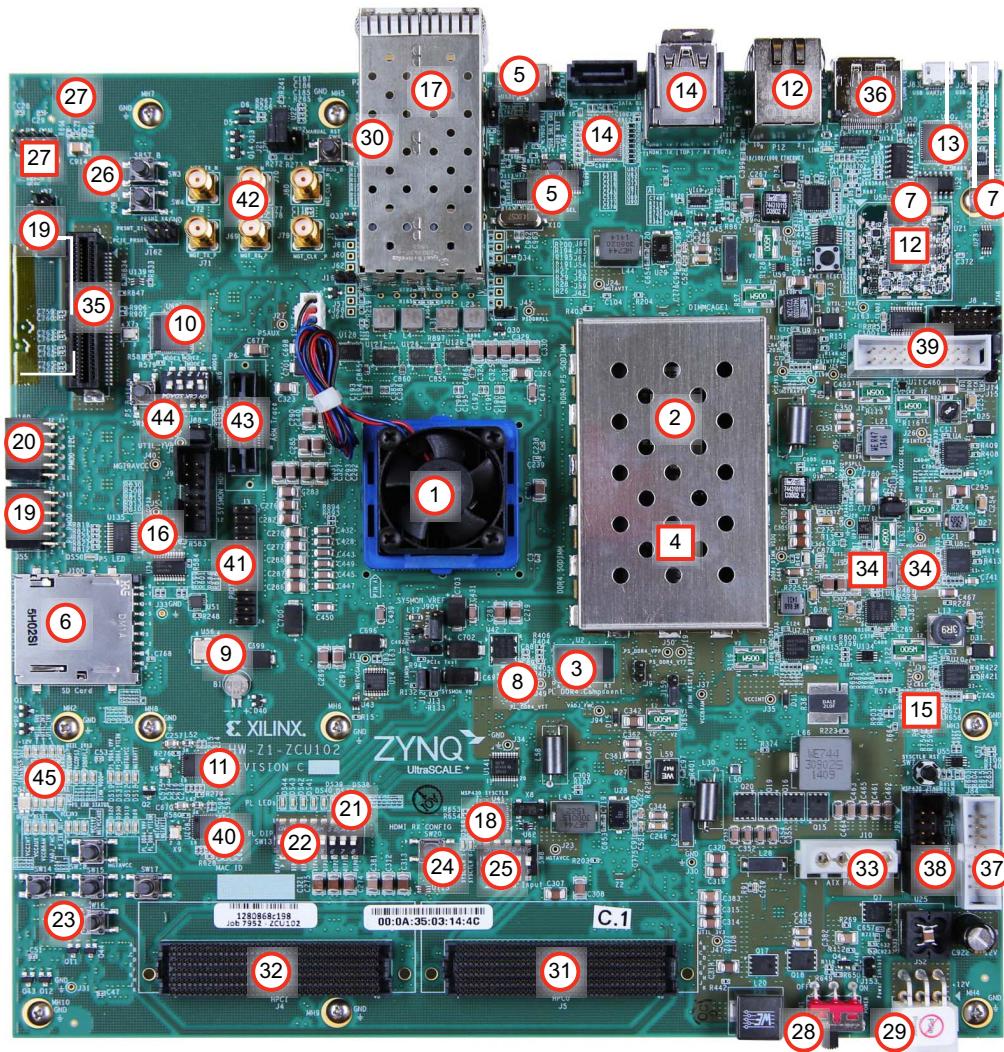


CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.

- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.



Round callout references a component
On the front side of the board
00

Square callout references a component
On the back side of the board
00

X16618-091718

Figure 2-1: ZCU102 Evaluation Board Components

Table 2-1: ZCU102 Board Components

| Callout | Ref. Des. | Feature/Component | Notes | Schematic 0381701 Page Number |
|---------|---------------|---|--|-------------------------------------|
| 1 | U1 | Zynq UltraScale XCZU9EG MPSoC with fan sink on soldered FPGA | XCZU9EG-2FFVB1156E Radian FA35+K52B+T710 | |
| 2 | J1 | PS-Side: DDR4 SODIMM Socket with DDR4 SODIMM | LOTES ADDR0067-P001A Micron MTA4ATF51264HZ-2G6E1 | 23 |
| 3 | U2 | PL-Side: DDR4 Component Memory, (4 Gb) | Micron MT40A256M16GE-075E:B | 25 |
| 4 | U119, U120 | Quad-SPI Flash Memory (MIO 0–12) (1 Gb total) | Micron MT25QU512ABB8ESF-OSIT | 46 |
| 5 | U116, J96 | USB 3.0 Transceiver and USB 2.0 ULPI PHY (USB micro-AB connector) | SMCS USB3320-EZK, KYON KMMX-AB10-SMT1SB30TR | 51 |
| 6 | J100 | SD Card Interface (connector) | Hirose DMIAA-SF-PET(21) | 47 |
| 7 | U21/J2 | Programmable Logic JTAG Programming Options (module with separate USB Micro-B conn.) | Digilent JTAG_2_NC, Hirose ZX62D-AB-5P8 | 22 |
| 8 | U42 | Programmable User Clock (300 MHz default, 3.3V LVDS) | Silicon Labs SI570BAB001614DG | 40 |
| 9 | U56 | Programmable User MGT Clock (156.250 MHz default, 3.3V LVDS) | Silicon Labs SI SI570BAB001544DG | 40 |
| 10 | U69 | SI5341B 10 Independent Output Any-Frequency Clock Generator (PS Reference Clock) (I2C programmable any frequency clock generator) | Silicon Labs SI5341B-B05071-GM | 39 |
| 11 | U20 | SFP/SFP+ Clock Recovery (jitter attenuated clock) | Silicon Labs SI5328B-C-GMR | 41 |
| 12 | U98/P12 | Ethernet PHY LED Interface Ethernet PHY U98 with P12 RJ45 with magnetics | TI DP83867IRPAP, Wurth 7499111221A | 52 |
| 13 | U40/J83 | CP2108 USB UART Interface (bridge IC/USB Micro-B connector) | Silicon Labs CP2108-B02-GM, Hirose ZX62D-AB-5P8 | 42 |
| 14 | U94/P7 | HDMI Video Output (controller/connector) | TI SN65DP159RGZ, TEC Connectivity 1888811-1 | 35 |
| 15 | U60, U61, U97 | I2C0 (MIO 14–15) bus switch and expanders) | TI PCA9544ARGYR, 2 ea. TI TCA6416APWR | 57 |
| 16 | U34, U135 | I2C1 (MIO 16–17) bus switches | TI TCA9548APWR, 2ea. | 58 |
| 17 | J54 | SFP/SFP+ Connector (quad) | Allbest R-OP-008080-6-F-N-26-F63 | 34 |
| 18 | U41 | TI MSP430 System Controller | TI MSP430F5342 | 38 |
| 19 | J55/J87 | User PMOD GPIO Headers (PMOD0-RA receptacle/PMOD1-vert. male pin hdr.) | SULLINS PPP0062LJBN-RC, SULLINS PBC36DAAN | 55 |

Table 2-1: ZCU102 Board Components (Cont'd)

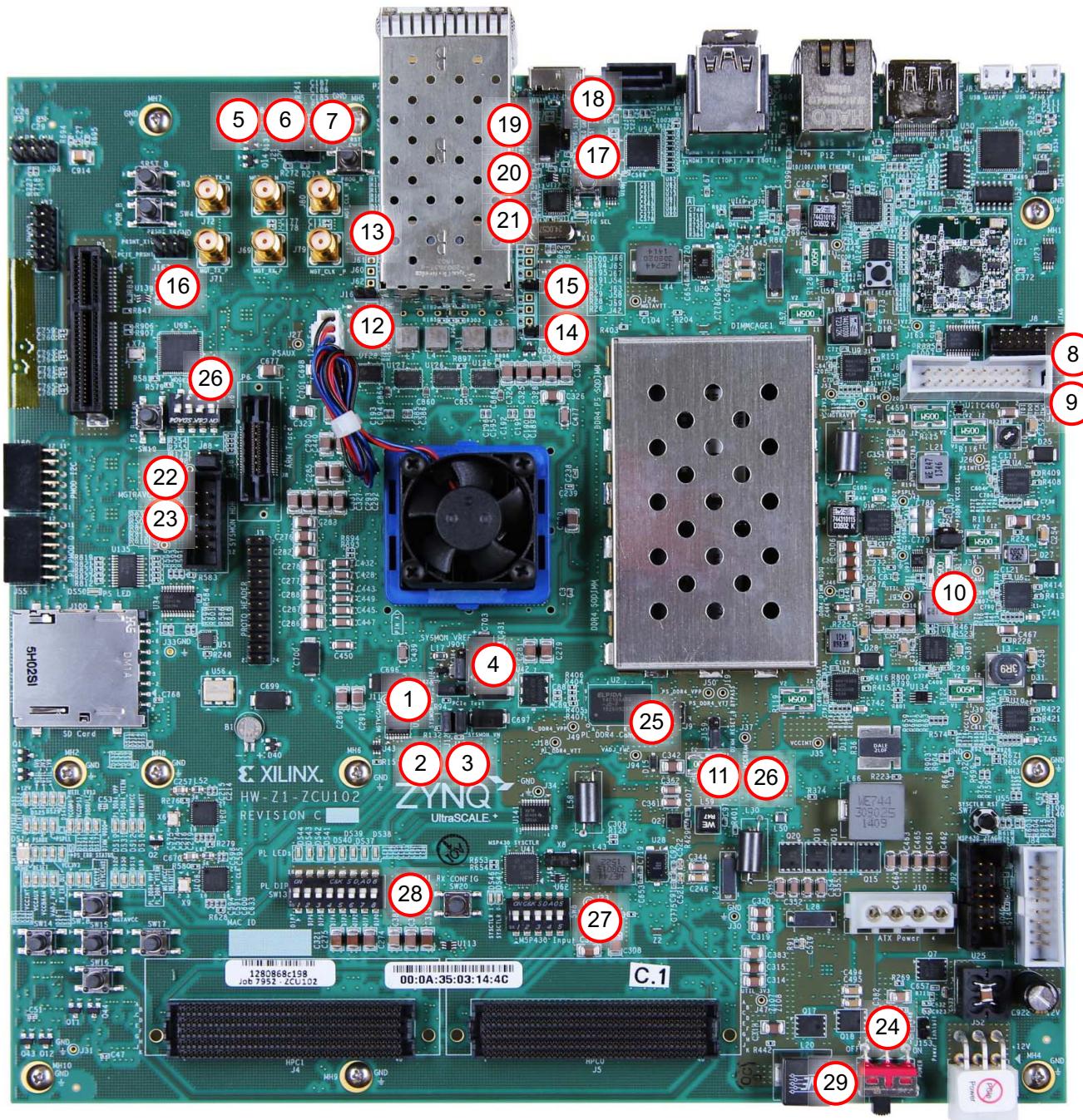
| Callout | Ref. Des. | Feature/Component | Notes | Schematic 0381701 Page Number |
|---------|-----------|---|--|-------------------------------------|
| 20 | J160 | For more information about PMOD connector compatible PMOD modules, see [Ref 30]. (PMOD I2C RA receptacle) | SULLINS PPP0062LJBN-RC | 49 |
| 21 | DS37-DS44 | User I/O (8 LEDs) | GPIO LEDs, GREEN 0603 | 53 |
| 22 | SW13 | User I/O (8-pole DIP switch) | C&K SDA08H1SBD | 53 |
| 23 | SW14-SW18 | User I/O (pushbutton switches, active-High) | E-Switch TL3301EP100QG placed in N, S, W, E, C pattern | 53 |
| 24 | SW20 | User I/O (CPU_RESET pushbutton switch, active-High) | E-Switch TL3301EP100QG | 53 |
| 25 | SW8 | DIP Switch, 5-pole, GPIO (TI MSP430 System Controller) | 5 pole C&K SDA05H1SBD | 38 |
| 26 | SW3, SW4 | Switches (SRST_RESET, POR_B pushbutton switches, active-Low) | E-Switch TL3301EP100QG | 12 |
| 27 | U122, J98 | CAN1 (MIO 24-25) (bus transceiver/2x4 male header) | TI SN65HVD232, SULLINS PBC36DAAN | 50 |
| 28 | SW1 | Power On/Off Slide Switch (Power On/Off slide switch) | C&K 1201M2S3AQE2 | 59 |
| 29 | J52 | Power connector (Power On/Off Slide Switch) | MOLEX 39-30-1060 | 59 |
| 30 | SW5 | Program_B Pushbutton (FPGA program) | E-Switch TL3301EP100QG | 12 |
| 31 | J5 | FMC HPC0 Connector J5 | Samtec ASP_134486_01 | 26-29 |
| 32 | J4 | FMC HPC1 Connector J4 | Samtec ASP_134486_01 | 30-33 |
| 33 | J10 | Switched output power connector | TEC Connectivity 794285-1 | 59 |
| 34 | - | Power management system (top and bottom) | Maxim Regulators | 59-86 |
| 35 | P1 | PCI Express Root Port Slot (PCIe 4-lane connector) | FCI 10061913-101CLF | 43 |
| 36 | P11 | DPAUX (MIO 27-30) (DisplayPort) | MOLEX 0472720001 | 44 |
| 37 | J84 | PMBus connector (Monitoring Voltage and Current) | ASSMANN AWHW16G-0202-T-R | 57 |
| 38 | J92 | JTAG connector (TI MSP430 System Controller) | TYCO 5103308-2 | 38 |
| 39 | J6 | Arm JTAG connector (Programmable Logic JTAG Programming Options) | ASSMANN AWHW20G-0202-T-R | 22 |
| 40 | U108 | HDMI Clock Recovery (High-Definition Multimedia Interface (HDMI™) jitter-attenuated clock) | Silicon Labs SI 5324C-C-GMR | 37 |
| 41 | J3 | For more information about PMOD connector compatible PMOD modules, see [Ref 30]. MPSOC U1 Bank 50 GPIO 2x12 male pin proto header | SULLINS PBC36DAAN | 56 |

Table 2-1: ZCU102 Board Components (Cont'd)

| Callout | Ref. Des. | Feature/Component | Notes | Schematic 0381701 Page Number |
|---------|--------------------|--|-----------------------------|-------------------------------------|
| 42 | J70-J72 J79-J80 | SMA (MGTH interface SMA connectors) | ROSENBERGER 32K10K-400L5 | 40 |
| 43 | P6 | EMIO Arm Trace Port (Arm Trace receptacle) | MICTOR 2-5767004-2 | 54 |
| 44 | SW6 | Switches (mode 4-pole DIP switch) | 4-pole C&K SDA04H1SBD | 12 |
| 45 | (Misc. DSnn) | Power and Status LEDs (Misc. LEDs) | Miscellaneous LEDs | 86 |

Default Switch and Jumper Settings

Figure 2-2 shows the board jumper header and DIP switch locations. Each numbered component shown in the figure is keyed to Table 2-2 (for default switch settings) or Table 2-3 (for default jumper settings). Both tables reference the respective schematic page numbers.



X16617-091718

Figure 2-2: DIP Switch and Board Header Jumper Locations

Switches

Table 2-2: Default Switch Settings

| DIP Switch | Function | Default | Figure 2-2 Callout | Schematic Page |
|------------|--|---------------------------------|--------------------|----------------|
| SW1 | Main Power Switch | OFF | 29 | 59 |
| SW6 | Switch PS_MODE select <ul style="list-style-type: none"> • ON = pull down = 0 • OFF = pull up = 1 • MODE[3:0] = 0010 (selects QSPI32) 4: PS_MODE3 3: PS_MODE2 2: PS_MODE1 1: PS_MODE0 | ON ON OFF ON | 26 | 12 |
| SW8 | MSP430 GPIO 5-POLE <ul style="list-style-type: none"> • ON = GND • OFF = Open 1: SW0 2: SW1 3: SW2 4: SW3 5: SW4 | OFF OFF OFF OFF OFF | 27 | 38 |
| SW13 | GPIO 8-POLE <ul style="list-style-type: none"> • OFF = pull down • ON = pull up | All OFF | 28 | 53 |

Jumpers

Table 2-3: Default Jumper Settings

| Jumper | Function | Default | Figure 2-2 Callout | Schematic Page |
|--------|--|---------|--------------------|----------------|
| J85 | POR_OVERRIDE <ul style="list-style-type: none"> • 1-2: Enable • 2-3: Disable | 2-3 | 1 | 3 |
| J12 | SYSMON I2C Address <ul style="list-style-type: none"> • Open: SYSMON_VP_R floating • 1-2: SYSMON_VP_P pulled down | 1-2 | 2 | 3 |
| J13 | SYSMON I2C Address <ul style="list-style-type: none"> • Open: SYSMON_VN_R floating • 1-2: SYSMON_VP_N pulled down | 1-2 | 3 | 3 |

Table 2-3: Default Jumper Settings (Cont'd)

| Jumper | Function | Default | Figure 2-2 Callout | Schematic Page |
|--------|--|---------|--------------------|----------------|
| J90 | SYSMON VREFP • 1-2: 1.25V VREFP connected to FPGA • 2-3: VREFP connected to GND | 1-2 | 4 | 3 |
| J20 | Reset Sequencer PS_POR_B • OFF: No sequencer control of PS_POR_B • 1-2: Sequencer can control PS_POR_B | 1-2 | 5 | 12 |
| J21 | Reset Sequencer PS_SRST_B • OFF: No sequence control of PS_SRST_B • 1-2: Sequencer can control PS_SRST_B | 1-2 | 6 | 12 |
| J22 | Reset Sequencer inhibit • OFF: Sequencer normal operation • 1-2: Sequencer inhibit (resets will stay asserted) | OFF | 7 | 12 |
| J14 | Arm Debug VTREF • Open: VTREF floating • 1-2: VTREF = VCCOPS3 (1.8V) | 1-2 | 8 | 22 |
| J15 | Arm Debug VSUPPLY • OFF: VSUPPLY floating • 1-2: VSUPPLY = VCCOPS3 (1.8V) | OFF | 9 | 22 |
| J56 | VCCO_PSDDR_504 select • 1-2: Switched DDR4 VDDQ • 3-4: Direct DDR4 VDDQ | 1-2 | 10 | 24 |
| J159 | DDR4 Reset Suspend Enable • 1-2: Suspend disabled (Gate bypass) • 2-3: Suspend enabled | 1-2 | 11 | 24 |
| J16 | SFP0 TX: ON = SFP TX Enabled; OFF = SFP TX Disabled, allows FPGA Control | OFF | 12 | 34 |
| J17 | SFP1 TX: ON = SFP TX Enabled; OFF = SFP TX Disabled, allows FPGA Control | OFF | 12 | 34 |
| J42 | SFP2 TX: ON = SFP TX Enabled; OFF = SFP TX Disabled, allows FPGA Control | OFF | 14 | 34 |
| J54 | SFP3 TX: ON = SFP TX Enabled; OFF = SFP TX Disabled, allows FPGA Control | OFF | 15 | 34 |
| J162 | PCIe PRSNT select • 1-2: x1 • 3-4: x4 • 5-6: GND (not used) | 5-6 | 16 | 43 |

Table 2-3: Default Jumper Settings (*Cont'd*)

| Jumper | Function | Default | Figure 2-2 Callout | Schematic Page |
|--------|---|---------|--------------------|----------------|
| J110 | USB ULPI CVBUS Select • 1-2: DEVICE or OTG Mode • 2-3: Host Mode | 1-2 | 17 | 51 |
| J109 | USB ULPI ID select • 1-2: Connector ID • 2-3: VDD33 ID | 2-3 | 18 | 51 |
| J112 | USB ULPI Shield GND select • 1-2: Capacitor • 2-3: GND | 1-2 | 19 | 51 |
| J7 | USB ULPI Device or Host select • 1-2: HOST/OTG • Open: Device | OPEN | 20 | 51 |
| J113 | USB ULPI Device/Host or OTG select • 1-2: Device or Host • 2-3: OTG | 1-2 | 21 | 51 |
| J88 | Arm Trace VTREF • 1-2: 3.3V • Open: 0V | 1-2 | 22 | 54 |
| J38 | Arm Trace power • 1-2: 3.3V • Open: 0V | 1-2 | 23 | 54 |
| J153 | Power inhibit • OFF: rails power on normally • 1-2: all rails (except UTIL) OFF | OFF | 24 | 59 |
| J9 | PS_DDR4_VPP_2V5 power inhibit (U39) • OFF: rail powers on normally • 1-2: PS_DDR4_VPP_2V5 OFF | OFF | 25 | 77 |
| J164 | MSP430 firmware upgrade header | OFF | 26 | 38 |

MPSOC Device Configuration

Zynq UltraScale+ XCZU9EG MPSOC devices use a multi-stage boot process documented in the Boot and Configuration chapter of the *Zynq UltraScale+ MPSOC Technical Reference Manual* (UG1085) [Ref 3].

Switch SW6 configuration option settings are identified in [Table 2-4](#).

Table 2-4: Switch SW6 Configuration Option Settings

| Boot Mode | Mode Pins [3:0] | Mode SW6 [4:1] |
|-----------|---------------------|-------------------|
| JTAG | 0000 | on, on, on, on |
| QSPI32 | 0010 ⁽¹⁾ | on, on, off, on |
| SD | 1110 | off, off, off, on |

Notes:

1. Default switch setting.
2. For this DIP switch, in relation to the arrow, moving the switch toward the label ON is a 0. DIP switch labels 1 through 4 are equivalent to Mode pins 0 through 3.

JTAG

Vivado, SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ MPSOC through one of the three provided JTAG interfaces:

1. Xilinx platform USB or cable PC4 connector (J8)
2. Arm 20-pin JTAG connector (J6)
3. Digilent SMT2.5 USB-to-JTAG module with off-module micro-USB connector (J2)

Quad-SPI

Booting from the dual Quad-SPI nonvolatile configuration memory is accomplished by storing a valid Zynq UltraScale+ MPSOC boot image into the Quad-SPI flash devices connected to the MIO Quad-SPI interface, setting the boot mode pins SW6 [4:1] = QSPI32 (see [Table 2-4](#)), then either power-cycling or pressing the power-on reset (POR) pushbutton. SW6 is callout 23 in [Figure 2-1](#).

SD

Booting from an SD card is accomplished by storing a valid Zynq UltraScale+ MPSOC boot image file onto an SD card (plugged into SD socket J100) connected to the MIO SD interface, setting the boot mode pins SW6 [4:1] = SD (see [Table 2-4](#)), then either power-cycling or pressing the power-on reset (POR) pushbutton.

See the *Zynq UltraScale+ MPSOC Technical Reference Manual* (UG1085) [Ref 3] for more information about Zynq UltraScale+ MPSOC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. [Table 2-1](#) identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in [Figure 2-1](#).

Component Descriptions

Zynq UltraScale XCZU9EG MPSoC

[[Figure 2-1](#), callout 1]

The ZCU102 board is populated with the Zynq UltraScale+ XCZU9EG-2FFVB1156E MPSoC which combines a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system in a Zynq UltraScale+ MPSoC features the Arm® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor.

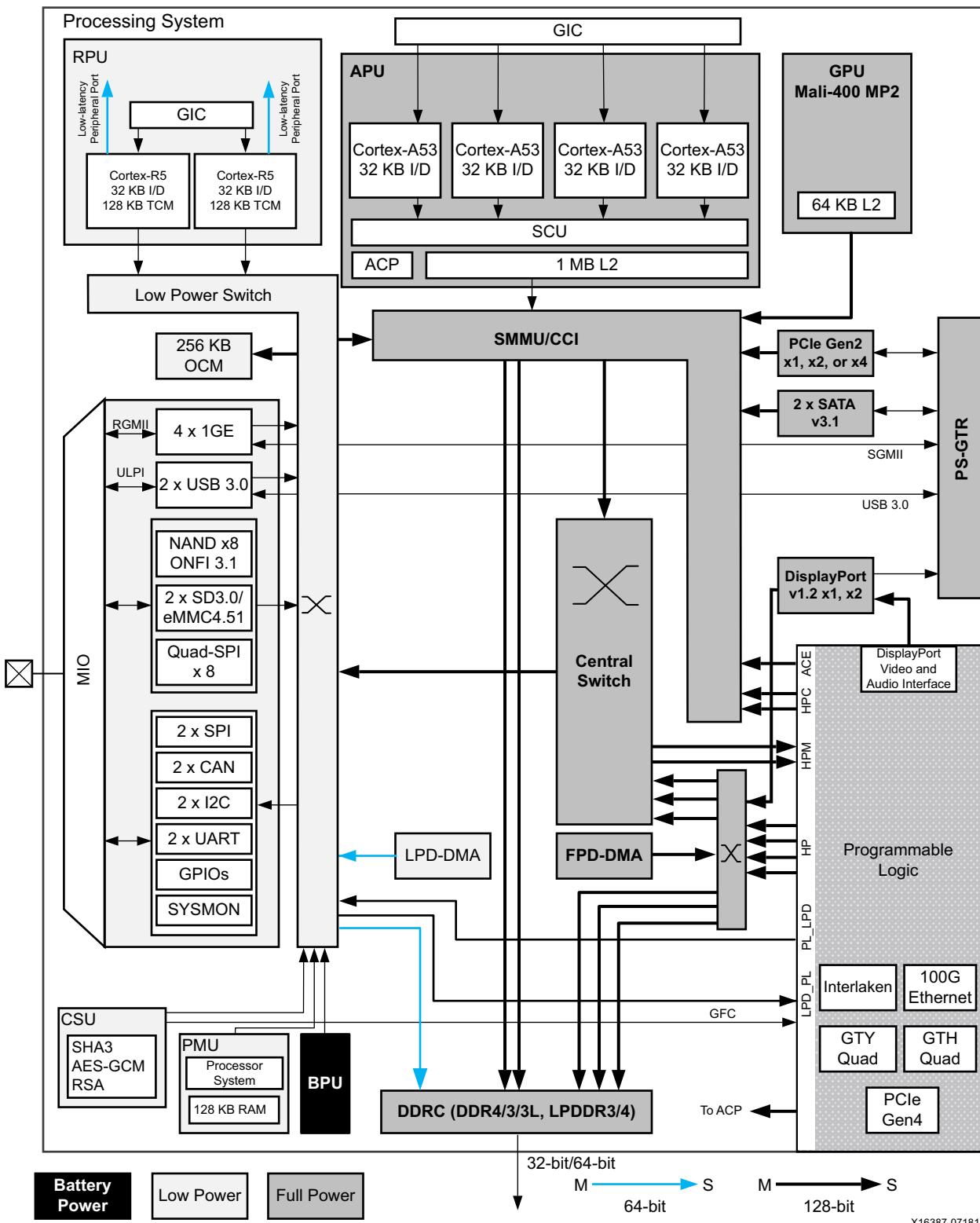
Production ZCU102 Evaluation boards will ship with -2 speed grade devices. Support of multiple speed grades requires voltage adjustments.

The PL-side V_{CCINT} supply will be user adjustable via PMBUS with the voltage ranges shown in [Table 3-1](#) to support multiple Zynq UltraScale+ MPSoC speed grades.

Table 3-1: Recommended Operating Conditions

| Symbol | Description | Min. | Typ. | Max. | Units |
|--------------------------------|--|-------|-------|-------|-------|
| Programmable Logic (PL) | | | | | |
| V_{CCINT} | PL internal supply voltage. | 0.825 | 0.850 | 0.876 | V |
| | For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PL internal supply voltage. | 0.698 | 0.720 | 0.742 | V |
| | For -3E devices: PL internal supply voltage. | 0.873 | 0.900 | 0.927 | V |

The top-level block diagram is shown in [Figure 3-1](#).



[Figure 3-1: Zynq UltraScale+ MPSoC Top-Level Block Diagram](#)

The Zynq UltraScale+ MPSoC PS block has three major processing units:

- Cortex-A53 application processing unit (APU)-Arm v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5 real-time processing unit (RPU)-Arm v7 architecture-based 32-bit dual real-time processing unit with dedicated tightly coupled memory (TCM).
- Mali-400 graphics processing unit (GPU)-graphics processing unit with pixel and geometry processor and 64 KB L2 cache.

The Zynq UltraScale+ MPSoC PS has four high-speed serial I/O (HSSIO) interfaces supporting the following protocols:

- Integrated block for PCI Express® interface-PCIe™ base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- DisplayPort interface-implements a DisplayPort source-only interface with video resolution up to 4K x 2K-30 (300 MHz pixel rate).
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the processing system. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ MPSoCs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO).and boots at power-up or reset.

For additional information on Zynq UltraScale+ MPSoC devices, see the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [\[Ref 1\]](#), and the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [\[Ref 3\]](#) for more information about Zynq UltraScale+ MPSoC configuration options.

Encryption Key Backup Circuit

The XCZU9EG MPSoC U1 implements bitstream encryption key technology. The ZCU102 board provides the encryption key backup battery circuit shown in [Figure 3-2](#).

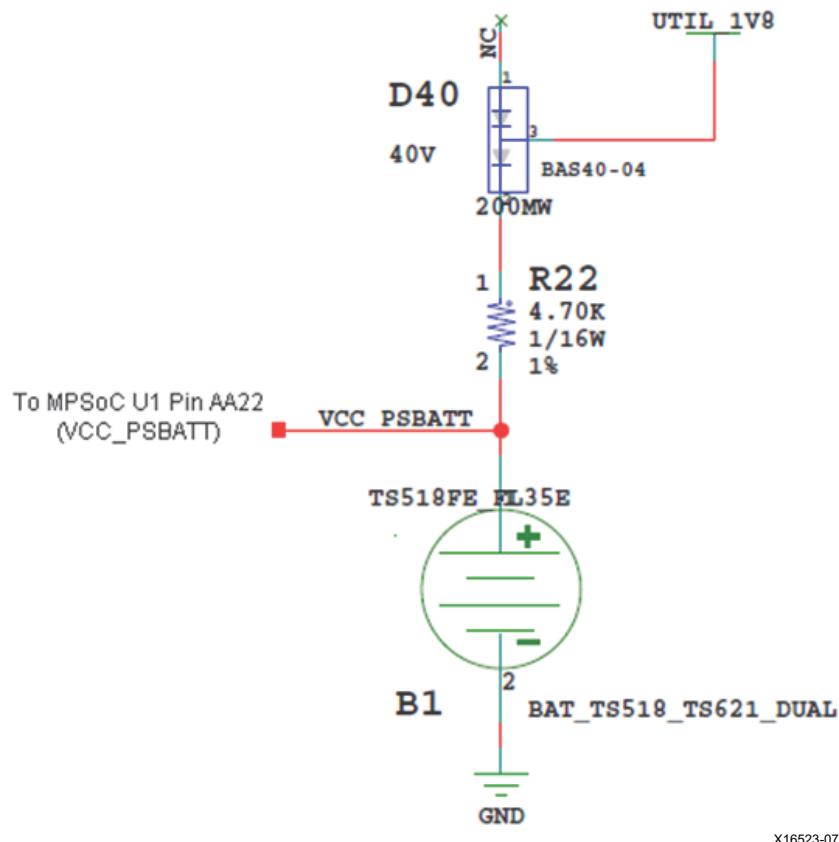


Figure 3-2: Encryption Key Backup Circuit

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCZU9EG MPSoC U1 V_{CC_PSBATT} pin AA22. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the UTIL_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 kΩ current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

There are nine PL I/O banks available on the XCZU9EG MPSoC. The voltages applied to the XCZU9EG MPSoC I/O banks used by the ZCU102 board are listed in [Table 3-2](#).

Table 3-2: I/O Voltage Rails

| XCZU9EG | Power Net Name | Voltage | Connected To |
|-----------------|-------------------------------------|---------|--|
| PL Bank 0 | NA | NA | MPSoC Configuration Bank 0 |
| PL Bank 44 | V _{CC3V3} | 3.3V | GPIO DIP SW, PB SW, LEDs, 74.25 MHz CLK |
| PL Bank 47 | V _{CC3V3} | 3.3V | GPIO PMOD0 (RT-ANG. FEMALE), PMOD1 (STR. MALE), PL I2C1, TRACEDATA, 125 MHz CLK |
| PL Bank 48 | V _{CC3V3} | 3.3V | TRACEDATA |
| PL Bank 49 | V _{CC3V3} | 3.3V | High-Definition Multimedia Interface (HDMI™) Codec, SYSMON I2C, SFP CTRL, UART2, MSP430 UCA1 |
| PL Bank 50 | V _{CC3V3} | 3.3V | HDMI Codec, MSP430 GPIO, PL I2C0, PROTO. HDR. IO |
| PL Bank 64 | V _{CC1V2} | 1.2V | DDR4 DQ[0:15], DDR4 ADDR/CTRL, USER_SI570 CLK |
| PL Bank 65 | V _{ADJ_FMC} ⁽¹⁾ | 1.8V | FMC_HPC1 LA BUS, HDMI TX |
| PL Bank 66 | V _{ADJ_FMC} ⁽¹⁾ | 1.8V | FMC_HPC0 LA BUS, HDMI REC CLK |
| PL Bank 67 | V _{ADJ_FMC} ⁽¹⁾ | 1.8V | FMC_HPC0 LA BUS, SFP REC CLK |
| PS Bank 500 | V _{CCOPS} | 1.8V | QSPI LWR, QSPI UPR, UART1, MIO_I2C0, MIO_I2C1, MIO_RXD/TXD, CAN IF |
| PS Bank 501 | V _{CCOPS} | 1.8V | MIO_SD IF, MIO_PMU IF, MIO_DP IF |
| PS Bank 502 | V _{CCOPS} | 1.8V | MIO_ENET, MIO_USB |
| PS Bank 503 | V _{CCOPS3} | 1.81V | PS CONFIGURATION IF |
| PS DDR Bank 504 | V _{CCO_PSDDR_504} | 1.2V | DDR4 SODIMM IF |

Notes:

1. The ZCU102 board is shipped with V_{ADJ_FMC} set to 1.8V by the MSP430 system controller.

PS-Side: DDR4 SODIMM Socket

[Figure 2-1, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ DDRC hard memory controller. The PS-side memory interface supports a 260-pin DDR4 SODIMM socket J1. The ZCU102 is shipped with a DDR4 SODIMM installed:

- Manufacturer: Micron
- Part Number: MTA4ATF51264HZ-2G6E1
- Description:
 - 4 GB DDR4 SODIMM, 260-pin
 - Single Rank x16
 - 512 Mbit x 64-bit
 - Supports up to DDR4-2666

The ZCU102 XCZU9EG FFVB MPSoC PS DDR interface performance is documented in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 2].

The ZCU102 supports full power-off suspend mode where only the system controller and the PS-side DDR4 SODIMM memory are powered. The DDR4 memory is kept in a self-refresh state and has its reset input controlled by the system controller such that the memory is not reset when waking-up from suspend mode. DDR4 SODIMM standard right angle Socket J1 connections are identified in Table 3-3.

Table 3-3: DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504

| XCZU9EG (U1) Pin | Net Name | DDR4 SODIMM Memory J1 | |
|---------------------|-----------------|-----------------------|----------|
| | | Pin Number | Pin Name |
| AP29 | DDR4_SODIMM_A0 | 144 | A0 |
| AP30 | DDR4_SODIMM_A1 | 133 | A1 |
| AP26 | DDR4_SODIMM_A2 | 132 | A2 |
| AP27 | DDR4_SODIMM_A3 | 131 | A3 |
| AP25 | DDR4_SODIMM_A4 | 128 | A4 |
| AN24 | DDR4_SODIMM_A5 | 126 | A5 |
| AM29 | DDR4_SODIMM_A6 | 127 | A6 |
| AM28 | DDR4_SODIMM_A7 | 122 | A7 |
| AM26 | DDR4_SODIMM_A8 | 125 | A8 |
| AM25 | DDR4_SODIMM_A9 | 121 | A9 |
| AL28 | DDR4_SODIMM_A10 | 146 | A10/AP |
| AK27 | DDR4_SODIMM_A11 | 120 | A11 |

Table 3-3: DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 (Cont'd)

| XCZU9EG (U1) Pin | Net Name | DDR4 SODIMM Memory J1 | |
|---------------------|------------------|-----------------------|----------|
| | | Pin Number | Pin Name |
| AJ25 | DDR4_SODIMM_A12 | 119 | A12 |
| AL25 | DDR4_SODIMM_A13 | 158 | A13 |
| AH26 | DDR4_SODIMM_BA0 | 150 | BA0 |
| AG26 | DDR4_SODIMM_BA1 | 145 | BA1 |
| AK28 | DDR4_SODIMM_BG0 | 115 | BG0 |
| AH27 | DDR4_SODIMM_BG1 | 113 | BG1 |
| AP20 | DDR4_SODIMM_DQ0 | 8 | DQ0 |
| AP18 | DDR4_SODIMM_DQ1 | 7 | DQ1 |
| AP19 | DDR4_SODIMM_DQ2 | 20 | DQ2 |
| AP17 | DDR4_SODIMM_DQ3 | 21 | DQ3 |
| AM20 | DDR4_SODIMM_DQ4 | 4 | DQ4 |
| AM19 | DDR4_SODIMM_DQ5 | 3 | DQ5 |
| AM18 | DDR4_SODIMM_DQ6 | 16 | DQ6 |
| AL18 | DDR4_SODIMM_DQ7 | 17 | DQ7 |
| AP22 | DDR4_SODIMM_DQ8 | 28 | DQ8 |
| AP21 | DDR4_SODIMM_DQ9 | 29 | DQ9 |
| AP24 | DDR4_SODIMM_DQ10 | 41 | DQ10 |
| AN23 | DDR4_SODIMM_DQ11 | 42 | DQ11 |
| AL21 | DDR4_SODIMM_DQ12 | 24 | DQ12 |
| AL22 | DDR4_SODIMM_DQ13 | 25 | DQ13 |
| AM23 | DDR4_SODIMM_DQ14 | 38 | DQ14 |
| AL23 | DDR4_SODIMM_DQ15 | 37 | DQ15 |
| AL20 | DDR4_SODIMM_DQ16 | 50 | DQ16 |
| AK20 | DDR4_SODIMM_DQ17 | 49 | DQ17 |
| AJ20 | DDR4_SODIMM_DQ18 | 62 | DQ18 |
| AK18 | DDR4_SODIMM_DQ19 | 63 | DQ19 |
| AG20 | DDR4_SODIMM_DQ20 | 46 | DQ20 |
| AH18 | DDR4_SODIMM_DQ21 | 45 | DQ21 |
| AG19 | DDR4_SODIMM_DQ22 | 58 | DQ22 |
| AG18 | DDR4_SODIMM_DQ23 | 59 | DQ23 |
| AG21 | DDR4_SODIMM_DQ24 | 70 | DQ24 |
| AH21 | DDR4_SODIMM_DQ25 | 71 | DQ25 |
| AG24 | DDR4_SODIMM_DQ26 | 83 | DQ26 |
| AG23 | DDR4_SODIMM_DQ27 | 84 | DQ27 |

Table 3-3: DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 (Cont'd)

| XCZU9EG (U1) Pin | Net Name | DDR4 SODIMM Memory J1 | |
|---------------------|------------------|-----------------------|----------|
| | | Pin Number | Pin Name |
| AK22 | DDR4_SODIMM_DQ28 | 66 | DQ28 |
| AJ21 | DDR4_SODIMM_DQ29 | 67 | DQ29 |
| AJ22 | DDR4_SODIMM_DQ30 | 79 | DQ30 |
| AK23 | DDR4_SODIMM_DQ31 | 80 | DQ31 |
| AG31 | DDR4_SODIMM_DQ32 | 174 | DQ32 |
| AG30 | DDR4_SODIMM_DQ33 | 173 | DQ33 |
| AG29 | DDR4_SODIMM_DQ34 | 187 | DQ34 |
| AG28 | DDR4_SODIMM_DQ35 | 186 | DQ35 |
| AJ30 | DDR4_SODIMM_DQ36 | 170 | DQ36 |
| AK29 | DDR4_SODIMM_DQ37 | 169 | DQ37 |
| AK30 | DDR4_SODIMM_DQ38 | 183 | DQ38 |
| AJ29 | DDR4_SODIMM_DQ39 | 182 | DQ39 |
| AE27 | DDR4_SODIMM_DQ40 | 195 | DQ40 |
| AF28 | DDR4_SODIMM_DQ41 | 194 | DQ41 |
| AF30 | DDR4_SODIMM_DQ42 | 207 | DQ42 |
| AF31 | DDR4_SODIMM_DQ43 | 208 | DQ43 |
| AD28 | DDR4_SODIMM_DQ44 | 191 | DQ44 |
| AD27 | DDR4_SODIMM_DQ45 | 190 | DQ45 |
| AD29 | DDR4_SODIMM_DQ46 | 203 | DQ46 |
| AD30 | DDR4_SODIMM_DQ47 | 204 | DQ47 |
| AH33 | DDR4_SODIMM_DQ48 | 216 | DQ48 |
| AJ34 | DDR4_SODIMM_DQ49 | 215 | DQ49 |
| AH34 | DDR4_SODIMM_DQ50 | 228 | DQ50 |
| AH32 | DDR4_SODIMM_DQ51 | 229 | DQ51 |
| AK34 | DDR4_SODIMM_DQ52 | 211 | DQ52 |
| AK33 | DDR4_SODIMM_DQ53 | 212 | DQ53 |
| AL32 | DDR4_SODIMM_DQ54 | 224 | DQ54 |
| AL31 | DDR4_SODIMM_DQ55 | 225 | DQ55 |
| AG33 | DDR4_SODIMM_DQ56 | 237 | DQ56 |
| AG34 | DDR4_SODIMM_DQ57 | 236 | DQ57 |
| AF32 | DDR4_SODIMM_DQ58 | 249 | DQ58 |
| AF33 | DDR4_SODIMM_DQ59 | 250 | DQ59 |
| AD31 | DDR4_SODIMM_DQ60 | 232 | DQ60 |
| AD32 | DDR4_SODIMM_DQ61 | 233 | DQ61 |

Table 3-3: DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 (Cont'd)

| XCZU9EG (U1) Pin | Net Name | DDR4 SODIMM Memory J1 | |
|---------------------|--------------------|-----------------------|-----------------|
| | | Pin Number | Pin Name |
| AD34 | DDR4_SODIMM_DQ62 | 245 | DQ62 |
| AD33 | DDR4_SODIMM_DQ63 | 246 | DQ63 |
| AN31 | DDR4_SODIMM_CB0 | 92 | CB0/NC |
| AP31 | DDR4_SODIMM_CB1 | 91 | CB1/NC |
| AP32 | DDR4_SODIMM_CB2 | 101 | CB2/NC |
| AP33 | DDR4_SODIMM_CB3 | 105 | CB3/NC |
| AM31 | DDR4_SODIMM_CB4 | 88 | CB4/NC |
| AM33 | DDR4_SODIMM_CB5 | 87 | CB5/NC |
| AM34 | DDR4_SODIMM_CB6 | 100 | CB6/NC |
| AL33 | DDR4_SODIMM_CB7 | 104 | CB7/NC |
| AN17 | DDR4_SODIMM_DM0_B | 12 | DM0_N/DBI0_N |
| AM21 | DDR4_SODIMM_DM1_B | 33 | DM1_N/DBI1_N |
| AK19 | DDR4_SODIMM_DM2_B | 54 | DM2_N/DBI2_N |
| AH24 | DDR4_SODIMM_DM3_B | 75 | DM3_N/DBI3_N |
| AH31 | DDR4_SODIMM_DM4_B | 178 | DM4_N/DBI4_N |
| AE30 | DDR4_SODIMM_DM5_B | 199 | DM5_N/DBI5_N |
| AJ31 | DDR4_SODIMM_DM6_B | 220 | DM6_N/DBI6_N |
| AE34 | DDR4_SODIMM_DM7_B | 241 | DM7_N/DBI7_N |
| AN34 | DDR4_SODIMM_DM8_B | 96 | DM8_N/DBI8_N/NC |
| AN18 | DDR4_SODIMM_DQS0_T | 13 | DQS0_T |
| AN19 | DDR4_SODIMM_DQS0_C | 11 | DQS0_C |
| AN21 | DDR4_SODIMM_DQS1_T | 34 | DQS1_T |
| AN22 | DDR4_SODIMM_DQS1_C | 32 | DQS1_C |
| AH19 | DDR4_SODIMM_DQS2_T | 55 | DQS2_T |
| AJ19 | DDR4_SODIMM_DQS2_C | 53 | DQS2_C |
| AH22 | DDR4_SODIMM_DQS3_T | 76 | DQS3_T |
| AH23 | DDR4_SODIMM_DQS3_C | 74 | DQS3_C |
| AH28 | DDR4_SODIMM_DQS4_T | 179 | DQS4_T |
| AH29 | DDR4_SODIMM_DQS4_C | 177 | DQS4_C |
| AE28 | DDR4_SODIMM_DQS5_T | 200 | DQS5_T |
| AE29 | DDR4_SODIMM_DQS5_C | 198 | DQS5_C |
| AJ32 | DDR4_SODIMM_DQS6_T | 221 | DQS6_T |
| AK32 | DDR4_SODIMM_DQS6_C | 219 | DQS6_C |
| AE32 | DDR4_SODIMM_DQS7_T | 242 | DQS7_T |

Table 3-3: DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 (Cont'd)

| XCZU9EG (U1) Pin | Net Name | DDR4 SODIMM Memory J1 | |
|---------------------|---------------------|-----------------------|-----------|
| | | Pin Number | Pin Name |
| AE33 | DDR4_SODIMM_DQS7_C | 240 | DQS7_C |
| AN32 | DDR4_SODIMM_DQS8_T | 97 | DQS8_T |
| AN33 | DDR4_SODIMM_DQS8_C | 95 | DQS8_C |
| AN27 | DDR4_SODIMM_CK0_C | 139 | CK0_C |
| AN26 | DDR4_SODIMM_CK0_T | 137 | CK0_T |
| AL27 | DDR4_SODIMM_CK1_C | 140 | CK1_C/NF |
| AL26 | DDR4_SODIMM_CK1_T | 138 | CK1_T/NF |
| AN29 | DDR4_SODIMM_CKE0 | 109 | CKE0 |
| AJ27 | DDR4_SODIMM_CKE1 | 110 | CKE1 |
| AM30 | DDR4_SODIMM_ODT0 | 155 | ODT0 |
| AJ26 | DDR4_SODIMM_ODT1 | 161 | ODT1 |
| AM24 | DDR4_SODIMM_RAS_B | 152 | RAS_N/A16 |
| AK24 | DDR4_SODIMM_CAS_B | 156 | CAS_N/A15 |
| AK25 | DDR4_SODIMM_WE_B | 151 | WE_N/A14 |
| AG25 | DDR4_SODIMM_ACT_B | 114 | ACT_N |
| AF22 | DDR4_SODIMM_ALERT_B | 116 | ALERT_N |
| AF20 | DDR4_SODIMM_PARITY | 143 | PARITY |
| AN28 | DDR4_SODIMM_CS0_B | 149 | CS0_N |
| AL30 | DDR4_SODIMM_CS1_B | 157 | CS1_N |

The ZCU102 DDR4 SODIMM interface adheres to the constraints guidelines documented in the PCB Guidelines for DDR4 section of *UltraScale Architecture PCB Design Guide* (UG583) [Ref 5]. The ZCU102 DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Guide* (PG150) [Ref 6].

PL-Side: DDR4 Component Memory

[Figure 2-1, callout 3]

The 4 Gb, 16-bit wide DDR4 memory system is comprised of one 256 Mb x 16 SDRAM at U2.

- Manufacturer: Micron
- Part Number: MT40A256M16GE-075E

- Description:
 - 4 Gb (256 Mb x16)
 - 1.2V 96 ball TFBGA
 - DDR4-2666

The ZCU102 XCZU9EG FFVB MPSoC PL DDR interface performance is documented in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 2].

This memory system is connected to the XCZU9EG device bank 64. The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U35. The connections between the DDR4 component memory and XCZU9EG device bank 64 are listed in [Table 3-4](#).

Table 3-4: DDR4 Component Memory Connection to the XCZU9EG MPSoC

| XCZU9EG (U1) Pin | Net Name | I/O Standard | DDR4 Component Memory | |
|---------------------|----------------|--------------|-----------------------|-----------|
| | | | Pin Number | Pin Name |
| AM8 | DDR4_A0 | SSTL12_DCI | P3 | A0 |
| AM9 | DDR4_A1 | SSTL12_DCI | P7 | A1 |
| AP8 | DDR4_A2 | SSTL12_DCI | R3 | A2 |
| AN8 | DDR4_A3 | SSTL12_DCI | N7 | A3 |
| AK10 | DDR4_A4 | SSTL12_DCI | N3 | A4 |
| AJ10 | DDR4_A5 | SSTL12_DCI | P8 | A5 |
| AP9 | DDR4_A6 | SSTL12_DCI | P2 | A6 |
| AN9 | DDR4_A7 | SSTL12_DCI | R8 | A7 |
| AP10 | DDR4_A8 | SSTL12_DCI | R2 | A8 |
| AP11 | DDR4_A9 | SSTL12_DCI | R7 | A9 |
| AM10 | DDR4_A10 | SSTL12_DCI | M3 | A10/AP |
| AL10 | DDR4_A11 | SSTL12_DCI | T2 | A11 |
| AM11 | DDR4_A12 | SSTL12_DCI | M7 | A12/BC_B |
| AL11 | DDR4_A13 | SSTL12_DCI | T8 | A13 |
| AK12 | DDR4_BA0 | SSTL12_DCI | N2 | BA0 |
| AJ12 | DDR4_BA1 | SSTL12_DCI | N8 | BA1 |
| AK7 | DDR4_BG0 | SSTL12_DCI | M2 | BG0 |
| AJ7 | DDR4_A14_WE_B | SSTL12_DCI | L2 | WE_B/A14 |
| AJ9 | DDR4_A16_RAS_B | SSTL12_DCI | L8 | RAS_B/A16 |
| AL5 | DDR4_A15_CAS_B | SSTL12_DCI | M8 | CAS_B/A15 |
| AN7 | DDR4_CK_T | DIFF_SSTL12 | K7 | CK_T |
| AP7 | DDR4_CK_C | DIFF_SSTL12 | K8 | CK_C |

Table 3-4: DDR4 Component Memory Connection to the XCZU9EG MPSoC (Cont'd)

| XCZU9EG (U1) Pin | Net Name | I/O Standard | DDR4 Component Memory | |
|---------------------|-----------------|--------------|-----------------------|--------------|
| | | | Pin Number | Pin Name |
| AM3 | DDR4_CKE | SSTL12_DCI | K2 | CKE |
| AK8 | DDR4_ACT_B | SSTL12_DCI | L3 | ACT_B |
| AP1 | DDR4_PAR | SSTL12_DCI | T3 | PAR |
| AH9 | DDR4_RESET_B_LS | LVCMOS18 | P1 | RESET_B |
| AK9 | DDR4_ODT | SSTL12_DCI | K3 | ODT |
| AP2 | DDR4_CS_B | SSTL12_DCI | L7 | CS_B |
| AK4 | DDR4_DQ0 | POD12_DCI | G2 | DQL0 |
| AK5 | DDR4_DQ1 | POD12_DCI | F7 | DQL1 |
| AN4 | DDR4_DQ2 | POD12_DCI | H3 | DQL2 |
| AM4 | DDR4_DQ3 | POD12_DCI | H7 | DQL3 |
| AP4 | DDR4_DQ4 | POD12_DCI | H2 | DQL4 |
| AP5 | DDR4_DQ5 | POD12_DCI | H8 | DQL5 |
| AM5 | DDR4_DQ6 | POD12_DCI | J3 | DQL6 |
| AM6 | DDR4_DQ7 | POD12_DCI | J7 | DQL7 |
| AK2 | DDR4_DQ8 | POD12_DCI | A3 | DQU0 |
| AK3 | DDR4_DQ9 | POD12_DCI | B8 | DQU1 |
| AL1 | DDR4_DQ10 | POD12_DCI | C3 | DQU2 |
| AK1 | DDR4_DQ11 | POD12_DCI | C7 | DQU3 |
| AN1 | DDR4_DQ12 | POD12_DCI | C2 | DQU4 |
| AM1 | DDR4_DQ13 | POD12_DCI | C8 | DQU5 |
| AP3 | DDR4_DQ14 | POD12_DCI | D3 | DQU6 |
| AN3 | DDR4_DQ15 | POD12_DCI | D7 | DQU7 |
| AN6 | DDR4_DQS0_T | DIFF_POD12 | G3 | DQSL_T |
| AP6 | DDR4_DQS0_C | DIFF_POD12 | F3 | DQSL_C |
| AL3 | DDR4_DQS1_T | DIFF_POD12 | B7 | DQSU_T |
| AL2 | DDR4_DQS1_C | DIFF_POD12 | A7 | DQSU_C |
| AL6 | DDR4_DM0 | POD12_DCI | E7 | DML_B/DBIL_B |
| AN2 | DDR4_DM1 | POD12_DCI | E2 | DMU_B/DBIU_B |

Note: The ZCU102 board DDR4 16-bit component memory interface adheres to the constraints guidelines documented in the PCB Guidelines for DDR4 section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 5]. The ZCU102 DDR4 component interface is a 40Ω impedance implementations. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Product Guide* (PG150) [Ref 6]. For more details, see the Micron MT40A256M16GE-075E data sheet at the Micron website [Ref 20].

PSMIO

[Table 3-5](#) provides PS MIO peripheral mapping implemented on the ZCU102 board. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3] for more information on PS MIO peripheral mapping.

Table 3-5: ZCU102 MIO Connections

| MIO [25:0] Bank 500 | ZU7EV U1 Pin No. | Schematic Net Name | Type | MIO [51:26] Bank 501 | ZU7EV U1 Pin No. | Schematic Net Name | Type | MIO [77:52] Bank 502 | ZU7EV U1 Pin No. | Schematic Net Name | Type |
|------------------------|------------------------|--------------------|-------|-------------------------|------------------------|---------------------|--------|-------------------------|------------------------|--------------------|-------|
| MIO25 | AE19 | MIO25_CAN_RX | CAN1 | MIO51 | N25 | MIO51_SDIO_CLK_R | SD1 | MIO77 | F25 | MIO77_ENET_MDIO | MDIO3 |
| MIO24 | AE20 | MIO24_CAN_TX | CAN1 | MIO50 | P25 | MIO50_SDIO_CMD_R | SD1 | MIO76 | H25 | MIO76_ENET_MDC | MDIO3 |
| MIO23 | AD19 | MIO23_LED | GPIO | MIO49 | K25 | MIO49_SDIO_DAT3_R | SD1 | MIO75 | D25 | MIO75_ENET_RX_CTRL | GEM3 |
| MIO22 | AD20 | MIO22_BUTTON | GPIO | MIO48 | M25 | MIO48_SDIO_DAT2_R | SD1 | MIO74 | G25 | MIO74_ENET_RX_D3 | GEM3 |
| MIO21 | AF18 | MIO21_UART1_RXD | UART1 | MIO47 | L25 | MIO47_SDIO_DAT1_R | SD1 | MIO73 | H24 | MIO73_ENET_RX_D2 | GEM3 |
| MIO20 | AD18 | MIO20_UART1_TXD | UART1 | MIO46 | J25 | MIO46_SDIO_DAT0_R | SD1 | MIO72 | E25 | MIO72_ENET_RX_D1 | GEM3 |
| MIO19 | AL17 | MIO19_UART0_RXD | UART0 | MIO45 | P24 | MIO45_SDIO_DETECT | SD1 | MIO71 | C27 | MIO71_ENET_RX_D0 | GEM3 |
| MIO18 | AE18 | MIO18_UART0_RXD | UART0 | MIO44 | N24 | MIO44_SDIO_PROTECT | SD1 | MIO70 | C26 | MIO70_ENET_RX_CLK | GEM3 |
| MIO17 | AP16 | MIO17_I2C1_SDA | I2C1 | MIO43 | K24 | Not Connected | NC | MIO69 | B27 | MIO69_ENET_TX_CTRL | GEM3 |
| MIO16 | AM16 | MIO16_I2C1_SCL | I2C1 | MIO42 | M24 | MIO42_SDIO_DIR_DAT1 | SD1 | MIO68 | B26 | MIO68_ENET_TX_D3 | GEM3 |
| MIO15 | AN16 | MIO15_I2C0_SDA | I2C0 | MIO41 | J24 | MIO41_SDIO_DIR_DAT0 | SD1 | MIO67 | B25 | MIO67_ENET_TX_D2 | GEM3 |
| MIO14 | AL16 | MIO14_I2C0_SCL | I2C0 | MIO40 | M23 | MIO40_SDIO_DIR_CMD | SD1 | MIO66 | A27 | MIO66_ENET_TX_D1 | GEM3 |
| MIO13 | AK17 | MIO13_PS_GPIO2 | GPIO | MIO39 | N23 | MIO39_SDIO_SEL | SD1 | MIO65 | A26 | MIO65_ENET_TX_D0 | GEM3 |
| MIO12 | AJ17 | MIO12_QSPI_UPR_CLK | QSP1 | MIO38 | L23 | MIO38_PS_GPIO1 | GPIO | MIO64 | A25 | MIO64_ENET_TX_CLK | GEM3 |
| MIO11 | AF17 | MIO11_QSPI_UPR_DQ3 | QSP1 | MIO37 | N22 | MIO37_PMU_GPO5 | PM OUT | MIO63 | D24 | MIO63_USB_DATA7_R | USB0 |
| MIO10 | AH17 | MIO10_QSPI_UPR_DQ2 | QSP1 | MIO36 | K23 | MIO36_PMU_GPO4 | PM OUT | MIO62 | G24 | MIO62_USB_DATA6_R | USB0 |
| MIO9 | AP15 | MIO9_QSPI_UPR_DQ1 | QSP1 | MIO35 | P22 | MIO35_PMU_GPO3 | PM OUT | MIO61 | C24 | MIO61_USB_DATA5_R | USB0 |
| MIO8 | AE17 | MIO8_QSPI_UPR_DQ0 | QSP1 | MIO34 | L22 | MIO34_PMU_GPO2 | PM OUT | MIO60 | E24 | MIO60_USB_DATA4_R | USB0 |
| MIO7 | AD17 | MIO7_QSPI_UPR_CS_B | QSP1 | MIO33 | H23 | MIO33_PMU_GPO1 | PM OUT | MIO59 | B24 | MIO59_USB_DATA3_R | USB0 |
| MIO6 | AL15 | Not Connected | NC | MIO32 | H22 | MIO32_PMU_GPO0 | PM OUT | MIO58 | G23 | MIO58_USB_STP_R | USB0 |
| MIO5 | AM15 | MIO5_QSPI_LWR_CS_B | QSP1 | MIO31 | J22 | MIO31_PCIE_RESET_N | PCIE | MIO57 | A23 | MIO57_USB_DATA1_R | USB0 |
| MIO4 | AH16 | MIO4_QSPI_LWR_DQ0 | QSP1 | MIO30 | L21 | MIO30_DP_AUX_IN | DPAUX | MIO56 | C23 | MIO56_USB_DATA0_R | USB0 |
| MIO3 | AG16 | MIO3_QSPI_LWR_DQ3 | QSP1 | MIO29 | K22 | MIO29_DP_OE | DPAUX | MIO55 | B23 | MIO55_USB_NXT | USB0 |
| MIO2 | AD16 | MIO2_QSPI_LWR_DQ2 | QSP1 | MIO28 | N21 | MIO28_DP_HPD | DPAUX | MIO54 | F23 | MIO54_USB_DATA2_R | USB0 |
| MIO1 | AJ16 | MIO1_QSPI_LWR_DQ1 | QSP1 | MIO27 | M21 | MIO27_DP_AUX_OUT | DPAUX | MIO53 | E23 | MIO53_USB_DIR | USB0 |
| MIO0 | AF16 | MIO0_QSPI_LWR_CLK | QSP1 | MIO26 | P21 | MIO26_PMU_INPUT | PMU IN | MIO52 | F22 | MIO52_USB_CLK | USB0 |

Quad-SPI Flash Memory (MIO 0–12)

[[Figure 2-1](#), callout 4]

The Micron dual MT25QU512ABB8ESF serial NOR flash Quad-SPI memories are capable of holding the boot image for the MPSoC system. To achieve higher performance two Quad-SPI devices are connected in parallel and provide an 8-bit data bus for booting and

configuration. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3].

The dual Quad-SPI flash memory located at U119/U120 provides 1 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABB8ESF-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: Various depending on Single/Dual/Quad mode

The connections between the SPI flash memory and the XCZU9EG MPSoC are listed in [Table 3-6](#).

Table 3-6: Quad-SPI Component Connections to FPGA U1

| XCZU9EG (U1) Pin | Net Name | Quad-SPI U119 (LWR), U120 (UPR) | |
|---------------------|------------------------|---------------------------------|----------------|
| | | Pin Number | Pin Name |
| AH16 | MIO4_QSPI_LWR_DQ0 | 15 | DQ0 |
| AJ16 | MIO1_QSPI_LWR_DQ1 | 8 | DQ1 |
| AD16 | MIO2_QSPI_LWR_DQ2 | 9 | DQ2_WP_B |
| AG16 | MIO3_QSPI_LWR_DQ3 | 1 | DQ3_RST_HOLD_B |
| AF16 | MIO0_QSPI_LWR_CLK | 16 | C |
| AM15 | MIO5_QSPI_LWR_CS_B | 7 | S_B |
| <hr/> | | | |
| AE17 | MIO8_QSPI_UPR_DQ0 | 15 | DQ0 |
| AP15 | MIO9_QSPI_UPR_DQ1 | 8 | DQ1 |
| AH17 | MIO10_QSPI_UPR_DQ 2 | 9 | DQ2_WP_B |
| AF17 | MIO11_QSPI_UPR_DQ 3 | 1 | DQ3_RST_HOLD_B |
| AJ17 | MIO12_QSPI_UPR_CLK | 16 | C |
| AD17 | MIO7_QSPI_UPR_CS_B | 7 | S_B |

The configuration and Quad-SPI section of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3] provides details on using the Quad-SPI flash memory. For more QSPI details, see the Micron MT25QU512ABB8ESF-0SIT data sheet at the Micron website [Ref 20].

USB0 (MIO 52-63)

The USB interface on the PS-side serves multiple roles as a host, device, and OTG controller. The USB 3.0 interface is supported by the MPSoC GTR interface while the USB 2.0

capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 micro USB type AB connector (J96).

USB 3.0 Transceiver and USB 2.0 ULPI PHY

[Figure 2-1, callout 5]

The ZCU102 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver at U116 to support a USB connection to the host computer (see [Figure 3-3](#)). A USB cable is supplied in the ZCU102 Evaluation Kit (standard-A connector to host computer, micro-B connector to ZCU102 board connector J96). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

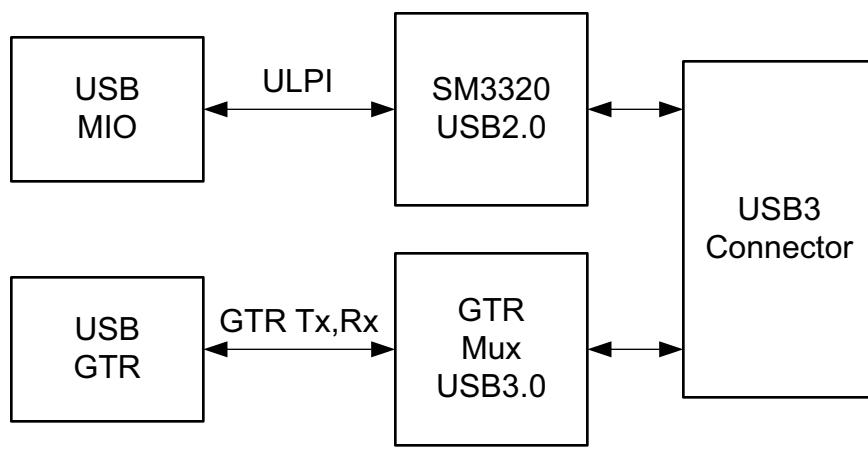


Figure 3-3: **USB Interface**

The USB3320 is clocked by a 24 MHz crystal. Consult the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [\[Ref 21\]](#).

The interface to the USB3320 PHY is implemented through the IP in the XCZU9EG MPSoC Processor System (PS).

[Table 3-7](#) describes the jumper settings for the USB 2.0 circuit. The default shunt positions are set for Device mode.

Table 3-7: USB Jumper Settings

| Header | Function | Shunt Position | Shunt Position | Shunt Position | Notes |
|---------------|----------------------------|-----------------------|-----------------------|-----------------------|--|
| | | Device Mode | Host Mode | OTG Mode | |
| J7 | V _{BUS} 5V supply | OFF | ON | ON | Shunt ON = Host or OTG mode Shunt OFF = Device mode |
| J109 | Cable ID select | 2-3 | 2-3 | 1-2 | Position 1-2 = A/B cable detect Position 2-3 = ID not used |
| J110 | CV _{BUS} select | 1-2 | 2-3 | 1-2 | Position 1-2 = OTG and Device mode (1 μF) Position 2-3 = Host mode (120 μF) |
| J112 | USB J96 shield connection | 1-2 | 1-2 | 1-2 | Position 1-2 = Shield floating Position 2-3 = Shield connected to GND |
| J113 | RV _{BUS} select | 1-2 | 1-2 | 2-3 | Position 1-2 = Host or Device mode (10 kΩ) Position 2-3 = OTG mode (1 kΩ) |

The connections between the USB 2.0 PHY at U116 and the XCZU9EG MPSoC are listed in [Table 3-8](#).

Table 3-8: USB 2.0 ULPI Transceiver Connections to the XCZU9EG MPSoC

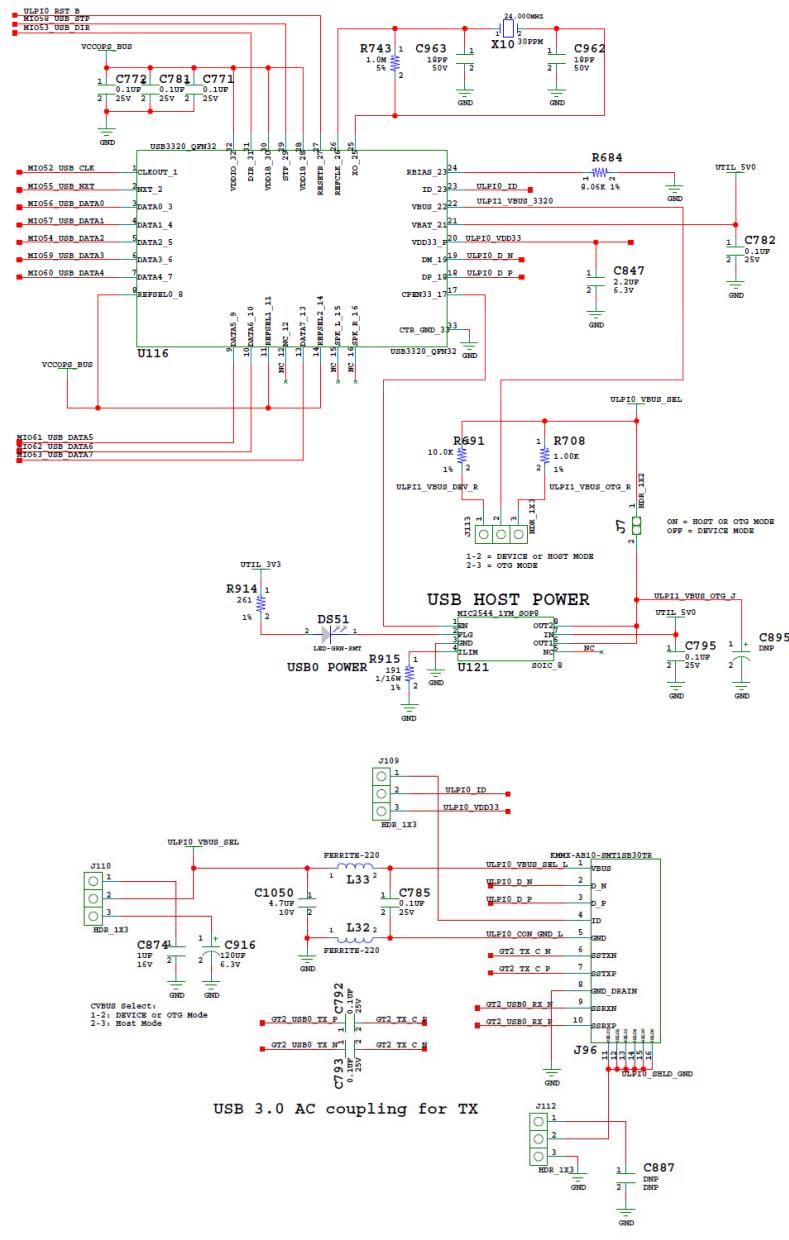
| XCZU9EG (U1) Pin | Net Name | USB3320 U116 | |
|-------------------------|-----------------|---------------------|-----------------|
| | | Pin Number | Pin Name |
| U117.4 ⁽¹⁾ | ULPIO_RST_B | 27 | RESET_B |
| G23 | MIO58_USB_STP | 29 | STP |
| E23 | MIO53_USB_DIR | 31 | DIR |
| F22 | MIO52_USB_CLK | 1 | CLKOUT |
| B23 | MIO55_USB_NXT | 2 | NXT |
| C23 | MIO56_USB_DATA0 | 3 | DATA0 |
| A23 | MIO57_USB_DATA1 | 4 | DATA1 |
| F23 | MIO54_USB_DATA2 | 5 | DATA2 |
| B24 | MIO59_USB_DATA3 | 6 | DATA3 |
| E24 | MIO60_USB_DATA4 | 7 | DATA4 |
| C24 | MIO61_USB_DATA5 | 9 | DATA5 |
| G24 | MIO62_USB_DATA6 | 10 | DATA6 |
| D24 | MIO63_USB_DATA7 | 13 | DATA7 |

Notes:

- PS_POR_B (U1.V23) or PS_MODE1 (DIP SW6.2) or PB SW2 drive U116 RST_B via OR gate U117.

Note that the shield for the USB 3.0 micro-B connector (J96) can be tied to GND by a jumper on header J112 pins 2-3. The USB shield can optionally be connected through a capacitor to GND by installing a capacitor (body size 0402) at location C887 and jumping pins 1-2 on header J112.

The USB3320 ULPI U116 transceiver circuit (see [Figure 3-4](#)) has a Micrel MIC2544 high-side programmable current limit switch (U121). This switch has an open-drain output fault flag on pin 2, which will turn on LED DS51 if overcurrent or thermal shutdown conditions are detected. DS51 is located in the U116 circuit area near push-button SW2 ([Figure 2-1](#), callout 5).



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Figure 3-4: ULPI U116 Transceiver Circuit

SD1 (MIO 39-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

SD Card Interface

[Figure 2-1, callout 6]

The ZCU102 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found at the SanDisk Corporation [Ref 22] or SD Association [Ref 23] websites. The ZCU102 SD card interface supports the SD1_LS configuration boot mode documented in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3].

The SDIO signals are connected to XCZU9EG MPSoC PS bank 501 which has its V_{CCMIO} set to 1.8V. Each of the six MIOxx_SDIO_* nets has a series 30 ohm resistor at the source. An NXP IP4856CX25 SD 3.0-compliant voltage level-translator U133 is present between the XCZU9EG MPSoC and the SD card connector (J100). The NXP IP4856CX25 U133 device provides SD3.0 capability with SDR104 performance. The NXP SD3.0 level shifter is mounted on an Aries adapter board that has the pin mapping shown in Table 3-9.

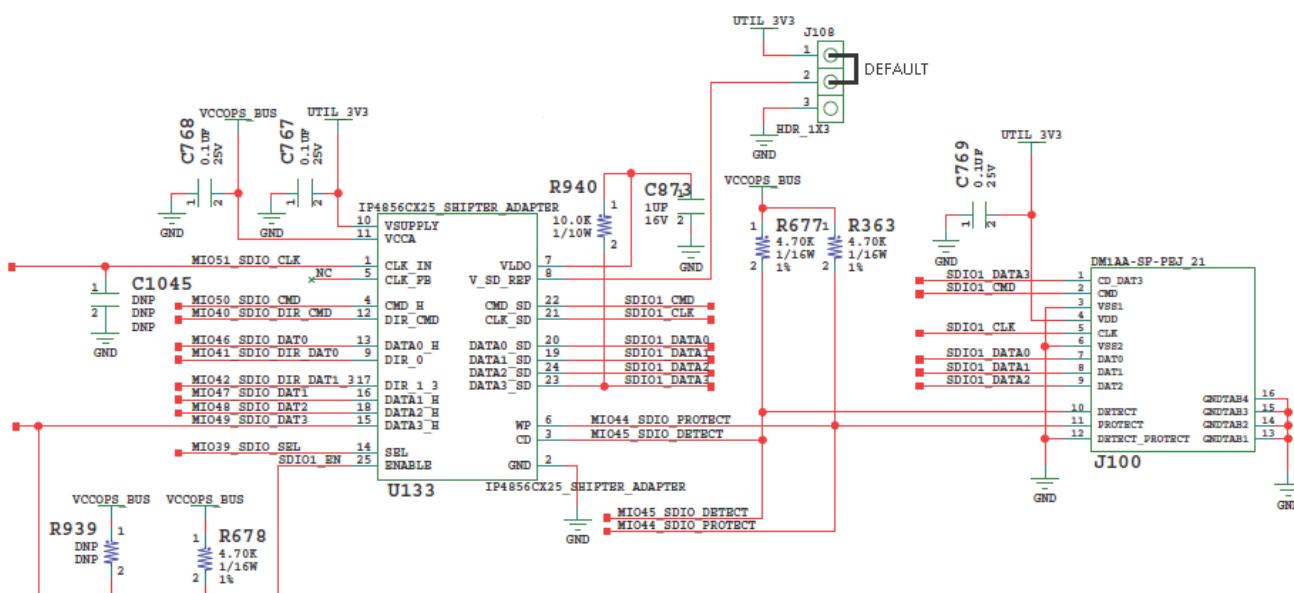
Table 3-9: U133 IP4856CX25 Adapter Pin-Out

| Aries Adapter Pin Number | IP4856CX25 U133 Pin Number | IP4856CX25 U133 Pin Name |
|--------------------------|----------------------------|--------------------------|
| 1 | C1 | CLK_IN |
| 2 | C3 | GND |
| 3 | D3 | CD |
| 4 | D2 | CMD_H |
| 5 | E2 | CLK_FB |
| 6 | E4 | WP |
| 7 | B4 | VLDO |
| 8 | C4 | V_{SD_REF} |
| 9 | A3 | DIR_0 |
| 10 | A4 | V_{SUPPLY} |
| 11 | B3 | V_{CCA} |
| 12 | A2 | DIR_CMD |
| 13 | D1 | DATA0_H |
| 14 | B2 | SEL |
| 15 | B1 | DATA3_H |
| 16 | E1 | DATA1_H |
| 17 | E3 | DIR_1_3 |
| 18 | A1 | DATA2_H |
| 19 | E5 | DATA1_SD |
| 20 | D5 | DATA0_SD |

Table 3-9: U133 IP4856CX25 Adapter Pin-Out (Cont'd)

| Aries Adapter Pin Number | IP4856CX25 U133 Pin Number | IP4856CX25 U133 Pin Name |
|--------------------------|----------------------------|--------------------------|
| 21 | C5 | CLK_SD |
| 22 | D4 | CMD_SD |
| 23 | B5 | DATA3_SD |
| 24 | A5 | DATA2_SD |
| 25 | C2 | ENABLE |

Figure 3-5 shows the connections of the SD card interface on the ZCU102 board.



X16378-071817

Figure 3-5: SD Card Interface

Table 3-10 lists the SD card interface connections to the XCZU9EG MPSoC.

Table 3-10: SD Interface Connections to the XCZU9EG MPSoC

| XCZU9EG (U1) Pin | Net Name | U133 IP4856CX25 Adapter | |
|---------------------|-----------------------|-------------------------|----------|
| | | Pin Number | Pin Name |
| N23 | MIO39_SDIO_SEL | 14 | SEL |
| M23 | MIO40_SDIO_DIR_CMD | 12 | DIR_CMD |
| J24 | MIO41_SDIO_DIR_DAT0 | 9 | DIR_0 |
| M24 | MIO42_SDIO_DIR_DAT1_3 | 17 | DIR_1_3 |
| J25 | MIO46_SDIO_DAT0 | 13 | DATA0_H |
| L25 | MIO47_SDIO_DAT1 | 16 | DATA1_H |
| M25 | MIO48_SDIO_DAT2 | 18 | DATA2_H |
| K25 | MIO49_SDIO_DAT3 | 15 | DATA3_H |
| P25 | MIO50_SDIO_CMD | 4 | CMD_H |
| N25 | MIO51_SDIO_CLK | 1 | CLK_IN |
| N24 | MIO44_SDIO_PROTECT | 6 | WP |
| P24 | MIO45_SDIO_DETECT | 3 | CD |

Programmable Logic JTAG Programming Options

[Figure 2-1, callouts 7 and 39]

ZCU102 JTAG chain:

- J2 USB micro AB connector connected to U21 Digilent USB JTAG
- J8 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J6 2x10 Arm JTAG male pin header

The ZCU102 board JTAG chain is shown in [Figure 3-6](#).

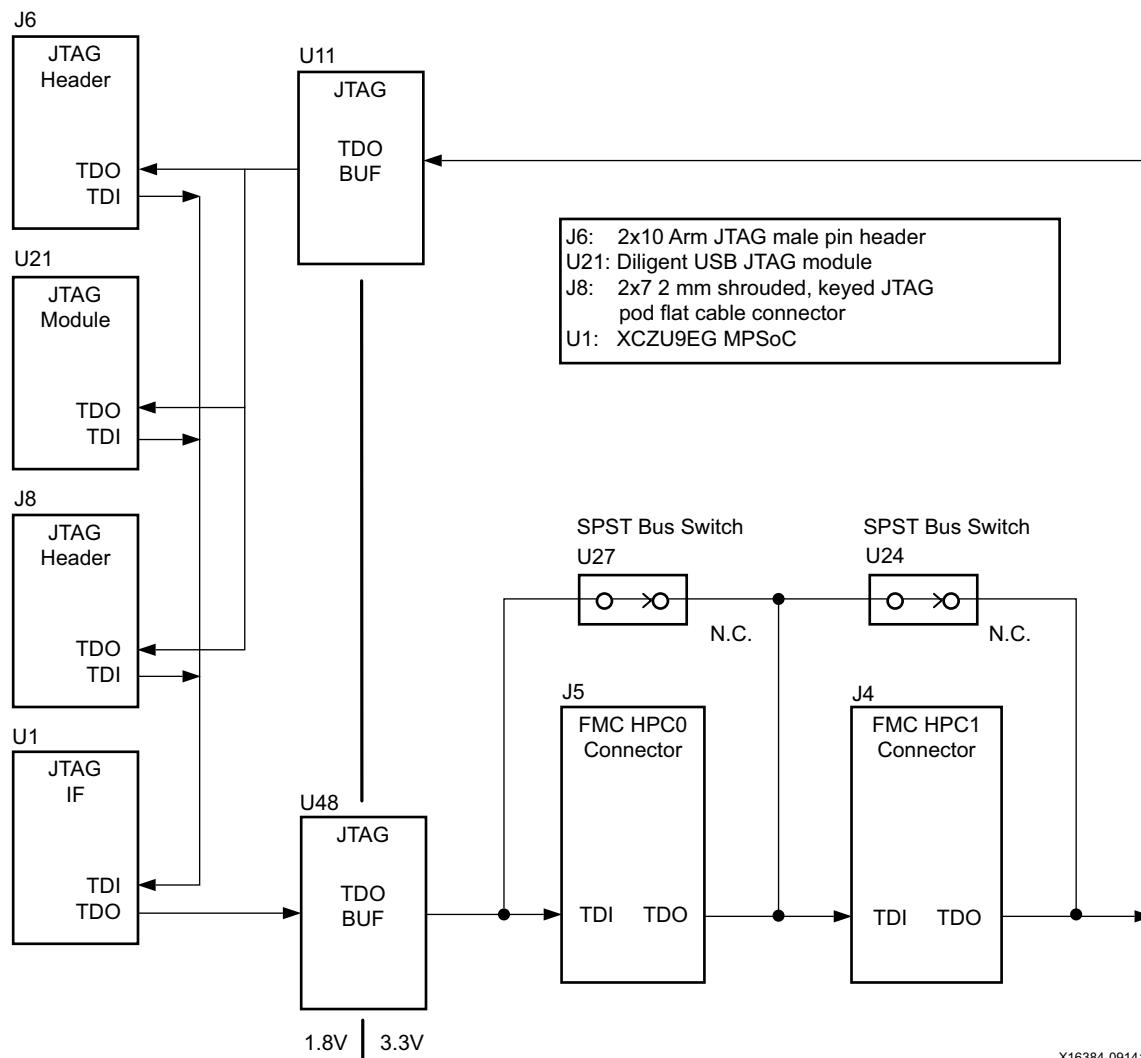


Figure 3-6: JTAG Chain Block Diagram

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J5 or J4 it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U27 and U24. The SPST switches are normally closed and transition to an open state when an FMC is attached. Switch U27 adds an attached FMC to the JTAG chain as determined by the FMC_HPC0_PRSNT_M2C_B signal. Switch U24 adds an attached FMC to the JTAG chain as determined by the FMC_HPC1_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the XCZU9EG MPSoC.

EMIO Arm Trace Port

[Figure 2-1, callout 43]

The ZCU102 evaluation board provides a trace/debug 38-pin Mictor connector, P6. Figure 3-7 shows connector P6 with its MPSoC Bank 47/48 connections.

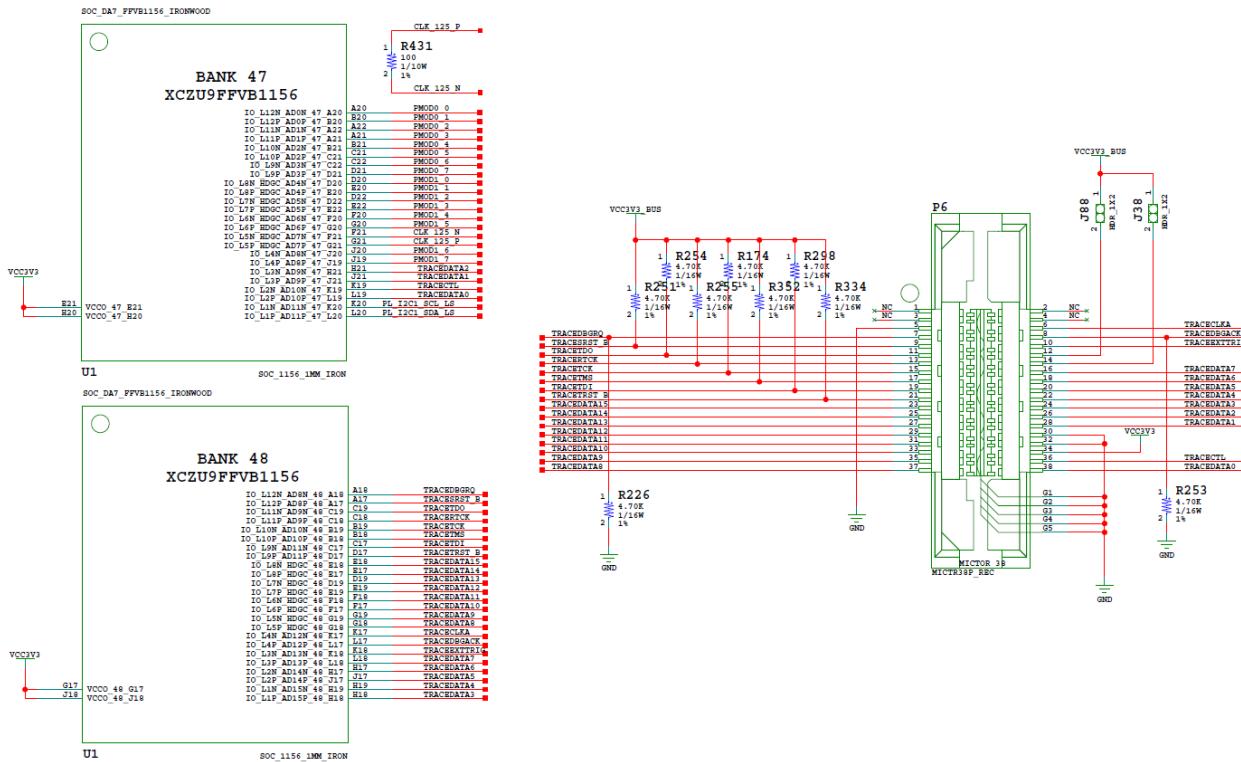


Table 3-11: Trace/Debug Conn. P6 Connections to the XCZU9EG MPSoC (Cont'd)

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Trace/Debug P6 Pin |
|---------------------|-----------------------|--------------|-----------------------|
| G18 | TRACEDATA8 | LVCMOS33 | 37 |
| G19 | TRACEDATA9 | LVCMOS33 | 35 |
| F17 | TRACEDATA1 | LVCMOS33 | 33 |
| F18 | TRACEDATA11 | LVCMOS33 | 31 |
| E19 | TRACEDATA12 | LVCMOS33 | 29 |
| D19 | TRACEDATA13 | LVCMOS33 | 27 |
| E17 | TRACEDATA14 | LVCMOS33 | 25 |
| E18 | TRACEDATA15 | LVCMOS33 | 23 |
| K17 | TRACECLKA | LVCMOS33 | 6 |
| C18 | TRACERTCK | LVCMOS33 | 13 |
| A18 | TRACEDBGRQ | LVCMOS33 | 7 |
| L17 | TRACEDBGACK | LVCMOS33 | 8 |
| K19 | TRACECTL | LVCMOS33 | 36 |
| K18 | TRACEEXTTRIG | LVCMOS33 | 10 |
| B19 | TRACETCK | LVCMOS33 | 15 |
| C17 | TRACETDI | LVCMOS33 | 19 |
| C19 | TRACETDO | LVCMOS33 | 11 |
| B18 | TRACETMS | LVCMOS33 | 17 |
| D17 | TRACETRST_B | LVCMOS33 | 21 |
| A17 | TRACESRST_B | LVCMOS33 | 9 |

For more information about managing the Zynq MPSoC extended MIO (EMIO) trace port connections refer to the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3].

Clock Generation

The ZCU102 board provides fixed and variable clock sources for the XCZU9EG MPSoC. [Table 3-12](#) lists the source devices for each clock.

Table 3-12: ZCU102 Board Clock Sources

| Clock Name | Frequency | Clock Source |
|--------------------------------------|----------------------|-----------------------------|
| Fixed Frequency Clocks | | |
| PS_REF_CLK | 33.33 MHz | U69 SI5341B Clock Generator |
| CLK_74_25 | 74.25 MHz | |
| CLK_125 | 125 MHz | |
| GTR_REF_CLK_PCIE | 100 MHz | |
| PCIE_SLOT_CLK | 100 MHz | |
| GTR_REF_CLK_SATA | 125 MHz | |
| GTR_REF_CLK_USB3 | 26 MHz | |
| GTR_REF_CLK_DP | 27 MHz | |
| Programmable Frequency Clocks | | |
| USER_SI570 | 300 MHz (Default) | U42 SI570 I2C PROG. OSC. |
| USER_MGT_SI570 | 156.2 MHz (Default) | U56 SI570 I2C PROG. OSC. |
| USER_MGT_SMA | User-Provided Source | J79 (P)/J80 (N) SMA CONN. |
| HDMI_SI5324_OUT | Variable | U108 Clock Recovery |
| SFP_SI5328_OUT | Variable | U20 Clock Recovery |

[Table 3-13](#) lists the source devices for each clock.

Table 3-13: Clock Connections, Source to XCZU9EG MPSoC

| Clock Source Ref. Des. and Pin | Schematic Net Name | I/O Standard | FPGA (U1) Pin |
|--------------------------------|--------------------|--------------|-------------------------|
| U69.59 | PS_REF_CLK | (1) | U24 |
| U69.45 | CLK_125_P | LVDS_25 | G21 |
| U69.44 | CLK_125_N | LVDS_25 | F21 |
| U69.51 | CLK_74_25_P | LVDS_25 | AK15 |
| U69.50 | CLK_74_25_N | LVDS_25 | AK14 |
| U69.38 | PCIE_SLOT_CLK_P | N/A | (PCIE CONNECTOR) P1.A13 |
| U69.37 | PCIE_SLOT_CLK_N | N/A | (PCIE CONNECTOR) P1.A14 |
| U69.42 | GTR_REF_CLK_PCIE_P | (2) | AA27 |
| U69.41 | GTR_REF_CLK_PCIE_N | (2) | AA28 |

Table 3-13: Clock Connections, Source to XCZU9EG MPSoC (Cont'd)

| Clock Source Ref. Des. and Pin | Schematic Net Name | I/O Standard | FPGA (U1) Pin |
|--------------------------------|-------------------------|--------------|-----------------------------|
| U69.35 | GTR_REF_CLK_SATA_P | (2) | W27 |
| U69.34 | GTR_REF_CLK_SATA_N | (2) | W28 |
| U69.31 | GTR_REF_CLK_USB3_P | (2) | U27 |
| U69.30 | GTR_REF_CLK_USB3_N | (2) | U28 |
| U69.24 | GTR_REF_CLK_DP_P | (2) | U31 |
| U69.23 | GTR_REF_CLK_DP_N | (2) | U32 |
| U42.4 | USER_SI570_P | DIFF_SSTL12 | AL8 |
| U42.5 | USER_SI570_N | DIFF_SSTL12 | AL7 |
| U56.4 | USER_MGT_SI570_P | (2) | (1-to-2 CLOCK BUFFER) U51.6 |
| U56.5 | USER_MGT_SI570_N | (2) | (1-to-2 CLOCK BUFFER) U51.7 |
| U51.11 | USER_MGT_SI570_CLOCK1_P | (2) | L27 |
| U51.12 | USER_MGT_SI570_CLOCK1_N | (2) | L28 |
| U51.13 | USER_MGT_SI570_CLOCK2_P | (2) | C8 |
| U51.14 | USER_MGT_SI570_CLOCK2_N | (2) | C7 |
| J79.1 | USER_SMA_MGT_CLOCK_P | (2) | N27 |
| J80.1 | USER_SMA_MGT_CLOCK_N | (2) | N28 |
| U108.28 | HDMI_SI5324_OUT_P | (2) | R27 |
| U108.29 | HDMI_SI5324_OUT_N | (2) | R28 |
| U20.28 | SFP_SI5328_OUT_P | (2) | B10 |
| U20.29 | SFP_SI5328_OUT_N | (2) | B9 |

Notes:

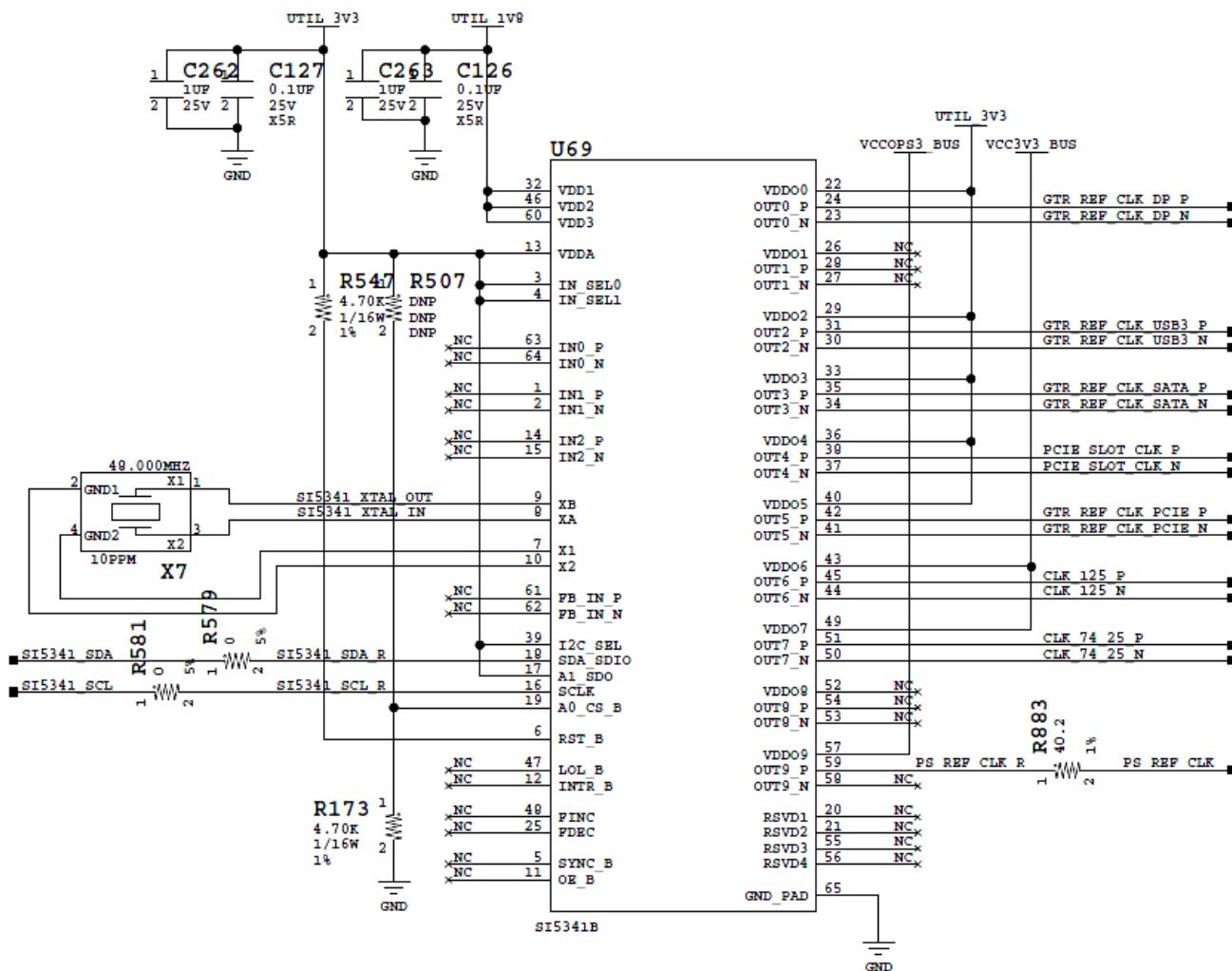
1. U1 XCU9EG Bank 503 supports LVCMOS level inputs.
2. U1 MGT (I/O standards do not apply).

SI5341B 10 Independent Output Any-Frequency Clock Generator (PS Reference Clock)

[Figure 2-1, callout 10]

- Clock generator: Silicon Labs SI5341B-B05071-GM
- Jitter: <100 fs RMS typical
- Differential and single-ended outputs

The SI5341B is a one-time programmable clock source. For more details refer to the SI5341B data sheet [Ref 24] for more details. The clock circuit is shown in Figure 3-8.



X16386-071817

Figure 3-8: SI5341B Clock Generator

Programmable User Clock

[Figure 2-1, callout 8]

The ZCU102 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U42) connected to the GC inputs of PL bank 64. This USER_SI570_P and USER_SI570_N clock signal pair is connected to XCZU9EG MPSoC U1 pins AL8 and AL7 respectively. On power-up the user clock defaults to an output frequency of 300.000 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZCU102 board reverts this user clock to the default frequency of 300.000 MHz.

This oscillator can be reprogrammed from MSP430 system controller U41 (see [TI MSP430 System Controller](#) for more information).

- Programmable oscillator: Silicon Labs Si570BAB001614DG (10 MHz-810 MHz)
- LVDS differential output
- Total Stability: 61.5 ppm

The user clock circuit is shown in [Figure 3-9](#). The Silicon Labs Si570 and Si53340 data sheets are available on the Silicon Labs website [\[Ref 24\]](#).

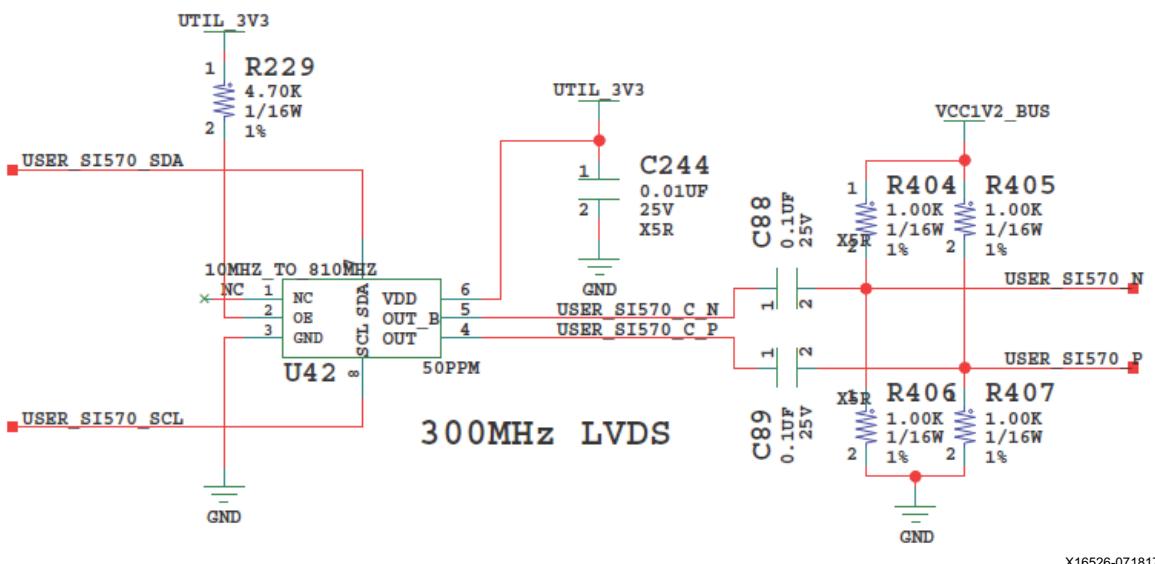


Figure 3-9: Programmable User Clock

Programmable User MGT Clock

[Figure 2-1, callout 9]

The ZCU102 board has a programmable low-jitter 3.3V LVDS SI570 differential oscillator (U56) connected to a 1-to-2 SI53340 clock driver (U51). On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZCU102 board reverts this user clock to the default frequency of 156.250 MHz.

This oscillator can be reprogrammed from MSP430 system controller U41 (see [TI MSP430 System Controller](#) for more information).

- Programmable oscillator: Silicon Labs Si570BAB000544DG (10 MHz-810 MHz)
- LVDS differential output
- Total stability: 61.5 ppm

The user clock MGT circuit is shown in [Figure 3-10](#). The Silicon Labs Si570 and Si53340 data sheets are available on the Silicon Labs website [\[Ref 24\]](#).

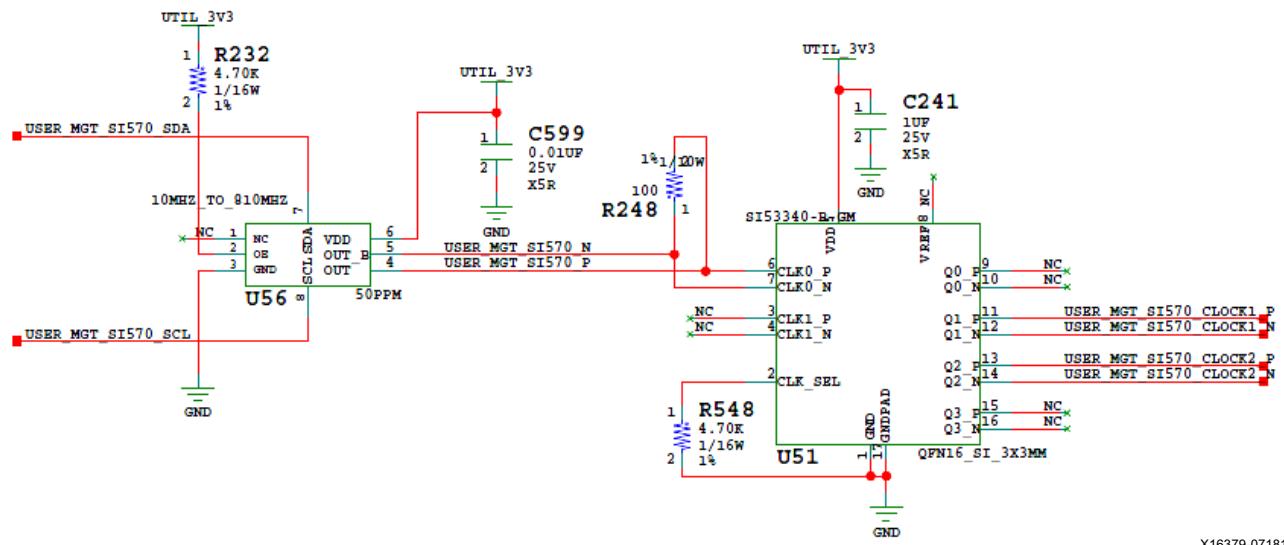


Figure 3-10: Programmable User MGT Clock

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User SMA MGT Clock

[Figure 2-1, callout 42]

The ZCU102 board provides a pair of SMAs for differential AC coupled user MGT clock input into FPGA U1 MGTH bank 129. This differential signal pair is series-capacitor coupled. The P-side SMA J79 signal USER_SMA_MGT_CLOCK_P is connected to U1 MGTRCLK1P pin J27, with the N-side SMA J80 signal USER_SMA_MGT_CLOCK_N connected to U1 MGTRCLK1N pin J28. The user SMA MGT clock circuit is shown in Figure 3-11.

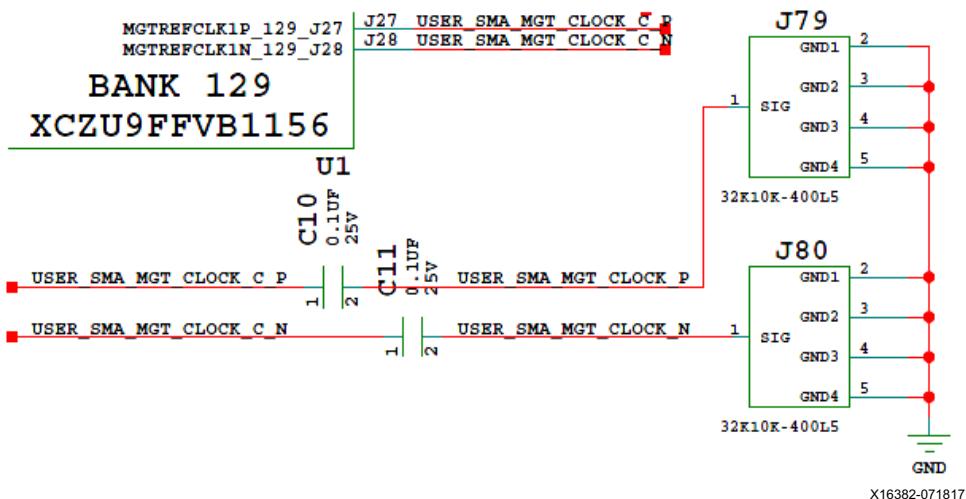
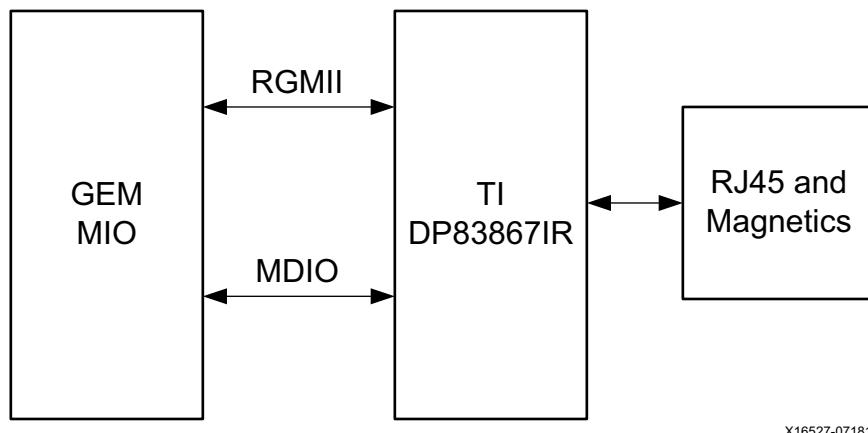


Figure 3-11: User SMA MGT Clock

GEM3 Ethernet (MIO 64-77)

[Figure 2-1, callout 12]

The PS-side Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface, shown in Figure 3-12, which connects to a TI DP83867IRPAP Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector. The RGMII Ethernet PHY is boot strapped to PHY address 5'b01100 (**0x0C**) and Auto Negotiation set to *Enable*. Communication with the device is covered in the DP83867 RGMII PHY data sheet [Ref 25].



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Figure 3-12: Ethernet Block Diagram

10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2-1, callout 12]

The ZCU102 board uses the TIDP83867IRPAP Ethernet RGMII PHY [Ref 25] at U98 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Wurth 7499111221A RJ-45 connector (P12) with built-in magnetics.

The Ethernet connections from XCZU9EG MPSoC U1 to the DP83867IRPAP PHY device at U98 are listed in [Table 3-14](#).

Table 3-14: Ethernet Connections, XCZU9EG MPSoC to the PHY Device

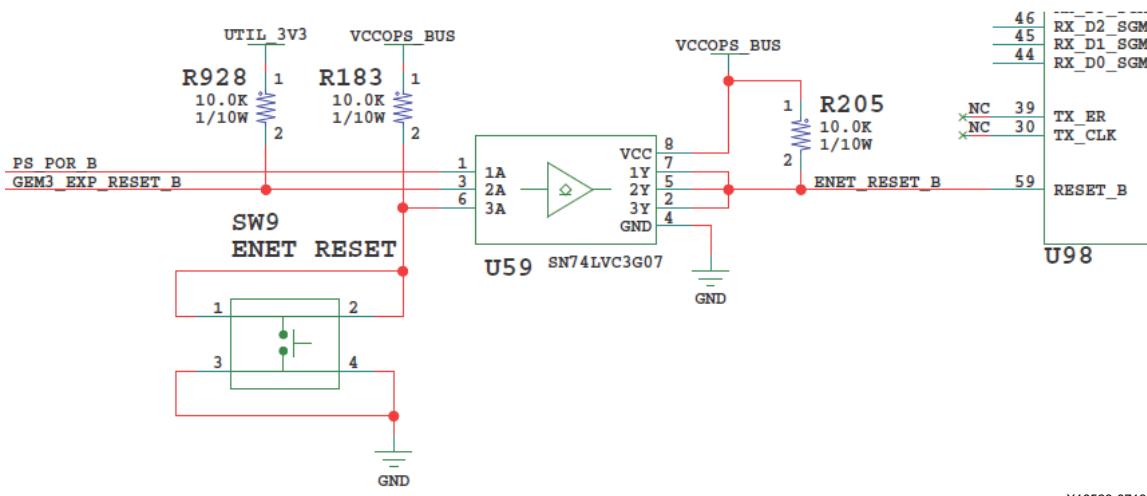
| XCZU9EG (U1) Pin | Schematic Net Name | DP83867 PHY U98 | |
|---------------------|--------------------|-----------------|---------------|
| | | Pin | Name |
| A25 | MIO64_ENET_TX_CLK | 40 | GTX_CLK |
| A26 | MIO65_ENET_TX_D0 | 38 | TX_DO |
| A27 | MIO66_ENET_TX_D1 | 37 | TX_D1 |
| B25 | MIO67_ENET_TX_D2 | 36 | TX_D2 |
| B26 | MIO68_ENET_TX_D3 | 35 | TX_D3 |
| B27 | MIO69_ENET_TX_CTRL | 52 | TX_EN_TX_CTRL |
| C26 | MIO70_ENET_RX_CLK | 43 | RX_CLK |
| C27 | MIO71_ENET_RX_D0 | 44 | RX_DO |
| E25 | MIO72_ENET_RX_D1 | 45 | RX_D1 |
| H24 | MIO73_ENET_RX_D2 | 46 | RX_D2 |
| G25 | MIO74_ENET_RX_D3 | 47 | RX_D3 |
| D25 | MIO75_ENET_RX_CTRL | 53 | RX_DV_RX_CTRL |

Table 3-14: Ethernet Connections, XCZU9EG MPSoC to the PHY Device (Cont'd)

| XCZU9EG (U1) Pin | Schematic Net Name | DP83867 PHY U98 | |
|---------------------|--------------------|-----------------|------|
| | | Pin | Name |
| H25 | MIO76_ENET_MDC | 20 | MDC |
| F25 | MIO77_ENET_MDIO | 21 | MDIO |

Ethernet PHY Reset

The DP83867IRPAP PHY U98 reset circuit is shown in Figure 3-13. The DP83867IRPAP can be reset by the SW9 push-button (U59.6), the MAX16025 U22 MPSoC PS-side POR device (U59.1), or the I2C0 connected U97 TCA6416A I/O expander port P06 pin 10 (U59.3).



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Figure 3-13: Ethernet PHY Reset Circuit

Ethernet PHY LED Interface

[Figure 2-1, callout 12]

The DP83867IRPAP PHY U98 LED interface (LED_0, LED_2) uses the two LEDs embedded in the P12 RJ45 connector bezel. The LED functional description is show in [Table 3-15](#).

Table 3-15: Ethernet PHY LED Functional Description

| Pin | | Type | Description |
|-------|-----|------------|---|
| Name | No. | | |
| LED_2 | 61 | S, I/O, PD | By default, this pin indicates receive or transmit activity. Additional functionality is configurable by means of LEDCR1[11:8] register bits. Note: This pin is a strap configuration pin for RGZ devices only. |
| LED_1 | 62 | S, I/O, PD | By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable by means of LEDCR1[7:4] register bits. |
| LED_0 | 63 | S, I/O, PD | By default, this pin indicates that link is established. Additional functionality is configurable by means of LEDCR1[3:0] register bits. |

The LED functions can be re-purposed with a LEDCR1 register write available through the PHY's management Data Interface, MDIO/MDC. LED_2 is assigned to ACT (activity indicator) and LED_0 indicates link established. For more Ethernet PHY details, see the TI DS83867 data sheet [\[Ref 25\]](#).

CP2108 USB UART Interface

[Figure 2-1, callout 13]

The CP2108 quad USB-UART on the ZCU102 board provides four level-shifted UART connections through single micro-B USB connector J83. Channel 0 and 1 are PS-side MIO connections described in the MIO section. Channel 2 is a PL-side connection and Channel 3 is connected to MSP430 system controller U41. The USB UART interface circuit is shown in [Figure 3-14](#). The Silicon Labs CP2108 data sheet is available on the Silicon Labs website [\[Ref 24\]](#).

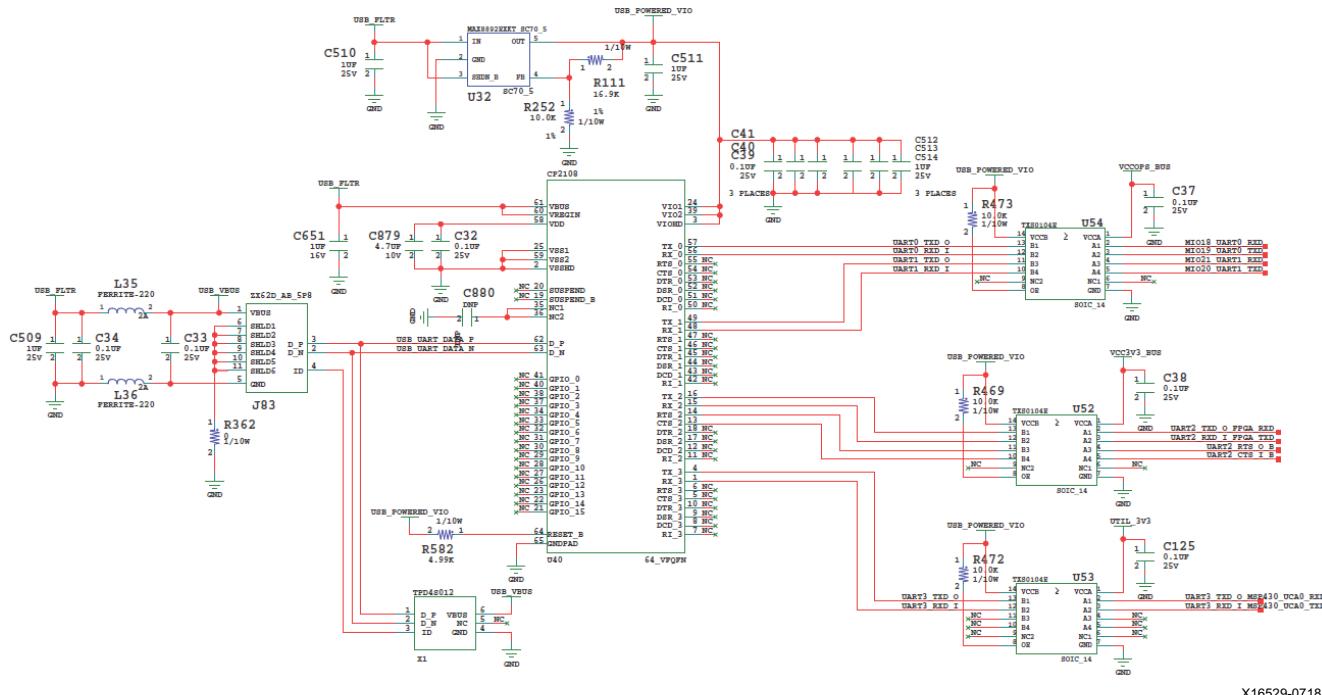


Figure 3-14: USB UART Interface

CP2108 Channel 2 PL-Side UART Interface

The CP2108 channel 2 PL-side UART interface circuit is shown in Figure 3-15. The connections from XCZU9EG MPSoC U1 to CP2108 U40 via TSX0104E level shifter U52 are listed in Table 3-16.

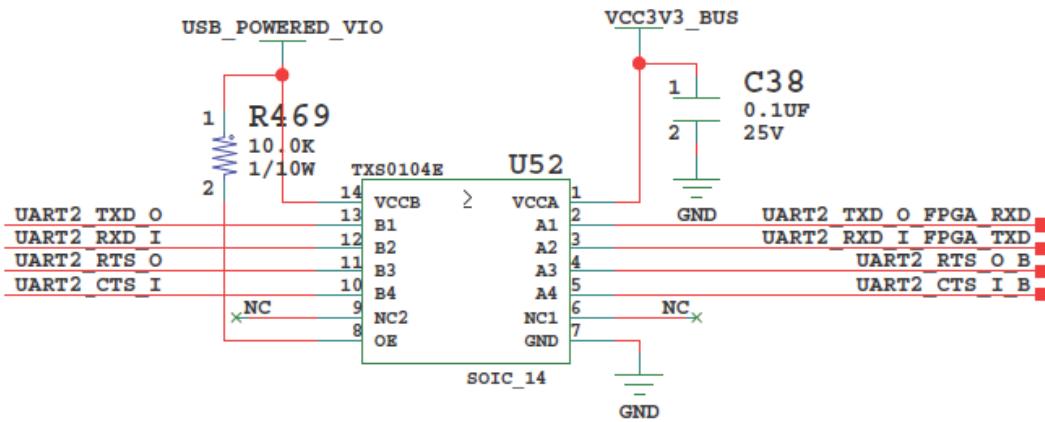


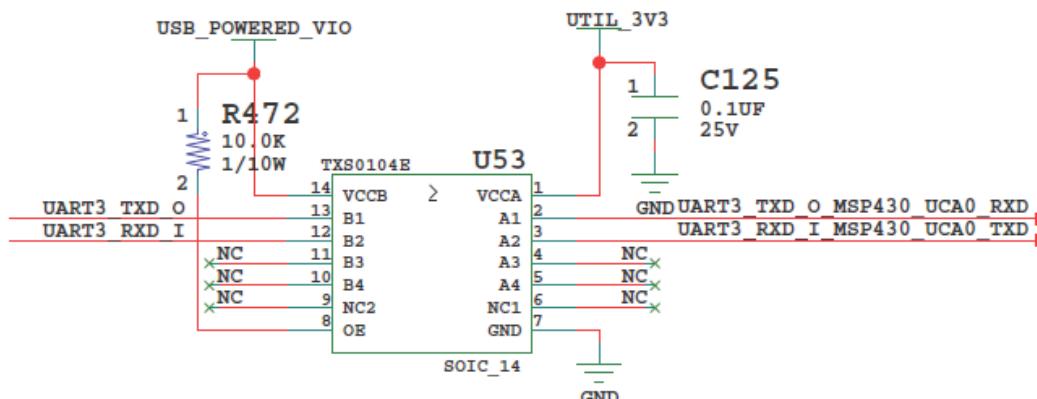
Figure 3-15: PL-Side USB UART Interface

Table 3-16: XCZU9EG U1 to CP2108 U40 Connections via L/S U52

| XCZU9EG (U1) Pin | Schematic Net Name | CP2108 U40 | |
|---------------------|----------------------|------------|---------|
| | | Pin Name | Pin No. |
| E13 | UART2_TXD_O_FPGA_RXD | TX_2 | 16 |
| F13 | UART2_RXD_I_FPGA_TXD | RX_2 | 15 |
| D12 | UART2_RTS_O_B | RTS_2 | 14 |
| E12 | UART2_CTS_I_B | CTS_2 | 13 |

CP2108 Channel 3 MSP430 UART Interface

The CP2108 Channel 3 MSP430 UART interface circuit is shown in Figure 3-16. The connections from MSP430 U41 to CP2108 U40 via TSX0104E level shifter U53 are listed in Table 3-17.



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Figure 3-16: MSP430 USB UART Interface

Table 3-17: MSP430 U41 to CP2108 U40 Connections via L/S U53

| MSP430 U41 | Pin Name | Pin No. | Schematic Net Name | CP2108 U40 | |
|------------|----------|---------|-----------------------------|------------|---------|
| | | | | Pin Name | Pin No. |
| | P3_3 | 26 | UART3_TXD_O_MSP430_UCA0_RXD | TX_3 | 4 |
| | P3_3 | 25 | UART3_RXD_I_MSP430_UCA0_TXD | RX_3 | 1 |

GPIO (MIO 13, 38)

These two (2) GPIO bits are connected to the U41 MSP430 system controller for general purpose signaling or communications between the Zynq UltraScale+ MPSoC and the MSP430 system controller. These signals are level-shifted by TSX0108E U141. The connections between the U41 system controller and the XCZU9EG MPSoC are listed in [Table 3-18](#).

Table 3-18: System Controller U41 GPIO Connections to XCZU9EG U1

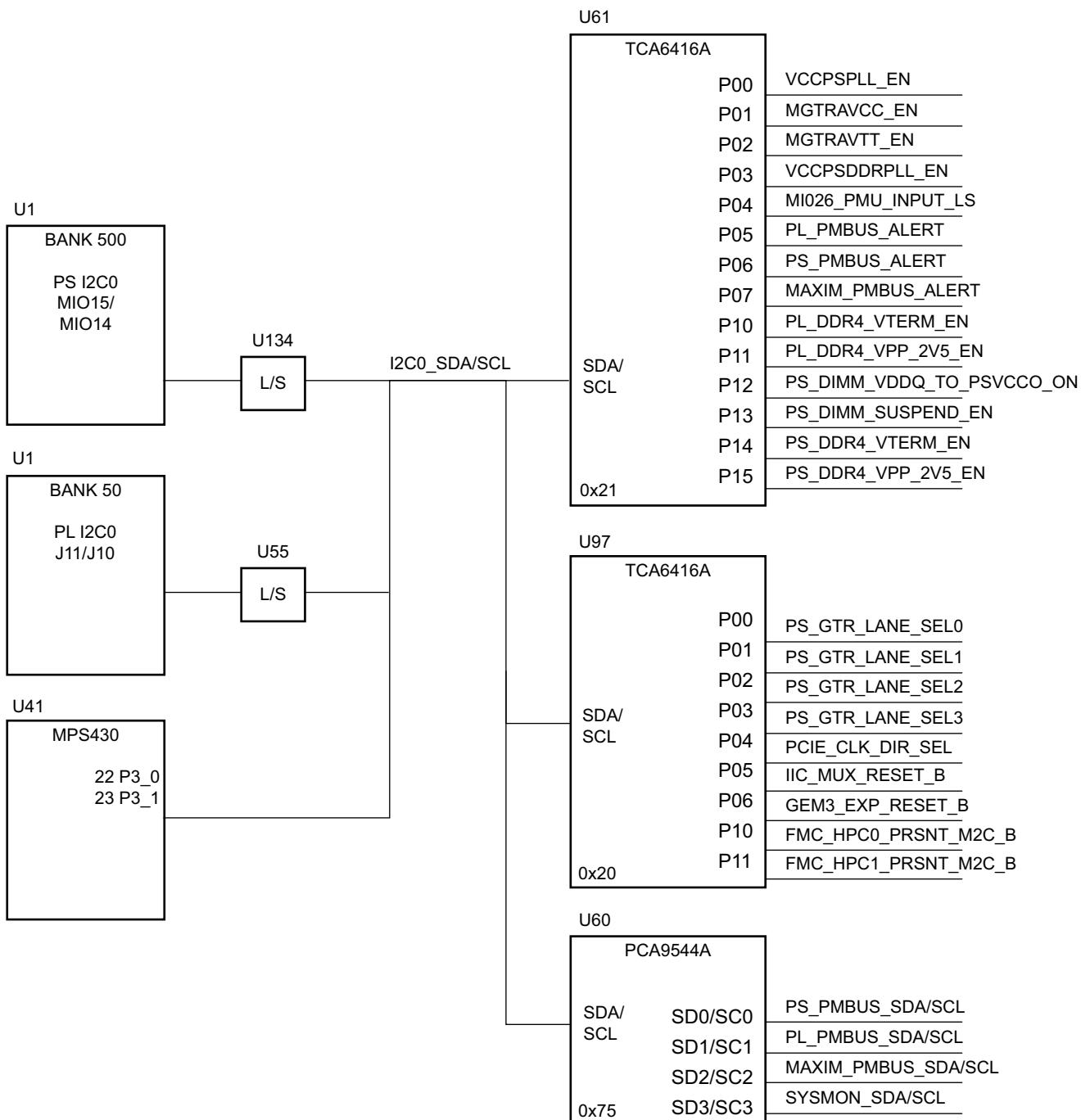
| XCZU9EG (U1) Pin | Net Name | MSP430 U41 | |
|---------------------|----------------|------------|---------|
| | | Pin Name | Pin No. |
| AK17 | MIO13_PS_GPIO2 | 20 | P1_7 |
| L23 | MIO38_PS_GPIO1 | 19 | P1_6 |

I2C0 (MIO 14-15)

I2C0 connects to MPSoC U1 PS Bank 500 and PL bank 50, and to system controller U41, as shown in [Figure 3-17](#). I2C0 connects to two GPIO 16-bit port expanders (TCA6416A U61 and U97) and an I2C SWITCH (PCA9544A U60) for controlling resets, GTR multiplexer settings, and power system enable pins, without requiring the PL-side to be configured. TCA6416A U97 is pin-strapped to respond to I2C address **0x20**, and U61 to **0x21**. The PCA9544A multiplexer is set to **0x75**.

The I2C0 bus also provides access to the PMBUS power controllers and PS-side and PL-side INA226 power monitors via the U60 PCA9544A bus switch. All PMBus controlled Maxim regulators are tied to the MAXIM_PMBUS, while the INA226 power monitors are separated on to PS_PMBUS and PL_PMBUS. [Figure 3-17](#) shows the I2C0 bus topology.

[Table 3-19](#) lists the I2C0 port expander TCA6416A U61 connections and [Table 3-20](#) the TCA6416A U97 connections. The devices on each bus of the I2C0 multiplexer U60 are identified in [Table 3-21](#) and the multiplexer bus connections are listed in [Table 3-22](#).



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 Figure 3-17: I_C0 Bus Topology

Table 3-19: I₂C0 Port Expander TCA6416A U61 Connections

| TCA6416A U61 | | Schematic Net Name | Connected To | | | |
|-----------------|------------|-------------------------------|--|-----------|--|--|
| Pin Name | Pin No. | | Pin Name | Pin No. | Reference Designation | Device |
| SDA | 23 | I ₂ C0_SDA | Refer to connections shown in Figure 3-17 . (TCA6416A U61 Addr. 0x21) | | | |
| SCL | 22 | I ₂ C0_SCL | | | | |
| P00 | 4 | VCCPSPLL_EN | B | 2 | U140 | SN74LVC1G08 |
| P01 | 5 | MGTRAVCC_EN | B | 2 | U112 | SN74LVC1G08 |
| P02 | 6 | MGTRAVTT_EN | B | 2 | U130 | SN74LVC1G08 |
| P03 | 7 | VCCPSDDRPLL_EN | B | 2 | U142 | SN74LVC1G08 |
| P04 | 8 | MIO26_PMU_INPUT_LS | B | 4 | U147 | SN74AVC1T45 |
| P05 | 9 | PL_PMBUS_ALERT | ALERT | 3 | U16, U65, U74, U75, U79, U80, U81, U84 | INA226 Op amps |
| P06 | 10 | PS_PMBUS_ALERT | ALERT | 3 | U15, U76, U77, U78, U87, U85, U86, U88, U92, U93 | INA226 Op amps |
| P07 | 11 | MAXIM_PMBUS_ALERT | ALERT | 9, 11, 13 | J84.7, U4, U8, U7, U9, U10, U13, U18, U46, U47, U49, U63, U95, U96 | MAX15301:9, MAX15303:11, MAX20751:13 |
| P10 | 13 | PL_DDR4_VTERM_EN | EN | 7 | U35 | TPS51200 |
| P11 | 14 | PL_DDR4_VPP2V5_EN | EN | 5 | U38 | MAX15027 |
| P12 | 15 | PS_DIMM_VDDQ_TO_ PSVCCO_ON | ON | C2 | U57 | TPS22924 |
| P13 | 16 | PS_DIMM_SUSPEND_EN | A | 1 | U26 | SN74AUC1G32 OR-gate |
| P14 | 17 | PS_DDR4_VTERM_EN | EN | 7 | U36 | TPS51200 |
| P15 | 18 | PS_DDR4_VPP_2V5_EN | EN | 5 | U39 | MAX15027 |

Table 3-20: I₂C0 Port Expander TCA6416A U97 Connections

| TCA6416A U97 | | Schematic Net Name | Connected To | | | |
|-----------------|------------|-----------------------|--|---------|-----------------------|-------------|
| Pin Name | Pin No. | | Pin Name | Pin No. | Reference Designation | Device |
| SDA | 23 | I ₂ C0_SDA | Refer to connections shown in Figure 3-17 . (TCA6416A U97 Addr. 0x20) | | | |
| SCL | 22 | I ₂ C0_SCL | | | | |
| P00 | 4 | PS_GTR_LANE_SEL0 | SEL | 3 | U125 | PI2DBS6212 |
| P01 | 5 | PS_GTR_LANE_SEL1 | SEL | 3 | U126 | PI2DBS6212 |
| P02 | 6 | PS_GTR_LANE_SEL2 | SEL | 3 | U127 | PI2DBS6212 |
| P03 | 7 | PS_GTR_LANE_SEL3 | SEL | 3 | U128 | PI2DBS6212 |
| P04 | 8 | PCIE_CLK_DIR_SEL | DIR | 5 | U139 | SN74AVC1T45 |

Table 3-20: I₂C Port Expander TCA6416A U97 Connections (Cont'd)

| TCA6416A U97 | | Schematic Net Name | Connected To | | | |
|-----------------|------------|----------------------|--------------|---------|-----------------------|---------------|
| Pin Name | Pin No. | | Pin Name | Pin No. | Reference Designation | Device |
| P05 | 9 | IIC_MUX_RESET_B | RESET_B | 3 | U34, U135 | TCA9548A |
| P06 | 10 | GEM3_EXP_RESET_B | 2A | 3 | U59 | SN74LVC3G07 |
| P10 | 13 | FMC_HPC0_PRSNT_M2C_B | OE | 4 | U27, J5.H2 | NC7SZ66, FMC0 |
| P11 | 14 | FMC_HPC1_PRSNT_M2C_B | OE | 4 | U24, J4.H2 | NC7SZ66, FMC1 |

Table 3-21: I₂C Multiplexer PCA9544A U60 (Addr. 0x75) Connections

| U60 I ₂ C Mux | MUX'd I ₂ C Bus | Reference Designation | Device(s) |
|--------------------------|----------------------------|--|-------------------------------------|
| 0 | PS_PMBUS | U76, U77, U78, U87, U85, U86, U93, U88, U15, U92 | INA226 Op amps |
| 1 | PL_PMBUS | U79, U81, U80, U84, U16, U65, U74, U75 | INA226 Op amps |
| 2 | MAXIM_PMBUS | J84.3, U47, U7, U6, U10, U9, U63, U95, U96, U46, U4, U18, U13, U49 | PMBUS connector, Voltage regulators |
| 3 | SYSMON | U135, U1 | I2C1MUX, MPSoC |

Table 3-22: I₂C U60 (Addr. 0x75) Mux Target Bus Connections

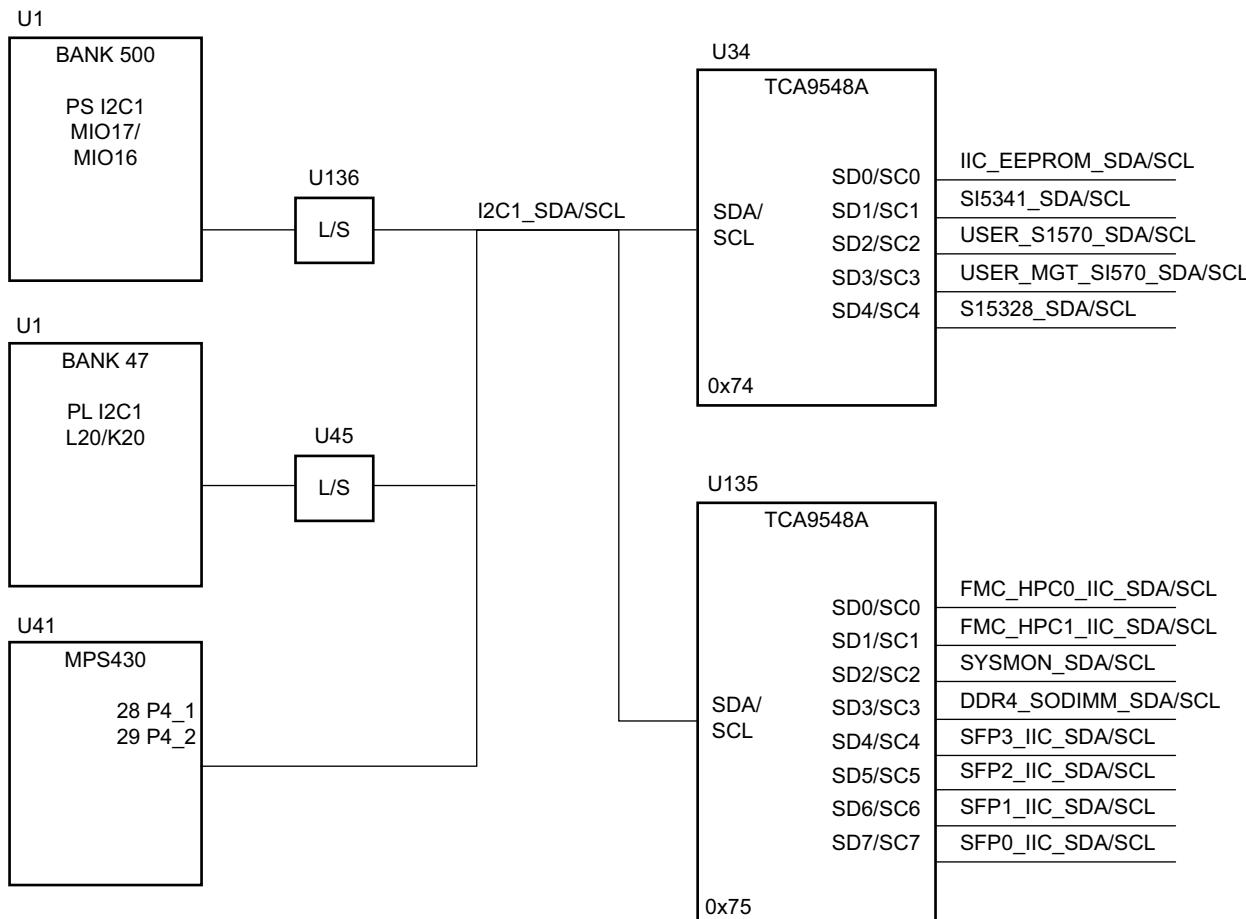
| Reference Designation | Address | Device(s) |
|-----------------------|---------|-----------------------|
| PS_PMBUS | | |
| U76 | 0x40 | INA226 VCCPSINTFP |
| U77 | 0x41 | INA226 VCCPSINTLP |
| U78 | 0x42 | INA226 VCCPSAUX |
| U87 | 0x43 | INA226 VCCPSPLL |
| U85 | 0x44 | INA226 MGTRAVCC |
| U86 | 0x45 | INA226 MGTRAVTT |
| U93 | 0x46 | INA226 VCCO_PSDDR_504 |
| U88 | 0x47 | INA226 VCCOPS |
| U15 | 0x4A | INA226 VCCOPS3 |
| U92 | 0x4B | INA226 VCCPSDDRPLL |
| PL_PMBUS | | |
| U79 | 0x40 | INA226 VCCINT |
| U81 | 0x41 | INA226 VCCBRAM |
| U80 | 0x42 | INA226 VCCAUX |
| U84 | 0x43 | INA226 VCC1V2 |

Table 3-22: I2C0 U60 (Addr. 0x75) Mux Target Bus Connections (Cont'd)

| Reference Designation | Address | Device(s) |
|-----------------------|---------|------------------------------------|
| U16 | 0x44 | INA226 VCC3V3 |
| U65 | 0x45 | INA226 VADJ_FMC |
| U74 | 0x46 | INA226 MGTAVCC |
| U75 | 0x47 | INA226 MGTAVTT |
| MAXIM_PMBUS | | |
| J84 | N/A | PMBUS Conn SDA Pin 3/SCL Pin 1 |
| U47 | 0x13 | MAX15301 VCCINT |
| U7 | 0x14 | MAX15303 VCCBRAM |
| U6 | 0x15 | MAX15303 VCCAUX |
| U10 | 0x16 | MAX15303 VCC1V2 |
| U9 | 0x17 | MAX15303 VCC3V3 |
| U63 | 0x18 | MAX15301 VADJ_FMC |
| U95 | 0x72 | MAX20751 MGTAVCC |
| U96 | 0x73 | MAX20751 MGTAVTT |
| U46 | 0x0A | MAX15301 VCCPSINTFP |
| U4 | 0x0B | MAX15303 VCCPSINTLP |
| U18 | 0x1D | MAX15303 DDR4_DIMM_VDDQ |
| U13 | 0x10 | MAX15303 VCCOPS |
| U49 | 0x1A | MAX15301 UTIL_3V3 |
| U8 | 0x1B | MAX15301 UTIL_5V0 |
| SYSMON | | |
| U1 | N/A | U1 BANK 49 SDA Pin B14/SCL Pin C14 |
| U135 | N/A | TCA9548A Mux I2C1 Bus Port 2 |

I2C1 (MIO 16-17)

The PS-side I2C1 interface provides access to I2C peripherals through a set of I2C switches. The I2C connection is shared with the PL-side and the system controller. Figure 3-18 shows a high-level view of the I2C1 bus connectivity represented in Table 3-23 and Table 3-24. TCA9548A U34 is set to **0x74** and TCA9548A U135 is set to **0x75**.



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Figure 3-18: I2C1 Bus Topology

Table 3-23: I2C1 TCA9548A U34 Multiplexer Connections

| U34 I2C Mux (Addr 0x74) Port | I2C BUS 1 Device(s) | I2C Address |
|------------------------------|-----------------------------|-------------|
| 0 | EEPROM U23 | 0x54 |
| 1 | Si5341 clock U69 | 0x36 |
| 2 | USER Si570 clock U42 | 0x5D |
| 3 | USER MGT Si570 clock U56 | 0x5D |
| 4 | Si5328 (clock recovery) U20 | 0x69 |

Table 3-23: I2C1 TCA9548A U34 Multiplexer Connections (Cont'd)

| U34 I2C Mux (Addr 0x74) Port | I2C BUS 1 Device(s) | I2C Address |
|---|----------------------------|--------------------|
| 5 | No connection | N/A |
| 6 | No connection | N/A |
| 7 | No connection | N/A |

Table 3-24: I2C1 TCA9548A U135 Multiplexer Connections

| U135 I2C Mux (Addr 0x75) Port | I2C BUS 1 Device(s) | I2C Address |
|--|----------------------------|--------------------|
| 0 | FMC HPC_0 | 0x## |
| 1 | FMC HPC_1 | 0x## |
| 2 | SYSMON | 0x32 |
| 3 | DDR4 SODIMM | 0x51 |
| 4 | SFP_3 | 0x50 |
| 5 | SFP_2 | 0x50 |
| 6 | SFP_1 | 0x50 |
| 7 | SFP_0 | 0x50 |

UART0 (MIO 18-19)

This is the primary Zynq UltraScale+ MPSoC PS-side UART interface and is connected to the U40 CP2108 USB-to-Quad-UART bridge with port assignments as listed in [Table 3-25](#). PS-side UART0 is accessed through the U40 CP2108 USB-to-Quad-UART bridge port 0.



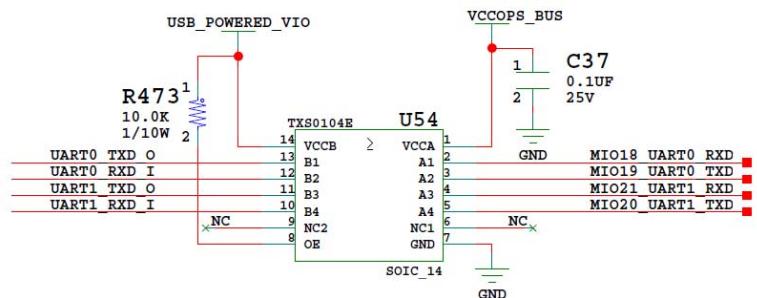
IMPORTANT: Use SiLabs CP210X VCP driver version 6.7.0 or later for proper USB enumeration as identified in [Table 3-25](#).

Table 3-25: CP2108 UART Assignments

| CP2108 U40 | Zynq UltraScale+ MPSoC |
|-------------------|-------------------------------|
| UART0 | PS_UART0 (MIO 18-19) |
| UART1 | PS_UART1 (MIO 20-21) |
| UART2 | PL-UART (HD Bank 49) |
| UART3 | U41 System Controller UART |

UART1 (MIO 20-21)

PS-side UART1 is accessed through the U40 CP2108 USB-to-Quad-UART Bridge port 1. The CP2108 Channel 1 PS-side UART interface circuit is shown in [Figure 3-19](#). The connections from XCZU9EG U1 to CP2108 U40 via L/S U54 are listed in [Table 3-26](#).



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Figure 3-19: CP2108 Channel 1 PS-Side UART Interface

Table 3-26: XCZU9EG U1 to CP2108 U40 Connections via L/S U54

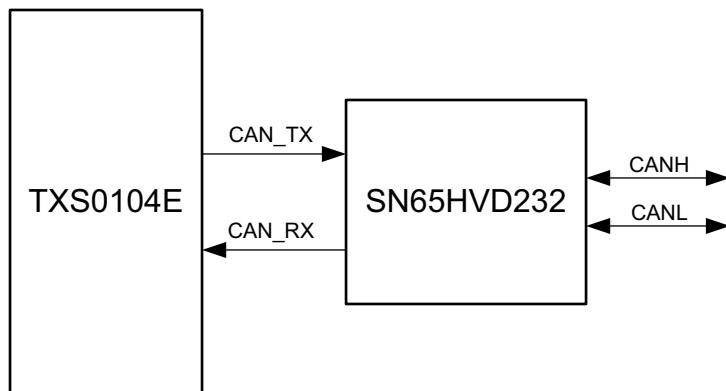
| XCZU9EG U1 | | Schematic Net Name | CP2108 U40 | |
|---------------|---------|--------------------|------------|---------|
| Pin Name | Pin No. | | Pin Name | Pin No. |
| PS_MIO18_AE18 | AE18 | MIO18_UART0_RXD | TX_0 | 57 |
| PS_MIO19_AL17 | AL17 | MIO19_UART0_TXD | RX_0 | 56 |
| PS_MIO21_AF18 | AF18 | MIO21_UART1_RXD | TX_1 | 49 |
| PS_MIO20_AD18 | AD18 | MIO20_UART1_TXD | RX_1 | 48 |

GPIO (MIO 22-23)

PS-side pushbutton SW19 is connected to MIO22 (pin U1.AD20). PS-side LED DS50, placed next to the pushbutton, is connected to MIO23 (pin U1.AD19).

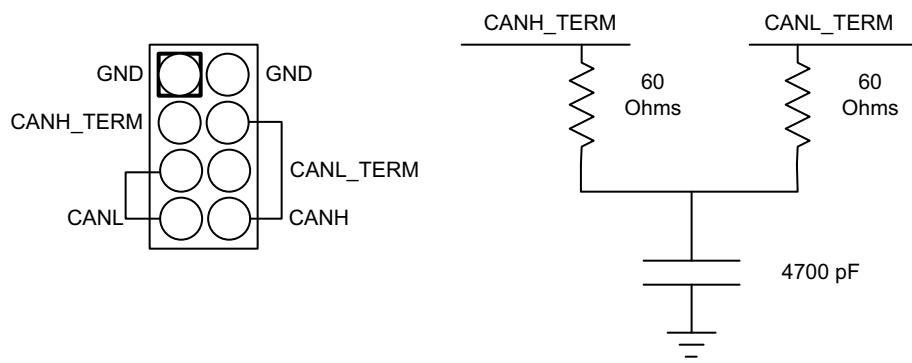
CAN1 (MIO 24-25)

The PS-side CAN bus TX and RX MIO pins go through TXS0104E level-translator U33 and TI SN65HVD232 CAN-bus transceiver U122 before being presented to the user on 0.1 inch centered 8-pin male header J98 (see [Figure 3-20](#) and [Figure 3-21](#)).



X16533-071817

Figure 3-20: PS-Side CAN Bus Interface Diagram



X16534-071817

Figure 3-21: PS-Side Can Bus Interface Connector

PMU GPI (MIO 26)

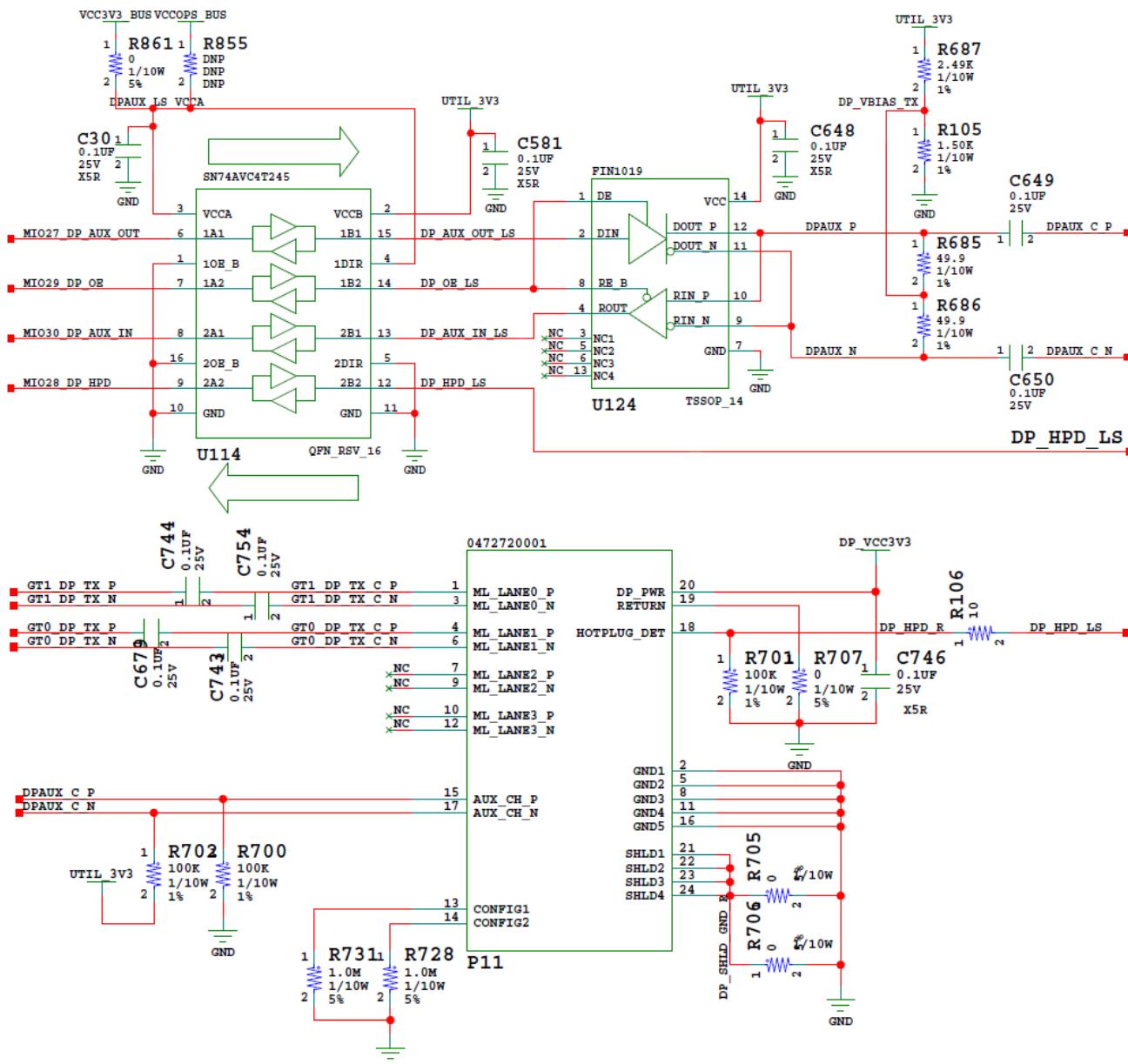
PS-side MIO 26 is reserved as an input to the PMU for indicating a warm boot. PS bank 501 MIO26 (U1.P21) is connected to the I2C0 U61 TCA6416APWR bus expander (port P04 U61.8) through L/S U147 SN74AVC1T45. Refer the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [[Ref 3](#)] for more details about the PMU interface.

DPAUX (MIO 27-30)

The Zynq UltraScale+ MPSoC provides a VESA DisplayPort 1.2 source-only controller that supports up to two lanes of main link data at rates of 1.62 Gb/s, 2.70 Gb/s, or 5.40 Gb/s. The DisplayPort standard defines an auxiliary channel that uses LVDS signaling at a 1 Mb/s data rate, which is translated from single-ended MIO signals to the differential DisplayPort AUX channel, DPAUX (see [Table 3-27](#)). The DisplayPort circuit is shown in [Figure 3-22](#).

Table 3-27: DPAUX/MIO Connections

| XCZU9EG (U1) Pin | Schematic Net Name | Level Shifter U114 | |
|---------------------|--------------------|--------------------|---------|
| | | Pin Name | Pin No. |
| L21 | MIO30_DP_AUX_IN | 2A1 | 8 |
| K22 | MIO29_DP_OE | 1A2 | 7 |
| N21 | MIO28_DP_HPD | 2A2 | 9 |
| M21 | MIO27_DP_AUX_OUT | 1A1 | 6 |



X16547-122118

Figure 3-22: DisplayPort Circuit

PCIe Reset (MIO 31)

The Zynq UltraScale+ MPSoC contains an integrated block for PCI Express interface based on the PCIe base v2.1 specification. The PS-side PCIe reset signal is wired to the PCIe Gen2 x4 root port slot P1. The MIO31 pin is an output for PCIe Root Port mode operation on the ZCU102.

PMU GPO (MIO 32-37)

The platform management unit (PMU) within the Zynq UltraScale+ MPSoC signals power domain changes using the PMU output pins for deep-sleep mode. The Zynq UltraScale+ MPSoC PMU GPO pins are connected to inputs of the MSP430 system controller via TXS0108E level-shifter U141. The connections from MPSoC U1 Bank 501 to MSP430 U41 are listed in [Table 3-28](#).

Table 3-28: XCZU9EG U1 to MSP430 Connections

| XCZU9EG (U1) Pin | Schematic Net Name | MSP430 U41 | |
|---------------------|--------------------|------------|---------|
| | | Pin Name | Pin No. |
| N22 | MIO37_PMU_GPO5 | P1_0 | 13 |
| K23 | MIO36_PMU_GPO4 | P1_1 | 14 |
| P22 | MIO35_PMU_GPO3 | P1_2 | 15 |
| L22 | MIO34_PMU_GPO2 | P1_3 | 16 |
| H23 | MIO33_PMU_GPO1 | P1_4 | 17 |
| H22 | MIO32_PMU_GPO0 | P1_5 | 18 |

Through the I²C0 Bus MPSoC MIO pins, the PMU has access to the board power controllers and power monitors. See [Figure 3-17](#) for more details.

Refer the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3] for more details about the PMU interface.

HDMI Video Output

[[Figure 2-1](#), callout 14]

The ZCU102 board provides a High-Definition Multimedia Interface (HDMI™) video output using a TI SN65DP159RGZ HDMI retimer at U94. The HDMI output is provided on a TE Connectivity 1888811-1 right-angle dual-stacked HDMI type-A receptacle at P7 (upper port). The SN65DP159RGZ device is a dual mode DisplayPort to transition-minimized differential signal (TMDS) retimer supporting digital video interface (DVI) 1.0 and HDMI 1.4b and 2.0 output signals. The SN65DP159RGZ device supports the dual mode standard version 1.1 type 1 and type 2 through the DDC link or AUX channel. The SN65DP159RGZ device supports data rates up to 6 Gb/s per data lane to support Ultra HD (4K x 2K / 60 Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 x 1080 / 60 Hz). The SN65DP159RGZ device can automatically configure itself as a re-driver at data rates <1 Gb/s, or as a retimer at more than this data rate. This feature can be turned off through I²C programming.

The HDMI video transmit/receive block diagram is shown in [Figure 3-23](#). The connections between the codec and the XCZU9EG MPSoC are listed in [Table 3-29](#).

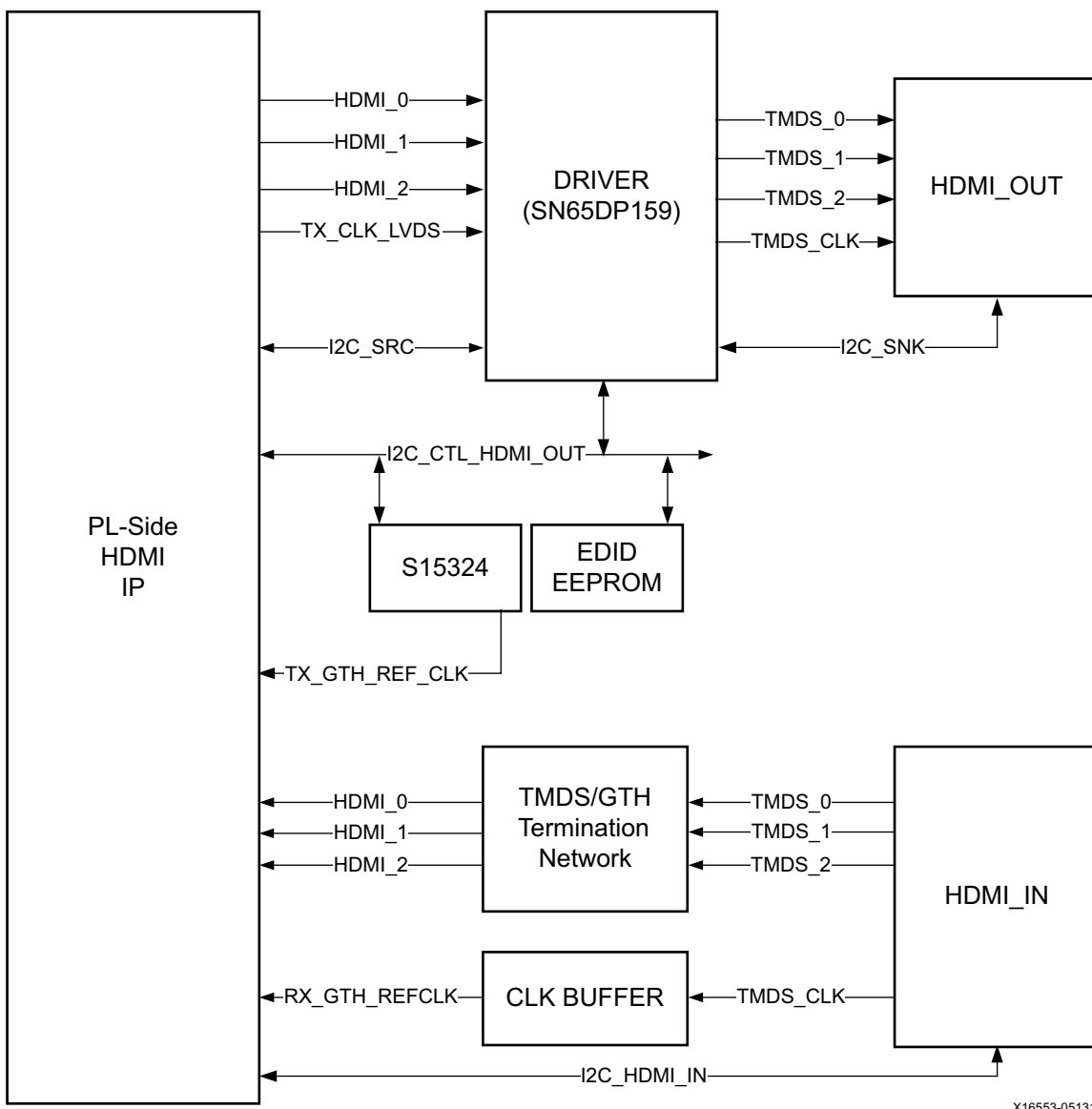


Figure 3-23: HDMI Interface Block Diagram

HDMI Video Input

[Figure 2-1, callout 14]

The ZCU102 board accepts HDMI video input on the TE Connectivity 1888811-1 right-angle dual-stacked HDMI type-A receptacle P7 (lower port). The series capacitor-connected HDMI RX signals are connected to U1 XCZU9F MGTH bank 128.

The ZCU102 HDMI RX interface supports up to 4K 60-Hz resolutions. See the Xilinx HDMI IP documentation for more details about resolutions, color spaces, and optional HDCP features supported by the Zynq® UltraScale+™ device [Ref 4].

The HDMI transmit and receive input interface circuits are shown in Figure 3-24 and Figure 3-25, respectively.

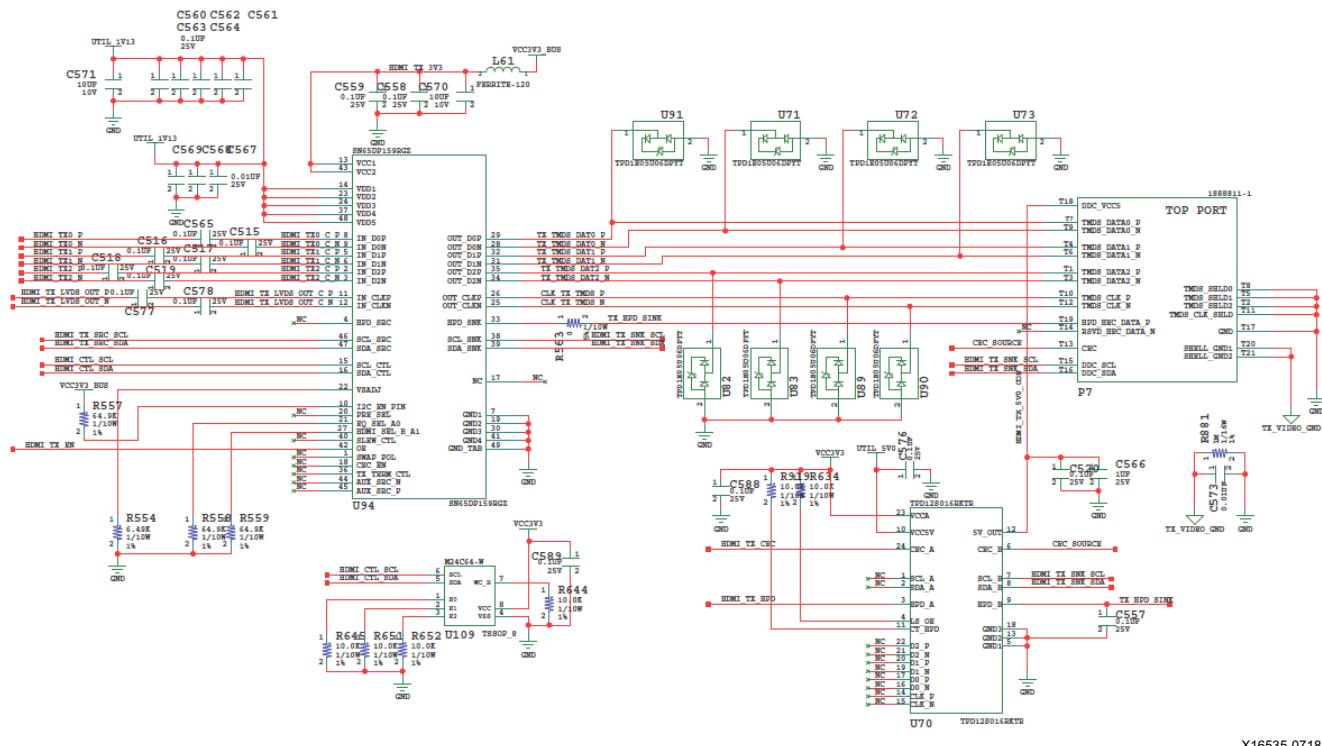


Figure 3-24: HDMI Interface TX Circuit (P7 Upper Port)

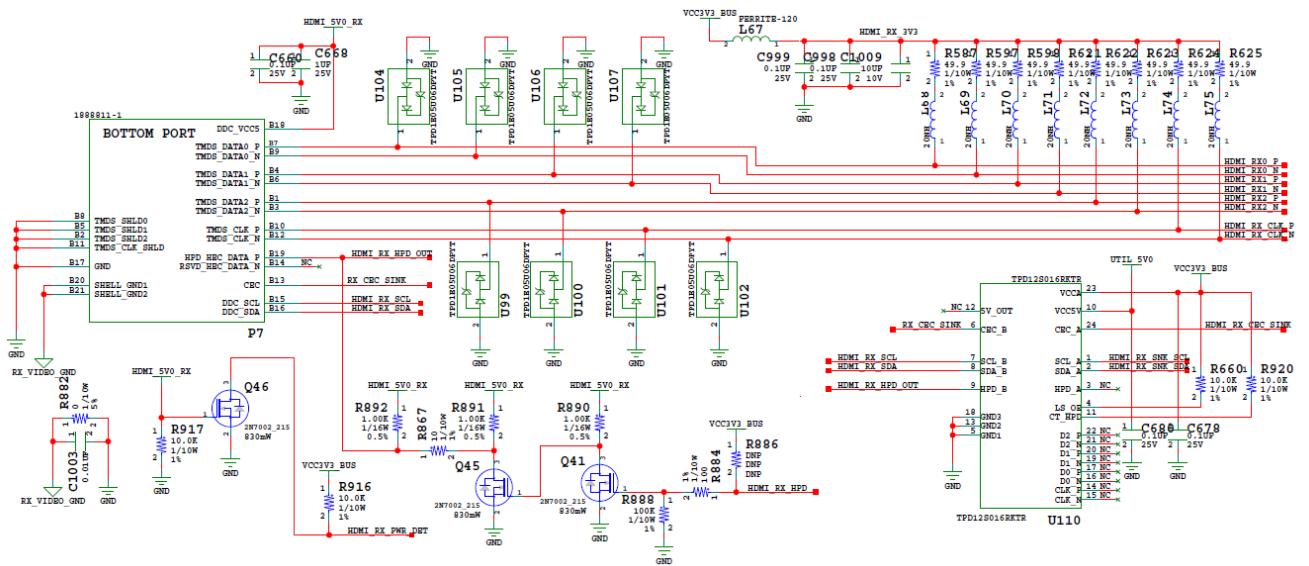


Figure 3-25: HDMI Interface RX Circuit (P7 Lower Port)

Table 3-29: HDMI Retimer U94 Connections to FPGA U1

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Connected Component | | |
|---------------------|---------------------|--------------|---------------------|--------------|-------------------------|
| | | | Pin No. | Pin Name | Device |
| T29 | HDMI_TX0_P | (1) | 8 | IN_D0P | SN65DP159 (U94) |
| T30 | HDMI_TX0_N | (1) | 9 | IN_D0N | |
| R31 | HDMI_TX1_P | (1) | 5 | IN_D1P | |
| R32 | HDMI_TX1_N | (1) | 6 | IN_D1N | |
| P29 | HDMI_TX2_P | (1) | 2 | IN_D2P | |
| P30 | HDMI_TX2_N | (1) | 3 | IN_D2N | |
| AF6 | HDMI_TX_LVDS_OUT_P | LVDS | 11 | IN_CLKP | |
| AG6 | HDMI_TX_LVDS_OUT_N | LVDS | 12 | IN_CLKN | |
| C16 | HDMI_TX_SRC_SCL | LVCMOS33 | 46 | SCL_SRC | |
| D16 | HDMI_TX_SRC_SDA | LVCMOS33 | 47 | SDA_SRC | |
| B15 | HDMI_TX_EN | LVCMOS33 | 42 | OE | |
| F15 | HDMI_CTL_SCL | LVCMOS33 | 15 | SCL_CTL | (2) |
| F16 | HDMI_CTL_SDA | LVCMOS33 | 16 | SDA_CTL | |
| D15 | HDMI_RX_CEC_SINK | LVCMOS33 | 24 | CEC_A | TPD12S016RK (U110) |
| E15 | HDMI_RX_SNK_SCL | LVCMOS33 | 1 | SCL_A | |
| A15 | HDMI_RX_SNK_SDA | LVCMOS33 | 1 | SDA_A | |
| A16 | HDMI_TX_CEC | LVCMOS33 | 24 | CEC_A | TPD12S016RK (U70) |
| B16 | HDMI_TX_HPD | LVCMOS33 | 3 | HPD_A | |
| H12 | HDMI_SI5324_LOL | LVCMOS33 | 18 | LOL | SI5324C (U108) |
| J12 | HDMI_SI5324_RST | LVCMOS33 | 1 | RST_B | |
| F11 | HDMI_SI5324_INT_ALM | LVCMOS33 | 3 | INT_C1B | |
| AG5 | HDMI_REC_CLOCK_C_P | LVDS | 16 | CKIN1_P | |
| AG4 | HDMI_REC_CLOCK_C_N | LVDS | 17 | CKIN1_N | |
| R27 | HDMI_SI5324_OUT_C_P | (1) | 28 | CKOUT1_P | |
| R28 | HDMI_SI5324_OUT_C_N | (1) | 29 | CKOUT1_N | |
| T33 | HDMI_RX0_C_P | (1) | B7 | TMDS_DATA0_P | HDMI BOTTOM PORT(P7) |
| T34 | HDMI_RX0_C_N | (1) | B9 | TMDS_DATA0_N | |
| P33 | HDMI_RX1_C_P | (1) | B4 | TMDS_DATA1_P | |
| P34 | HDMI_RX1_C_N | (1) | B6 | TMDS_DATA1_N | |
| N31 | HDMI_RX2_C_P | (1) | B1 | TMDS_DATA2_P | |
| N32 | HDMI_RX2_C_N | (1) | B3 | TMDS_DATA2_N | |
| N27 | HDMI_RX_CLK_C_P | (1) | B10 | TMDS_CLK_P | |
| N28 | HDMI_RX_CLK_C_N | (1) | B12 | TMDS_CLK_N | |

Table 3-29: HDMI Retimer U94 Connections to FPGA U1 (Cont'd)

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Connected Component | | |
|---------------------|--------------------|--------------|---------------------|----------|--------|
| | | | Pin No. | Pin Name | Device |
| D14 | HDMI_RX_PWR_DET | LVCMS33 | 3 | D | Q46 |
| E14 | HDMI_RX_HPD | LVCMS33 | 1 | G | Q41 |

Notes:

1. U1 MGT (I/O standards do not apply).
2. SN65DP159 (U94), M24C64-W (U109), SI5324C (U108).

HDMI Clock Recovery

[Figure 2-1, callout 40]

The ZCU102 board includes a Silicon Labs Si5324C jitter attenuator U70 (2 kHz - 945 MHz). The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 66 (HDMI_REC_CLOCK_C_P, pin Y8 and HDMI_REC_CLOCK_C_N, pin Y7) for jitter attenuation.

The jitter attenuated clock (HDMI_SI5324_OUT_C_P (U108 pin 28), HDMI_SI5324_OUT_C_N (U108 pin 29) is then routed as a reference clock to GTH Quad 128 inputs MGTRCLK0P (U1 pin R27) and MGTRCLK0N (U1 pin R28).

The Si5324 jitter attenuator is used to generate the reference clock for the HDMI Transmitter Subsystem. When the HDMI transmitter is used standalone, the Si5324 operates in free running mode and uses an external oscillator as the reference. When the HDMI is in pass-through mode, the Si5324 generates a jitter-attenuated reference clock to drive the HDMI Transmitter Subsystem with a phase-aligned version of the HDMI RX Subsystem HDMI RX TMDS clock, so that they are phase aligned. Si5324 clock and jitter enable functions are controlled by HDMI IP. Communication with the Si5324 is available over the HDMI_CTL_SDA/SCL bus connected to the XCZU9 MPSoC U1 PL bank 49. The jitter attenuated clock circuit is shown in [Figure 3-26](#).



IMPORTANT: The Silicon Labs Si5324C U108 pin 1 reset net HDMI_SI5324_RST must be driven High to enable the device. U108 pin 1 net HDMI_SI5324_RST is connected to FPGA U1 bank 50 pin J12.

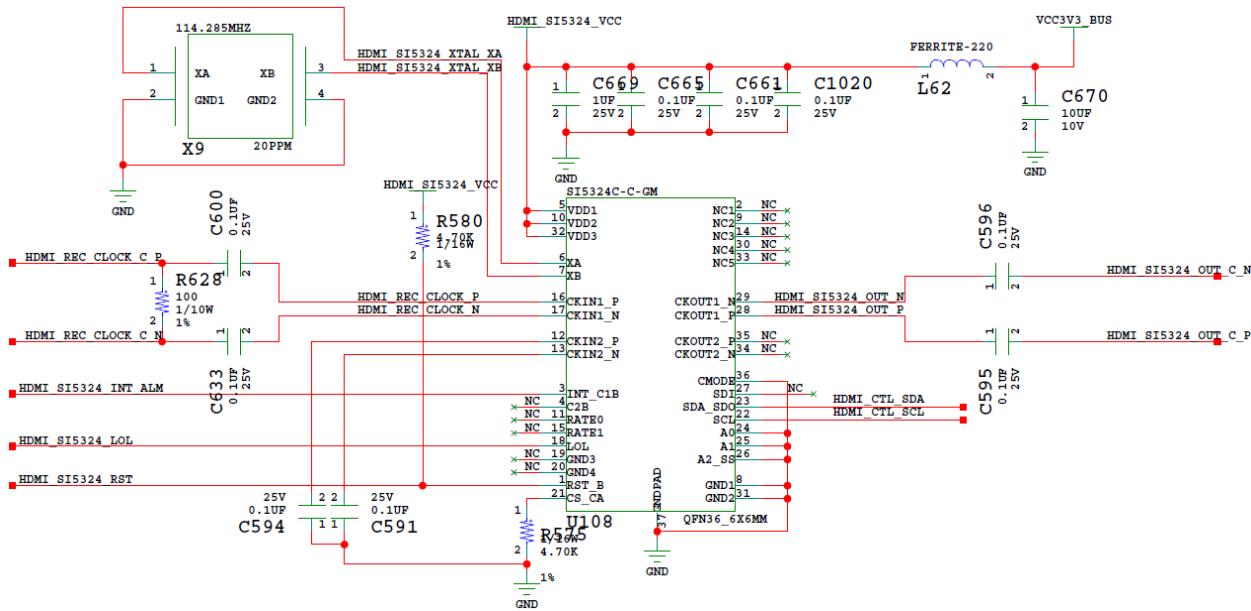


Figure 3-26: HDMI Interface Clock Recovery

For Xilinx HDMI IP details, see the *HDMI 1.4/2.0 Transmitter Subsystem LogiCORE IP Product Guide* (PG235) [Ref 13] and the *HDMI Transmitter and Receiver Subsystem Answer Record 70514* [Ref 14].

See the *HDMI Transmitter and Receiver Subsystem Answer Record 70514* [Ref 14] regarding HDMI-compliant references.

SFP/SFP+ Connector

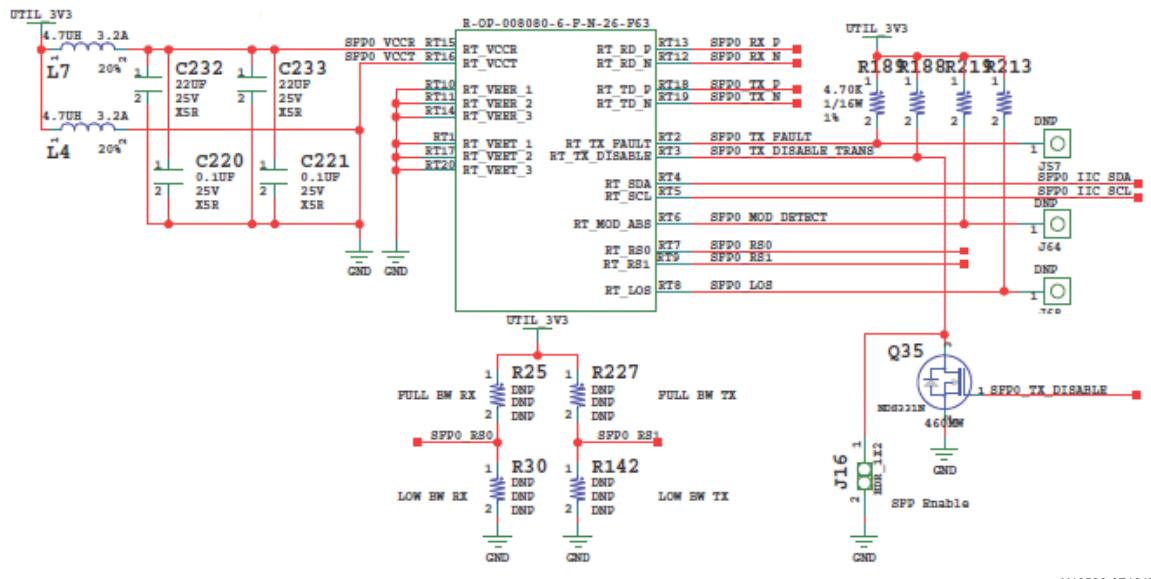
[Figure 2-1, callout 17]

The ZCU102 board contains a small form-factor pluggable (SFP+) 2x2 quad-connector and cage assembly that accepts SFP or SFP+ modules. Figure 3-27 shows a typical SFP+ module connector circuitry implementation. Table 3-30 lists the connections between the connectors and the XCZU9EG MPSoC.

Note: The SFP module RT_TX_DISABLE pin 3:

- RT_TX_DISABLE module pin 3 SFP Enable 2-pin jumper OFF = logic High = SFP TX disabled, allows FPGA control.
- RT_TX_DISABLE module pin 3 SFP Enable 2-pin jumper ON = logic Low = SFP TX enabled, overrides FPGA control.

- Also, note that the SFPx_TX_DISABLE_TRANS default 2-pin jumper strapping is Open which means the SFPx_TX_DISABLE_TRANS net/SFP module pin 3 is pulled High. Hence, disabling the TX output of SFP module by default.
- The default open TX Enable jumpers allow user-FPGA IP to control activation of each modules' SFPx_TX_DISABLE_TRANS pin independently.
- User-FPGA logic can drive the TX control transistor base (net SFPx_TX_DISABLE) logic Low to disable the SFP module TX, or drive it High to enable the SFP module TX (because the TX control transistor is an inverter).



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Figure 3-27: Quad-SFP Interface

Table 3-30: XCZU9EG U1 to P2 SFP+ Module Quad-Connector

| XCZU9EG (U1) Pin | Schematic Net Name | SFP+ Pin | SFP+ Pin Name |
|----------------------------------|--------------------------------|----------|---------------|
| Location Right Top SFP0 | | | |
| E4 | SFP0_TX_P | RT18 | RT_TD_P |
| E3 | SFP0_TX_N | RT19 | RT_TD_N |
| D2 | SFP0_RX_P | RT13 | RT_RD_P |
| D1 | SFP0_RX_N | RT12 | RT_RD_N |
| A12 | SFP0_TX_DISABLE ⁽¹⁾ | RT3 | RT_TX_DISABLE |
| Location Right Lower SFP1 | | | |
| D6 | SFP1_TX_P | RL18 | RL_TD_P |
| D5 | SFP1_TX_N | RL19 | RL_TD_N |
| C4 | SFP1_RX_P | RL13 | RL_RD_P |
| C3 | SFP1_RX_N | RL12 | RL_RD_N |
| A13 | SFP1_TX_DISABLE ⁽¹⁾ | RL3 | RL_TX_DISABLE |

Table 3-30: XCZU9EG U1 to P2 SFP+ Module Quad-Connector (*Cont'd*)

| XCZU9EG (U1) Pin | Schematic Net Name | SFP+ Pin | SFP+ Pin Name |
|---------------------------------|--------------------------------|----------|---------------|
| Location Left Top SFP2 | | | |
| B6 | SFP2_TX_P | LT18 | LT_TD_P |
| B5 | SFP2_TX_N | LT19 | LT_TD_N |
| B2 | SFP2_RX_P | LT13 | LT_RD_P |
| B1 | SFP2_RX_N | LT12 | LT_RD_N |
| B13 | SFP2_TX_DISABLE ⁽¹⁾ | LT3 | LT_TX_DISABLE |
| Location Left Lower SFP3 | | | |
| A8 | SFP3_TX_P | LL18 | LL_TD_P |
| A7 | SFP3_TX_N | LL19 | LL_TD_N |
| A4 | SFP3_RX_P | LL13 | LL_RD_P |
| A3 | SFP3_RX_N | LL12 | LL_RD_N |
| C13 | SFP3_TX_DISABLE ⁽¹⁾ | LL3 | LL_TX_DISABLE |

Notes:

1. SFPx_TX_DISABLE pins should implement the LVCMOS33 I/O standard.

SFP/SFP+ Clock Recovery

[Figure 2-1, callout 11]

The ZCU102 board includes a Silicon Labs Si5328B jitter attenuator U20 (8 kHz - 808 MHz). The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 67 (SFP_REC_CLOCK_C_P, pin R10 and SFP_REC_CLOCK_C_N, pin R9) for jitter attenuation.

The jitter attenuated clock (SFP_SI5328_OUT_C_P (U20 pin 28), SFP_SI5328_OUT_C_N (U20 pin 29)) is then routed as a reference clock to GTH Quad 230 inputs MGTREFCLK1P (U1 pin B10) and MGTREFCLK1N (U1 pin B9).

The primary purpose of this clock is to support synchronous protocols such as CPRI or OBSAI to perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTH transceiver. The system controller configures the SI5328B in free-run mode (see [TI MSP430 System Controller](#)). Enabling the jitter attenuation feature requires additional user programming

from the FPGA through the I²C bus. The jitter attenuated clock circuit is shown in Figure 3-29.

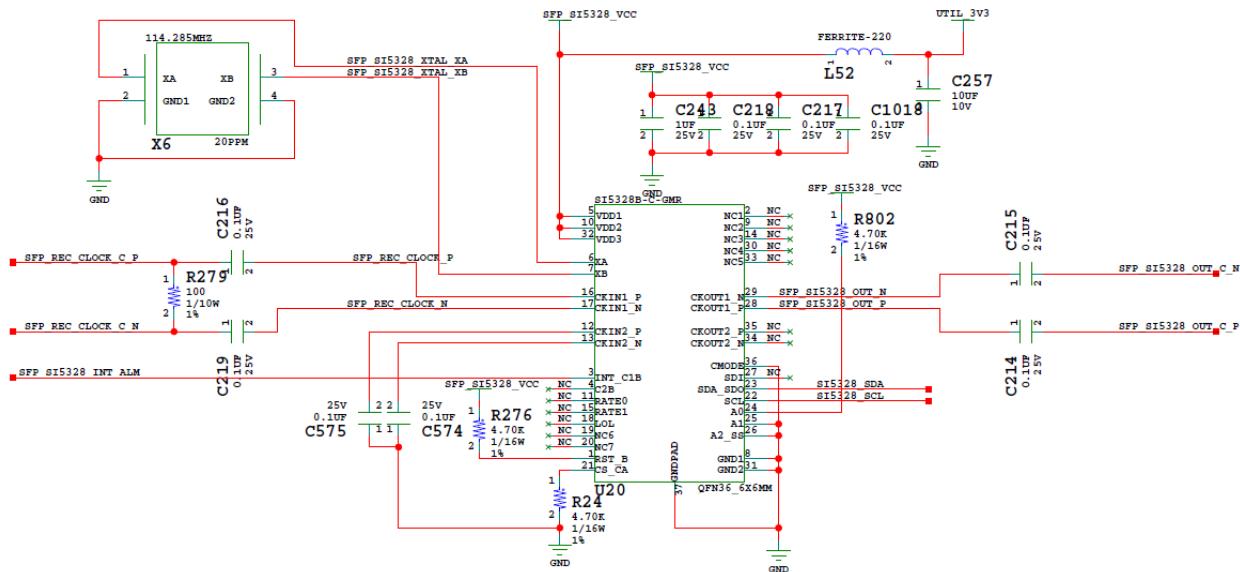


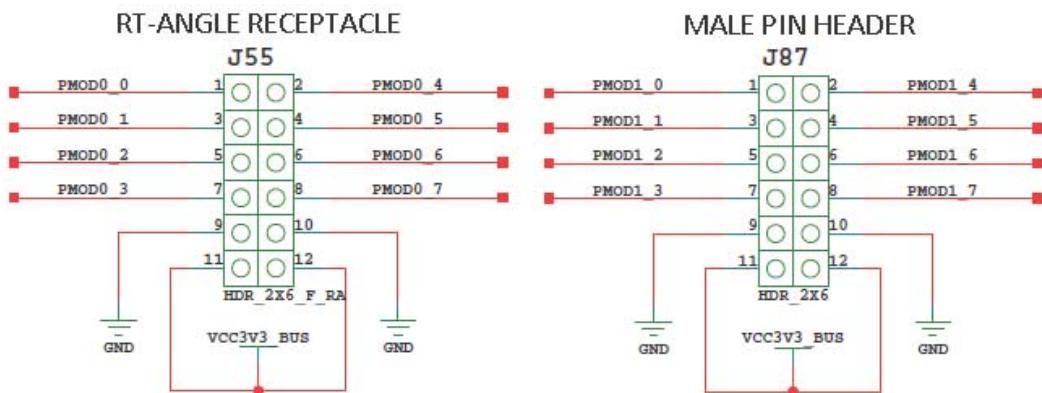
Figure 3-28: SFP/SFP+ Clock Recovery

User PMOD GPIO Headers

[Figure 2-1, callout 19]

The ZCU102 evaluation board supports two PMOD GPIO headers J55 (right-angle female) and J87 (vertical male). The PMOD nets are wired to the XCZU9EG device U1 bank 47.

Figure 3-29 shows the GPIO PMOD headers J55 and J87. Table 3-31 lists the connections between the XCZU9EG MPSoC and the PMOD connectors.



X16537-071817

Figure 3-29: PMOD Connectors

Table 3-31: XCZU9EG U1 to PMOD Connections

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | PMOD Pin |
|---------------------|-----------------------|--------------|----------|
| A20 | PMOD0_0 | LVCMOS33 | J55.1 |
| B20 | PMOD0_1 | LVCMOS33 | J55.3 |
| A22 | PMOD0_2 | LVCMOS33 | J55.5 |
| A21 | PMOD0_3 | LVCMOS33 | J55.7 |
| B21 | PMOD0_4 | LVCMOS33 | J55.2 |
| C21 | PMOD0_5 | LVCMOS33 | J55.4 |
| C22 | PMOD0_6 | LVCMOS33 | J55.6 |
| D21 | PMOD0_7 | LVCMOS33 | J55.8 |
| D20 | PMOD1_0 | LVCMOS33 | J87.1 |
| E20 | PMOD1_1 | LVCMOS33 | J87.3 |
| D22 | PMOD1_2 | LVCMOS33 | J87.5 |
| E22 | PMOD1_3 | LVCMOS33 | J87.7 |
| F20 | PMOD1_4 | LVCMOS33 | J87.2 |
| G20 | PMOD1_5 | LVCMOS33 | J87.4 |
| J20 | PMOD1_6 | LVCMOS33 | J87.6 |
| J19 | PMOD1_7 | LVCMOS33 | J77.8 |

For more information about PMOD connector compatible PMOD modules, see [\[Ref 30\]](#).

Prototype Header

[Figure 2-1, callout 41]

The ZCU102 evaluation board provides a 2x12 male header prototype header J3 which makes ten Bank 50 GPIO connections available. Figure 3-30 shows connector J3 with its MPSoC (U1) Bank 50 connections.

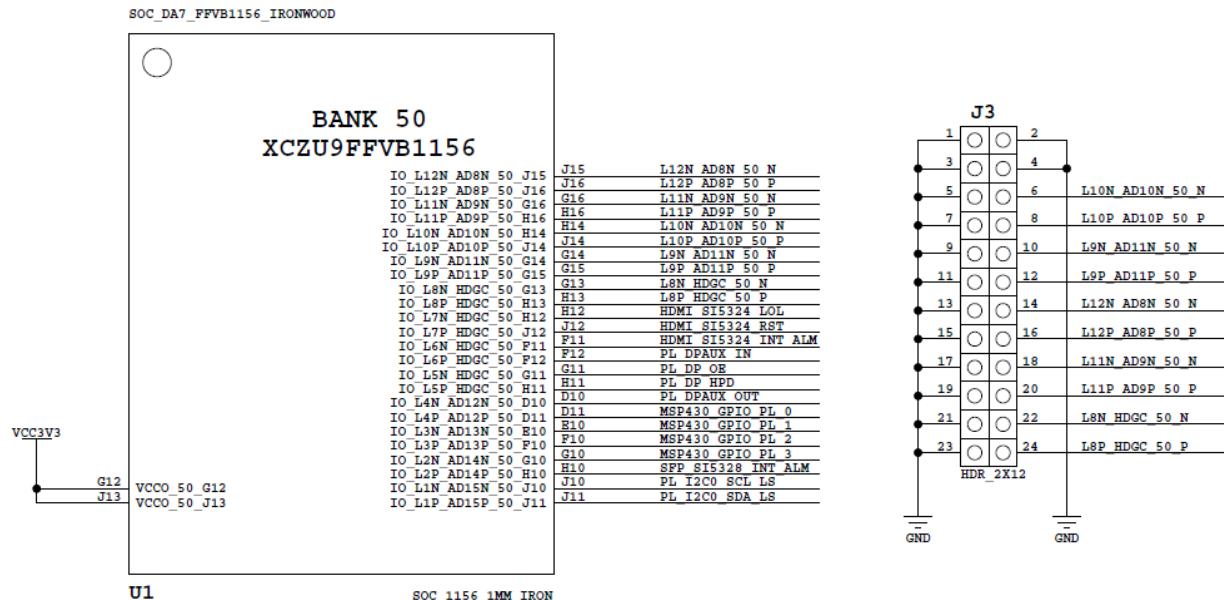


Figure 3-30: Prototype Header J3

The J3 connector to MPSoC connections are listed in Table 3-32.

Table 3-32: Prototype Header J3 Connections to the XCZU9EG MPSoC

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Prototype Header J3 Pin |
|------------------|--------------------|--------------|-------------------------|
| J15 | L12N_AD8N_50_N | LVCMOS33 | 14 |
| J16 | L12N_AD8P_50_P | LVCMOS33 | 16 |
| G16 | L11N_AD9N_50_N | LVCMOS33 | 18 |
| H16 | L11N_AD9P_50_P | LVCMOS33 | 20 |
| H14 | L10N_AD10N_50_N | LVCMOS33 | 6 |
| J14 | L10N_AD10P_50_P | LVCMOS33 | 8 |
| G14 | L9N_AD11N_50_N | LVCMOS33 | 10 |
| G15 | L9N_AD11P_50_P | LVCMOS33 | 12 |
| G13 | L8N_HDGC_50_P | LVCMOS33 | 22 |
| H13 | L8N_HDGC_50_N | LVCMOS33 | 24 |

User I^C0 Receptacle

[Figure 2-1, callout 20]

The ZCU102 evaluation board supports a PMOD 2X6 receptacle (right-angle female) J160. Figure 3-31 shows the I^C0 PMOD receptacle J160. The I^C0 nets are a branch of the I^C0 main bus (see Figure 3-17 and I^C0 (MIO 14-15) for more details).

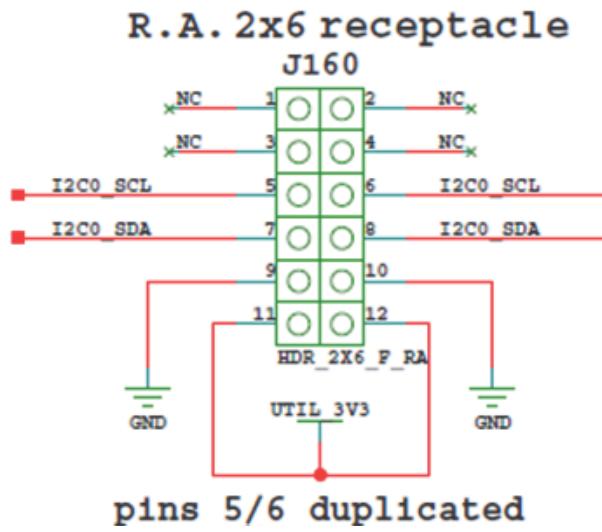


Figure 3-31: J160 PMOD I^C0 R.A. Receptacle

User I/O

[Figure 2-1, callouts 21-23]

The ZCU102 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 21)
 - GPIO_LED[7:0]: DS38, DS37, DS39, DS40, DS41, DS42, DS43, DS44
- 8-position user DIP Switch (callout 22)
 - GPIO_DIP_SW[7:0]: SW13
- Five user pushbuttons and CPU reset switch (callout 23)
 - GPIO_SW_[NESWC]: SW18, SW17, SW16, SW14, SW15
 - CPU_RESET: SW20

Figures [Figure 3-32](#) through [Figure 3-34](#) show the GPIO circuits, and [Table 3-33](#) lists the GPIO to XCZU9EG U1 connections.

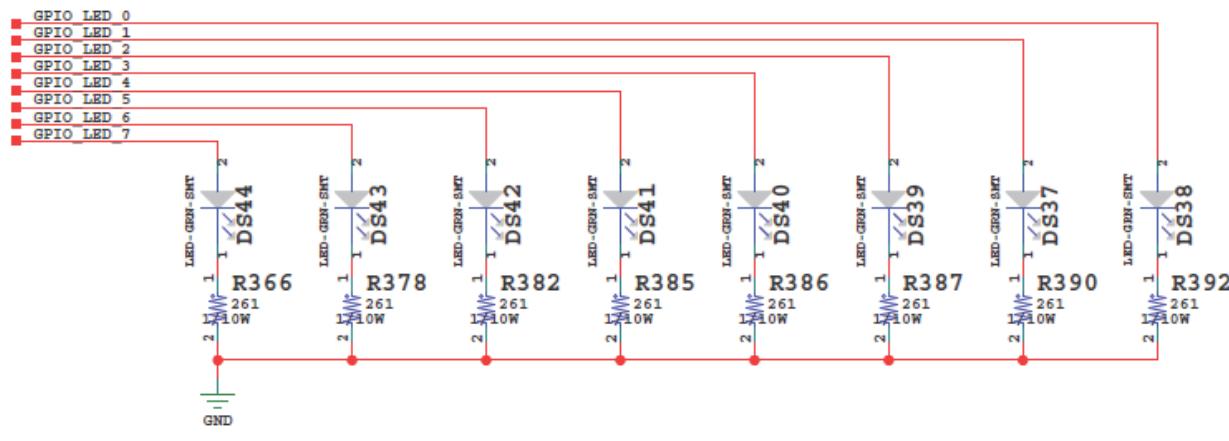


Figure 3-32: GPIO LEDs

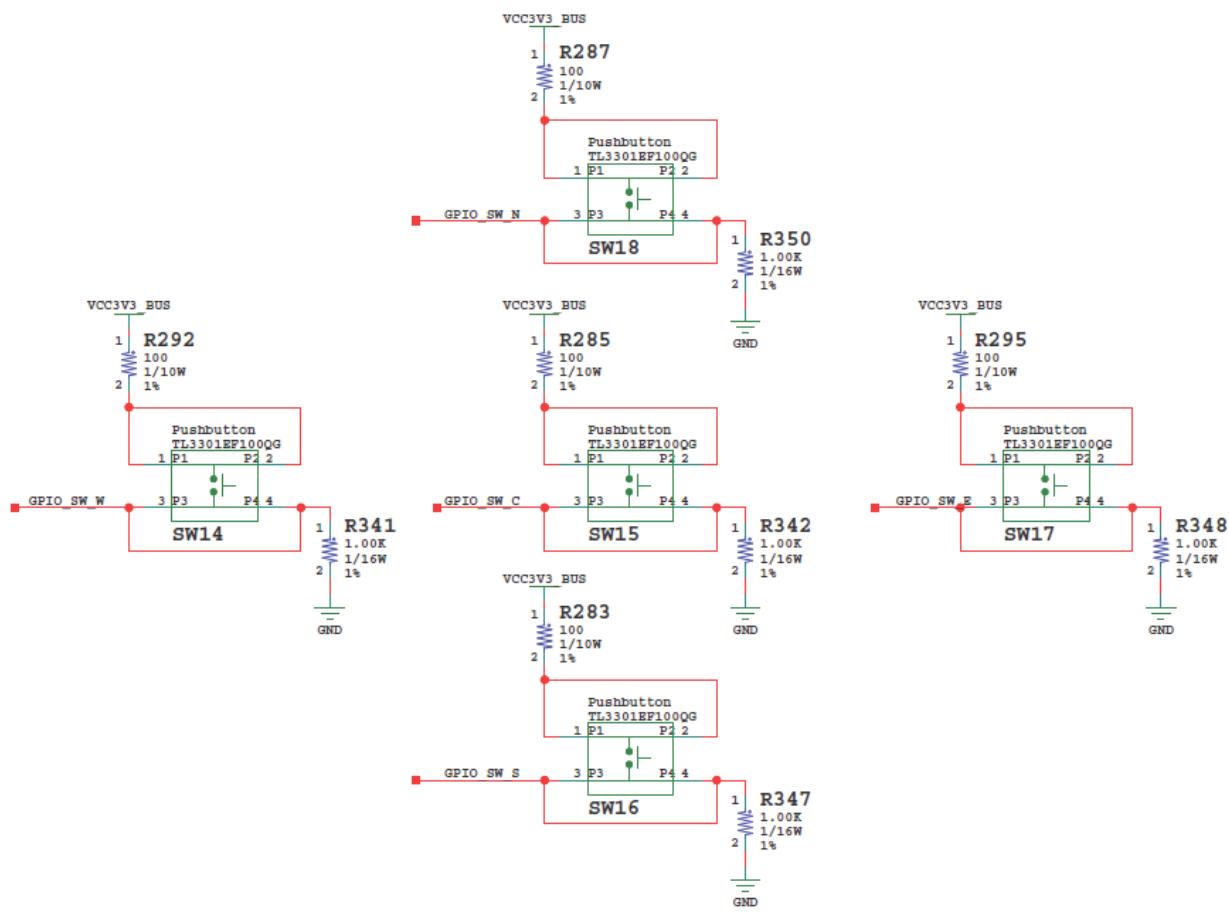
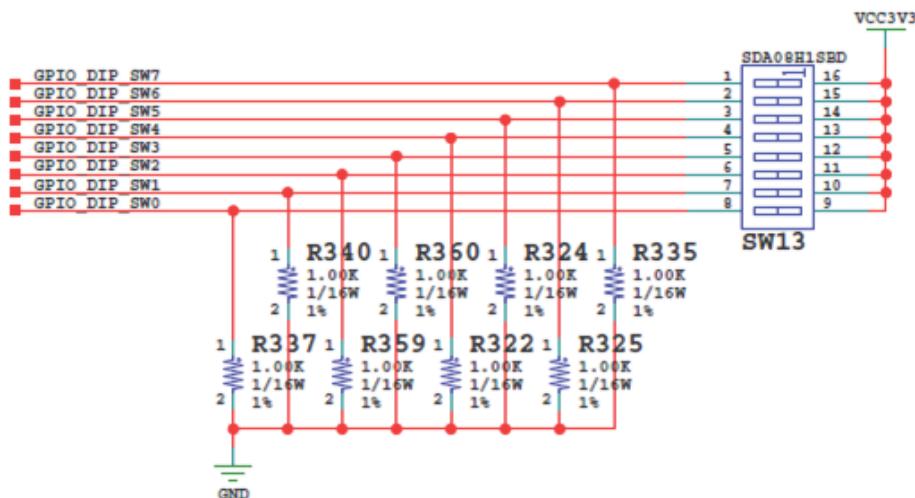


Figure 3-33: GPIO Pushbutton Switches



X16542-071817

Figure 3-34: GPIO 8-Pole DIP Switch

Table 3-33: XCZU9EG U1 to GPIO Connections

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Device |
|--|-----------------------|--------------|--------|
| GPIO LEDs (Active-High) | | | |
| AG14 | GPIO_LED_0 | LVCMOS33 | DS38.2 |
| AF13 | GPIO_LED_1 | LVCMOS33 | DS37.2 |
| AE13 | GPIO_LED_2 | LVCMOS33 | DS39.2 |
| AJ14 | GPIO_LED_3 | LVCMOS33 | DS40.2 |
| AJ15 | GPIO_LED_4 | LVCMOS33 | DS41.2 |
| AH13 | GPIO_LED_5 | LVCMOS33 | DS42.2 |
| AH14 | GPIO_LED_6 | LVCMOS33 | DS43.2 |
| AL12 | GPIO_LED_7 | LVCMOS33 | DS44.2 |
| Directional Pushbuttons (Active-High) | | | |
| AG15 | GPIO_SW_N | LVCMOS33 | SW18.3 |
| AE14 | GPIO_SW_E | LVCMOS33 | SW17.3 |
| AF15 | GPIO_SW_W | LVCMOS33 | SW14.3 |
| AE15 | GPIO_SW_S | LVCMOS33 | SW16.3 |
| AG13 | GPIO_SW_C | LVCMOS33 | SW15.3 |
| CPU Reset Pushbutton (Active-High) | | | |
| AM13 | CPU_RESET | LVCMOS33 | SW20.3 |
| GPIO DIP SW (Active-High) | | | |
| AN14 | GPIO_DIP_SW0 | LVCMOS33 | SW13.8 |

Table 3-33: XCZU9EG U1 to GPIO Connections (Cont'd)

| XCZU9EG (U1) Pin | Schematic Net Name | I/O Standard | Device |
|---------------------|-----------------------|--------------|--------|
| AP14 | GPIO_DIP_SW1 | LVCMS33 | SW13.7 |
| AM14 | GPIO_DIP_SW2 | LVCMS33 | SW13.6 |
| AN13 | GPIO_DIP_SW3 | LVCMS33 | SW13.5 |
| AN12 | GPIO_DIP_SW4 | LVCMS33 | SW13.4 |
| AP12 | GPIO_DIP_SW5 | LVCMS33 | SW13.3 |
| AL13 | GPIO_DIP_SW6 | LVCMS33 | SW13.2 |
| AK13 | GPIO_DIP_SW7 | LVCMS33 | SW13.1 |

Power and Status LEDs

[Figure 2-1, callout 21]

Table 3-34 defines the power and status LEDs. For user-controlled LEDs see [User I/O](#).

Table 3-34: Power and Status LEDs

| Reference Designator | Schematic Net Name | LED Color | Description |
|-------------------------|----------------------|-----------|---|
| DS1 | FPGA_INIT_B | Green/Red | Green: FPGA initialization was successful Red: FPGA initialization is in progress |
| DS2 | VCC12_SW | Green | 12VDC Power ON |
| DS3 | VCCAUX_PGOOD | Green | VCCAUX 1.8VDC Power ON |
| DS4 | VCC3V3_PGOOD | Green | VCC3V3 3.3VDC Power ON |
| DS5 | VCCINT_PGOOD | Green | VCCINT 0.85VDC Power ON |
| DS6 | VADJ_FMC_PGOOD | Green | VADJ_FMC 1.8VDC (Nom.) Power ON |
| DS7 | VCC1V2_PGOOD | Green | VCC1V2 1.2VDC Power ON |
| DS8 | VCCBRAM_PGOOD | Green | VCCBRAM 0.85VDC Power ON |
| DS9 | MGTAVTT_PGOOD | Green | MGTAVTT 1.2VDC Power ON |
| DS10 | MGTAVCC_PGOOD | Green | MGTAVCC 0.9VDC Power ON |
| DS11 | VCCPSINTFP_PGOOD | Green | VCCPSINTFP 0.85VDC Power ON |
| DS12 | MGTRAVCC_PGOOD | Green | MGTRAVCC 0.85VDC Power ON |
| DS13 | MGTVCVCAUX_PGOOD | Green | MGTVCVCAUX 1.81VDC Power ON |
| DS14 | VCCPSAUX_PGOOD | Green | VCCPSAUX 1.81VDC Power ON |
| DS15 | VCCPSPLL_PGOOD | Green | VCCPSPLL 1.2VDC Power ON |
| DS16 | VCCPSINTLP_PGOOD | Green | VCCPSINTLP 0.85VDC Power ON |
| DS17 | DDR4_DIMM_VDDQ_PGOOD | Green | DDR4_DIMM_VDDQ 1.2VDC Power ON |
| DS18 | MGTRAVTT_PGOOD | Green | MGTRAVTT 1.81VDC Power ON |

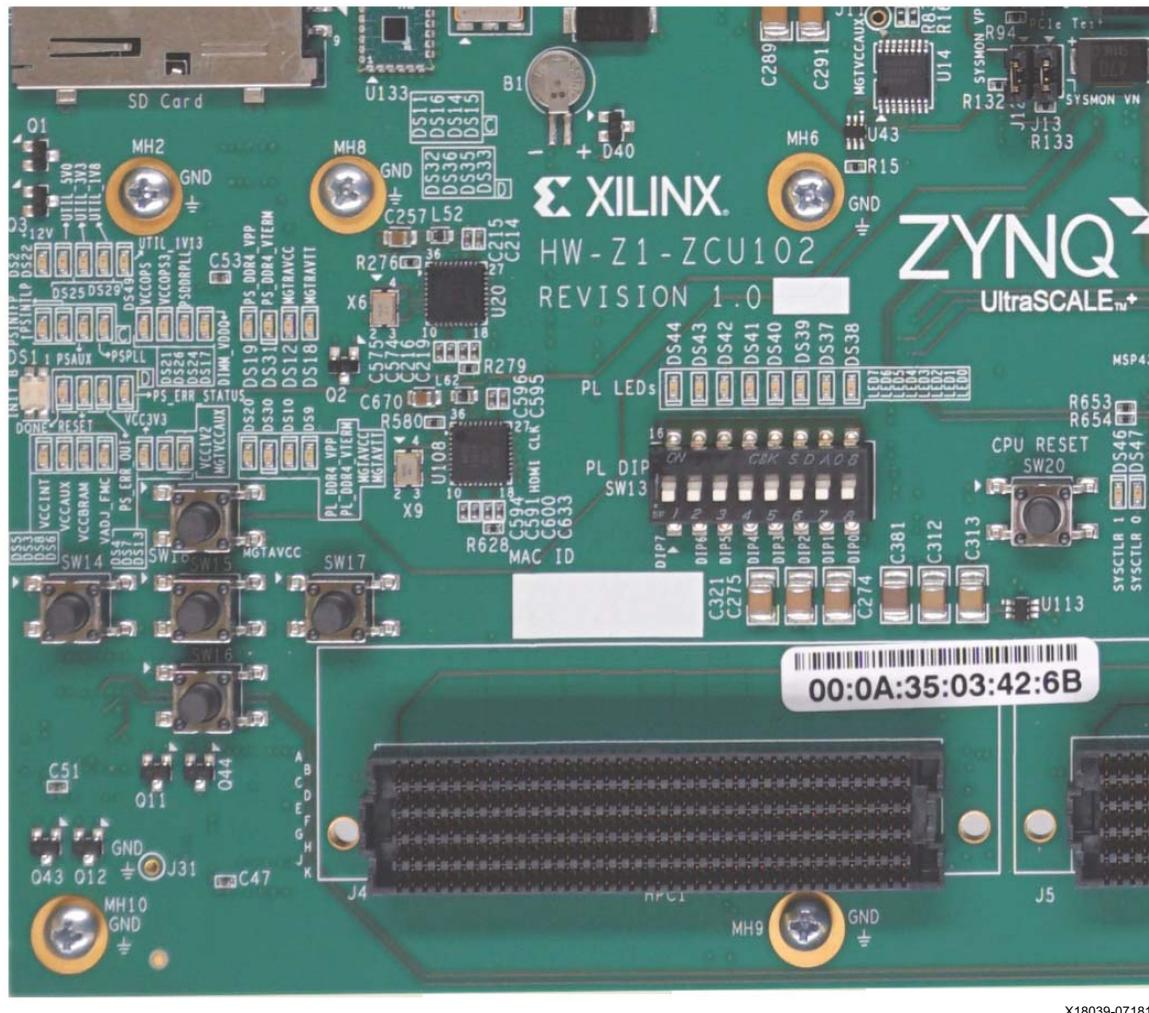
Table 3-34: Power and Status LEDs (Cont'd)

| Reference Designator | Schematic Net Name | LED Color | Description |
|----------------------|------------------------------|-----------|--|
| DS19 | PS_DDR4_VPP_2V5 | Green | PS_DDR4_VPP_2V5 2.5VDC Power ON |
| DS20 | PL_DDR4_VPP_2V6 | Green | PL_DDR4_VPP_2V5 2.5VDC Power ON |
| DS21 | VCCOPS_PGOOD | Green | VCCOPS 1.80VDC Power ON |
| DS22 | UTIL_5V0_PGOOD | Green | UTIL_5V0 5VDC Power ON |
| DS24 | VCCPSSDDRPLL_PGOOD | Green | VCCPSSDDRPLL 1.81VDC Power ON |
| DS25 | UTIL_3V3_PGOOD | Green | UTIL_3V3 3.3VDC Power ON |
| DS26 | VCCOPS3_PGOOD | Green | VCCOPS3 1.81VDC Power ON |
| DS27 | ENET_LED_1 | Green | EHPY U98 1000BASE-T link is established |
| DS29 | UTIL_1V8 | Green | UTIL_1V8 1.8VDC Power ON |
| DS30 | PL_DDR4_VTERM_0V60_PGOOD | Green | PL_DDR4_VTERM 0.6VDC Power ON |
| DS31 | PS_DDR4_VTERM_0V60_PGOOD | Green | PS_DDR4_VTERM 0.6VDC Power ON |
| DS32 | DONE | Green | MPSoC U1 bit file download is complete |
| DS33 | PS_ERR_STATUS ⁽¹⁾ | Green | PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status. |
| DS34 | DP_VCC3V3 | Green | Display Port 3.3VDC Power ON |
| DS35 | PS_ERR_OUT ⁽¹⁾ | Red | PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU. |
| DS36 | POR_RST_B | Red | POR U22 asserts RST_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_goes low, or MR is asserted. |
| DS37-DS44 | GPIO_LED_1, GPIO_LED_[0:2:7] | Green | USER GPIO LEDs |
| DS46 | MSP430_LED1 | Green | MSP430 U41 GPIO LED |
| DS47 | MSP430_LED0 | Green | MSP430 U41 GPIO LED |
| DS49 | UTIL_1V13_PG | Green | UTIL_1V13 1.13VDC Power ON |
| DS50 | MIO23_LED | Green | MPSoC U1 Bank 500 GPIO LED |
| DS51 | MIC2544_U121_FLG | Green | PS USB 3.0 ULPI VBUS Power Error |

Notes:

- See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3] for more information about Zynq UltraScale+ MPSoC configuration pins.

Figure 3-35 shows the power and status LEDs.



X18039-071817

Figure 3-35: Power and Status LEDs

GTH Transceivers

[Figure 2-1, callout 1]

The Zynq UltraScale+ MPSoC has 24 GTH gigabit transceivers (16.3 Gb/s capable) on the PL-side.

The GTH transceivers in the XCZU9EG device are grouped into four channels referred to as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTH Quad of interest. There are six GTH Quads on the ZCU102 board with connectivity as shown here:

- Two of the GTH transceivers are wired to the FMC0 HPC connector (J5)
- Two of the GTH transceivers are wired to the FMC1 HPC connector (J4)

- One of the GTH transceivers is wired to SFP/SFP+ Quad-Module connector (P2)
- One GTH transceiver is wired to the HDMI retimer U94 and a set of GTH SMAs

Quad 128:

- MGTREFCLK0 - HDMI_SI5324_OUT_C_P/N
- MGTREFCLK1 - HDMI_RX_CLK_C_P/N
- Contains 3 GTH transceivers allocated to HDMI_TX/RX[0:2]_P/N
- Contains 1 GTH transceiver allocated to a set of SMA connectors (SMA_MGT_TX and RX P/N)

Quad 129:

- MGTREFCLK0 - USER_MGT_SI570_CLOCK1_C_P/N
- MGTREFCLK1 - USER_SMA_MGT_CLOCK_C_P/N
- Contains 4 GTH transceivers allocated to FMC_HPC1_DP[4:7]_C2M/M2C_P/N

Quad 130:

- MGTREFCLK0 - FMC_HPC1_GBTCLK0_M2C_P/N
- MGTREFCLK1 - FMC_HPC1_GBTCLK1_M2C_P/N
- Contains 4 GTH transceivers allocated to FMC_HPC1_DP[0:3]_C2M/M2C_P/N

Quad 228:

- MGTREFCLK0 - FMC_HPC0_GBTCLK1_M2C_P/N
- MGTREFCLK1 - Not connected
- Contains 4 GTH transceivers allocated to FMC_HPC0_DP[4:7]_C2M/M2C_P/N

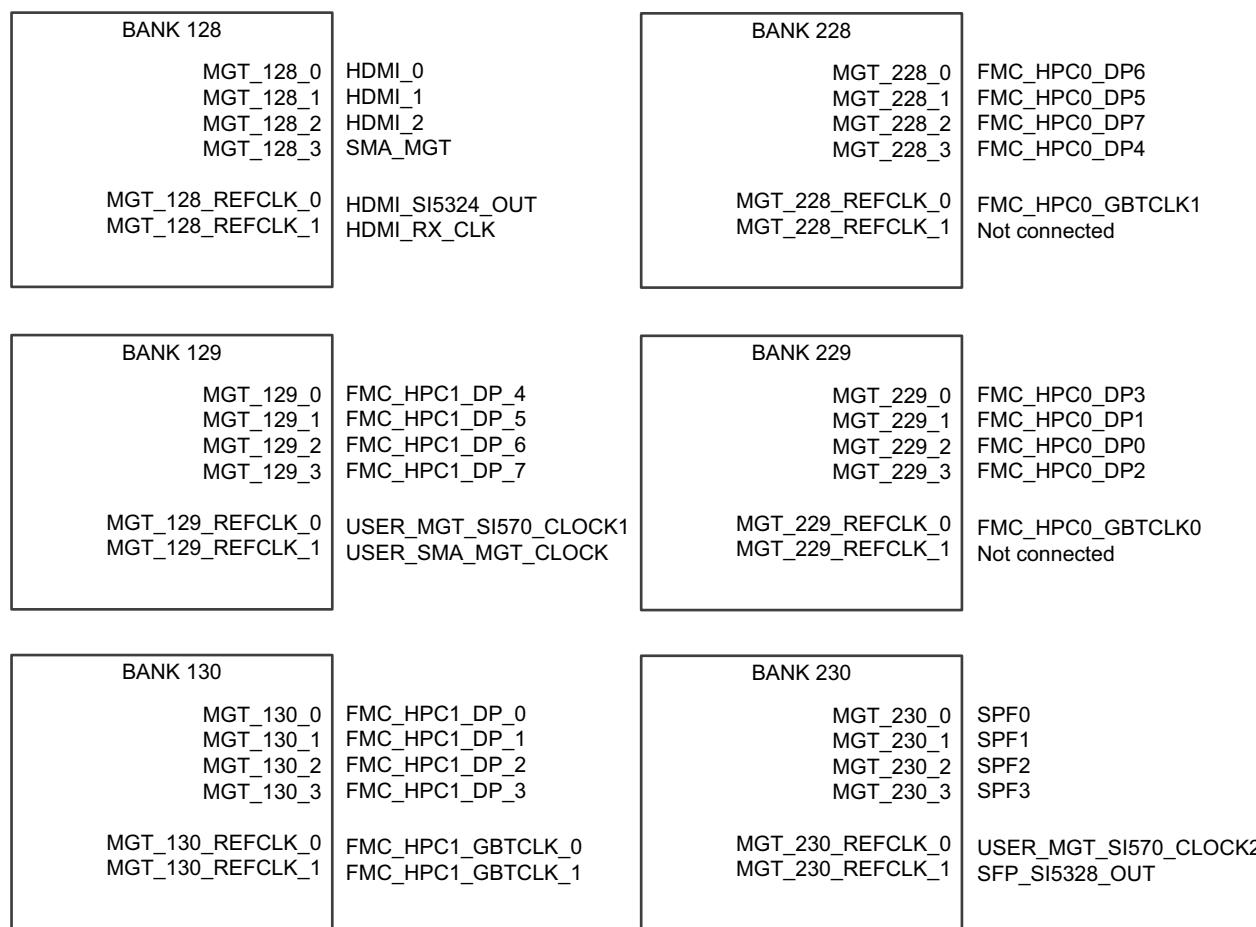
Quad 229:

- MGTREFCLK0 - FMC_HPC0_GBTCLK0_M2C_P/N
- MGTREFCLK1 - Not connected
- Contains 4 GTH transceivers allocated to FMC_HPC0_DP[0:3]_C2M/M2C_P/N

Quad 230:

- MGTREFCLK0 - USER_MGT_SI570_CLOCK2_C_P/N
- MGTREFCLK1 - SFP_SI5328_OUT_C_P/N
- Contains 4 GTH transceivers allocated to SFP[0:3]_TX/RX_P/N

GTH usage on the ZCU102 is shown in Figure 3-36.



X16543-071917

Figure 3-36: GTH Bank Assignments

FMC HPC_0

Eight (8) MGTs in a common FPGA column are provided by PL-side MGT banks 228 and 229. Available MGT reference clocks include the FMC defined GBT clocks 0 and 1 for HPC_0, a programmable Si570 clock, and a jitter attenuated recovered clock from a Si5328. The MGT reference clocks are located in adjacent MGT banks, 228, 229, and 230.

FMC HPC_1

Eight (8) MGTs in a common FPGA column are provided by PL-side MGT banks 129 and 130. Available MGT reference clocks include the FMC defined GBT clocks 0 and 1 for HPC_1, a programmable Si570 clock, and a user provided SMA clock. The MGT reference clocks are located in adjacent MGT banks, 128, 129, and 130.

SFP+

Four (4) PL-side GTH transceivers in Bank 230 are provided for the quad SFP+ interface. Available GTH reference clocks include a programmable Si570 clock, and a jitter attenuated recovered clock from a Si5328.

SFP+ modules typically provide an I2C based control interface. This I2C interface is accessible for each individual SFP+ module through the I2C multiplexer topology on the ZCU102.

HDMI

Three (3) PL-side GTH transceivers are dedicated for HDMI source and sink. Modes supported are 4K, 2K at 60 f/s and 2160p60. External circuitry for interfacing TMDS signals with the GTH transceivers is required.

SMA

One (1) MGT in Bank 128 is provided on a SMA connector pair. Available MGT clocks include a user provided MGT reference clock on an SMA connector pair, and a programmable Si570 clock. [Table 3-35](#) lists GTH bank 128 connections.

Table 3-35: ZCU102 GTH Bank 128 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|-----------------------------------|--------------|--------------|--|
| | | | Pin No. | Pin Name | Device |
| T29 | MGTHTXP0_128 | HDMI_TX0_P | 8 | IN_D0P | TI SN65DP159RGZ HDMI RETIMER U94 |
| T30 | MGTHTXN0_128 | HDMI_TX0_N | 9 | IN_D0N | |
| R31 | MGTHTXP1_128 | HDMI_TX1_P | 5 | IN_D1P | |
| R32 | MGTHTXN1_128 | HDMI_TX1_N | 6 | IN_D1N | |
| P29 | MGTHTXP2_128 | HDMI_TX2_P | 2 | IN_D2P | |
| P30 | MGTHTXN2_128 | HDMI_TX2_N | 3 | IN_D2N | |
| T33 | MGTHRXP0_128 | HDMI_RX0_C_P ⁽¹⁾ | B7 | TMDS_DATA0_P | MOLEX HDMI BOTTOM PORT P7 |
| T34 | MGTHRxn0_128 | HDMI_RX0_C_N ⁽¹⁾ | B9 | TMDS_DATA0_N | |
| P33 | MGTHRXP1_128 | HDMI_RX1_C_P ⁽¹⁾ | B4 | TMDS_DATA1_P | |
| P34 | MGTHRxn1_128 | HDMI_RX1_C_N ⁽¹⁾ | B6 | TMDS_DATA1_N | |
| N31 | MGTHRXP2_128 | HDMI_RX2_C_P ⁽¹⁾ | B1 | TMDS_DATA2_P | |
| N32 | MGTHRxn2_128 | HDMI_RX2_C_N ⁽¹⁾ | B3 | TMDS_DATA2_N | |
| N27 | MGTREFCLK1P_18 | HDMI_RX_CLK_C_P ⁽¹⁾ | B10 | TMDS_CLK_P | SMA J71 |
| N28 | MGTREFCLK1N_128 | HDMI_RX_CLK_C_N ⁽¹⁾ | B12 | TMDS_CLK_N | |
| M29 | MGTHTXP3_128 | SMA_MGT_TX_P | 1 | SIG | SMA J71 |
| M30 | MGTHTXN3_128 | SMA_MGT_TX_N | 1 | SIG | SMA J72 |

Table 3-35: ZCU102 GTH Bank 128 Interface Connections (Cont'd)

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|------------------------------------|--------------|----------|----------------|
| | | | Pin No. | Pin Name | Device |
| M33 | MGTHRXP3_128 | SMA_MGT_RX_C_P ⁽¹⁾ | 1 | SIG | SMA J69 |
| M34 | MGTHRxn3_128 | SMA_MGT_RX_C_N ⁽¹⁾ | 1 | SIG | SMA J70 |
| R27 | MGTREFCLK0P_128 | HDMI_SI5324_OUT_C_P ⁽¹⁾ | 28 | CKOUT1_P | SI5324C JITTER |
| R28 | MGTREFCLK0N_128 | HDMI_SI5324_OUT_C_N ⁽¹⁾ | 29 | CKOUT1_N | ATTEN. U108 |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-36 lists GTH bank 129 connections.

Table 3-36: ZCU102 GTH Bank 129 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|--|--------------|-----------|-------------------------------------|
| | | | Pin No. | Pin Name | Device |
| K29 | MGTHXP0_129 | FMC_HPC1_DP4_C2M_P | A34 | DP4_C2M_P | FMC HPC1 J4 |
| K30 | MGHTXN0_129 | FMC_HPC1_DP4_C2M_N | A35 | DP4_C2M_N | |
| L31 | MGTHRXP0_129 | FMC_HPC1_DP4_M2C_P | A14 | DP4_M2C_P | |
| L32 | MGTHRxn0_129 | FMC_HPC1_DP4_M2C_N | A15 | DP4_M2C_N | |
| J31 | MGTHXP1_129 | FMC_HPC1_DP5_C2M_P | A38 | DP5_C2M_P | |
| J32 | MGHTXN1_129 | FMC_HPC1_DP5_C2M_N | A39 | DP5_C2M_N | |
| K33 | MGTHRXP1_129 | FMC_HPC1_DP5_M2C_P | A18 | DP5_M2C_P | |
| K34 | MGTHRxn1_129 | FMC_HPC1_DP5_M2C_N | A19 | DP5_M2C_N | |
| H29 | MGTHXP2_129 | FMC_HPC1_DP6_C2M_P | B36 | DP6_C2M_P | |
| H30 | MGHTXN2_129 | FMC_HPC1_DP6_C2M_N | B37 | DP6_C2M_N | |
| H33 | MGTHRXP2_129 | FMC_HPC1_DP6_M2C_P | B16 | DP6_M2C_P | |
| H34 | MGTHRxn2_129 | FMC_HPC1_DP6_M2C_N | B17 | DP6_M2C_N | |
| G31 | MGTHXP3_129 | FMC_HPC1_DP7_C2M_P | B32 | DP7_C2M_P | |
| G32 | MGHTXN3_129 | FMC_HPC1_DP7_C2M_N | B33 | DP7_C2M_N | |
| F33 | MGTHRXP3_129 | FMC_HPC1_DP7_M2C_P | B12 | DP7_M2C_P | SI53340 ⁽³⁾ BUFF. U51 |
| F34 | MGTHRxn3_129 | FMC_HPC1_DP7_M2C_N | B13 | DP7_M2C_N | |
| L27 | MGTREFCLK0P_129 | USER_MGT_SI570_CLOCK1_C_P ⁽¹⁾ | 11 | Q1_P | |
| L28 | MGTREFCLK0N_129 | USER_MGT_SI570_CLOCK1_C_N ⁽¹⁾ | 12 | Q1_N | |
| J27 | MGTREFCLK1P_129 | USER_SMA_MGT_CLOCK_C_P ⁽¹⁾ | 1 | SIG | J79 |

Table 3-36: ZCU102 GTH Bank 129 Interface Connections (Cont'd)

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|---------------------------------------|--------------|----------|--------|
| | | | Pin No. | Pin Name | Device |
| J28 | MGTREFCLK1N_129 | USER_SMA_MGT_CLOCK_C_N ⁽¹⁾ | 1 | SIG | J80 |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.
3. U51 buffer driven by SI570 U56 (156.250 MHz default)

Table 3-37 lists GTH bank 130 connections.

Table 3-37: ZCU102 GTH Bank 130 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|---|--------------|---------------|-------------|
| | | | Pin No. | Pin Name | Device |
| F29 | MGTHTXP0_130 | FMC_HPC1_DP0_C2M_P | C2 | DP0_C2M_P | FMC HPC1 J4 |
| F30 | MGTHTXN0_130 | FMC_HPC1_DP0_C2M_N | C3 | DP0_C2M_N | |
| E31 | MGTHRXP0_130 | FMC_HPC1_DP0_M2C_P | C6 | DP0_M2C_P | |
| E32 | MGTHRNXN0_130 | FMC_HPC1_DP0_M2C_N | C7 | DP0_M2C_N | |
| D29 | MGTHTXP1_130 | FMC_HPC1_DP1_C2M_P | A22 | DP1_C2M_P | |
| D30 | MGTHTXN1_130 | FMC_HPC1_DP1_C2M_N | A23 | DP1_C2M_N | |
| D33 | MGTHRXP1_130 | FMC_HPC1_DP1_M2C_P | A2 | DP1_M2C_P | |
| D34 | MGTHRNXN1_130 | FMC_HPC1_DP1_M2C_N | A3 | DP1_M2C_N | |
| B29 | MGTHTXP2_130 | FMC_HPC1_DP2_C2M_P | A26 | DP2_C2M_P | |
| B30 | MGTHTXN2_130 | FMC_HPC1_DP2_C2M_N | A27 | DP2_C2M_N | |
| C31 | MGTHRXP2_130 | FMC_HPC1_DP2_M2C_P | A6 | DP2_M2C_P | |
| C32 | MGTHRNXN2_130 | FMC_HPC1_DP2_M2C_N | A7 | DP2_M2C_N | |
| A31 | MGTHTXP3_130 | FMC_HPC1_DP3_C2M_P | A30 | DP3_C2M_P | |
| A32 | MGTHTXN3_130 | FMC_HPC1_DP3_C2M_N | A31 | DP3_C2M_N | |
| B33 | MGTHRXP3_130 | FMC_HPC1_DP3_M2C_P | A10 | DP3_M2C_P | |
| B34 | MGTHRNXN3_130 | FMC_HPC1_DP3_M2C_N | A11 | DP3_M2C_N | |
| G27 | MGTREFCLK0P_130 | FMC_HPC1_GBTCLK0_M2C_C_P ⁽¹⁾ | D4 | GBTCLK0_M2C_P | |
| G28 | MGTREFCLK0N_130 | FMC_HPC1_GBTCLK0_M2C_C_N ⁽¹⁾ | D5 | GBTCLK0_M2C_N | |
| E27 | MGTREFCLK1P_130 | FMC_HPC1_GBTCLK1_M2C_C_P ⁽¹⁾ | B20 | GBTCLK1_M2C_P | |
| E28 | MGTREFCLK1N_130 | FMC_HPC1_GBTCLK1_M2C_C_N ⁽¹⁾ | B21 | GBTCLK1_M2C_N | |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-38 lists GTH bank 228 connections.

Table 3-38: ZCU102 GTH Bank 228 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|---|--------------|---------------|-------------|
| | | | Pin No. | Pin Name | Device |
| R4 | MGTHTXP0_228 | FMC_HPC0_DP6_C2M_P | B36 | DP6_C2M_P | FMC HPC0 J5 |
| R3 | MGTHTXN0_228 | FMC_HPC0_DP6_C2M_N | B37 | DP6_C2M_N | |
| T2 | MGTHRXP0_228 | FMC_HPC0_DP6_M2C_P | B16 | DP6_M2C_P | |
| T1 | MGTHRxn0_228 | FMC_HPC0_DP6_M2C_N | B17 | DP6_M2C_N | |
| P6 | MGTHTXP1_228 | FMC_HPC0_DP5_C2M_P | A38 | DP5_C2M_P | |
| P5 | MGTHTXN1_228 | FMC_HPC0_DP5_C2M_N | A39 | DP5_C2M_N | |
| P2 | MGTHRXP1_228 | FMC_HPC0_DP5_M2C_P | A18 | DP5_M2C_P | |
| P1 | MGTHRxn1_228 | FMC_HPC0_DP5_M2C_N | A19 | DP5_M2C_N | |
| N4 | MGTHTXP2_228 | FMC_HPC0_DP7_C2M_P | B32 | DP7_C2M_P | |
| N3 | MGTHTXN2_228 | FMC_HPC0_DP7_C2M_N | B33 | DP7_C2M_N | |
| M2 | MGTHRXP2_228 | FMC_HPC0_DP7_M2C_P | B12 | DP7_M2C_P | |
| M1 | MGTHRxn2_228 | FMC_HPC0_DP7_M2C_N | B13 | DP7_M2C_N | |
| M6 | MGTHTXP3_228 | FMC_HPC0_DP4_C2M_P | A34 | DP4_C2M_P | |
| M5 | MGTHTXN3_228 | FMC_HPC0_DP4_C2M_N | A35 | DP4_C2M_N | |
| L4 | MGTHRXP3_228 | FMC_HPC0_DP4_M2C_P | A14 | DP4_M2C_P | |
| L3 | MGTHRxn3_228 | FMC_HPC0_DP4_M2C_N | A15 | DP4_M2C_N | |
| L8 | MGTREFCLK0P_228 | FMC_HPC0_GBTCLK1_M2C_C_P ⁽¹⁾ | B20 | GBTCLK1_M2C_P | |
| L7 | MGTREFCLK0N_228 | FMC_HPC0_GBTCLK1_M2C_C_N ⁽¹⁾ | B21 | GBTCLK1_M2C_N | |
| J8 | MGTREFCLK1P_228 | NC | NA | NA | N/A |
| J7 | MGTREFCLK1N_228 | NC | NA | NA | N/A |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-39 lists GTH bank 229 connections.

Table 3-39: ZCU102 GTH Bank 229 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|---|--------------|---------------|-------------|
| | | | Pin No. | Pin Name | Device |
| K6 | MGTHTXP0_229 | FMC_HPC0_DP3_C2M_P | A30 | DP3_C2M_P | FMC HPC0 J5 |
| K5 | MGTHTXN0_229 | FMC_HPC0_DP3_C2M_N | A31 | DP3_C2M_N | |
| K2 | MGTHRXP0_229 | FMC_HPC0_DP3_M2C_P | A10 | DP3_M2C_P | |
| K1 | MGTHRxn0_229 | FMC_HPC0_DP3_M2C_N | A11 | DP3_M2C_N | |
| H6 | MGTHTXP1_229 | FMC_HPC0_DP1_C2M_P | A22 | DP1_C2M_P | |
| H5 | MGTHTXN1_229 | FMC_HPC0_DP1_C2M_N | A23 | DP1_C2M_N | |
| J4 | MGTHRXP1_229 | FMC_HPC0_DP1_M2C_P | A2 | DP1_M2C_P | |
| J3 | MGTHRxn1_229 | FMC_HPC0_DP1_M2C_N | A3 | DP1_M2C_N | |
| G4 | MGTHTXP2_229 | FMC_HPC0_DP0_C2M_P | C2 | DP0_C2M_P | |
| G3 | MGTHTXN2_229 | FMC_HPC0_DP0_C2M_N | C3 | DP0_C2M_N | |
| H2 | MGTHRXP2_229 | FMC_HPC0_DP0_M2C_P | C6 | DP0_M2C_P | |
| H1 | MGTHRxn2_229 | FMC_HPC0_DP0_M2C_N | C7 | DP0_M2C_N | |
| F6 | MGTHTXP3_229 | FMC_HPC0_DP2_C2M_P | A26 | DP2_C2M_P | |
| F5 | MGTHTXN3_229 | FMC_HPC0_DP2_C2M_N | A27 | DP2_C2M_N | |
| F2 | MGTHRXP3_229 | FMC_HPC0_DP2_M2C_P | A6 | DP2_M2C_P | |
| F1 | MGTHRxn3_229 | FMC_HPC0_DP2_M2C_N | A7 | DP2_M2C_N | |
| G8 | MGTREFCLK0P_229 | FMC_HPC0_GBTCLK0_M2C_C_P ⁽¹⁾ | D4 | GBTCLK0_M2C_P | |
| G7 | MGTREFCLK0N_229 | FMC_HPC0_GBTCLK0_M2C_C_N ⁽¹⁾ | D5 | GBTCLK0_M2C_N | |
| E8 | MGTREFCLK1P_229 | NC | NA | NA | NA |
| E7 | MGTREFCLK1N_229 | NC | NA | NA | NA |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-40 lists GTH bank 230 connections.

Table 3-40: ZCU102 GTH Bank 230 Interface Connections

| XCZU9EG (U1) Pin | XCZU9EG (U1) Pin Name | Schematic Net Name ⁽²⁾ | Connected To | | |
|---------------------|--------------------------|--|--------------|-----------|-------------------------------------|
| | | | Pin No. | Pin Name | Device |
| E4 | MGTHTXP0_230 | SFP0_TX_P | RT18 | RT_TD_P | QUAD SFP P2 |
| E3 | MGTHTXN0_230 | SFP0_RX_N | RT19 | RT_TD_N | |
| D2 | MGTHRXP0_230 | SFP0_RX_P | RT13 | RT_RD_P | |
| D1 | MGTHRxn0_230 | SFP0_RX_N | RT12 | RT_RD_N | |
| D6 | MGTHTXP1_230 | SFP1_TX_P | RL18 | RL_TD_P | |
| D5 | MGTHTXN1_230 | SFP1_RX_N | RL19 | RL_TD_N | |
| C4 | MGTHRXP1_230 | SFP1_RX_P | RL13 | RL_RD_P | |
| C3 | MGTHRxn1_230 | SFP1_RX_N | RL12 | RL_RD_N | |
| B6 | MGTHTXP2_230 | SFP2_TX_P | LT18 | LT_TD_P | |
| B5 | MGTHTXN2_230 | SFP2_RX_N | LT19 | LT_TD_N | |
| B2 | MGTHRXP2_230 | SFP2_RX_P | LT13 | LT_RD_P | |
| B1 | MGTHRxn2_230 | SFP2_RX_N | LT12 | LT_RD_N | |
| A8 | MGTHTXP3_230 | SFP3_TX_P | LL18 | LL_TD_P | |
| A7 | MGTHTXN3_230 | SFP3_RX_N | LL19 | LL_TD_N | |
| A4 | MGTHRXP3_230 | SFP3_RX_P | LL13 | LL_RD_P | |
| A3 | MGTHRxn3_230 | SFP3_RX_N | LL12 | LL_RD_N | |
| C8 | MGTREFCLK0P_230 | USER_MGT_SI570_CLOCK2_C_P ⁽¹⁾ | 13 | Q2_P | SI53340 ⁽³⁾ BUFF. U51 |
| C7 | MGTREFCLK0N_230 | USER_MGT_SI570_CLOCK2_C_N ⁽¹⁾ | 14 | Q2_N | |
| B10 | MGTREFCLK1P_230 | SFP_SI5328_OUT_C_P ⁽¹⁾ | 28 | CLKOUT1_P | SI5328B U20 |
| B9 | MGTREFCLK1N_230 | SFP_SI5328_OUT_C_N ⁽¹⁾ | 29 | CLKOUT1_N | |

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.
3. U51 buffer driven by SI570 U56 (156.250 MHz default).

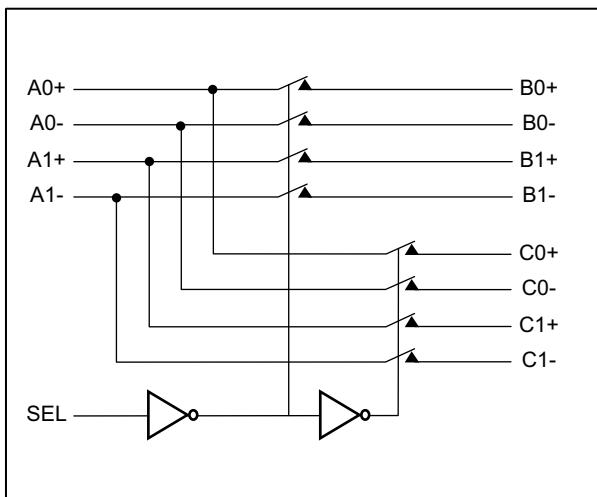
For additional information on GTH transceivers, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 7]. For additional information about UltraScale FPGA PCIe functionality, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156) [Ref 8]. Additional information about the PCI Express standard is available at the PCI Express website [Ref 26].

PS-Side: GTR Transceivers

[Figure 2-1, callout 1]

The PS-side GTR transceivers are shared through on-board bidirectional 2:1 multiplexer/de-multiplexer switches U125-U128 (Pericom PI2DBS6212 [Ref 27]) capable of 6.5 Gb/s operation (see Figure 3-37).

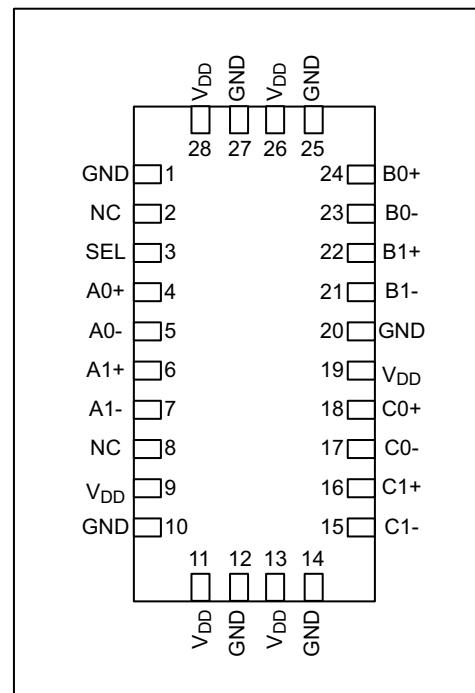
Block Diagram



Truth Table

| Function | SEL |
|----------|-----|
| A to B | L |
| A to C | H |

Pin Description



X16616-071817

Figure 3-37: Pericom GTR Switch Block Diagram

The external GT-switch selection must be set by the user to ensure consistency with the ZU9EG's internal GT interconnect matrix (ICM) settings. There are PS-side MIO GPIO(s) that control the Pericom GT switch settings via PS-side I2C0 and the external GPIO port expander.

The functionality of each ZU9EG GTR lane is controlled through the MPSoC's ICM and is defined in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3]. Table 3-41 lists the interconnect matrix (ICM). Table 3-42 lists the interconnect matrix settings and GTR lane functionality.

Table 3-41: XCZU9EG Interconnect Matrix

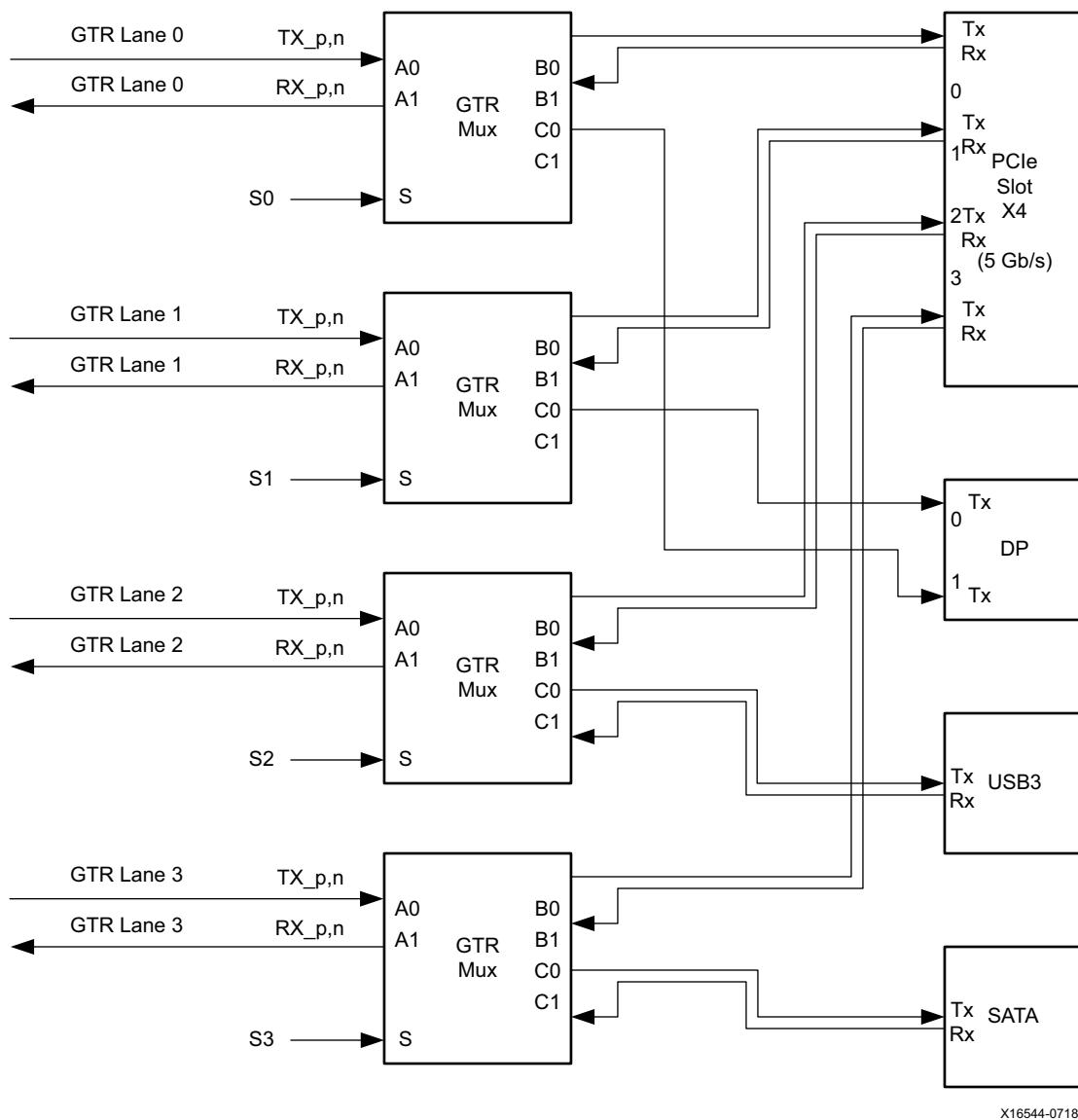
| Protocol | PHY Lane 0 | PHY Lane 1 | PHY Lane 2 | PHY Lane 3 |
|-------------|------------|------------|------------|------------|
| PCIe | PCIe.0 | PCIe.0 | PCIe.0 | PCIe.0 |
| SATA | SATA.0 | SATA.1 | SATA.0 | SATA.1 |
| USB0 | USB0 | USB0 | USB0 | |
| USB1 | | | | USB1 |
| DisplayPort | DP.1 | DP.0 | DP.1 | DP.0 |
| SGMII0 | SGMII0 | | | |
| SGMII1 | | SGMII1 | | |
| SGMII2 | | | SGMII2 | |
| SGMII3 | | | | SGMII3 |

Table 3-42: Interconnect Matrix Settings and GTR Lane Functionality

| Protocol | Values |
|-------------|--------|
| Power down | 3`h0 |
| PCIe | 3`h1 |
| SATA | 3`h2 |
| USB | 3`h3 |
| DisplayPort | 3`h4 |
| SGMII | 3`h5 |

The GTR selections provided with GT switch topology shown in Figure 3-38 are:

1. PCIe Gen2/1 x4
2. DisplayPort (2-Lanes), USB, SATA
3. PCIe Gen2/1 x2, USB, SATA
4. PCIe Gen2/1 x1, DisplayPort (1-Lane), USB, SATA



X16544-071817

Figure 3-38: GTR External Switch Connectivity

The ICM settings for lane functionality must be set consistent with the external U125 Pericom PI2DBS6212 GTR multiplexer settings to provide appropriate functionality on the connectors wired to the PS-side GTR transceivers. The external GTR multiplexer selection is controlled by the PS-side I2C0 GPIO port expander (U97) connected to the multiplexer's "S" input. S = 0 connects the A input to the B output, whereas S = 1, connects the A input to the

C output. The "S" select logic is implemented with GPIO pins to support the settings listed in [Table 3-43](#).

Table 3-43: Supported GTR Connector Functionality

| SEL (S3,2,1,0) | ICM Settings (Lane 0,1,2, 3) | PCIe Connector | DP Connector | USB Connector | SATA Connector |
|-------------------|-----------------------------------|----------------|--------------|---------------|----------------|
| 0000 | PCIe.0, PCIe.1, PCIe.2, PCIe.3 | PCIe Gen2 x4 | N.C. | N.C. | N.C. |
| 1111 | DP.1, DP.0, USB, SATA | N.C. | DP.0, DP.1 | USB0 | SATA1 |
| 1100 | PCIe.0, PCIe.1, USB, SATA | PCIe Gen2 x2 | N.C. | USB0 | SATA1 |
| 1110 | PCIe.0, DP.0, USB, SATA | PCIe Gen2 x1 | DP.0 | USB0 | SATA1 |

PCIe (MIO 31)

The ZCU102 hosts a 4-lane PCIe root port connector similar to those commonly used on many micro-ATX motherboards. The PS-side GTR transceivers can be set to provide a PCI Express interface that operates at GEN2 speeds with a width of 1-lane (x1), 2-lanes (x2), or 4-lanes (x4).

The Zynq UltraScale+ MPSoC contains an integrated block for PCI Express interface based on the PCIe base v2.1 specification. The PS-side, PCIe reset signal (PS Bank 501 MIO31 pin J22) is wired to the PCIe Gen2 x4 root port slot P1. This MIO pin is an output for Root Port mode operation. The primary purpose of the ZCU102 is for PCIe root port operation.

PCI Express Root Port Slot

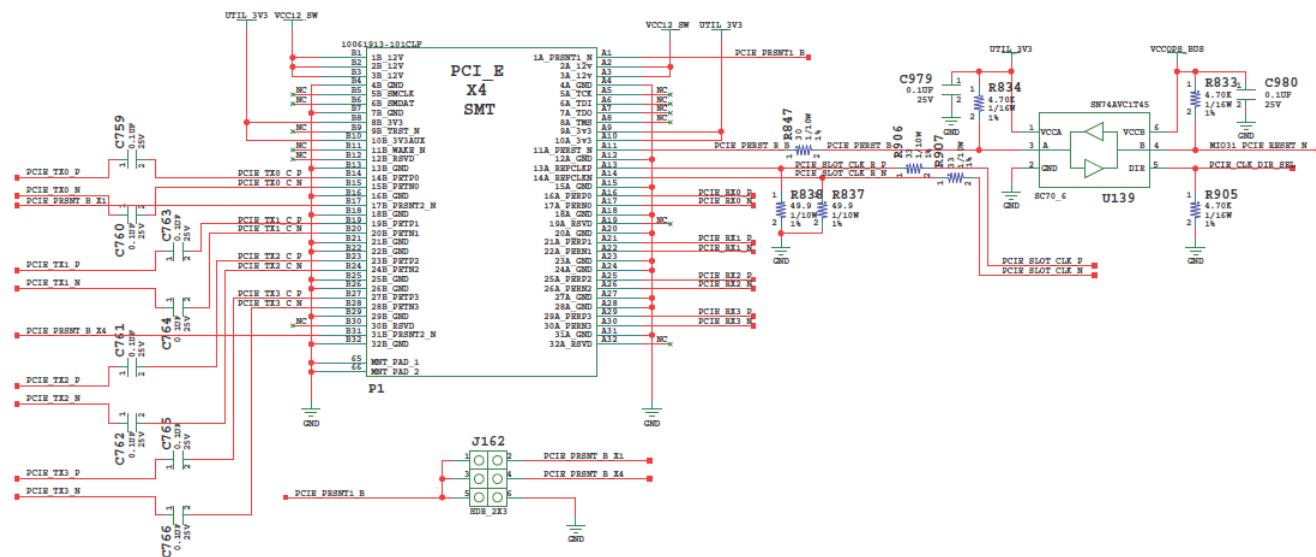
[[Figure 2-1](#), callout 35]

Production ZCU102s implement an x8 PCIe connector P1 supporting x4 PCIe. This allows for flexibility so the ZCU102 can accommodate PCIe boards that are designed for up to x8 without requiring an x8-to-x4 PCIe lane reducer.

The PCI Express connector P1 performs data transfers at the rate of 5.0 GT/s for Gen2 applications. The PCIe clock is routed as a 100Ω differential pair. The PCIe transmit and receive signal data paths are routed with a differential characteristic impedance of $85 \pm 10\%$ with an insertion loss of <4 dB up to 8 GHz. The XCZU9EG-L2FFVB1156E (-2 speed grade) device included with the ZCU102 board supports up to Gen3 x4. The PCIe reference clock output is wired to the P1 connector. PCIE_SLOT_CLK_P is connected to clock driver U69

Si5341B pin 38, and the _N net is connected to pin 37. The PCI Express clock circuit is shown in [Figure 3-8](#). PCIe 4-lane connector P1 is shown in [Figure 3-39](#).

The ZCU102 board's PCIe Host connector supports power requirements consistent with the PCI Express® Card Electromechanical Specification Revision 2.0 PCIe add-in cards up to 25W max (2.1A max on PCIe +12V and 3.0A max on PCIe +3.3V).



[Figure 3-39: PCIe Connector P1](#)

The 4-lane PCIe connector lane TX/RX nets are wired to the MPSOC U1 PS GTR Bank 505 transceiver channels through four 2-to-1 Pericom PI2DBS6212 [Ref 27] high speed multiplexers.

FPGA Mezzanine Card Interface

[[Figure 2-1](#), callout 31, 32]

The ZCU102 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification [Ref 29] by providing subset implementations of high pin count connectors at J5 (HPC0) and J4 (HPC1). HPC connectors use a 10 x 40 form factor, populated with 400 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the ZCU102 evaluation board, faces away from the board.

FMC HPC0 Connector J5

[[Figure 2-1](#), callout 31]

The FMC connector at J5 (HPC0) implements a subset of the full FMC HPC connectivity:

- 68 single-ended, or 34 differential user-defined pairs (34 LA pairs: LA[00:33])

- Eight GTH transceiver DP differential pairs
- Two GBTCLK differential clocks
- 159 ground and 15 power connections

The ZCU102 board FMC VADJ voltage VADJ_FMC_BUS for the J5 (HPC0) and J4 (HPC1) FMC connectors is determined by the MAX15301 U63 voltage regulator described in [ZCU102 Board Power System](#). The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The HPC0 J5 connections to XCZU9EG U1 are shown in [Table 3-44](#) through [Table 3-48](#).

Table 3-44: J5 HPC0 FMC Section A and B Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|---------------------------------------|--------------|--------|
| A2 | FMC_HPC0_DP1_M2C_P | | J4 | B1 | NC | | |
| A3 | FMC_HPC0_DP1_M2C_N | | J3 | B4 | NC | | |
| A6 | FMC_HPC0_DP2_M2C_P | | F2 | B5 | NC | | |
| A7 | FMC_HPC0_DP2_M2C_N | | F1 | B8 | NC | | |
| A10 | FMC_HPC0_DP3_M2C_P | | K2 | B9 | NC | | |
| A11 | FMC_HPC0_DP3_M2C_N | | K1 | B12 | FMC_HPC0_DP7_M2C_P | M2 | |
| A14 | FMC_HPC0_DP4_M2C_P | | L4 | B13 | FMC_HPC0_DP7_M2C_N | M1 | |
| A15 | FMC_HPC0_DP4_M2C_N | | L3 | B16 | FMC_HPC0_DP6_M2C_P | T2 | |
| A18 | FMC_HPC0_DP5_M2C_P | | P2 | B17 | FMC_HPC0_DP6_M2C_N | T1 | |
| A19 | FMC_HPC0_DP5_M2C_N | | P1 | B20 | FMC_HPC0_GBTCLK1_M2C_P ⁽¹⁾ | L8 | |
| A22 | FMC_HPC0_DP1_C2M_P | | H6 | B21 | FMC_HPC0_GBTCLK1_M2C_N ⁽¹⁾ | L7 | |
| A23 | FMC_HPC0_DP1_C2M_N | | H5 | B24 | NC | | |
| A26 | FMC_HPC0_DP2_C2M_P | | F6 | B25 | NC | | |
| A27 | FMC_HPC0_DP2_C2M_N | | F5 | B28 | NC | | |
| A30 | FMC_HPC0_DP3_C2M_P | | K6 | B29 | NC | | |
| A31 | FMC_HPC0_DP3_C2M_N | | K5 | B32 | FMC_HPC0_DP7_C2M_P | N4 | |
| A34 | FMC_HPC0_DP4_C2M_P | | M6 | B33 | FMC_HPC0_DP7_C2M_N | N3 | |
| A35 | FMC_HPC0_DP4_C2M_N | | M5 | B36 | FMC_HPC0_DP6_C2M_P | R4 | |
| A38 | FMC_HPC0_DP5_C2M_P | | P6 | B37 | FMC_HPC0_DP6_C2M_N | R3 | |
| A39 | FMC_HPC0_DP5_C2M_N | | P5 | B40 | NC | | |

Notes:

1. Series capacitor coupled to XCZU9EG U1 pin.

Table 3-45: J5 HPC0 FMC Section C and D Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|---------------------------------|--------------|--------|--------|---|--------------|-----------------------------|
| C2 | FMC_HPC0_DP0_C2M_P | | G4 | D1 | VADJ_FMC_PGOOD ⁽⁵⁾ | | J4.D1, U63.32 , U66.6 |
| C3 | FMC_HPC0_DP0_C2M_N | | G3 | D4 | FMC_HPC0_GBTCLK0_M2C_P ⁽¹⁾ | | G8 |
| C6 | FMC_HPC0_DP0_M2C_P | | H2 | D5 | FMC_HPC0_GBTCLK0_M2C_N ⁽¹⁾ | | G7 |
| C7 | FMC_HPC0_DP0_M2C_N | | H1 | D8 | FMC_HPC0_LA01_CC_P | LVCMOS18 | AB4 |
| C10 | FMC_HPC0_LA06_P | LVCMOS18 | AC2 | D9 | FMC_HPC0_LA01_CC_N | LVCMOS18 | AC4 |
| C11 | FMC_HPC0_LA06_N | LVCMOS18 | AC1 | D11 | FMC_HPC0_LA05_P | LVCMOS18 | AB3 |
| C14 | FMC_HPC0_LA10_P | LVCMOS18 | W5 | D12 | FMC_HPC0_LA05_N | LVCMOS18 | AC3 |
| C15 | FMC_HPC0_LA10_N | LVCMOS18 | W4 | D14 | FMC_HPC0_LA09_P | LVCMOS18 | W2 |
| C18 | FMC_HPC0_LA14_P | LVCMOS18 | AC7 | D15 | FMC_HPC0_LA09_N | LVCMOS18 | W1 |
| C19 | FMC_HPC0_LA14_N | LVCMOS18 | AC6 | D17 | FMC_HPC0_LA13_P | LVCMOS18 | AB8 |
| C22 | FMC_HPC0_LA18_CC_P | LVCMOS18 | N9 | D18 | FMC_HPC0_LA13_N | LVCMOS18 | AC8 |
| C23 | FMC_HPC0_LA18_CC_N | LVCMOS18 | N8 | D20 | FMC_HPC0_LA17_CC_P | LVCMOS18 | P11 |
| C26 | FMC_HPC0_LA27_P | LVCMOS18 | M10 | D21 | FMC_HPC0_LA17_CC_N | LVCMOS18 | N11 |
| C27 | FMC_HPC0_LA27_N | LVCMOS18 | L10 | D23 | FMC_HPC0_LA23_P | LVCMOS18 | L16 |
| C30 | FMC_HPC0_IIC_SCL ⁽²⁾ | | | D24 | FMC_HPC0_LA23_N | LVCMOS18 | K16 |
| C31 | FMC_HPC0_IIC_SDA ⁽²⁾ | | | D26 | FMC_HPC0_LA26_P | LVCMOS18 | L15 |
| C34 | GND | | | D27 | FMC_HPC0_LA26_N | LVCMOS18 | K15 |
| C35 | VCC12_SW | | | D29 | FMC_HPC0_TCK_BUF ⁽³⁾ | | |
| C37 | VCC12_SW | | | D30 | FPGA_TDO_FMC_TDI_BUF ⁽⁴⁾ | | |
| C39 | UTIL_3V3 | | | D31 | FMC_HPC0_TDO_HPC1_TDI ⁽³⁾⁽⁴⁾ | | |
| | | | | D32 | UTIL_3V3_10A | | |
| | | | | D33 | FMC_HPC0_TMS_BUF (3) | | |
| | | | | D34 | NC | | |
| | | | | D35 | GND | | |
| | | | | D36 | UTIL_3V3 | | |
| | | | | D38 | UTIL_3V3 | | |
| | | | | D40 | UTIL_3V3 | | |

Notes:

1. Series capacitor coupled to XCZU9EG U1 pin.
2. Connected to I2C switch U135 pins 4 and 5.
3. XCZU9EG U1 JTAG TCK, TMS, TDO pins R25, R24, T25 are buffered by U48 SN74AVC8T245.
4. J5 HPC0 TDO-TDI connections to U27 HPC0 FMC JTAG bypass switch (N.C. normally-closed/bypassing J5 until an FMC card is plugged onto J5).
5. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.

Table 3-46: J5 HPC0 FMC Section E and F Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|--------------------|----------------------|--------|
| E2 | NC | | | F1 | FMC_HPC0_PG_M2C | P/U to 3.3V via R277 | |
| E3 | NC | | | F4 | NC | | |
| E6 | NC | | | F5 | NC | | |
| E7 | NC | | | F7 | NC | | |
| E9 | NC | | | F8 | NC | | |
| E10 | NC | | | F10 | NC | | |
| E12 | NC | | | F11 | NC | | |
| E13 | NC | | | F13 | NC | | |
| E15 | NC | | | F14 | NC | | |
| E16 | NC | | | F16 | NC | | |
| E18 | NC | | | F17 | NC | | |
| E19 | NC | | | F19 | NC | | |
| E21 | NC | | | F20 | NC | | |
| E22 | NC | | | F22 | NC | | |
| E24 | NC | | | F23 | NC | | |
| E25 | NC | | | F25 | NC | | |
| E27 | NC | | | F26 | NC | | |
| E28 | NC | | | F28 | NC | | |
| E30 | NC | | | F29 | NC | | |
| E31 | NC | | | F31 | NC | | |
| E33 | NC | | | F32 | NC | | |
| E34 | NC | | | F34 | NC | | |
| E36 | NC | | | F35 | NC | | |
| E37 | NC | | | F37 | NC | | |
| E39 | VADJ_FMC_BUS | | | F38 | NC | | |
| | | | | F40 | VADJ_FMC_BUS | | |

Table 3-47: J5 HPC0 FMC Section G and H Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|---------------------|--------------|--------|--------|-------------------------------------|--------------|--------|
| G2 | FMC_HPC0_CLK1_M2C_P | LVDS | T8 | H1 | NC | | |
| G3 | FMC_HPC0_CLK1_M2C_N | LVDS | R8 | H2 | FMC_HPC0_PRSNT_M2C_B ⁽¹⁾ | | |
| G6 | FMC_HPC0_LA00_CC_P | LVCMOS18 | Y4 | H4 | FMC_HPC0_CLK0_M2C_P | LVDS | AA7 |
| G7 | FMC_HPC0_LA00_CC_N | LVCMOS18 | Y3 | H5 | FMC_HPC0_CLK0_M2C_N | LVDS | AA6 |
| G9 | FMC_HPC0_LA03_P | LVCMOS18 | Y2 | H7 | FMC_HPC0_LA02_P | LVCMOS18 | V2 |
| G10 | FMC_HPC0_LA03_N | LVCMOS18 | Y1 | H8 | FMC_HPC0_LA02_N | LVCMOS18 | V1 |
| G12 | FMC_HPC0_LA08_P | LVCMOS18 | V4 | H10 | FMC_HPC0_LA04_P | LVCMOS18 | AA2 |
| G13 | FMC_HPC0_LA08_N | LVCMOS18 | V3 | H11 | FMC_HPC0_LA04_N | LVCMOS18 | AA1 |
| G15 | FMC_HPC0_LA12_P | LVCMOS18 | W7 | H13 | FMC_HPC0_LA07_P | LVCMOS18 | U5 |
| G16 | FMC_HPC0_LA12_N | LVCMOS18 | W6 | H14 | FMC_HPC0_LA07_N | LVCMOS18 | U4 |
| G18 | FMC_HPC0_LA16_P | LVCMOS18 | Y12 | H16 | FMC_HPC0_LA11_P | LVCMOS18 | AB6 |
| G19 | FMC_HPC0_LA16_N | LVCMOS18 | AA12 | H17 | FMC_HPC0_LA11_N | LVCMOS18 | AB5 |
| G21 | FMC_HPC0_LA20_P | LVCMOS18 | N13 | H19 | FMC_HPC0_LA15_P | LVCMOS18 | Y10 |
| G22 | FMC_HPC0_LA20_N | LVCMOS18 | M13 | H20 | FMC_HPC0_LA15_N | LVCMOS18 | Y9 |
| G24 | FMC_HPC0_LA22_P | LVCMOS18 | M15 | H22 | FMC_HPC0_LA19_P | LVCMOS18 | L13 |
| G25 | FMC_HPC0_LA22_N | LVCMOS18 | M14 | H23 | FMC_HPC0_LA19_N | LVCMOS18 | K13 |
| G27 | FMC_HPC0_LA25_P | LVCMOS18 | M11 | H25 | FMC_HPC0_LA21_P | LVCMOS18 | P12 |
| G28 | FMC_HPC0_LA25_N | LVCMOS18 | L11 | H26 | FMC_HPC0_LA21_N | LVCMOS18 | N12 |
| G30 | FMC_HPC0_LA29_P | LVCMOS18 | U9 | H28 | FMC_HPC0_LA24_P | LVCMOS18 | L12 |
| G31 | FMC_HPC0_LA29_N | LVCMOS18 | U8 | H29 | FMC_HPC0_LA24_N | LVCMOS18 | K12 |
| G33 | FMC_HPC0_LA31_P | LVCMOS18 | V8 | H31 | FMC_HPC0_LA28_P | LVCMOS18 | T7 |
| G34 | FMC_HPC0_LA31_N | LVCMOS18 | V7 | H32 | FMC_HPC0_LA28_N | LVCMOS18 | T6 |
| G36 | FMC_HPC0_LA33_P | LVCMOS18 | V12 | H34 | FMC_HPC0_LA30_P | LVCMOS18 | V6 |
| G37 | FMC_HPC0_LA33_N | LVCMOS18 | V11 | H35 | FMC_HPC0_LA30_N | LVCMOS18 | U6 |
| G39 | VADJ_FMC_BUS | | | H37 | FMC_HPC0_LA32_P | LVCMOS18 | U11 |
| | | | | H38 | FMC_HPC0_LA32_N | LVCMOS18 | T11 |
| | | | | H40 | VADJ_FMC_BUS | | |

Notes:

1. FMC_HPC0_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U27.4 OE control signal is driven from I2C I/O expander U97.13.

Table 3-48: J5 HPC0 FMC Section J and K Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|--------------------|--------------|--------|
| J2 | NC | | | K1 | NC | | |
| J3 | NC | | | K4 | NC | | |
| J6 | NC | | | K5 | NC | | |
| J7 | NC | | | K7 | NC | | |
| J9 | NC | | | K8 | NC | | |
| J10 | NC | | | K10 | NC | | |
| J12 | NC | | | K11 | NC | | |
| J13 | NC | | | K13 | NC | | |
| J15 | NC | | | K14 | NC | | |
| J16 | NC | | | K16 | NC | | |
| J18 | NC | | | K17 | NC | | |
| J19 | NC | | | K19 | NC | | |
| J21 | NC | | | K20 | NC | | |
| J22 | NC | | | K22 | NC | | |
| J24 | NC | | | K23 | NC | | |
| J25 | NC | | | K25 | NC | | |
| J27 | NC | | | K26 | NC | | |
| J28 | NC | | | K28 | NC | | |
| J30 | NC | | | K29 | NC | | |
| J31 | NC | | | K31 | NC | | |
| J33 | NC | | | K32 | NC | | |
| J34 | NC | | | K34 | NC | | |
| J36 | NC | | | K35 | NC | | |
| J37 | NC | | | K37 | NC | | |
| J39 | NC | | | K38 | NC | | |
| | | | | K40 | NC | | |

FMC HPC1 Connector J4

[Figure 2-1, callout 32]

The FMC connector at J4 (HPC1) implements a subset of the full FMC HPC connectivity:

- 60 single-ended, or 30 differential user-defined pairs (LA[00:29])
- Eight GTH transceiver DP differential pairs
- Two GBTCLK differential clocks

- 159 ground and 15 power connections

The ZCU102 board FMC VADJ voltage VADJ_FMC_BUS for the J5 (HPC0) and J4 (HPC1) FMC connectors is determined by the MAX15301 U63 voltage regulator described in [ZCU102 Board Power System](#). The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The HPC1 J4 connections to XCZU9EG U1 are shown in [Table 3-49](#) through [Table 3-53](#).

Table 3-49: J4 HPC1 FMC Section A and B Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|---------------------------------------|--------------|--------|
| A2 | FMC_HPC1_DP1_M2C_P | | D33 | B1 | NC | | |
| A3 | FMC_HPC1_DP1_M2C_N | | D34 | B4 | NC | | |
| A6 | FMC_HPC1_DP2_M2C_P | | C31 | B5 | NC | | |
| A7 | FMC_HPC1_DP2_M2C_N | | C32 | B8 | NC | | |
| A10 | FMC_HPC1_DP3_M2C_P | | B33 | B9 | NC | | |
| A11 | FMC_HPC1_DP3_M2C_N | | B34 | B12 | FMC_HPC1_DP7_M2C_P | | F33 |
| A14 | FMC_HPC1_DP4_M2C_P | | L31 | B13 | FMC_HPC1_DP7_M2C_N | | F34 |
| A15 | FMC_HPC1_DP4_M2C_N | | L32 | B16 | FMC_HPC1_DP6_M2C_P | | H33 |
| A18 | FMC_HPC1_DP5_M2C_P | | K33 | B17 | FMC_HPC1_DP6_M2C_N | | H34 |
| A19 | FMC_HPC1_DP5_M2C_N | | K34 | B20 | FMC_HPC1_GBTCLK1_M2C_P ⁽¹⁾ | | E27 |
| A22 | FMC_HPC1_DP1_C2M_P | | D29 | B21 | FMC_HPC1_GBTCLK1_M2C_N ⁽¹⁾ | | E28 |
| A23 | FMC_HPC1_DP1_C2M_N | | D30 | B24 | NC | | |
| A26 | FMC_HPC1_DP2_C2M_P | | B29 | B25 | NC | | |
| A27 | FMC_HPC1_DP2_C2M_N | | B30 | B28 | NC | | |
| A30 | FMC_HPC1_DP3_C2M_P | | A31 | B29 | NC | | |
| A31 | FMC_HPC1_DP3_C2M_N | | A32 | B32 | FMC_HPC1_DP7_C2M_P | | G31 |
| A34 | FMC_HPC1_DP4_C2M_P | | K29 | B33 | FMC_HPC1_DP7_C2M_N | | G32 |
| A35 | FMC_HPC1_DP4_C2M_N | | K30 | B36 | FMC_HPC1_DP6_C2M_P | | H29 |
| A38 | FMC_HPC1_DP5_C2M_P | | J31 | B37 | FMC_HPC1_DP6_C2M_N | | H30 |
| A39 | FMC_HPC1_DP5_C2M_N | | J32 | B40 | NC | | |

Notes:

1. Series capacitor coupled to XCZU9EG U1 pin.

Table 3-50: J4 HPC1 FMC Section C and D Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|---------------------------------|--------------|--------|--------|---|--------------|----------------------------|
| C2 | FMC_HPC1_DP0_C2M_P | | F29 | D1 | VADJ_FMC_PGOOD ⁽⁵⁾ | | J5.D1, U63.32, U66.6 |
| C3 | FMC_HPC1_DP0_C2M_N | | F30 | D4 | FMC_HPC1_GBTCLK0_M2C_P ⁽¹⁾ | | G27 |
| C6 | FMC_HPC1_DP0_M2C_P | | E31 | D5 | FMC_HPC1_GBTCLK0_M2C_N ⁽¹⁾ | | G28 |
| C7 | FMC_HPC1_DP0_M2C_N | | E32 | D8 | FMC_HPC1_LA01_CC_P | LVCMOS18 | AJ6 |
| C10 | FMC_HPC1_LA06_P | LVCMOS18 | AH2 | D9 | FMC_HPC1_LA01_CC_N | LVCMOS18 | AJ5 |
| C11 | FMC_HPC1_LA06_N | LVCMOS18 | AJ2 | D11 | FMC_HPC1_LA05_P | LVCMOS18 | AG3 |
| C14 | FMC_HPC1_LA10_P | LVCMOS18 | AH4 | D12 | FMC_HPC1_LA05_N | LVCMOS18 | AH3 |
| C15 | FMC_HPC1_LA10_N | LVCMOS18 | AJ4 | D14 | FMC_HPC1_LA09_P | LVCMOS18 | AE2 |
| C18 | FMC_HPC1_LA14_P | LVCMOS18 | AH7 | D15 | FMC_HPC1_LA09_N | LVCMOS18 | AE1 |
| C19 | FMC_HPC1_LA14_N | LVCMOS18 | AH6 | D17 | FMC_HPC1_LA13_P | LVCMOS18 | AG8 |
| C22 | FMC_HPC1_LA18_CC_P | LVCMOS18 | Y8 | D18 | FMC_HPC1_LA13_N | LVCMOS18 | AH8 |
| C23 | FMC_HPC1_LA18_CC_N | LVCMOS18 | Y7 | D20 | FMC_HPC1_LA17_CC_P | LVCMOS18 | Y5 |
| C26 | FMC_HPC1_LA27_P | LVCMOS18 | U10 | D21 | FMC_HPC1_LA17_CC_N | LVCMOS18 | AA5 |
| C27 | FMC_HPC1_LA27_N | LVCMOS18 | T10 | D23 | FMC_HPC1_LA23_P | LVCMOS18 | AE12 |
| C30 | FMC_HPC1_IIC_SCL ⁽²⁾ | | | D24 | FMC_HPC1_LA23_N | LVCMOS18 | AF12 |
| C31 | FMC_HPC1_IIC_SDA ⁽²⁾ | | | D26 | FMC_HPC1_LA26_P | LVCMOS18 | T12 |
| C34 | GND | | | D27 | FMC_HPC1_LA26_N | LVCMOS18 | R12 |
| C35 | VCC12_SW | | | D29 | FMC_HPC1_TCK_BUF ⁽³⁾ | | |
| C37 | VCC12_SW | | | D30 | FPGA_TDO_FMC_TDI_BUF ⁽⁴⁾ | | |
| C39 | UTIL_3V3 | | | D31 | FMC_HPC1_TDO_HPC1_TDI ⁽³⁾⁽⁴⁾ | | |
| | | | | D32 | UTIL_3V3_10A | | |
| | | | | D33 | FMC_HPC1_TMS_BUF ⁽³⁾ | | |
| | | | | D34 | NC | | |
| | | | | D35 | GND | | |
| | | | | D36 | UTIL_3V3 | | |
| | | | | D38 | UTIL_3V3 | | |
| | | | | D40 | UTIL_3V3 | | |

Notes:

1. Series capacitor coupled to XCZU9EG U1 pin.
2. Connected to I2C switch U135 pins 6 and 7.
3. XCZU9EG U1 JTAG TCK, TMS, TDO pins R25, R24, T25 are buffered by U48 SN74AVC8T245.
4. J5 HPC0 TDO-TDI connections to U27 HPC0 FMC JTAG bypass switch (N.C. normally-closed/bypassing J5 until an FMC card is plugged onto J5).
5. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.

Table 3-51: J4 HPC1 FMC Section E and F Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|--------------------|--------------|----------------------|
| E2 | NC | | | F1 | FMC_HPC0_PG_M2C | | P/U to 3.3V via R250 |
| E3 | NC | | | F4 | NC | | |
| E6 | NC | | | F5 | NC | | |
| E7 | NC | | | F7 | NC | | |
| E9 | NC | | | F8 | NC | | |
| E10 | NC | | | F10 | NC | | |
| E12 | NC | | | F11 | NC | | |
| E13 | NC | | | F13 | NC | | |
| E15 | NC | | | F14 | NC | | |
| E16 | NC | | | F16 | NC | | |
| E18 | NC | | | F17 | NC | | |
| E19 | NC | | | F19 | NC | | |
| E21 | NC | | | F20 | NC | | |
| E22 | NC | | | F22 | NC | | |
| E24 | NC | | | F23 | NC | | |
| E25 | NC | | | F25 | NC | | |
| E27 | NC | | | F26 | NC | | |
| E28 | NC | | | F28 | NC | | |
| E30 | NC | | | F29 | NC | | |
| E31 | NC | | | F31 | NC | | |
| E33 | NC | | | F32 | NC | | |
| E34 | NC | | | F34 | NC | | |
| E36 | NC | | | F35 | NC | | |
| E37 | NC | | | F37 | NC | | |
| E39 | VADJ_FMC_BUS | | | F38 | NC | | |
| | | | | F40 | VADJ_FMC_BUS | | |

Table 3-52: J4 HPC1 FMC Section G and H Connections to XCZU9EG U1

| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|---------------------|--------------|--------|--------|-------------------------------------|--------------|--------|
| G2 | FMC_HPC1_CLK1_M2C_P | LVDS | P10 | H1 | NC | | |
| G3 | FMC_HPC1_CLK1_M2C_N | LVDS | P9 | H2 | FMC_HPC1_PRSNT_M2C_B ⁽¹⁾ | | |
| G6 | FMC_HPC1_LA00_CC_P | LVCMOS18 | AE5 | H4 | FMC_HPC1_CLK0_M2C_P | LVDS | AE7 |
| G7 | FMC_HPC1_LA00_CC_N | LVCMOS18 | AF5 | H5 | FMC_HPC1_CLK0_M2C_N | LVDS | AF7 |
| G9 | FMC_HPC1_LA03_P | LVCMOS18 | AH1 | H7 | FMC_HPC1_LA02_P | LVCMOS18 | AD2 |
| G10 | FMC_HPC1_LA03_N | LVCMOS18 | AJ1 | H8 | FMC_HPC1_LA02_N | LVCMOS18 | AD1 |
| G12 | FMC_HPC1_LA08_P | LVCMOS18 | AE3 | H10 | FMC_HPC1_LA04_P | LVCMOS18 | AF2 |
| G13 | FMC_HPC1_LA08_N | LVCMOS18 | AF3 | H11 | FMC_HPC1_LA04_N | LVCMOS18 | AF1 |
| G15 | FMC_HPC1_LA12_P | LVCMOS18 | AD7 | H13 | FMC_HPC1_LA07_P | LVCMOS18 | AD4 |
| G16 | FMC_HPC1_LA12_N | LVCMOS18 | AD6 | H14 | FMC_HPC1_LA07_N | LVCMOS18 | AE4 |
| G18 | FMC_HPC1_LA16_P | LVCMOS18 | AG10 | H16 | FMC_HPC1_LA11_P | LVCMOS18 | AE8 |
| G19 | FMC_HPC1_LA16_N | LVCMOS18 | AG9 | H17 | FMC_HPC1_LA11_N | LVCMOS18 | AF8 |
| G21 | FMC_HPC1_LA20_P | LVCMOS18 | AB11 | H19 | FMC_HPC1_LA15_P | LVCMOS18 | AD10 |
| G22 | FMC_HPC1_LA20_N | LVCMOS18 | AB10 | H20 | FMC_HPC1_LA15_N | LVCMOS18 | AE9 |
| G24 | FMC_HPC1_LA22_P | LVCMOS18 | AF11 | H22 | FMC_HPC1_LA19_P | LVCMOS18 | AA11 |
| G25 | FMC_HPC1_LA22_N | LVCMOS18 | AG11 | H23 | FMC_HPC1_LA19_N | LVCMOS18 | AA10 |
| G27 | FMC_HPC1_LA25_P | LVCMOS18 | AE10 | H25 | FMC_HPC1_LA21_P | LVCMOS18 | AC12 |
| G28 | FMC_HPC1_LA25_N | LVCMOS18 | AF10 | H26 | FMC_HPC1_LA21_N | LVCMOS18 | AC11 |
| G30 | FMC_HPC1_LA29_P | LVCMOS18 | W12 | H28 | FMC_HPC1_LA24_P | LVCMOS18 | AH12 |
| G31 | FMC_HPC1_LA29_N | LVCMOS18 | W11 | H29 | FMC_HPC1_LA24_N | LVCMOS18 | AH11 |
| G33 | FMC_HPC1_LA31_P | | NC | H31 | FMC_HPC1_LA28_P | LVCMOS18 | T13 |
| G34 | FMC_HPC1_LA31_N | | NC | H32 | FMC_HPC1_LA28_N | LVCMOS18 | R13 |
| G36 | FMC_HPC1_LA33_P | | NC | H34 | FMC_HPC1_LA30_P | | NC |
| G37 | FMC_HPC1_LA33_N | | NC | H35 | FMC_HPC1_LA30_N | | NC |
| G39 | VADJ_FMC_BUS | | | H37 | FMC_HPC1_LA32_P | | NC |
| | | | | H38 | FMC_HPC1_LA32_N | | NC |
| | | | | H40 | VADJ_FMC_BUS | | |

Notes:

1. FMC_HPC0_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U27.4 OE control signal is driven from I2C I/O expander U97.13.

Table 3-53: J4 HPC1 FMC Section J and K Connections to XCZU9EG U1

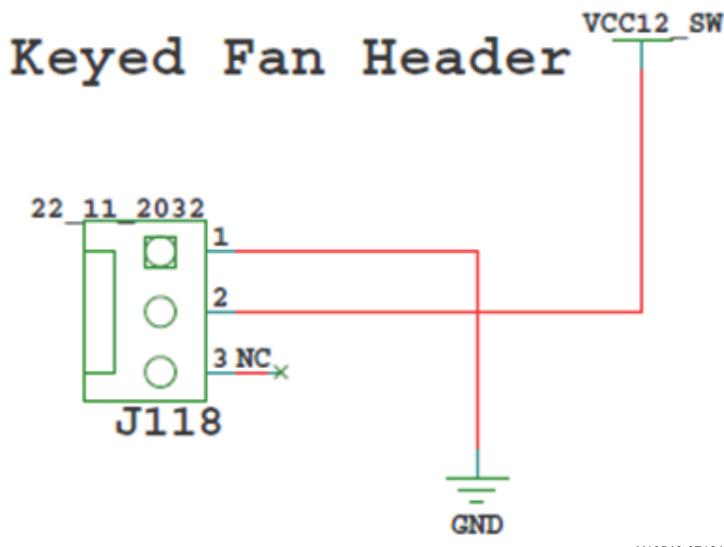
| J5 Pin | Schematic Net Name | I/O Standard | U1 Pin | J5 Pin | Schematic Net Name | I/O Standard | U1 Pin |
|--------|--------------------|--------------|--------|--------|--------------------|--------------|--------|
| J2 | NC | | | K1 | NC | | |
| J3 | NC | | | K4 | NC | | |
| J6 | NC | | | K5 | NC | | |
| J7 | NC | | | K7 | NC | | |
| J9 | NC | | | K8 | NC | | |
| J10 | NC | | | K10 | NC | | |
| J12 | NC | | | K11 | NC | | |
| J13 | NC | | | K13 | NC | | |
| J15 | NC | | | K14 | NC | | |
| J16 | NC | | | K16 | NC | | |
| J18 | NC | | | K17 | NC | | |
| J19 | NC | | | K19 | NC | | |
| J21 | NC | | | K20 | NC | | |
| J22 | NC | | | K22 | NC | | |
| J24 | NC | | | K23 | NC | | |
| J25 | NC | | | K25 | NC | | |
| J27 | NC | | | K26 | NC | | |
| J28 | NC | | | K28 | NC | | |
| J30 | NC | | | K29 | NC | | |
| J31 | NC | | | K31 | NC | | |
| J33 | NC | | | K32 | NC | | |
| J34 | NC | | | K34 | NC | | |
| J36 | NC | | | K35 | NC | | |
| J37 | NC | | | K37 | NC | | |
| J39 | NC | | | K38 | NC | | |
| | | | | K40 | NC | | |

See the ANSI/VITA 57.1 FPGA mezzanine card (FMC) specification [Ref 29] for additional information on the FPGA FMC.

Cooling Fan Connector

[Figure 2-1, near callout 42]

The XCZU9EG U1 cooling fan connector is shown in Figure 3-40. The fan turns on when the ZCU102 is powered up.



X16546-071817

Figure 3-40: ZCU102 12V Fan Header

VADJ_FMC Power Rail

The ZCU102 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the V_{ADJ_FMC} power rail is managed by the U41 system controller. This rail powers both the FMC HPC0 (J5) and the FMC HPC1 (J4) V_{ADJ} pins, as well as the XCZU9EG HP banks 65, 66 and 67. The valid values of the V_{ADJ_FMC} rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is connected to each interface:

- If no cards are attached to the FMC ports, the V_{ADJ} voltage is set to 1.8V.
- When one FMC card is attached, its IIC EEPROM is read to find a V_{ADJ} voltage supported by both the ZCU102 board and the FMC module, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing V_{ADJ} requirements, V_{ADJ_FMC} is set to the lowest value compatible with the ZCU102 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- If no valid information is found in an FMC card IIC EEPROM, the V_{ADJ_FMC} rail is set to 0.0V.

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_FMC rail. Override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA57.1 specification.

TI MSP430 System Controller

[Figure 2-1, callout 18]

The ZCU102 board includes an on-board MSP430 with integrated Power Advantage demo and System Controller firmware. A Host PC resident system controller user interface (SCUI) is provided on the [ZCU102 web page](#). This GUI enables you to query and control select programmable features such as clocks, FMC functionality, power systems, and the Zynq UltraScale+ MPSoC GTR selection compatible with your design. The ZCU102 web page also includes a tutorial on the SCUI (XTP433) [\[Ref 17\]](#) and board setup instructions (XTP435) [\[Ref 18\]](#). The following briefly summarizes these instructions:

1. Ensure that the Silicon Labs VCP USB-UART drivers are installed.
2. Download the SCUI Host PC application.
3. Connect the micro-USB to ZCU102 USB-UART connector (J83).
4. Power-cycle the ZCU102.
5. Observe that SYSCTRL LED0 (DS47) blinks and LED1 DS46 is illuminated.
6. Launch the SCUI.

The SCUI GUI is shown in [Figure 3-41](#).

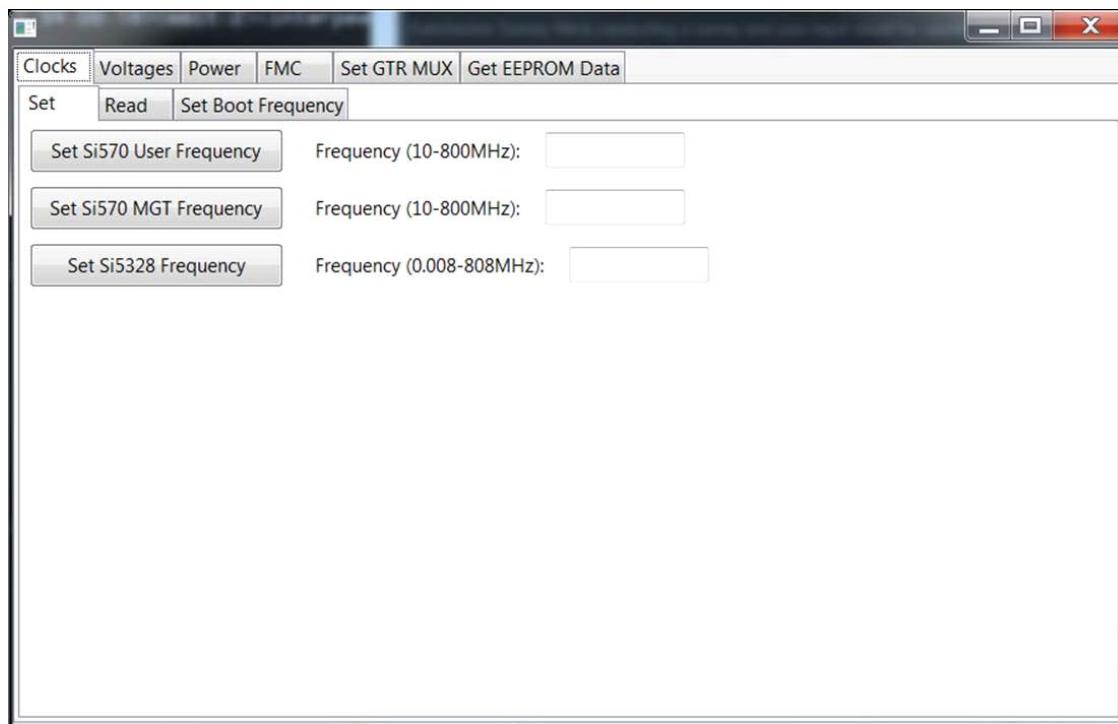


Figure 3-41: SCUI Graphical User Interface

On first use of the SCUI, go to the FMC > Set VADJ > Boot-up tab and click **USE FMC EEPROM Voltage**. The SCUI buttons gray-out during command execution and return to their original appearance when ready to accept a new command.

See the *System Controller Tutorial* (XTP433) and the *ZCU102 Software Install and Board Setup Tutorial* (XTP435) for more information on installing and using the System Controller utility.

The MSP430 uses ID resistor encoding to allow the System Controller utility awareness of which board type is active. See [Table 3-54](#) for the configuration of the ID encoding resistors R516 and R517.

Table 3-54: MSP430 Board ID Encoding

| Zynq UltraScale+ Board | R516 | R517 |
|------------------------|------|------|
| ZCU102 | DNP | DNP |
| ZCU106 | DNP | 10K |
| Reserved | 10K | DNP |
| Reserved | 10K | 10K |

Note: The MSP430 firmware might be updated in the event new capability is added in the future. The MSP430 upgrade header, J164, is reserved for this purpose. Xilinx will provide information on the update procedure via future updates to XTP433 [Ref 17].

Switches

[Figure 2-1, callouts 26, 28, 30, and 44]

The ZCU102 board includes power, configuration and reset switches:

- SW1 Power On/Off slide switch (callout 28)
- SW5 (PS_PROG_B), active-Low pushbutton (callout 30)
- SW3 (SRST_B), active-Low pushbutton (callout 26)
- SW4 (POR_B), active-Low pushbutton (callout 26)
- SW6 U1 MPSoC PS bank 503 4-pole mode DIP switch (callout 44)

Power On/Off Slide Switch

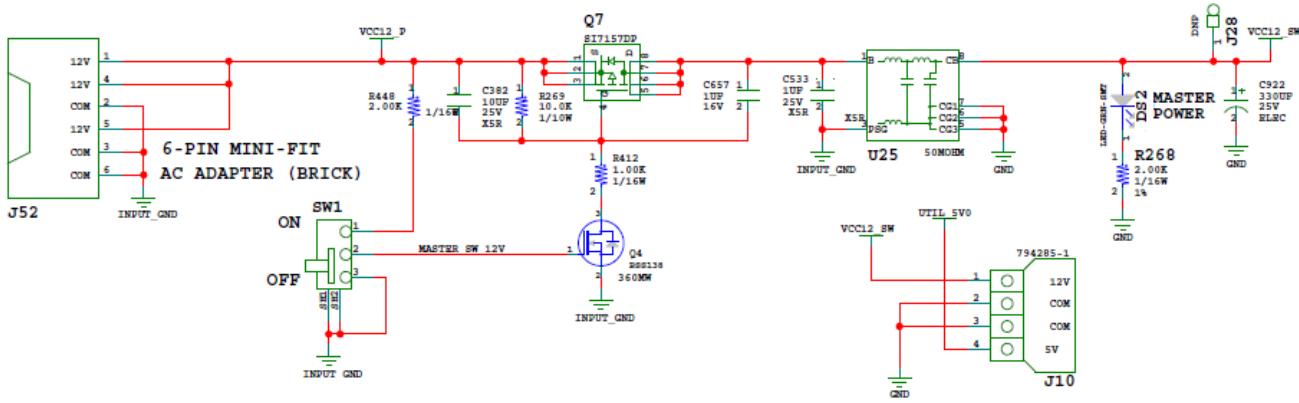
[Figure 2-1, callout 28]

The ZCU102 board power switch is SW1. Sliding the switch actuator from the *Off* to *On* position applies 12V power from J52, a 6-pin mini-fit connector. Green LED DS2 illuminates when the ZCU102 board power is on. See [ZCU102 Board Power System](#) for details on the on-board power system.



CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into J52 on the ZCU102 board. The ATX 6-pin connector has a different pin-out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU102 board and voids the board warranty.

Figure 3-42 shows the power connector J52, power switch SW1, and LED indicator DS2.



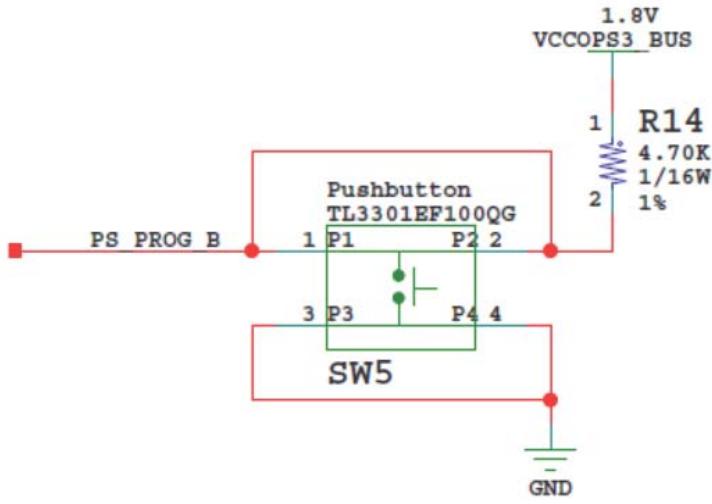
X16548-071817

Figure 3-42: Power On/Off Switch SW1

Program_B Pushbutton

[Figure 2-1, callout 30]

PS_PROG_B pushbutton switch SW5 grounds the XCZU9EG MPSoC PS_PROG_B pin U21 when pressed (see Figure 3-43). This action clears programmable logic configuration, which the PS software can then act on. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 3] for information about Zynq UltraScale+ MPSoC configuration.



X16549-071817

Figure 3-43: PS_PROG_B Pushbutton Switch SW5

System Reset Pushbuttons

[Figure 2-1, callout 26]

Figure 3-44 shows the reset circuitry for the processing system.

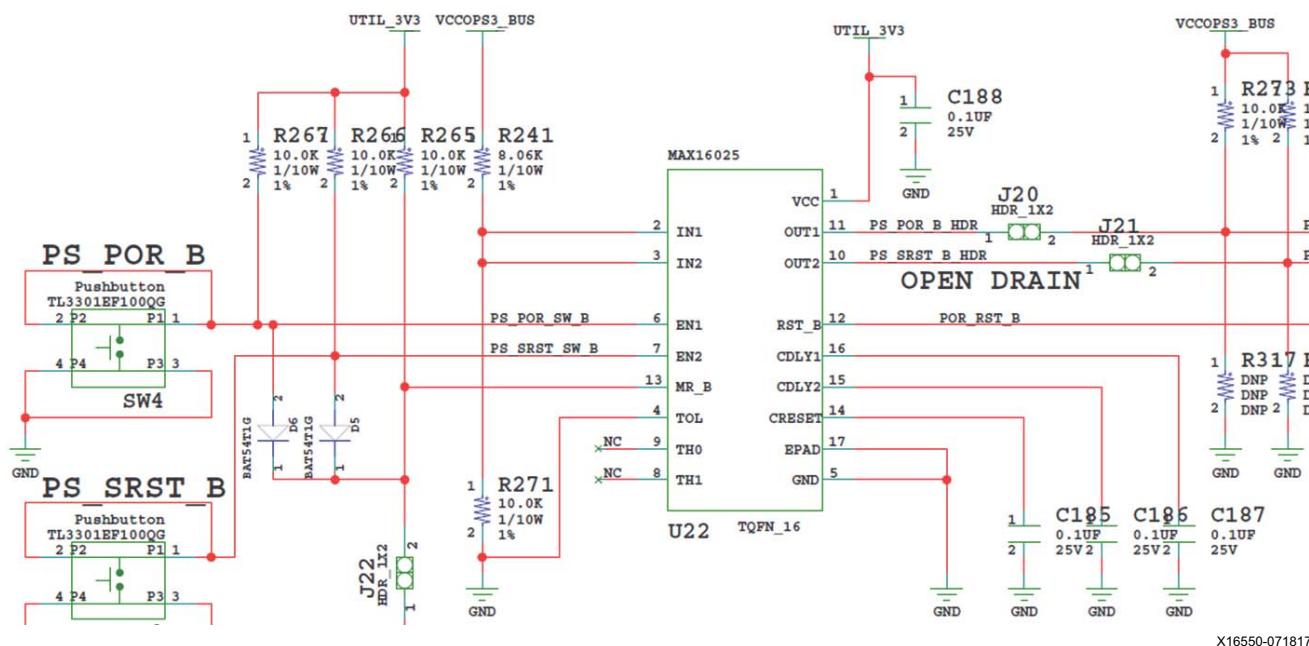


Figure 3-44: PS_SRST_B and POR_B Pushbutton Switches SW3 and SW4

PS_POR_B Reset

Depressing and then releasing pushbutton SW4 causes net PS_POR_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal. When the voltage at IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS_POR_B) goes Low.

PS_SRST_B Reset

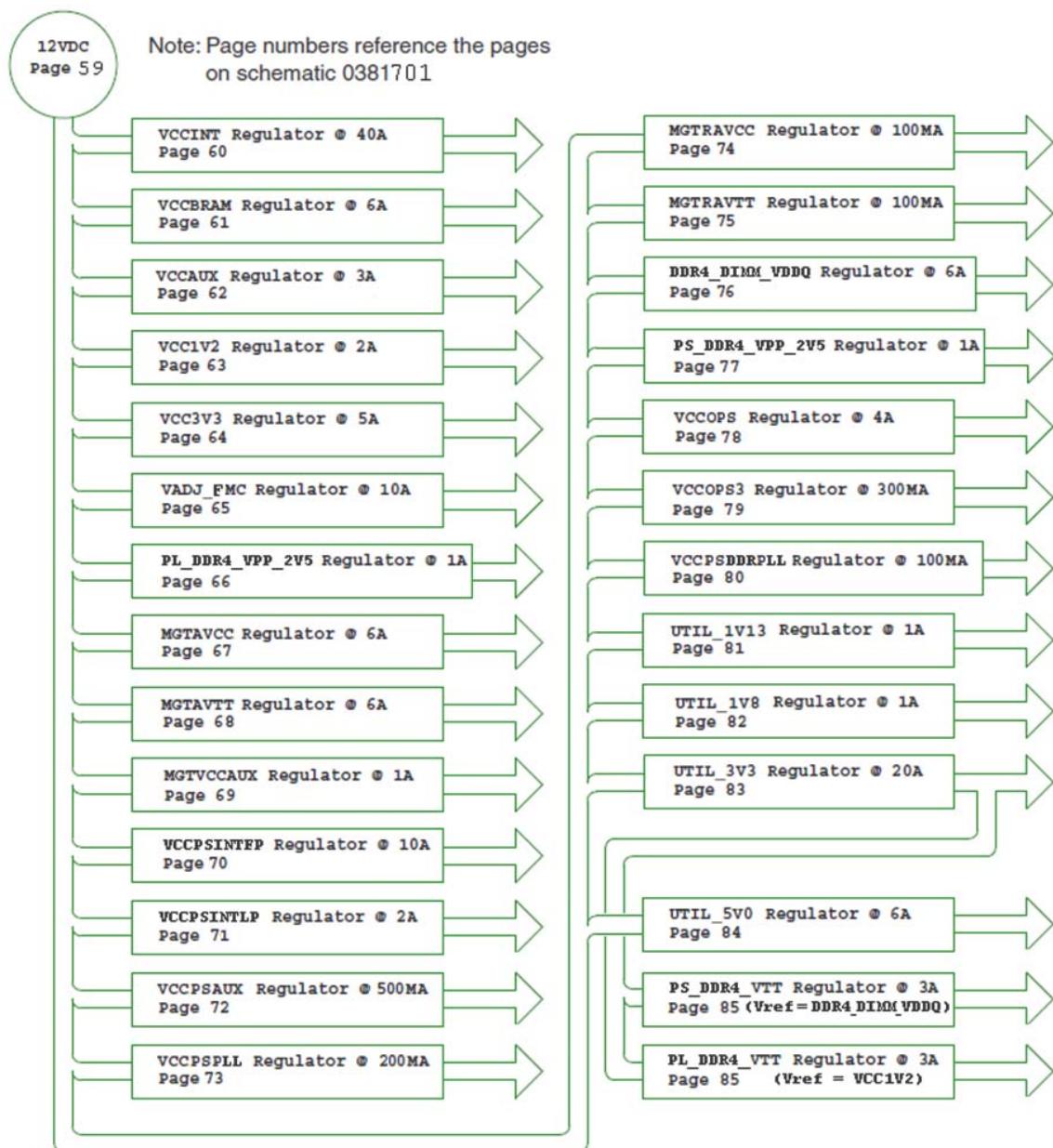
Depressing and then releasing pushbutton SW3 causes net PS_SRST_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW3 is pressed) goes Low, OUT2 (PS_SRST_B) goes Low.

Active-Low Reset Output RST_B asserts when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes Low, or MR is asserted. RST_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN_ are High, all OUT_ are high, and MR is deasserted. See the *Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085)* [Ref 3] for information for information concerning the resets.

ZCU102 Board Power System

[Figure 2-1, callout 34]

The ZCU102 hosts a Maxim PMBus based power system. Each individual Maxim MAX20751EKX, MAX15301, or MAX15303 voltage regulator has a PMBus interface. Figure 3-45 shows the ZCU102 power system block diagram.



X16551-071817

Figure 3-45: ZCU102 Power System Block Diagram

The ZCU102 evaluation board uses power regulators and PMBus compliant POL controllers from Maxim Integrated Circuits [Ref 28] to supply the core and auxiliary voltages listed in [Table 3-55](#). The schematic page references are to 0381701.

Table 3-55: ZCU102 Power System Devices

| Device Type | Ref. Des. | PMBus Address | Description | Power Rail Net Name | Power Rail Voltage | INA226 Address | Schematic Page |
|-------------|-----------|---------------|---|---------------------|--------------------|----------------|----------------|
| MAX15301 | U47 | 0x13 | Maxim InTune digital POL controller 40A | VCCINT | 0.85V | 0x40 | 60 |
| MAX15303 | U7 | 0x14 | Maxim InTune digital POL controller 6A | VCCBRAM | 0.85V | 0x41 | 61 |
| MAX15303 | U6 | 0x15 | Maxim InTune digital POL controller 3A | VCCAUX | 1.80V | 0x42 | 62 |
| MAX15303 | U10 | 0x16 | Maxim InTune digital POL controller 2A | VCC1V2 | 1.20V | 0x43 | 63 |
| MAX15303 | U9 | 0x17 | Maxim InTune digital POL controller 5A | VCC3V3 | 3.30V | 0x44 | 64 |
| MAX15301 | U63 | 0x18 | Maxim InTune digital POL controller 10A | VADJ_FMC | 1.80V | 0x45 | 65 |
| MAX15027 | U38 | N/A | Maxim LDO Regulator 1A | PL_DDR4_VPP_2V5 | 2.5V | N/A | 66 |
| MAX20751EKX | U95 | 0x72 | Maxim multiphase master with smart slave VT77518 6A | MGTAVCC | 0.90V | 0x46 | 67 |
| MAX20751EKX | U96 | 0x73 | Maxim multiphase master with smart slave VT77518 6A | MGTAVTT | 1.20V | 0x47 | 68 |
| MAX8869E | U14 | N/A | Maxim LDO Regulator 1A | MGTVCCAUX | 1.81V | N/A | 69 |
| MAX15301 | U46 | 0x0A | Maxim InTune digital POL controller 10A | VCCPSINTFP | 0.85V | 0x40 | 70 |
| MAX15303 | U4 | 0x0B | Maxim InTune digital POL controller 2A | VCCPSINTLP | 0.85V | 0x41 | 71 |
| MAX8869E | U3 | N/A | Maxim LDO Regulator 500 MA | VCCPSAUX | 1.81V | 0x42 | 72 |
| MAX8869E | U17 | N/A | Maxim LDO Regulator 200 MA | VCCPSPLL | 1.20V | 0x43 | 73 |
| MAX8869E | U5 | N/A | Maxim LDO Regulator 400 MA | MGTRAVCC | 0.85V | 0x44 | 74 |
| MAX8869E | U12 | N/A | Maxim LDO Regulator 100 MA | MGTRAVTT | 1.81V | 0x45 | 75 |
| MAX15303 | U18 | 0x1D | Maxim InTune digital POL controller 6A | DDR4_DIMM_VDD_Q | 1.20V | N/A | 76 |
| MAX15027 | U39 | N/A | Maxim LDO Regulator 1A | PS_DDR4_VPP_2V5 | 2.50V | N/A | 77 |
| MAX15303 | U13 | 0x10 | Maxim InTune digital POL controller 4A | VCCOPS | 1.80V | 0x47 | 78 |
| MAX8869E | U31 | N/A | Maxim LDO Regulator 300 MA | VCCOPS3 | 1.81V | 0x4A | 79 |
| MAX8869E | U30 | N/A | Maxim LDO Regulator 100 MA | VCCPSDDRPLL | 1.81V | 0x4B | 80 |

Table 3-55: ZCU102 Power System Devices (Cont'd)

| Device Type | Ref. Des. | PMBus Address | Description | Power Rail Net Name | Power Rail Voltage | INA226 Address | Schematic Page |
|-------------|-----------|---------------|---|---------------------|--------------------|----------------|----------------|
| MAX8869E | U143 | N/A | Maxim LDO Regulator 1A | UTIL_1V13 | 1.13V | NA | 81 |
| MAX8869E | U37 | N/A | Maxim LDO Regulator 1A | UTIL_1V8 | 1.80V | NA | 82 |
| MAX15301 | U49 | 0x1A | Maxim InTune digital POL controller 20A | UTIL_3V3 | 3.30V | NA | 83 |
| MAX15303 | U8 | 0x1B | Maxim InTune digital POL controller 6A | UTIL_5V0 | 5.00V | NA | 84 |
| TPS15200 | U36 | N/A | Memory Vtt Sink-Source Regulator 3A | PS_DDR4_VTT | 0.6V | NA | 85 |
| TPS15200 | U35 | N/A | Memory Vtt Sink-Source Regulator 3A | PL_DDR4_VTT | 0.6V | NA | 85 |

The FMC HPC0 (J5) and FMC HPC1 (J4) VADJ pins are wired to the programmable rail VADJ_FMC_BUS. The VADJ_FMC_BUS rail is programmed to 1.80V by default. The VADJ_FMC derivative rail powers the XCZU9EG HP banks 64 - 67 (refer to [Table 3-2](#)).

Documentation describing PMBUS programming for the Maxim InTune power controllers is available at the Maxim website [\[Ref 28\]](#). The PCB layout and power system design meets the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [\[Ref 5\]](#).

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Maxim power system controllers through the Maxim PowerTool graphical user interface. The on-board Maxim InTune power controllers listed in [Table 3-55](#) are accessed through the 2x8 keyed shrouded PMBus connector J84, which is provided for use with the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL001#), which can be ordered from the Maxim website [\[Ref 28\]](#). The associated Maxim PowerTool GUI can be downloaded from the Maxim website. This is the simplest and most convenient way to monitor the voltage and current values for the Maxim PMBus programmed power rails listed in [Table 3-55](#).

Each PMBus programmable Maxim controller programmable is capable of reporting the voltage and current of its controlled rail to the Maxim GUI for display to the user. A subset of the programmable rails and two fixed rails have a TI INA226 PMBus power monitor circuit with connections to the rail sense net and taps on a series current sense resistor. This

arrangement permits the INA226 to report the sensed parameters on the PMBus. The subset of rails configured with the INA226 power monitors is shown in [Table 3-56](#).

Table 3-56: ZCU102 Power Rails with INA226 Power Monitors

| Device Type | Ref. Des. | PMBus Address | Power Rail Net Name | INA226 Address | Schematic Page |
|-------------|-----------|---------------|---------------------|----------------|----------------|
| MAX15301 | U47 | 0x13 | VCCINT | PL: 0x40 | 60 |
| MAX15303 | U7 | 0x14 | VCCBRAM | PL: 0x41 | 61 |
| MAX15303 | U6 | 0x15 | VCCAUX | PL: 0x42 | 62 |
| MAX15303 | U10 | 0x16 | VCC1V2 | PL: 0x43 | 63 |
| MAX15303 | U9 | 0x17 | VCC3V3 | PL: 0x44 | 64 |
| MAX15301 | U63 | 0x18 | VADJ_FMC | PL: 0x45 | 65 |
| MAX20751 | U95 | 0x72 | MGTAVCC | PL: 0x46 | 67 |
| MAX20751 | U96 | 0x73 | MGTAVTT | PL: 0x47 | 68 |
| MAX15301 | U46 | 0x0A | VCCPSINTFP | PS: 0x40 | 70 |
| MAX15303 | U4 | 0x0B | VCCPSINTLP | PS: 0x41 | 71 |
| MAX8869E | U3 | NA | VCCPSAUX | PS: 0x42 | 72 |
| MAX8869E | U17 | NA | VCCPSPLL | PS: 0x43 | 73 |
| MAX8869E | U5 | NA | MGTRAVCC | PS: 0x44 | 74 |
| MAX8869E | U12 | NA | MGTRAVTT | PS: 0x45 | 75 |
| MAX15303 | U13 | 0x10 | VCCOPS | PS: 0x47 | 78 |
| MAX8869E | U31 | NA | VCCOPS3 | PS: 0x4A | 79 |
| MAX8869E | U30 | NA | VCCPSDDRPLL | PS: 0x4B | 80 |

As noted in the [I2C0 \(MIO 14-15\)](#), the I2C0 bus provides access to the PMBus power controllers and PS-side and PL-side INA226 power monitors via the U60 PCA9544A bus switch. All PMBus controlled Maxim regulators are tied to the MAXIM_PMBUS, while the INA226 power monitors are separated on to PS_PMBUS and PL_PMBUS.

[Figure 3-17](#) and [Table 3-19](#) document the I2C0 bus access path to the Maxim PMBus controllers and INA226 power monitor op amps. Also refer to schematic 0381701.

The MPSoC core related power rail measurements (PL_PMBUS) and PS related power measurements (PS_PMBUS) are accessible to the system controller and PL logic through their respective I2C0 bus connections. These measurements are displayed in the system controller menu selections. The Maxim controller PMBus is also accessible by the system controller, which can also display the rail voltage measurement made by its sourcing Maxim controller. User IP in the PL can access the same set of PMBus resident devices through the logic I2C0 connections.

VITA 57.1 FMC Connector Pinouts

Overview

[Figure A-1](#) shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZCU102 evaluation board implements the FMC specification, see [FPGA Mezzanine Card Interface](#), [FMC HPC0 Connector J5](#), and [FMC HPC1 Connector J4](#).

| | K | J | H | G | F | E | D | C | B | A |
|----|--------------|--------------|-------------|------------|-----------|-----------|-------------|-------------|-------------|-----------|
| 1 | VREF B M2C | GND | VREF A M2C | GND | PG M2C | GND | PG C2M | GND | CLK DIR | GND |
| 2 | GND | CLK3_BIDIR_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_BIDIR_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_BIDIR_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C | GND | DP9_M2C_P | GND |
| 5 | CLK2_BIDIR_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | DP7_M2C_N | GND | |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GBTCLK1_M2C | GND | |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_P | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | DP9_C2M_N | GND | |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | DP8_C2M_P | GND | |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

X22901-051519

Figure A-1: FMC HPC Connector Pinout

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the ZCU102 board provides for designs targeting the ZCU102 evaluation board. Net names in the constraints correlate with net names on the latest ZCU102 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 12] for more information.

The FMC connectors J5 (HPC0) and J4 (HPC1) are connected to MPSoC banks powered by the variable voltage V_{AJ_FMC} . Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.



IMPORTANT: The XDC file can be accessed on the [Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit website](#).

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

[ZCU102 Evaluation Kit Master Answer Record 66752](#)

For Technical Support, open a [Support Service Request](#).

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

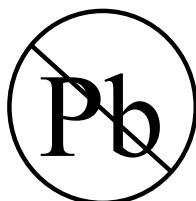
Markings



In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

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This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.



This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

References

The most up to date information related to the ZCU102 board and its documentation is available on the following websites.

[ZCU102 Evaluation Kit](#)

[ZCU102 Evaluation Kit Master Answer Record 66752](#)

These Xilinx documents provide supplemental material useful with this guide:

1. *Zynq UltraScale+ MPSoC Data Sheet: Overview* ([DS891](#))
2. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* ([DS925](#))
3. *Zynq UltraScale+ MPSoC Technical Reference Manual* ([UG1085](#))
4. [Xilinx HDMI IP documentation](#)
5. *UltraScale Architecture PCB Design User Guide* ([UG583](#))
6. *UltraScale Architecture FPGAs Memory Interface Solutions LogiCORE IP Product Guide* ([PG150](#))
7. *UltraScale Architecture GTH Transceivers User Guide* ([UG576](#))
8. *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* ([PG156](#))
9. *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#))
10. *Silicon Labs CP210x USB-to-UART Installation Guide* ([UG1033](#))
11. *Tera Term Terminal Emulator Installation Guide* ([UG1036](#))
12. *Vivado Design Suite User Guide: Using Constraints User Guide* ([UG903](#))
13. *HDMI 1.4/2.0 Transmitter Subsystem LogiCORE IP Product Guide* ([PG235](#))
14. [HDMI Transmitter and Receiver Subsystem Answer Record 70514](#)
15. *HDMI 1.4/2.0 Receiver Subsystem LogiCORE IP Product Guide* ([PG236](#))
16. *UltraScale Architecture System Monitor User Guide* ([UG580](#))
17. *ZCU102 System Controller Tutorial* ([XTP433](#))
18. *ZCU102 Software Install and Board Setup Tutorial* ([XTP435](#))
19. [Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit Design Hub](#)

The following websites provide supplemental material useful with this guide:

20. Micron Technology: www.micron.com
(MTA4ATF51264HZ-2G6E1, MT41J256M8HX-15E, MT25QU512ABB8ESF-0SIT data sheets)
21. Standard Microsystems Corporation (SMSC):
www.microchip.com/redirect-notifications/smsc
(USB3320 data sheet)
22. SanDisk Corporation: www.sandisk.com/
23. SD Association: www.sdcard.org/
24. Silicon Labs: www.silabs.com/Pages/default.aspx
(SI5341B-B05071, Si570BAB001614DG Si570BAB0000544DG, Si570, Si53340, CP2108 data sheets)
25. Texas Instruments <http://www.ti.com/product/DP83867IR>
(TI DP83867 data sheet)
26. PCI website: <https://pcisig.com/specifications>
27. Pericom PI2DBS6212: <https://www.pericom.com/assets/Datasheets/PI2DBS6212.pdf>
28. Maxim Integrated Circuits: <https://www.maximintegrated.com>
29. VITA FMC Marketing Alliance website: <http://www.vita.com/fmc>
30. Digilent: www.digilentinc.com (USB JTAG Module, Pmod peripheral modules)

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