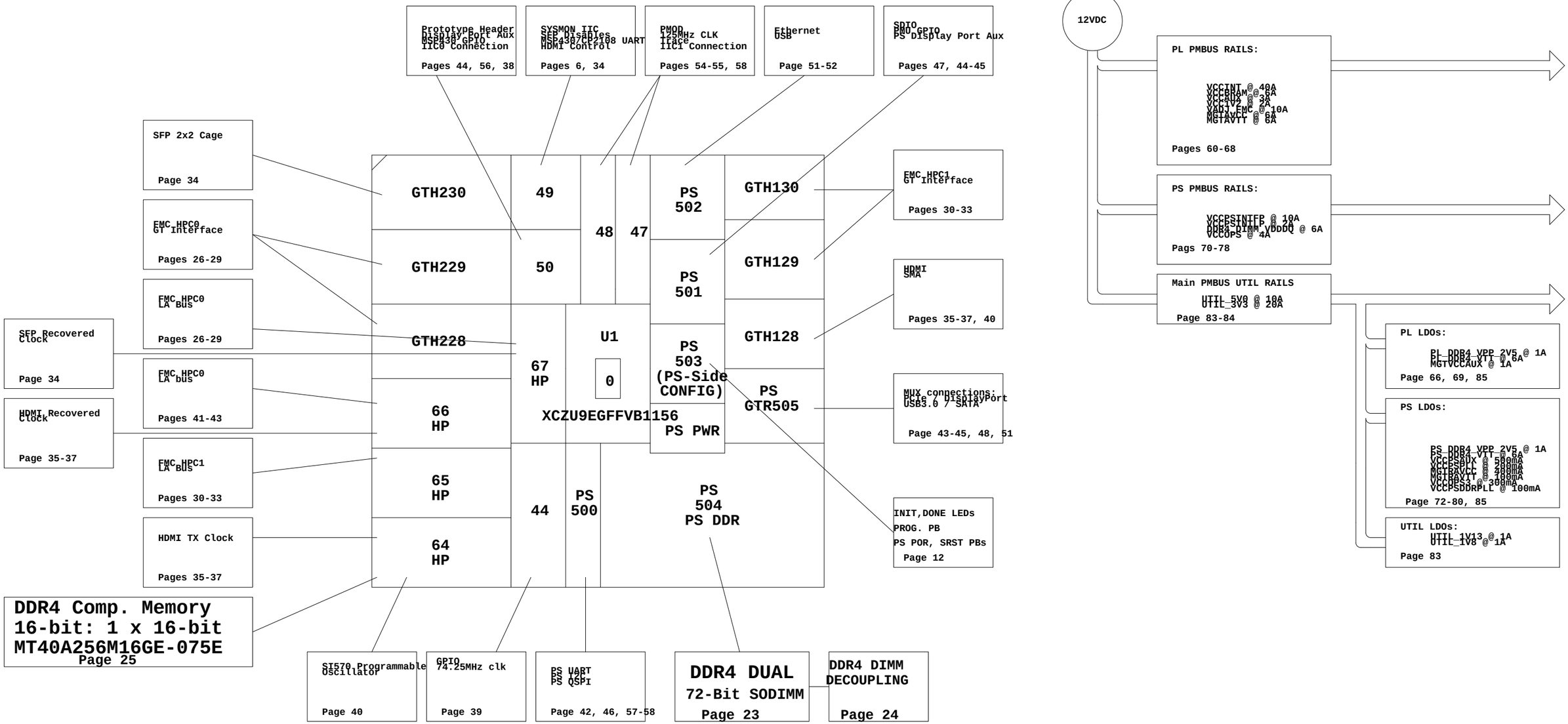
HW-Z1-ZCU102 Evaluation Board (XCZU9EG-FFVB1156)

XILINX

TITLE: Title Page SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 1 OF 87	DRAWN BY: BF



BANK#	PAGE#	BANK#	PAGE#
BANK 0	3	BANK 47	5
PS 503	12	BANK 48	5
PSDDR 504	13	BANK 49	6
BANK 64	7	BANK 50	6
BANK 66	8	MGTH128-130	9
BANK 65	7	MGTH228-230	10
BANK 67	8	MGTR 505	14
PS 500	11	PWR CONNECTORS	59
PS 501, 502	11		
BANK 44	4		

PS/PL/System
Clock devices
Pages 39-41

JTAG CONN.
Page 22

GTR Muxes
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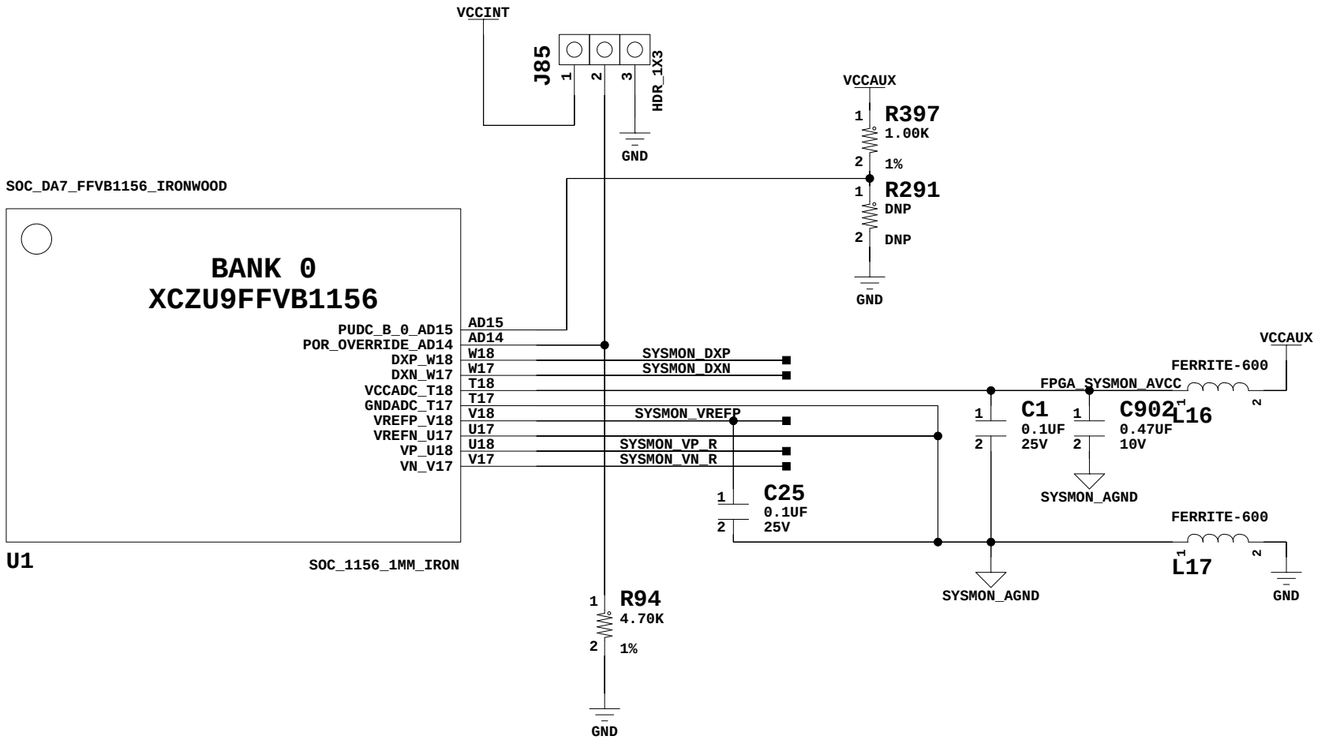
MECHANICALS
Page 87

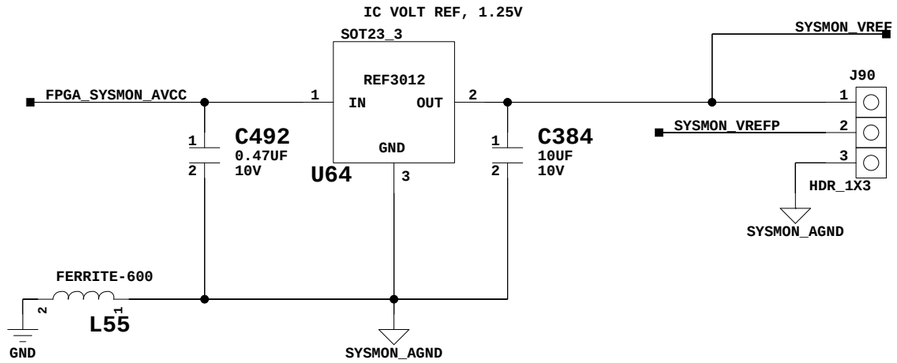
XILINX

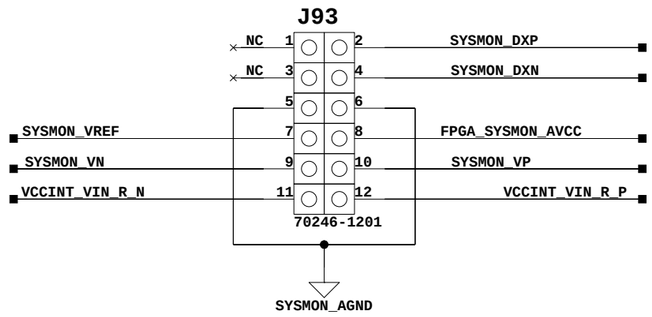
TITLE: Block Diagram
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

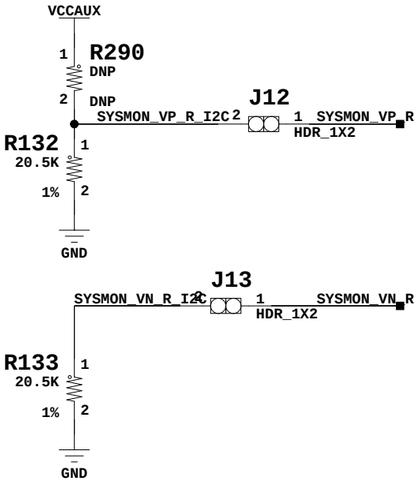
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 2 OF 87	DRAWN BY: BF

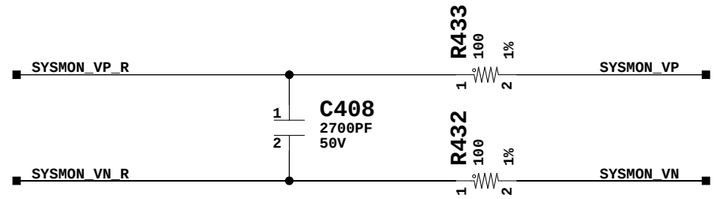








SYSMON I2C Address jumpers



Zynq Bank 0

XILINX

TITLE: Zynq Bank 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 3 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 44
XCZU9FFVB1156

IO_L12N_AD0N_44_AE14	AE14	GPIO_SW_E
IO_L12P_AD0P_44_AE15	AE15	GPIO_SW_S
IO_L11N_AD1N_44_AG15	AG15	GPIO_SW_N
IO_L11P_AD1P_44_AF15	AF15	GPIO_SW_W
IO_L10N_AD2N_44_AG13	AG13	GPIO_SW_C
IO_L10P_AD2P_44_AG14	AG14	GPIO_LED_0
IO_L9N_AD3N_44_AF13	AF13	GPIO_LED_1
IO_L9P_AD3P_44_AE13	AE13	GPIO_LED_2
IO_L8N_HDGC_AD4N_44_AJ14	AJ14	GPIO_LED_3
IO_L8P_HDGC_AD4P_44_AJ15	AJ15	GPIO_LED_4
IO_L7N_HDGC_AD5N_44_AH13	AH13	GPIO_LED_5
IO_L7P_HDGC_AD5P_44_AH14	AH14	GPIO_LED_6
IO_L6N_HDGC_AD6N_44_AL12	AL12	GPIO_LED_7
IO_L6P_HDGC_AD6P_44_AK13	AK13	GPIO_DIP_SW7
IO_L5N_HDGC_AD7N_44_AK14	AK14	CLK_74_25_N
IO_L5P_HDGC_AD7P_44_AK15	AK15	CLK_74_25_P
IO_L4N_AD8N_44_AM13	AM13	CPU_RESET
IO_L4P_AD8P_44_AL13	AL13	GPIO_DIP_SW6
IO_L3N_AD9N_44_AP12	AP12	GPIO_DIP_SW5
IO_L3P_AD9P_44_AN12	AN12	GPIO_DIP_SW4
IO_L2N_AD10N_44_AN13	AN13	GPIO_DIP_SW3
IO_L2P_AD10P_44_AM14	AM14	GPIO_DIP_SW2
IO_L1N_AD11N_44_AP14	AP14	GPIO_DIP_SW1
IO_L1P_AD11P_44_AN14	AN14	GPIO_DIP_SW0

VCC3V3

AF14	VCCO_44_AF14
AJ13	VCCO_44_AJ13

U1

SOC_1156_1MM_IRON

CLK_74_25_P

R430
100
1/10W
1%

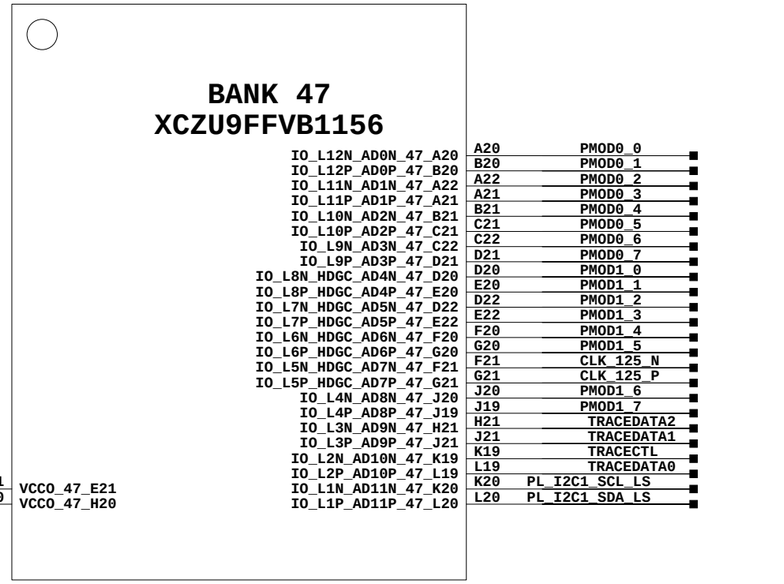
CLK_74_25_N

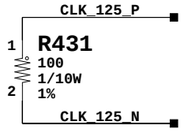
Zynq Banks 44

XILINX

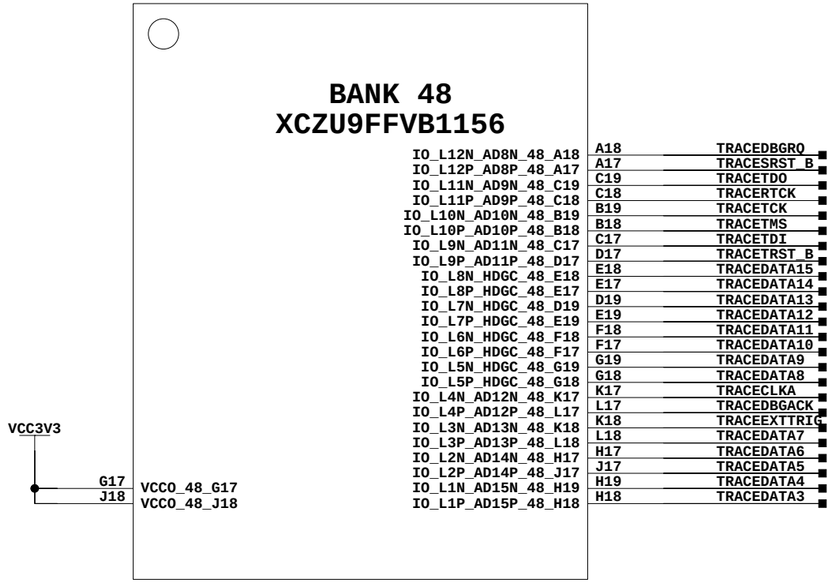
TITLE: Zynq Banks 44 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 4 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD





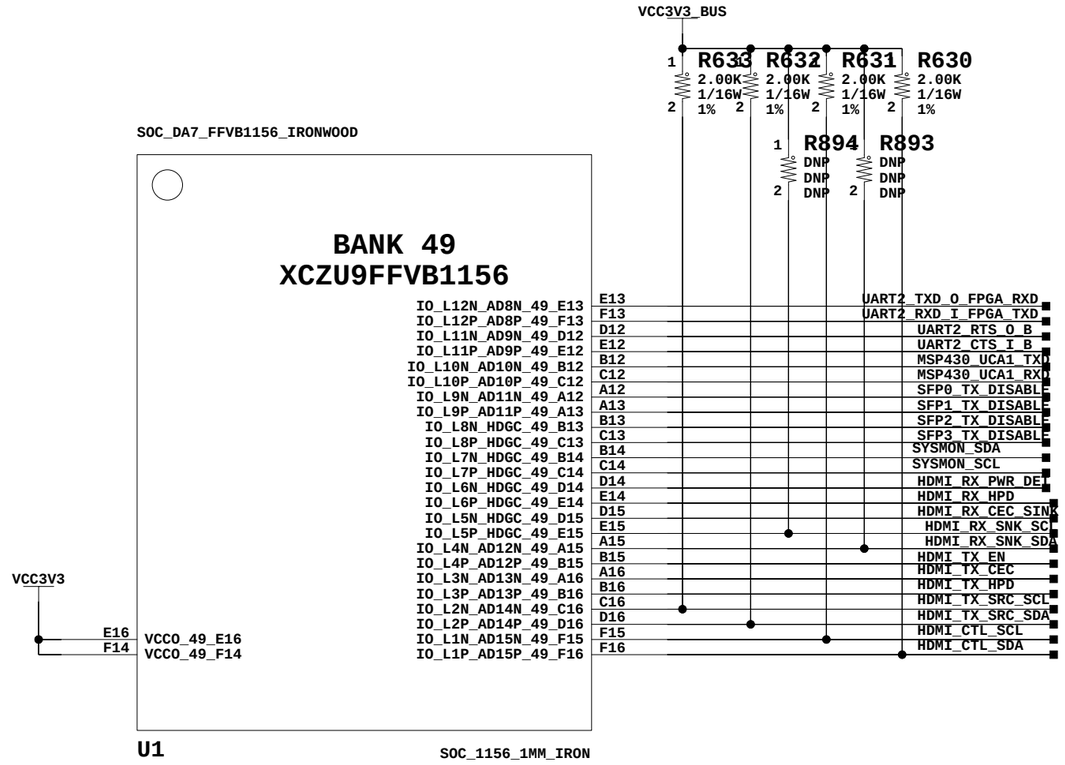
SOC_DA7_FFVB1156_IRONWOOD

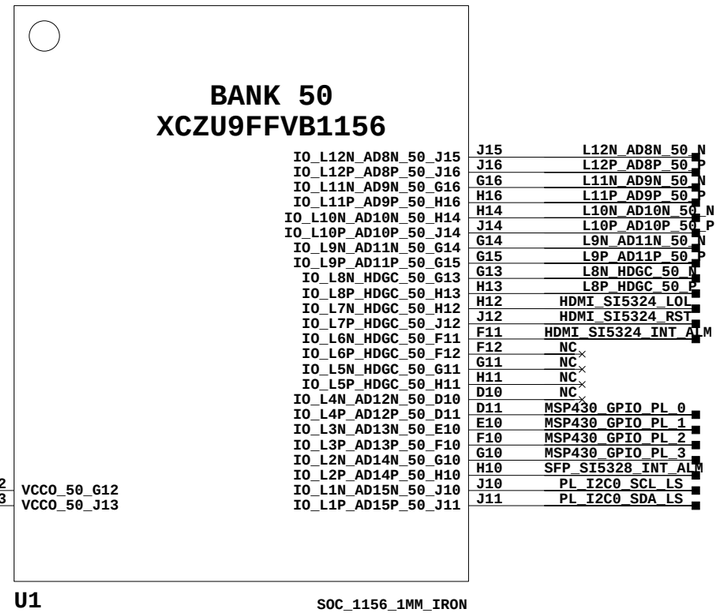


Zynq Banks 47 48

XILINX

TITLE: Zynq Banks 47 48 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 5 OF 87	DRAWN BY: BF



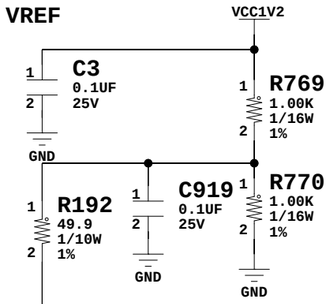


Zynq Banks 49 50

TITLE: Zynq Banks 49 50 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 6 OF 87	DRAWN BY: BF

Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via



SOC_DA7_FFVB1156_IRONWOOD

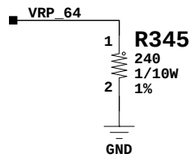
BANK 64
XCZU9FFVB1156

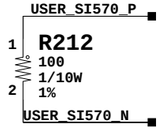
IO_T3U_N12_64_AP1	AP1	DDR4_PAR
IO_L24N_T3U_N11_64_AK2	AK2	DDR4_DQ8
IO_L24P_T3U_N10_64_AK3	AK3	DDR4_DQ9
IO_L23N_T3U_N9_64_AL1	AL1	DDR4_DQ10
IO_L23P_T3U_N8_64_AK1	AK1	DDR4_DQ11
IO_L22N_T3U_N7_DBC_AD0N_64_AL2	AL2	DDR4_DQS1_C
IO_L22P_T3U_N6_DBC_AD0P_64_AL3	AL3	DDR4_DQS1_T
IO_L21N_T3L_N5_AD8N_64_AN1	AN1	DDR4_DQ12
IO_L21P_T3L_N4_AD8P_64_AM1	AM1	DDR4_DQ13
IO_L20N_T3L_N3_AD1N_64_AP3	AP3	DDR4_DQ14
IO_L20P_T3L_N2_AD1P_64_AN3	AN3	DDR4_DQ15
IO_L19N_T3L_N1_DBC_AD9N_64_AP2	AP2	DDR4_CS_B
IO_L19P_T3L_N0_DBC_AD9P_64_AN2	AN2	DDR4_DM1
IO_T2U_N12_64_AM3	AM3	DDR4_CKE
IO_L18N_T2U_N11_AD2N_64_AK4	AK4	DDR4_DQ0
IO_L18P_T2U_N10_AD2P_64_AK5	AK5	DDR4_DQ1
IO_L17N_T2U_N9_AD10N_64_AN4	AN4	DDR4_DQ2
IO_L17P_T2U_N8_AD10P_64_AM4	AM4	DDR4_DQ3
IO_L16N_T2U_N7_QBC_AD3N_64_AP6	AP6	DDR4_DQS0_C
IO_L16P_T2U_N6_QBC_AD3P_64_AN6	AN6	DDR4_DQS0_T
IO_L15N_T2L_N5_AD11N_64_AP4	AP4	DDR4_DQ4
IO_L15P_T2L_N4_AD11P_64_AP5	AP5	DDR4_DQ5
IO_L14N_T2L_N3_GC_64_AM5	AM5	DDR4_DQ6
IO_L14P_T2L_N2_GC_64_AM6	AM6	DDR4_DQ7
IO_L13N_T2L_N1_GC_QBC_64_AL5	AL5	DDR4_A15_CAS_B
IO_L13P_T2L_N0_GC_QBC_64_AL6	AL6	DDR4_DM0
IO_T1U_N12_64_AJ7	AJ7	DDR4_A14_WE_B
IO_L12N_T1U_N11_GC_64_AL7	AL7	USER_SI570_N
IO_L12P_T1U_N10_GC_64_AL8	AL8	USER_SI570_P
IO_L11N_T1U_N9_GC_64_AK7	AK7	DDR4_BG0
IO_L11P_T1U_N8_GC_64_AK8	AK8	DDR4_ACT_B
IO_L10N_T1U_N7_QBC_AD4N_64_AP7	AP7	DDR4_CK_C
IO_L10P_T1U_N6_QBC_AD4P_64_AN7	AN7	DDR4_CK_T
IO_L9N_T1L_N5_AD12N_64_AK9	AK9	DDR4_ODT
IO_L9P_T1L_N4_AD12P_64_AJ9	AJ9	DDR4_A16_RAS_B
IO_L8N_T1L_N3_AD5N_64_AM8	AM8	DDR4_A0
IO_L8P_T1L_N2_AD5P_64_AM9	AM9	DDR4_A1
IO_L7N_T1L_N1_QBC_AD13N_64_AP8	AP8	DDR4_A2
IO_L7P_T1L_N0_QBC_AD13P_64_AN8	AN8	DDR4_A3
IO_T0U_N12_VRP_64_AN11	AN11	VRP_64
IO_L6N_T0U_N11_AD6N_64_AK10	AK10	DDR4_A4
IO_L6P_T0U_N10_AD6P_64_AJ10	AJ10	DDR4_A5
IO_L5N_T0U_N9_AD14N_64_AP9	AP9	DDR4_A6
IO_L5P_T0U_N8_AD14P_64_AN9	AN9	DDR4_A7
IO_L4N_T0U_N7_DBC_AD7N_64_AP10	AP10	DDR4_A8
IO_L4P_T0U_N6_DBC_AD7P_64_AP11	AP11	DDR4_A9
IO_L3N_T0L_N5_AD15N_64_AM10	AM10	DDR4_A10
IO_L3P_T0L_N4_AD15P_64_AL10	AL10	DDR4_A11
IO_L2N_T0L_N3_64_AM11	AM11	DDR4_A12
IO_L2P_T0L_N2_64_AL11	AL11	DDR4_A13
IO_L1N_T0L_N1_DBC_64_AK12	AK12	DDR4_BA0
IO_L1P_T0L_N0_DBC_64_AJ12	AJ12	DDR4_BA1
VREF_64_AJ11	AJ11	

AJ8	VCCO_64_AJ8	VCC1V2
AK11	VCCO_64_AK11	VCC1V2
AL9	VCCO_64_AL9	VCC1V2

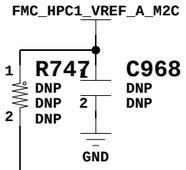
U1

SOC_1156_1MM_IRON





SOC_DA7_FFVB1156_IRONWOOD



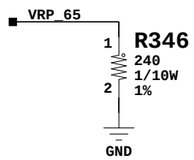
BANK 65
XCZU9FFVB1156

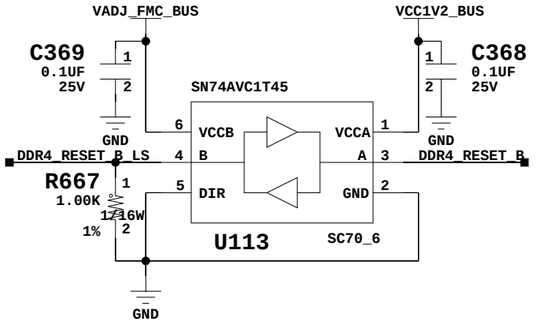
IO_T3U_N12_65_AG1	AG1	NC
IO_L24N_T3U_N11_PERSTN0_65_AE1	AE1	FMC_HPC1_LA09_N
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65_AE2	AE2	FMC_HPC1_LA09_P
IO_L23N_T3U_N9_65_AD1	AD1	FMC_HPC1_LA02_N
IO_L23P_T3U_N8_I2C_SCLK_65_AD2	AD2	FMC_HPC1_LA02_P
IO_L22N_T3U_N7_DBC_AD0N_65_AJ1	AJ1	FMC_HPC1_LA03_N
IO_L22P_T3U_N6_DBC_AD0P_65_AH1	AH1	FMC_HPC1_LA03_P
IO_L21N_T3L_N5_AD8N_65_AF1	AF1	FMC_HPC1_LA04_N
IO_L21P_T3L_N4_AD8P_65_AF2	AF2	FMC_HPC1_LA04_P
IO_L20N_T3L_N3_AD1N_65_AH3	AH3	FMC_HPC1_LA05_N
IO_L20P_T3L_N2_AD1P_65_AG3	AG3	FMC_HPC1_LA05_P
IO_L19N_T3L_N1_DBC_AD9N_65_AJ2	AJ2	FMC_HPC1_LA06_N
IO_L19P_T3L_N0_DBC_AD9P_65_AH2	AH2	FMC_HPC1_LA06_P
IO_T2U_N12_65_AD5	AD5	NC
IO_L18N_T2U_N11_AD2N_65_AE4	AE4	FMC_HPC1_LA07_N
IO_L18P_T2U_N10_AD2P_65_AD4	AD4	FMC_HPC1_LA07_P
IO_L17N_T2U_N9_AD10N_65_AF3	AF3	FMC_HPC1_LA08_N
IO_L17P_T2U_N8_AD10P_65_AE3	AE3	FMC_HPC1_LA08_P
IO_L16N_T2U_N7_QBC_AD3N_65_AJ5	AJ5	FMC_HPC1_LA01_CC_N
IO_L16P_T2U_N6_QBC_AD3P_65_AJ6	AJ6	FMC_HPC1_LA01_CC_P
IO_L15N_T2L_N5_AD11N_65_AJ4	AJ4	FMC_HPC1_LA10_N
IO_L15P_T2L_N4_AD11P_65_AH4	AH4	FMC_HPC1_LA10_P
IO_L14N_T2L_N3_GC_65_AG4	AG4	HDMI_REC_CLOCK_C_N
IO_L14P_T2L_N2_GC_65_AG5	AG5	HDMI_REC_CLOCK_C_P
IO_L13N_T2L_N1_GC_QBC_65_AF5	AF5	FMC_HPC1_LA00_CC_N
IO_L13P_T2L_N0_GC_QBC_65_AE5	AE5	FMC_HPC1_LA00_CC_P
IO_T1U_N12_65_AH9	AH9	DDR4_RESET_B_LS
IO_L12N_T1U_N11_GC_65_AF7	AF7	FMC_HPC1_CLK0_M2C_N
IO_L12P_T1U_N10_GC_65_AE7	AE7	FMC_HPC1_CLK0_M2C_P
IO_L11N_T1U_N9_GC_65_AG6	AG6	HDMI_TX_LVDS_OUT_N
IO_L11P_T1U_N8_GC_65_AF6	AF6	HDMI_TX_LVDS_OUT_P
IO_L10N_T1U_N7_QBC_AD4N_65_AF8	AF8	FMC_HPC1_LA11_N
IO_L10P_T1U_N6_QBC_AD4P_65_AE8	AE8	FMC_HPC1_LA11_P
IO_L9N_T1L_N5_AD12N_65_AD6	AD6	FMC_HPC1_LA12_N
IO_L9P_T1L_N4_AD12P_65_AD7	AD7	FMC_HPC1_LA12_P
IO_L8N_T1L_N3_AD5N_65_AH8	AH8	FMC_HPC1_LA13_N
IO_L8P_T1L_N2_AD5P_65_AG8	AG8	FMC_HPC1_LA13_P
IO_L7N_T1L_N1_QBC_AD13N_65_AH6	AH6	FMC_HPC1_LA14_N
IO_L7P_T1L_N0_QBC_AD13P_65_AH7	AH7	FMC_HPC1_LA14_P
IO_T0U_N12_VRP_65_AD9	AD9	VRP_65
IO_L6N_T0U_N11_AD6N_65_AE9	AE9	FMC_HPC1_LA15_N
IO_L6P_T0U_N10_AD6P_65_AD10	AD10	FMC_HPC1_LA15_P
IO_L5N_T0U_N9_AD14N_65_AG9	AG9	FMC_HPC1_LA16_N
IO_L5P_T0U_N8_AD14P_65_AG10	AG10	FMC_HPC1_LA16_P
IO_L4N_T0U_N7_DBC_AD7N_65_AG11	AG11	FMC_HPC1_LA22_N
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65_AF11	AF11	FMC_HPC1_LA22_P
IO_L3N_T0L_N5_AD15N_65_AF12	AF12	FMC_HPC1_LA23_N
IO_L3P_T0L_N4_AD15P_65_AE12	AE12	FMC_HPC1_LA23_P
IO_L2N_T0L_N3_65_AH11	AH11	FMC_HPC1_LA24_N
IO_L2P_T0L_N2_65_AH12	AH12	FMC_HPC1_LA24_P
IO_L1N_T0L_N1_DBC_65_AF10	AF10	FMC_HPC1_LA25_N
IO_L1P_T0L_N0_DBC_65_AE10	AE10	FMC_HPC1_LA25_P
VREF_65_AD11	AD11	

AD8	VCCO_65_AD8	VADJ_FMC
AF9	VCCO_65_AF9	VADJ_FMC
AG7	VCCO_65_AG7	VADJ_FMC

U1

SOC_1156_1MM_IRON





Zynq Banks 64 65

XILINX

TITLE: Zynq Banks 64 65 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 7 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

FMC_HPC0_VREF_A_M2C

R748 DNP DNP DNP

C969 DNP DNP DNP

GND

BANK 66
XCZU9FFVB1156

IO_T3U_N12_66_AB1	AB1	NC
IO_L24N_T3U_N11_66_W1	W1	FMC_HPC0_LA09_N
IO_L24P_T3U_N10_66_W2	W2	FMC_HPC0_LA09_P
IO_L23N_T3U_N9_66_V1	V1	FMC_HPC0_LA02_N
IO_L23P_T3U_N8_66_V2	V2	FMC_HPC0_LA02_P
IO_L22N_T3U_N7_DBC_AD0N_66_Y1	Y1	FMC_HPC0_LA03_N
IO_L22P_T3U_N6_DBC_AD0P_66_Y2	Y2	FMC_HPC0_LA03_P
IO_L21N_T3L_N5_AD8N_66_AA1	AA1	FMC_HPC0_LA04_N
IO_L21P_T3L_N4_AD8P_66_AA2	AA2	FMC_HPC0_LA04_P
IO_L20N_T3L_N3_AD1N_66_AC3	AC3	FMC_HPC0_LA05_N
IO_L20P_T3L_N2_AD1P_66_AB3	AB3	FMC_HPC0_LA05_P
IO_L19N_T3L_N1_DBC_AD9N_66_AC1	AC1	FMC_HPC0_LA06_N
IO_L19P_T3L_N0_DBC_AD9P_66_AC2	AC2	FMC_HPC0_LA06_P
IO_T2U_N12_66_AA3	AA3	NC
IO_L18N_T2U_N11_AD2N_66_U4	U4	FMC_HPC0_LA07_N
IO_L18P_T2U_N10_AD2P_66_U5	U5	FMC_HPC0_LA07_P
IO_L17N_T2U_N9_AD10N_66_V3	V3	FMC_HPC0_LA08_N
IO_L17P_T2U_N8_AD10P_66_V4	V4	FMC_HPC0_LA08_P
IO_L16N_T2U_N7_QBC_AD3N_66_AC4	AC4	FMC_HPC0_LA01_CC_N
IO_L16P_T2U_N6_QBC_AD3P_66_AB4	AB4	FMC_HPC0_LA01_CC_P
IO_L15N_T2L_N5_AD11N_66_W4	W4	FMC_HPC0_LA10_N
IO_L15P_T2L_N4_AD11P_66_W5	W5	FMC_HPC0_LA10_P
IO_L14N_T2L_N3_GC_66_AA5	AA5	FMC_HPC1_LA17_CC_N
IO_L14P_T2L_N2_GC_66_Y5	Y5	FMC_HPC1_LA17_CC_P
IO_L13N_T2L_N1_GC_QBC_66_Y3	Y3	FMC_HPC0_LA00_CC_N
IO_L13P_T2L_N0_GC_QBC_66_Y4	Y4	FMC_HPC0_LA00_CC_P
IO_T1U_N12_66_AA8	AA8	NC
IO_L12N_T1U_N11_GC_66_AA6	AA6	FMC_HPC0_CLK0_M2C_N
IO_L12P_T1U_N10_GC_66_AA7	AA7	FMC_HPC0_CLK0_M2C_P
IO_L11N_T1U_N9_GC_66_Y7	Y7	FMC_HPC1_LA18_CC_N
IO_L11P_T1U_N8_GC_66_Y8	Y8	FMC_HPC1_LA18_CC_P
IO_L10N_T1U_N7_QBC_AD4N_66_AB5	AB5	FMC_HPC0_LA11_N
IO_L10P_T1U_N6_QBC_AD4P_66_AB6	AB6	FMC_HPC0_LA11_P
IO_L9N_T1L_N5_AD12N_66_W6	W6	FMC_HPC0_LA12_N
IO_L9P_T1L_N4_AD12P_66_W7	W7	FMC_HPC0_LA12_P
IO_L8N_T1L_N3_AD5N_66_AC8	AC8	FMC_HPC0_LA13_N
IO_L8P_T1L_N2_AD5P_66_AB8	AB8	FMC_HPC0_LA13_P
IO_L7N_T1L_N1_QBC_AD13N_66_AC6	AC6	FMC_HPC0_LA14_N
IO_L7P_T1L_N0_QBC_AD13P_66_AC7	AC7	FMC_HPC0_LA14_P
IO_T0U_N12_VRP_66_W9	W9	NC
IO_L6N_T0U_N11_AD6N_66_Y9	Y9	FMC_HPC0_LA15_N
IO_L6P_T0U_N10_AD6P_66_Y10	Y10	FMC_HPC0_LA15_P
IO_L5N_T0U_N9_AD14N_66_AA12	AA12	FMC_HPC0_LA16_N
IO_L5P_T0U_N8_AD14P_66_Y12	Y12	FMC_HPC0_LA16_P
IO_L4N_T0U_N7_DBC_AD7N_66_AC9	AC9	NC
IO_L4P_T0U_N6_DBC_AD7P_66_AB9	AB9	NC
IO_L3N_T0L_N5_AD15N_66_AA10	AA10	FMC_HPC1_LA19_N
IO_L3P_T0L_N4_AD15P_66_AA11	AA11	FMC_HPC1_LA19_P
IO_L2N_T0L_N3_66_AB10	AB10	FMC_HPC1_LA20_N
IO_L2P_T0L_N2_66_AB11	AB11	FMC_HPC1_LA20_P
IO_L1N_T0L_N1_DBC_66_AC11	AC11	FMC_HPC1_LA21_N
IO_L1P_T0L_N0_DBC_66_AC12	AC12	FMC_HPC1_LA21_P
VREF_66_AD12	AD12	

VADJ_FMC

AA9	VCCO_66_AA9
W8	VCCO_66_W8
Y11	VCCO_66_Y11

U1

SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

FMC_HPC0_VREF_A_M2C

R749 DNP DNP DNP

C970 DNP DNP DNP

GND

BANK 67
XCZU9FFVB1156

IO_T3U_N12_67_K14	K14	NC
IO_L24N_T3U_N11_67_K15	K15	FMC_HPC0_LA26_N
IO_L24P_T3U_N10_67_L15	L15	FMC_HPC0_LA26_P
IO_L23N_T3U_N9_67_K13	K13	FMC_HPC0_LA19_N
IO_L23P_T3U_N8_67_L13	L13	FMC_HPC0_LA19_P
IO_L22N_T3U_N7_DBC_AD0N_67_M13	M13	FMC_HPC0_LA20_N
IO_L22P_T3U_N6_DBC_AD0P_67_N13	N13	FMC_HPC0_LA20_P
IO_L21N_T3L_N5_AD8N_67_N12	N12	FMC_HPC0_LA21_N
IO_L21P_T3L_N4_AD8P_67_P12	P12	FMC_HPC0_LA21_P
IO_L20N_T3L_N3_AD1N_67_M14	M14	FMC_HPC0_LA22_N
IO_L20P_T3L_N2_AD1P_67_M15	M15	FMC_HPC0_LA22_P
IO_L19N_T3L_N1_DBC_AD9N_67_K16	K16	FMC_HPC0_LA23_N
IO_L19P_T3L_N0_DBC_AD9P_67_L16	L16	FMC_HPC0_LA23_P
IO_T2U_N12_67_K10	K10	NC
IO_L18N_T2U_N11_AD2N_67_K12	K12	FMC_HPC0_LA24_N
IO_L18P_T2U_N10_AD2P_67_L12	L12	FMC_HPC0_LA24_P
IO_L17N_T2U_N9_AD10N_67_L11	L11	FMC_HPC0_LA25_N
IO_L17P_T2U_N8_AD10P_67_M11	M11	FMC_HPC0_LA25_P
IO_L16N_T2U_N7_QBC_AD3N_67_N8	N8	FMC_HPC0_LA18_CC_N
IO_L16P_T2U_N6_QBC_AD3P_67_N9	N9	FMC_HPC0_LA18_CC_P
IO_L15N_T2L_N5_AD11N_67_L10	L10	FMC_HPC0_LA27_N
IO_L15P_T2L_N4_AD11P_67_M10	M10	FMC_HPC0_LA27_P
IO_L14N_T2L_N3_GC_67_P9	P9	FMC_HPC1_CLK1_M2C_N
IO_L14P_T2L_N2_GC_67_P10	P10	FMC_HPC1_CLK1_M2C_P
IO_L13N_T2L_N1_GC_QBC_67_N11	N11	FMC_HPC0_LA17_CC_N
IO_L13P_T2L_N0_GC_QBC_67_P11	P11	FMC_HPC0_LA17_CC_P
IO_T1U_N12_67_V9	V9	NC
IO_L12N_T1U_N11_GC_67_R8	R8	FMC_HPC0_CLK1_M2C_N
IO_L12P_T1U_N10_GC_67_T8	T8	FMC_HPC0_CLK1_M2C_P
IO_L11N_T1U_N9_GC_67_R9	R9	SFP_REC_CLOCK_C_N
IO_L11P_T1U_N8_GC_67_R10	R10	SFP_REC_CLOCK_C_P
IO_L10N_T1U_N7_QBC_AD4N_67_T6	T6	FMC_HPC0_LA28_N
IO_L10P_T1U_N6_QBC_AD4P_67_T7	T7	FMC_HPC0_LA28_P
IO_L9N_T1L_N5_AD12N_67_U8	U8	FMC_HPC0_LA29_N
IO_L9P_T1L_N4_AD12P_67_U9	U9	FMC_HPC0_LA29_P
IO_L8N_T1L_N3_AD5N_67_U6	U6	FMC_HPC0_LA30_N
IO_L8P_T1L_N2_AD5P_67_V6	V6	FMC_HPC0_LA30_P
IO_L7N_T1L_N1_QBC_AD13N_67_V7	V7	FMC_HPC0_LA31_N
IO_L7P_T1L_N0_QBC_AD13P_67_V8	V8	FMC_HPC0_LA31_P
IO_T0U_N12_VRP_67_W10	W10	NC
IO_L6N_T0U_N11_AD6N_67_T11	T11	FMC_HPC0_LA32_N
IO_L6P_T0U_N10_AD6P_67_U11	U11	FMC_HPC0_LA32_P
IO_L5N_T0U_N9_AD14N_67_V11	V11	FMC_HPC0_LA33_N
IO_L5P_T0U_N8_AD14P_67_V12	V12	FMC_HPC0_LA33_P
IO_L4N_T0U_N7_DBC_AD7N_67_R12	R12	FMC_HPC1_LA26_N
IO_L4P_T0U_N6_DBC_AD7P_67_T12	T12	FMC_HPC1_LA26_P
IO_L3N_T0L_N5_AD15N_67_T10	T10	FMC_HPC1_LA27_N
IO_L3P_T0L_N4_AD15P_67_U10	U10	FMC_HPC1_LA27_P
IO_L2N_T0L_N3_67_R13	R13	FMC_HPC1_LA28_N
IO_L2P_T0L_N2_67_T13	T13	FMC_HPC1_LA28_P
IO_L1N_T0L_N1_DBC_67_W11	W11	FMC_HPC1_LA29_N
IO_L1P_T0L_N0_DBC_67_W12	W12	FMC_HPC1_LA29_P
VREF_67_N14	N14	

VADJ_FMC

P8	VCCO_67_P8
T9	VCCO_67_T9
U7	VCCO_67_U7

U1

SOC_1156_1MM_IRON

Zynq Banks 66 67

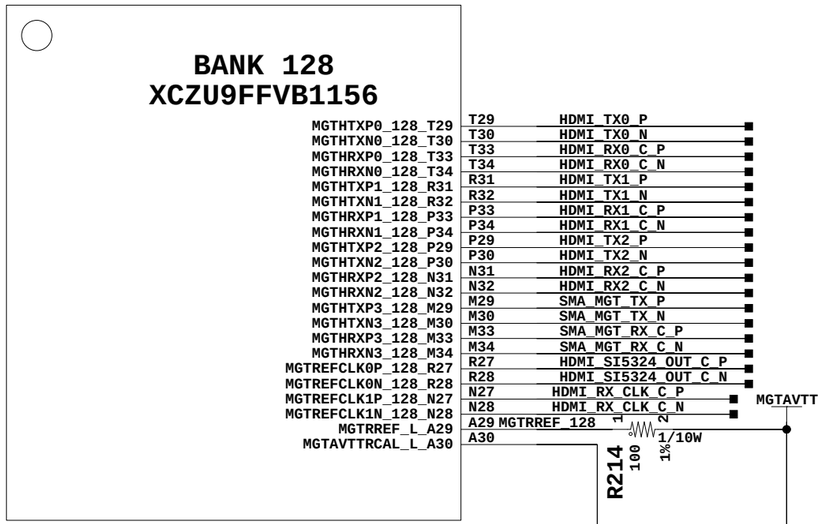
XILINX

TITLE: Zynq Banks 66 67
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

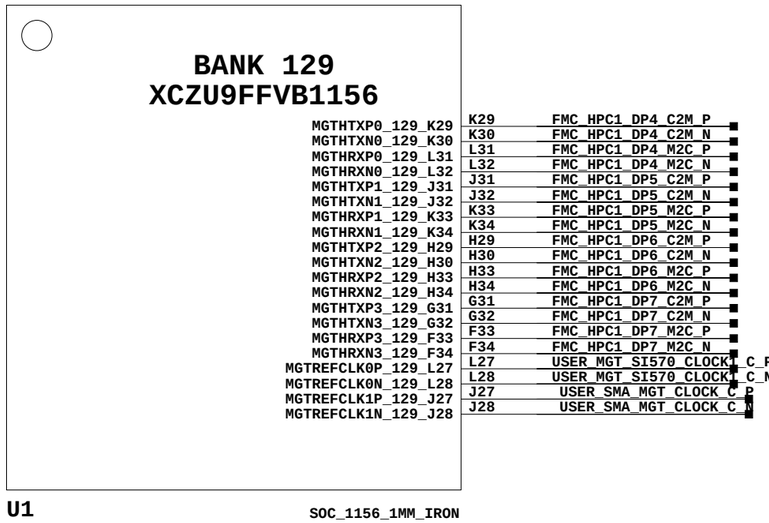
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 8 OF 87	DRAWN BY: BF

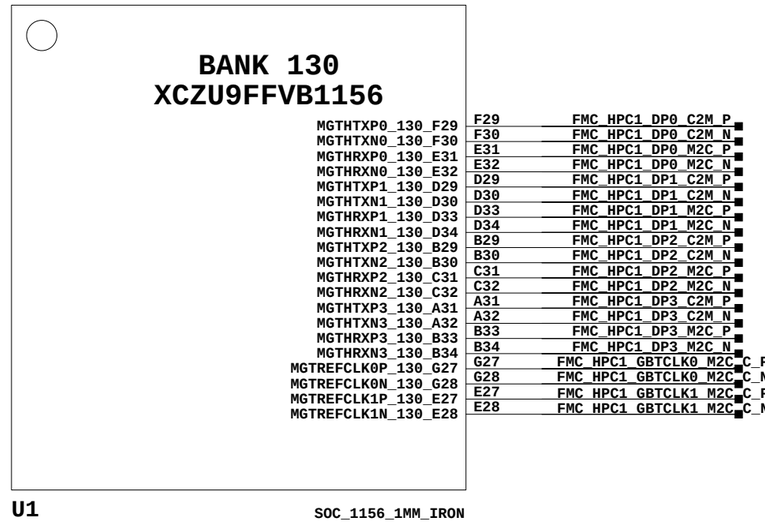
SOC_DA7_FFVB1156_IRONWOOD

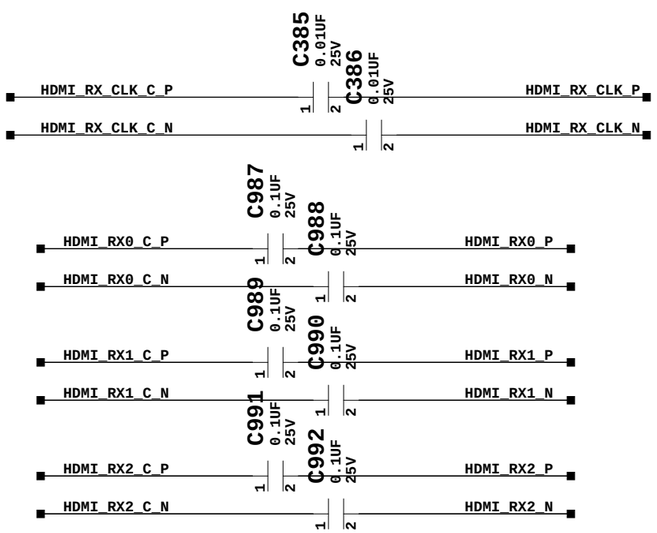


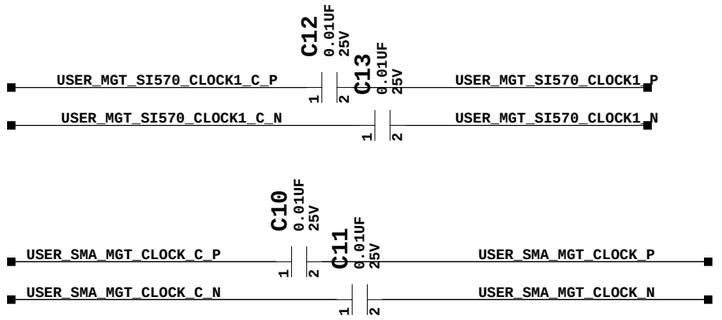
SOC_DA7_FFVB1156_IRONWOOD

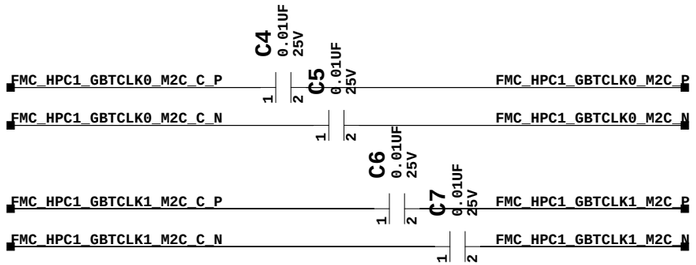


SOC_DA7_FFVB1156_IRONWOOD









Zynq Banks 128 129 130

XILINX

TITLE: Zynq Banks 128 129 130 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 9 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 228
XCZU9FFVB1156

MGTHTXP0_228_R4	R4	FMC_HPC0_DP6_C2M_P
MGTHTXN0_228_R3	R3	FMC_HPC0_DP6_C2M_N
MGTHRXP0_228_T2	T2	FMC_HPC0_DP6_M2C_P
MGTHRXN0_228_T1	T1	FMC_HPC0_DP6_M2C_N
MGTHTXP1_228_P6	P6	FMC_HPC0_DP5_C2M_P
MGTHTXN1_228_P5	P5	FMC_HPC0_DP5_C2M_N
MGTHRXP1_228_P2	P2	FMC_HPC0_DP5_M2C_P
MGTHRXN1_228_P1	P1	FMC_HPC0_DP5_M2C_N
MGTHTXP2_228_N4	N4	FMC_HPC0_DP7_C2M_P
MGTHTXN2_228_N3	N3	FMC_HPC0_DP7_C2M_N
MGTHRXP2_228_M2	M2	FMC_HPC0_DP7_M2C_P
MGTHRXN2_228_M1	M1	FMC_HPC0_DP7_M2C_N
MGTHTXP3_228_M6	M6	FMC_HPC0_DP4_C2M_P
MGTHTXN3_228_M5	M5	FMC_HPC0_DP4_C2M_N
MGTHRXP3_228_L4	L4	FMC_HPC0_DP4_M2C_P
MGTHRXN3_228_L3	L3	FMC_HPC0_DP4_M2C_N
MGTREFCLK0P_228_L8	L8	FMC_HPC0_GBTCLK1_M2C_C_P
MGTREFCLK0N_228_L7	L7	FMC_HPC0_GBTCLK1_M2C_C_N
MGTREFCLK1P_228_J8	J8	NC
MGTREFCLK1N_228_J7	J7	NC
MGTREF_R_A6	A6	
MGTAVTTRCAL_R_A5	A5	

MGTAVTT

R236 100 1%

U1

SOC_1156_1MM_IRON

C169 0.01UF 25V
C170 0.01UF 25V
C171 0.01UF 25V
C172 0.01UF 25V

FMC_HPC0_GBTCLK0_M2C_C_P	FMC_HPC0_GBTCLK0_M2C_P
FMC_HPC0_GBTCLK0_M2C_C_N	FMC_HPC0_GBTCLK0_M2C_N
FMC_HPC0_GBTCLK1_M2C_C_P	FMC_HPC0_GBTCLK1_M2C_P
FMC_HPC0_GBTCLK1_M2C_C_N	FMC_HPC0_GBTCLK1_M2C_N

SOC_DA7_FFVB1156_IRONWOOD

BANK 229
XCZU9FFVB1156

MGTHTXP0_229_K6	K6	FMC_HPC0_DP3_C2M_P
MGTHTXN0_229_K5	K5	FMC_HPC0_DP3_C2M_N
MGTHRXP0_229_K2	K2	FMC_HPC0_DP3_M2C_P
MGTHRXN0_229_K1	K1	FMC_HPC0_DP3_M2C_N
MGTHTXP1_229_H6	H6	FMC_HPC0_DP1_C2M_P
MGTHTXN1_229_H5	H5	FMC_HPC0_DP1_C2M_N
MGTHRXP1_229_J4	J4	FMC_HPC0_DP1_M2C_P
MGTHRXN1_229_J3	J3	FMC_HPC0_DP1_M2C_N
MGTHTXP2_229_G4	G4	FMC_HPC0_DP0_C2M_P
MGTHTXN2_229_G3	G3	FMC_HPC0_DP0_C2M_N
MGTHRXP2_229_H2	H2	FMC_HPC0_DP0_M2C_P
MGTHRXN2_229_H1	H1	FMC_HPC0_DP0_M2C_N
MGTHTXP3_229_F6	F6	FMC_HPC0_DP2_C2M_P
MGTHTXN3_229_F5	F5	FMC_HPC0_DP2_C2M_N
MGTHRXP3_229_F2	F2	FMC_HPC0_DP2_M2C_P
MGTHRXN3_229_F1	F1	FMC_HPC0_DP2_M2C_N
MGTREFCLK0P_229_G8	G8	FMC_HPC0_GBTCLK0_M2C_C_P
MGTREFCLK0N_229_G7	G7	FMC_HPC0_GBTCLK0_M2C_C_N
MGTREFCLK1P_229_E8	E8	NC
MGTREFCLK1N_229_E7	E7	NC

U1

SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK 230
XCZU9FFVB1156

MGTHTXP0_230_E4	E4	SFP0_TX_P
MGTHTXN0_230_E3	E3	SFP0_TX_N
MGTHRXP0_230_D2	D2	SFP0_RX_P
MGTHRXN0_230_D1	D1	SFP0_RX_N
MGTHTXP1_230_D6	D6	SFP1_TX_P
MGTHTXN1_230_D5	D5	SFP1_TX_N
MGTHRXP1_230_C4	C4	SFP1_RX_P
MGTHRXN1_230_C3	C3	SFP1_RX_N
MGTHTXP2_230_B6	B6	SFP2_TX_P
MGTHTXN2_230_B5	B5	SFP2_TX_N
MGTHRXP2_230_B2	B2	SFP2_RX_P
MGTHRXN2_230_B1	B1	SFP2_RX_N
MGTHTXP3_230_A8	A8	SFP3_TX_P
MGTHTXN3_230_A7	A7	SFP3_TX_N
MGTHRXP3_230_A4	A4	SFP3_RX_P
MGTHRXN3_230_A3	A3	SFP3_RX_N
MGTREFCLK0P_230_C8	C8	USER_MGT_SI570_CLOCK2_C_P
MGTREFCLK0N_230_C7	C7	USER_MGT_SI570_CLOCK2_C_N
MGTREFCLK1P_230_B10	B10	SFP_SI5328_OUT_C_P
MGTREFCLK1N_230_B9	B9	SFP_SI5328_OUT_C_N

U1

SOC_1156_1MM_IRON

C206 0.01UF 25V
C207 0.01UF 25V

USER_MGT_SI570_CLOCK2_C_P	USER_MGT_SI570_CLOCK2_P
USER_MGT_SI570_CLOCK2_C_N	USER_MGT_SI570_CLOCK2_N

Zynq Banks 228 229 230

XILINX

TITLE: Zynq Banks 228 229 230
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0

ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179

DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 10 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 500
XCZU9FFVB1156

PS_MIO25_AE19	AE19	MIO25_CAN_RX
PS_MIO24_AE20	AE20	MIO24_CAN_TX
PS_MIO23_AD19	AD19	MIO23_LED
PS_MIO22_AD20	AD20	MIO22_BUTTON
PS_MIO21_AF18	AF18	MIO21_UART1_RXD
PS_MIO20_AD18	AD18	MIO20_UART1_TXD
PS_MIO19_AL17	AL17	MIO19_UART0_TXD
PS_MIO18_AE18	AE18	MIO18_UART0_RXD
PS_MIO17_AP16	AP16	MIO17_I2C1_SDA
PS_MIO16_AM16	AM16	MIO16_I2C1_SCL
PS_MIO15_AN16	AN16	MIO15_I2C0_SDA
PS_MIO14_AL16	AL16	MIO14_I2C0_SCL
PS_MIO13_AK17	AK17	MIO13_PS_GPIO2
PS_MIO12_AJ17	AJ17	MIO12_QSPI_UPR_CLK
PS_MIO11_AF17	AF17	MIO11_QSPI_UPR_DQ3
PS_MIO10_AH17	AH17	MIO10_QSPI_UPR_DQ2
PS_MIO9_AP15	AP15	MIO9_QSPI_UPR_DQ1
PS_MIO8_AE17	AE17	MIO8_QSPI_UPR_DQ0
PS_MIO7_AD17	AD17	MIO7_QSPI_UPR_CS_B
PS_MIO6_AL15	AL15	NC
PS_MIO5_AM15	AM15	MIO5_QSPI_LWR_CS_B
PS_MIO4_AH16	AH16	MIO4_QSPI_LWR_DQ0
PS_MIO3_AG16	AG16	MIO3_QSPI_LWR_DQ3
PS_MIO2_AD16	AD16	MIO2_QSPI_LWR_DQ2
PS_MIO1_AJ16	AJ16	MIO1_QSPI_LWR_DQ1
PS_MIO0_AF16	AF16	MIO0_QSPI_LWR_CLK

VCCOPS

AE16	VCCO_PSIO0_500_AE16
AG17	VCCO_PSIO0_500_AG17
AK16	VCCO_PSIO0_500_AK16

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK 501
XCZU9FFVB1156

PS_MIO51_N25	N25	MIO51_SDIO_CLK_R
PS_MIO50_P25	P25	MIO50_SDIO_CMD_R
PS_MIO49_K25	K25	MIO49_SDIO_DAT3_R
PS_MIO48_M25	M25	MIO48_SDIO_DAT2_R
PS_MIO47_L25	L25	MIO47_SDIO_DAT1_R
PS_MIO46_J25	J25	MIO46_SDIO_DAT0_R
PS_MIO45_P24	P24	MIO45_SDIO_DETECT
PS_MIO44_N24	N24	MIO44_SDIO_PROTECT
PS_MIO43_K24	K24	NC
PS_MIO42_M24	M24	MIO42_SDIO_DIR_DAT1_3
PS_MIO41_J24	J24	MIO41_SDIO_DIR_DAT0
PS_MIO40_M23	M23	MIO40_SDIO_DIR_CMD
PS_MIO39_N23	N23	MIO39_SDIO_SEL
PS_MIO38_L23	L23	MIO38_PS_GPIO1
PS_MIO37_N22	N22	MIO37_PMU_GPO5
PS_MIO36_K23	K23	MIO36_PMU_GPO4
PS_MIO35_P22	P22	MIO35_PMU_GPO3
PS_MIO34_L22	L22	MIO34_PMU_GPO2
PS_MIO33_H23	H23	MIO33_PMU_GPO1
PS_MIO32_H22	H22	MIO32_PMU_GPO0
PS_MIO31_J22	J22	MIO31_PCIE_RESET_N
PS_MIO30_L21	L21	MIO30_DP_AUX_IN
PS_MIO29_K22	K22	MIO29_DP_OE
PS_MIO28_N21	N21	MIO28_DP_HPD
PS_MIO27_M21	M21	MIO27_DP_AUX_OUT
PS_MIO26_P21	P21	MIO26_PMU_INPUT

R931 30 R934 30 R935 30 R936 30 R937 30 R938 30

MIO51_SDIO_CLK_R	R931	MIO51_SDIO_CLK
MIO50_SDIO_CMD_R	R934	MIO50_SDIO_CMD
MIO49_SDIO_DAT3_R	R935	MIO49_SDIO_DAT3
MIO48_SDIO_DAT2_R	R936	MIO48_SDIO_DAT2
MIO47_SDIO_DAT1_R	R937	MIO47_SDIO_DAT1
MIO46_SDIO_DAT0_R	R938	MIO46_SDIO_DAT0

VCCOPS

L24	VCCO_PSIO1_501_L24
M22	VCCO_PSIO1_501_M22

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK 502
XCZU9FFVB1156

PS_MIO77_F25	F25	MIO77_ENET_MDIO
PS_MIO76_H25	H25	MIO76_ENET_MDC
PS_MIO75_D25	D25	MIO75_ENET_RX_CTRL
PS_MIO74_G25	G25	MIO74_ENET_RX_D3
PS_MIO73_H24	H24	MIO73_ENET_RX_D2
PS_MIO72_E25	E25	MIO72_ENET_RX_D1
PS_MIO71_C27	C27	MIO71_ENET_RX_D0
PS_MIO70_C26	C26	MIO70_ENET_RX_CLK
PS_MIO69_B27	B27	MIO69_ENET_TX_CTRL
PS_MIO68_B26	B26	MIO68_ENET_TX_D3
PS_MIO67_B25	B25	MIO67_ENET_TX_D2
PS_MIO66_A27	A27	MIO66_ENET_TX_D1
PS_MIO65_A26	A26	MIO65_ENET_TX_D0
PS_MIO64_A25	A25	MIO64_ENET_TX_CLK
PS_MIO63_D24	D24	MIO63_USB_DATA7_R
PS_MIO62_G24	G24	MIO62_USB_DATA6_R
PS_MIO61_C24	C24	MIO61_USB_DATA5_R
PS_MIO60_E24	E24	MIO60_USB_DATA4_R
PS_MIO59_B24	B24	MIO59_USB_DATA3_R
PS_MIO58_G23	G23	MIO58_USB_STP_R
PS_MIO57_A23	A23	MIO57_USB_DATA1_R
PS_MIO56_C23	C23	MIO56_USB_DATA0_R
PS_MIO55_B23	B23	MIO55_USB_NXT
PS_MIO54_F23	F23	MIO54_USB_DATA2_R
PS_MIO53_E23	E23	MIO53_USB_DIR
PS_MIO52_F22	F22	MIO52_USB_CLK

R941 30 R942 30 R943 30 R944 30 R945 30 R946 30 R947 30 R949 30 R948 30

MIO63_USB_DATA7_R	R941	MIO63_USB_DATA7
MIO62_USB_DATA6_R	R942	MIO62_USB_DATA6
MIO61_USB_DATA5_R	R943	MIO61_USB_DATA5
MIO60_USB_DATA4_R	R944	MIO60_USB_DATA4
MIO59_USB_DATA3_R	R945	MIO59_USB_DATA3
MIO58_USB_STP_R	R946	MIO58_USB_STP
MIO57_USB_DATA1_R	R947	MIO57_USB_DATA1
MIO56_USB_DATA0_R	R949	MIO56_USB_DATA0
MIO54_USB_DATA2_R	R948	MIO54_USB_DATA2

VCCOPS

D23	VCCO_PSIO2_502_D23
F24	VCCO_PSIO2_502_F24
G22	VCCO_PSIO2_502_G22

U1 SOC_1156_1MM_IRON

Zynq Banks 500 501 502 - MIO

XILINX

TITLE: Zynq Banks 500 501 502 - MIO SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 11 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 503
XCZU9FFVB1156

U1

SOC_1156_1MM_IRON

PS_POR_B_V23
PS_ERROR_STATUS_R21
PS_ERROR_OUT_T21
PS_SRST_B_U23
PS_REF_CLK_U24
PS_JTAG_TCK_R25
PS_JTAG_TMS_R24
PS_JTAG_TDO_T25
PS_JTAG_TDI_U25
PS_INIT_B_V24
PS_PROG_B_U21
PS_DONE_W21
PS_PADI_V21
PS_PADO_V22
PS_MODE3_R23
PS_MODE2_T23
PS_MODE1_R22
PS_MODE0_T22

V23 PS_POR_B
R21 PS_ERR_STATUS
T21 PS_ERR_OUT
U23 PS_SRST_B
U24 PS_REF_CLK
R25 JTAG_TCK
R24 JTAG_TMS
T25 FPGA_TDO_FMC_TDI
U25 JTAG_TDI
V24 PS_INIT_B
U21 PS_PROG_B
W21 PS_DONE
V21 PS_PADI
V22 PS_PADO
R23
T23
R22
T22

VCCOPS3
T24 VCCO_PSIO3_503_T24
U22 VCCO_PSIO3_503_U22

R921 20 1/16W 1%
C1033 33PF 50V C0G, NP0
GND

VCCOPS3_BUS
R19 R18 R17 R16 4.70K 1/16W 1%
SDA04H1SBD
SW6
PS_MODE3
PS_MODE2
PS_MODE1
PS_MODE0

PS_PADI
PS_PADO
R143 4.7M 1/10W 5%
32.768KHZ
X1
X2
20PPM
X5
C876 22PF 50V
C875 22PF 50V
GND

1.8V
VCCOPS3_BUS
UTIL_3V3
C183 0.1UF 25V
R15 4.70K 1/16W 1%
C86 0.1UF 25V
R323 261 1/10W 1%
LED-GRN-RED
DS1
R326 261 1/10W 1%
SN74AVC1T45
U43
SC70_6
PS_INIT_B
INIT_B = 0, RED LED ON
INIT_B = 1, GRN LED ON

R237 R238 R239 R240 499 1/10W 1%

C181 0.1UF 25V
R13 4.70K 1/16W 1%
C87 0.1UF 25V
DS32
LED-GRN-SMT
R328 261 1/10W 1%
U44
PS_DONE
DONE_0 = 0, DONE LED OFF
DONE_0 = 1, DONE LED ON

UTIL_3V3
VCCOPS3_BUS
R267 R266 R265 10.0K 1/10W 1%
R241 8.06K 1/10W 1%
MAX16025
C188 0.1UF 25V
J20 HDR_1X2
J21 HDR_1X2
OPEN DRAIN
R273 R272 4.70K 1/16W 1%
R354 261 1/10W 1%
LED-RED-SMT
DS36
R317 R318 DNP
U22
TQFN_16
VCC
OUT1 PS_POR_B_HDR
OUT2 PS_SRST_B_HDR
EN1 PS_POR_SW_B
EN2 PS_SRST_SW_B
MR_B
TOL
TH0 NC
TH1 NC
RST_B POR_RST_B
CDLY1
CDLY2
CRESET
EPAD
GND
IN1 PS_POR_B
IN2 PS_SRST_B
C185 C186 C187 0.1UF 25V
R271 10.0K 1/10W 1%
J22 HDR_1X2

PS_POR_B
Pushbutton
TL3301EF100QG
SW4
PS_SRST_B
Pushbutton
TL3301EF100QG
SW3
BAT54T1G D6
BAT54T1G D5

R355 R356 261 1/10W 1%
LED-RED-SMT DS35
LED-GRN-SMT DS33
Q13 Q14
NDS331N 460MW
R154 R187 499 1/10W 1%
PS_ERR_OUT
PS_ERR_STATUS
PS ERROR STATUS LEDs

1.8V
VCCOPS3_BUS
R14 4.70K 1/16W 1%
Pushbutton
TL3301EF100QG
PS_PROG_B
SW5

Zynq Banks 503 - Config

XILINX

TITLE: Zynq Banks 503 - Config SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 12 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK 504
XCZU9FFVB1156

DDR4_SODIMM_A0	AP29	PS_DDR_A0_AP29	
DDR4_SODIMM_A1	AP30	PS_DDR_A1_AP30	
DDR4_SODIMM_A2	AP26	PS_DDR_A2_AP26	
DDR4_SODIMM_A3	AP27	PS_DDR_A3_AP27	
DDR4_SODIMM_A4	AP25	PS_DDR_A4_AP25	
DDR4_SODIMM_A5	AN24	PS_DDR_A5_AN24	
DDR4_SODIMM_A6	AM29	PS_DDR_A6_AM29	
DDR4_SODIMM_A7	AM28	PS_DDR_A7_AM28	
DDR4_SODIMM_A8	AM26	PS_DDR_A8_AM26	
DDR4_SODIMM_A9	AM25	PS_DDR_A9_AM25	
DDR4_SODIMM_A10	AL28	PS_DDR_A10_AL28	
DDR4_SODIMM_A11	AK27	PS_DDR_A11_AK27	
DDR4_SODIMM_A12	AJ25	PS_DDR_A12_AJ25	
DDR4_SODIMM_A13	AL25	PS_DDR_A13_AL25	
DDR4_SODIMM_WE_B	AK25	PS_DDR_A14_AK25	
DDR4_SODIMM_CAS_B	AK24	PS_DDR_A15_AK24	
DDR4_SODIMM_RAS_B	AM24	PS_DDR_A16_AM24	
NC	AF25	PS_DDR_A17_AF25	
DDR4_SODIMM_BA0	AH26	PS_DDR_BA0_AH26	
DDR4_SODIMM_BA1	AG26	PS_DDR_BA1_AG26	
DDR4_SODIMM_ACT_B	AG25	PS_DDR_ACT_N_AG25	
DDR4_SODIMM_ALERT_B	AF22	PS_DDR_ALERT_N_AF22	
DDR4_SODIMM_PARITY	AF20	PS_DDR_PARITY_AF20	
ZYNQ_DDR4_SODIMM_RESET_B	AF21	PS_DDR_RAM_RST_N_AF21	
DDR4_SODIMM_BG0	AK28	PS_DDR_BG0_AK28	
DDR4_SODIMM_BG1	AH27	PS_DDR_BG1_AH27	
DDR4_SODIMM_CS0_B	AN28	PS_DDR_CS_N0_AN28	
DDR4_SODIMM_CS1_B	AL30	PS_DDR_CS_N1_AL30	
DDR4_SODIMM_CK0_T	AN26	PS_DDR_CK0_AN26	
DDR4_SODIMM_CK0_C	AN27	PS_DDR_CK_N0_AN27	
DDR4_SODIMM_CK1_T	AL26	PS_DDR_CK1_AL26	
DDR4_SODIMM_CK1_C	AL27	PS_DDR_CK_N1_AL27	
DDR4_SODIMM_CKE0	AN29	PS_DDR_CKE0_AN29	
DDR4_SODIMM_CKE1	AJ27	PS_DDR_CKE1_AJ27	
DDR4_SODIMM_ODT0	AM30	PS_DDR_ODT0_AM30	
DDR4_SODIMM_ODT1	AJ26	PS_DDR_ODT1_AJ26	
DDR4_SODIMM_DQS0_T	AN18	PS_DDR_DQS_P0_AN18	
DDR4_SODIMM_DQS0_C	AN19	PS_DDR_DQS_N0_AN19	
DDR4_SODIMM_DQS1_T	AN21	PS_DDR_DQS_P1_AN21	
DDR4_SODIMM_DQS1_C	AN22	PS_DDR_DQS_N1_AN22	
DDR4_SODIMM_DQS2_T	AH19	PS_DDR_DQS_P2_AH19	
DDR4_SODIMM_DQS2_C	AJ19	PS_DDR_DQS_N2_AJ19	
DDR4_SODIMM_DQS3_T	AH22	PS_DDR_DQS_P3_AH22	
DDR4_SODIMM_DQS3_C	AH23	PS_DDR_DQS_N3_AH23	
DDR4_SODIMM_DQS4_T	AH28	PS_DDR_DQS_P4_AH28	
DDR4_SODIMM_DQS4_C	AH29	PS_DDR_DQS_N4_AH29	
DDR4_SODIMM_DQS5_T	AE28	PS_DDR_DQS_P5_AE28	
DDR4_SODIMM_DQS5_C	AE29	PS_DDR_DQS_N5_AE29	
DDR4_SODIMM_DQS6_T	AJ32	PS_DDR_DQS_P6_AJ32	
DDR4_SODIMM_DQS6_C	AK32	PS_DDR_DQS_N6_AK32	
DDR4_SODIMM_DQS7_T	AE32	PS_DDR_DQS_P7_AE32	
DDR4_SODIMM_DQS7_C	AE33	PS_DDR_DQS_N7_AE33	
DDR4_SODIMM_DQS8_T	AN32	PS_DDR_DQS_P8_AN32	
DDR4_SODIMM_DQS8_C	AN33	PS_DDR_DQS_N8_AN33	
DDR4_SODIMM_DM0_B	AN17	PS_DDR_DM0_AN17	
DDR4_SODIMM_DM1_B	AM21	PS_DDR_DM1_AM21	
DDR4_SODIMM_DM2_B	AK19	PS_DDR_DM2_AK19	
DDR4_SODIMM_DM3_B	AH24	PS_DDR_DM3_AH24	
DDR4_SODIMM_DM4_B	AH31	PS_DDR_DM4_AH31	
DDR4_SODIMM_DM5_B	AE30	PS_DDR_DM5_AE30	
DDR4_SODIMM_DM6_B	AJ31	PS_DDR_DM6_AJ31	
DDR4_SODIMM_DM7_B	AE34	PS_DDR_DM7_AE34	
DDR4_SODIMM_DM8_B	AN34	PS_DDR_DM8_AN34	

PS_DDR_DQ0_AP20	AP20	DDR4_SODIMM_DQ0	
PS_DDR_DQ1_AP18	AP18	DDR4_SODIMM_DQ1	
PS_DDR_DQ2_AP19	AP19	DDR4_SODIMM_DQ2	
PS_DDR_DQ3_AP17	AP17	DDR4_SODIMM_DQ3	
PS_DDR_DQ4_AM20	AM20	DDR4_SODIMM_DQ4	
PS_DDR_DQ5_AM19	AM19	DDR4_SODIMM_DQ5	
PS_DDR_DQ6_AM18	AM18	DDR4_SODIMM_DQ6	
PS_DDR_DQ7_AL18	AL18	DDR4_SODIMM_DQ7	
PS_DDR_DQ8_AP22	AP22	DDR4_SODIMM_DQ8	
PS_DDR_DQ9_AP21	AP21	DDR4_SODIMM_DQ9	
PS_DDR_DQ10_AP24	AP24	DDR4_SODIMM_DQ10	
PS_DDR_DQ11_AN23	AN23	DDR4_SODIMM_DQ11	
PS_DDR_DQ12_AL21	AL21	DDR4_SODIMM_DQ12	
PS_DDR_DQ13_AL22	AL22	DDR4_SODIMM_DQ13	
PS_DDR_DQ14_AM23	AM23	DDR4_SODIMM_DQ14	
PS_DDR_DQ15_AL23	AL23	DDR4_SODIMM_DQ15	
PS_DDR_DQ16_AL20	AL20	DDR4_SODIMM_DQ16	
PS_DDR_DQ17_AK20	AK20	DDR4_SODIMM_DQ17	
PS_DDR_DQ18_AJ20	AJ20	DDR4_SODIMM_DQ18	
PS_DDR_DQ19_AK18	AK18	DDR4_SODIMM_DQ19	
PS_DDR_DQ20_AG20	AG20	DDR4_SODIMM_DQ20	
PS_DDR_DQ21_AH18	AH18	DDR4_SODIMM_DQ21	
PS_DDR_DQ22_AG19	AG19	DDR4_SODIMM_DQ22	
PS_DDR_DQ23_AG18	AG18	DDR4_SODIMM_DQ23	
PS_DDR_DQ24_AG21	AG21	DDR4_SODIMM_DQ24	
PS_DDR_DQ25_AH21	AH21	DDR4_SODIMM_DQ25	
PS_DDR_DQ26_AG24	AG24	DDR4_SODIMM_DQ26	
PS_DDR_DQ27_AG23	AG23	DDR4_SODIMM_DQ27	
PS_DDR_DQ28_AK22	AK22	DDR4_SODIMM_DQ28	
PS_DDR_DQ29_AJ21	AJ21	DDR4_SODIMM_DQ29	
PS_DDR_DQ30_AJ22	AJ22	DDR4_SODIMM_DQ30	
PS_DDR_DQ31_AK23	AK23	DDR4_SODIMM_DQ31	
PS_DDR_DQ32_AG31	AG31	DDR4_SODIMM_DQ32	
PS_DDR_DQ33_AG30	AG30	DDR4_SODIMM_DQ33	
PS_DDR_DQ34_AG29	AG29	DDR4_SODIMM_DQ34	
PS_DDR_DQ35_AG28	AG28	DDR4_SODIMM_DQ35	
PS_DDR_DQ36_AJ30	AJ30	DDR4_SODIMM_DQ36	
PS_DDR_DQ37_AK29	AK29	DDR4_SODIMM_DQ37	
PS_DDR_DQ38_AK30	AK30	DDR4_SODIMM_DQ38	
PS_DDR_DQ39_AJ29	AJ29	DDR4_SODIMM_DQ39	
PS_DDR_DQ40_AE27	AE27	DDR4_SODIMM_DQ40	
PS_DDR_DQ41_AF28	AF28	DDR4_SODIMM_DQ41	
PS_DDR_DQ42_AF30	AF30	DDR4_SODIMM_DQ42	
PS_DDR_DQ43_AF31	AF31	DDR4_SODIMM_DQ43	
PS_DDR_DQ44_AD28	AD28	DDR4_SODIMM_DQ44	
PS_DDR_DQ45_AD27	AD27	DDR4_SODIMM_DQ45	
PS_DDR_DQ46_AD29	AD29	DDR4_SODIMM_DQ46	
PS_DDR_DQ47_AD30	AD30	DDR4_SODIMM_DQ47	
PS_DDR_DQ48_AH33	AH33	DDR4_SODIMM_DQ48	
PS_DDR_DQ49_AJ34	AJ34	DDR4_SODIMM_DQ49	
PS_DDR_DQ50_AH34	AH34	DDR4_SODIMM_DQ50	
PS_DDR_DQ51_AH32	AH32	DDR4_SODIMM_DQ51	
PS_DDR_DQ52_AK34	AK34	DDR4_SODIMM_DQ52	
PS_DDR_DQ53_AK33	AK33	DDR4_SODIMM_DQ53	
PS_DDR_DQ54_AL32	AL32	DDR4_SODIMM_DQ54	
PS_DDR_DQ55_AL31	AL31	DDR4_SODIMM_DQ55	
PS_DDR_DQ56_AG33	AG33	DDR4_SODIMM_DQ56	
PS_DDR_DQ57_AG34	AG34	DDR4_SODIMM_DQ57	
PS_DDR_DQ58_AF32	AF32	DDR4_SODIMM_DQ58	
PS_DDR_DQ59_AF33	AF33	DDR4_SODIMM_DQ59	
PS_DDR_DQ60_AD31	AD31	DDR4_SODIMM_DQ60	
PS_DDR_DQ61_AD32	AD32	DDR4_SODIMM_DQ61	
PS_DDR_DQ62_AD34	AD34	DDR4_SODIMM_DQ62	
PS_DDR_DQ63_AD33	AD33	DDR4_SODIMM_DQ63	
PS_DDR_DQ64_AN31	AN31	DDR4_SODIMM_CB0	
PS_DDR_DQ65_AP31	AP31	DDR4_SODIMM_CB1	
PS_DDR_DQ66_AP32	AP32	DDR4_SODIMM_CB2	
PS_DDR_DQ67_AP33	AP33	DDR4_SODIMM_CB3	
PS_DDR_DQ68_AM31	AM31	DDR4_SODIMM_CB4	
PS_DDR_DQ69_AM33	AM33	DDR4_SODIMM_CB5	
PS_DDR_DQ70_AM34	AM34	DDR4_SODIMM_CB6	
PS_DDR_DQ71_AL33	AL33	DDR4_SODIMM_CB7	
PS_SENSE_DDRPHY_VREF_N_AF27	AF27	NC	
PS_SENSE_DDRPHY_VREF_P_AF26	AF26	NC	
PS_DDR_ZQ_AF23	AF23	UDIMM_PS_ZQ	

VCCO_PSDDR_504

AN30	VCCO_PSDDR_504_AN30
AN25	VCCO_PSDDR_504_AN25
AL29	VCCO_PSDDR_504_AL29
AL24	VCCO_PSDDR_504_AL24
AJ28	VCCO_PSDDR_504_AJ28
AJ24	VCCO_PSDDR_504_AJ24
AG27	VCCO_PSDDR_504_AG27

R351
240
1/10W
1%
GND

U1

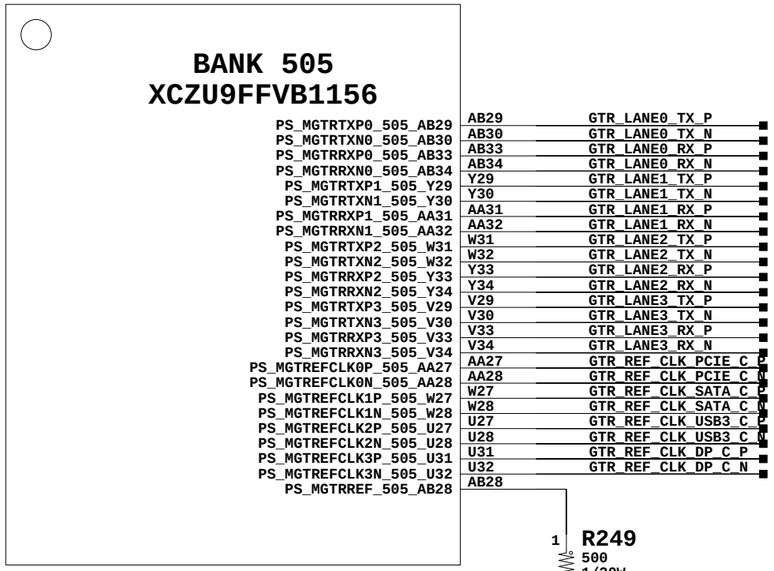
SOC_1156_1MM_IRON

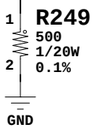
Zynq Banks 504 - Memory

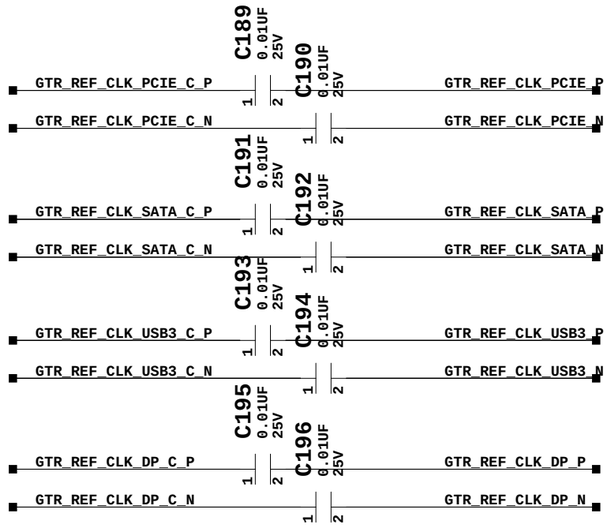
XILINX

TITLE: Zynq Banks 504 - Memory SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0		ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER:	1.0
SHEET SIZE: B	REV:	01
SHEET 13 OF 87	DRAWN BY:	BF

SOC_DA7_FFVB1156_IRONWOOD







Zynq Banks 505 - GTR

XILINX

TITLE: Zynq Banks 505 - GTR SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 14 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTAVCC_R
XCZU9FFVB1156

MGTAVCC_R_K8	K8
MGTAVCC_R_G6	G6
MGTAVCC_R_E5	E5
MGTAVCC_R_D7	D7
MGTAVCC_R_C6	C6
MGTAVCC_R_B8	B8
MGTAVCC_R_A10	A10

MGTAVCC

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTAVTT_R
XCZU9FFVB1156

MGTAVTT_R_P3	P3
MGTAVTT_R_N5	N5
MGTAVTT_R_M4	M4
MGTAVTT_R_L6	L6
MGTAVTT_R_K3	K3
MGTAVTT_R_J5	J5
MGTAVTT_R_H4	H4
MGTAVTT_R_F3	F3
MGTAVTT_R_D4	D4
MGTAVTT_R_B3	B3

MGTAVTT

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTVCCAUX_R
XCZU9FFVB1156

MGTVCCAUX_R_H7	H7
MGTVCCAUX_R_F8	F8

MGTVCCAUX

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTAVCC_L
XCZU9FFVB1156

MGTAVCC_L_R29	R29
MGTAVCC_L_P28	P28
MGTAVCC_L_L29	L29
MGTAVCC_L_H27	H27
MGTAVCC_L_G29	G29
MGTAVCC_L_F28	F28

MGTAVCC

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTAVTT_L
XCZU9FFVB1156

MGTAVTT_L_P31	P31
MGTAVTT_L_N30	N30
MGTAVTT_L_M32	M32
MGTAVTT_L_K31	K31
MGTAVTT_L_J30	J30
MGTAVTT_L_H32	H32
MGTAVTT_L_F31	F31
MGTAVTT_L_E30	E30
MGTAVTT_L_D32	D32
MGTAVTT_L_C29	C29
MGTAVTT_L_B31	B31

MGTAVTT

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK MGTVCCAUX_L
XCZU9FFVB1156

MGTVCCAUX_L_M27	M27
MGTVCCAUX_L_K28	K28

MGTVCCAUX

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK VCCAUX
XCZU9FFVB1156

VCCAUX_U14	U14
VCCAUX_T14	T14

VCCAUX

U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK VCCAUX_IO
XCZU9FFVB1156

VCCAUX_IO_V14	V14
VCCAUX_IO_V13	V13
VCCAUX_IO_U13	U13

VCCAUX

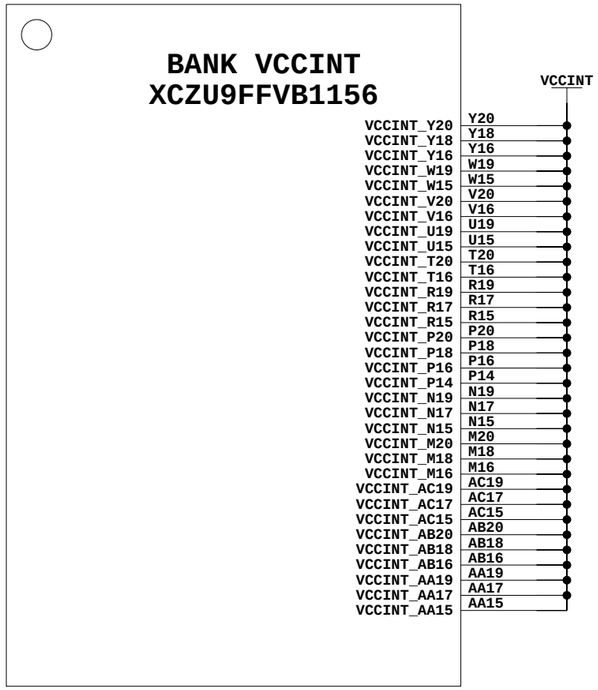
U1 SOC_1156_1MM_IRON

Zynq Power 1

XILINX

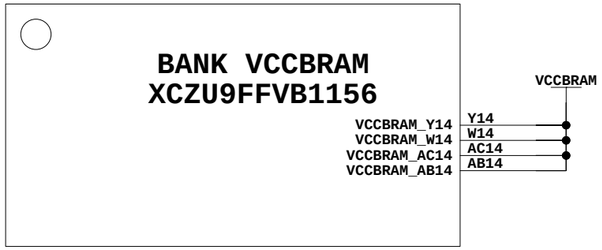
TITLE: Zynq Power 1 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 15 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD



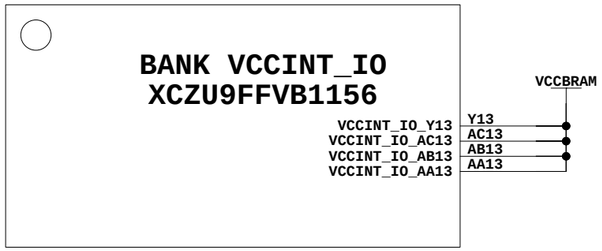
U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD



U1 SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD



U1 SOC_1156_1MM_IRON

Zynq Power 2

XILINX

TITLE: Zynq Power 2 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 16 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD

BANK PS_MGTRAVCC
XCZU9FFVB1156

PS_MGTRAVCC_Y27 Y27
PS_MGTRAVCC_W30 W30
PS_MGTRAVCC_V28 V28
PS_MGTRAVCC_AA29 AA29

MGTRAVCC

U1

SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK PS_MGTRAVTT
XCZU9FFVB1156

PS_MGTRAVTT_Y31 Y31
PS_MGTRAVTT_V32 V32
PS_MGTRAVTT_AB32 AB32

MGTRAVTT

U1

SOC_1156_1MM_IRON

SOC_DA7_FFVB1156_IRONWOOD

BANK PS_POWER
XCZU9FFVB1156

VCC_PSPLL_W25 W25
VCC_PSPLL_W24 W24
VCC_PSPLL_W22 W22
VCC_PSINTLP_AC23 AC23
VCC_PSINTLP_AC22 AC22
VCC_PSINTLP_AC21 AC21
VCC_PSINTLP_AB23 AB23
VCC_PSINTLP_AB21 AB21
VCC_PSINTLP_AA21 AA21
VCC_PSINTFP_DDR_AE25 AE25
VCC_PSINTFP_DDR_AE24 AE24
VCC_PSINTFP_DDR_AD24 AD24
VCC_PSINTFP_AE23 AE23
VCC_PSINTFP_AE22 AE22
VCC_PSINTFP_AD26 AD26
VCC_PSINTFP_AD25 AD25
VCC_PSINTFP_AD22 AD22
VCC_PSINTFP_AD21 AD21
VCC_PSINTFP_AC24 AC24
VCC_PSDDR_PLL_Y25 Y25
VCC_PSDDR_PLL_Y24 Y24
VCC_PSBATT_AA22 AA22
VCC_PSAUX_Y23 Y23
VCC_PSAUX_Y22 Y22
VCC_PSAUX_AA25 AA25
VCC_PSAUX_AA23 AA23
VCC_PSADC_AC26 AC26
VCC_PSADC_AB25 AB25
GND_PSADC_AC25 AC25
GND_PSADC_AB24 AB24

VCCPSPLL
VCCPSINTLP
VCCPSINTFP
VCCPSDDRPLL
VCCPSAUX
VCC_PSBATT

VCCPSAUX
FERRITE-600
PS_SYSMON_AVCC
C168 0.1UF 25V X5R
C917 0.47UF 10V X5R
L18
PS_SYSMON_AGND
FERRITE-600
L19
PS_SYSMON_AGND
GND

U1

SOC_1156_1MM_IRON

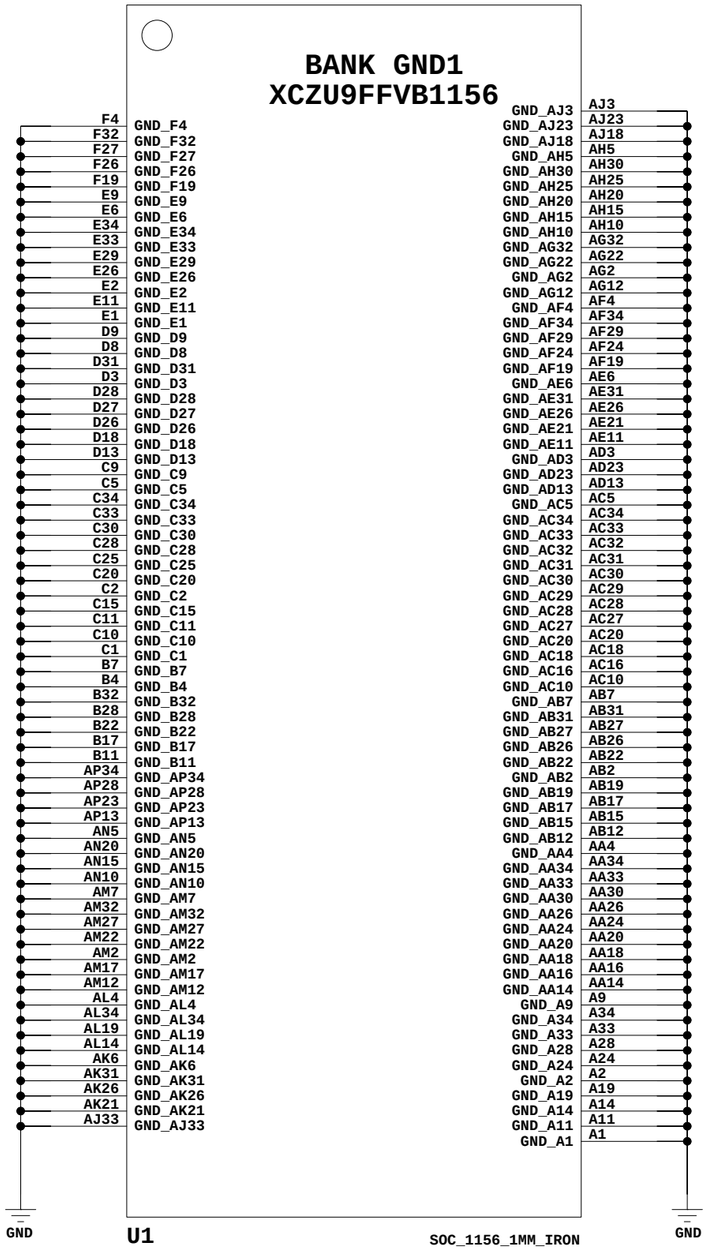
UTIL_1V8
NC
D40
40V
200MW
BAS40-04
R22
4.70K
1/16W
1%
VCC_PSBATT
TS518FE_FL35E
B1
BAT_TS518_TS621_DUAL
GND

Zynq Power 3

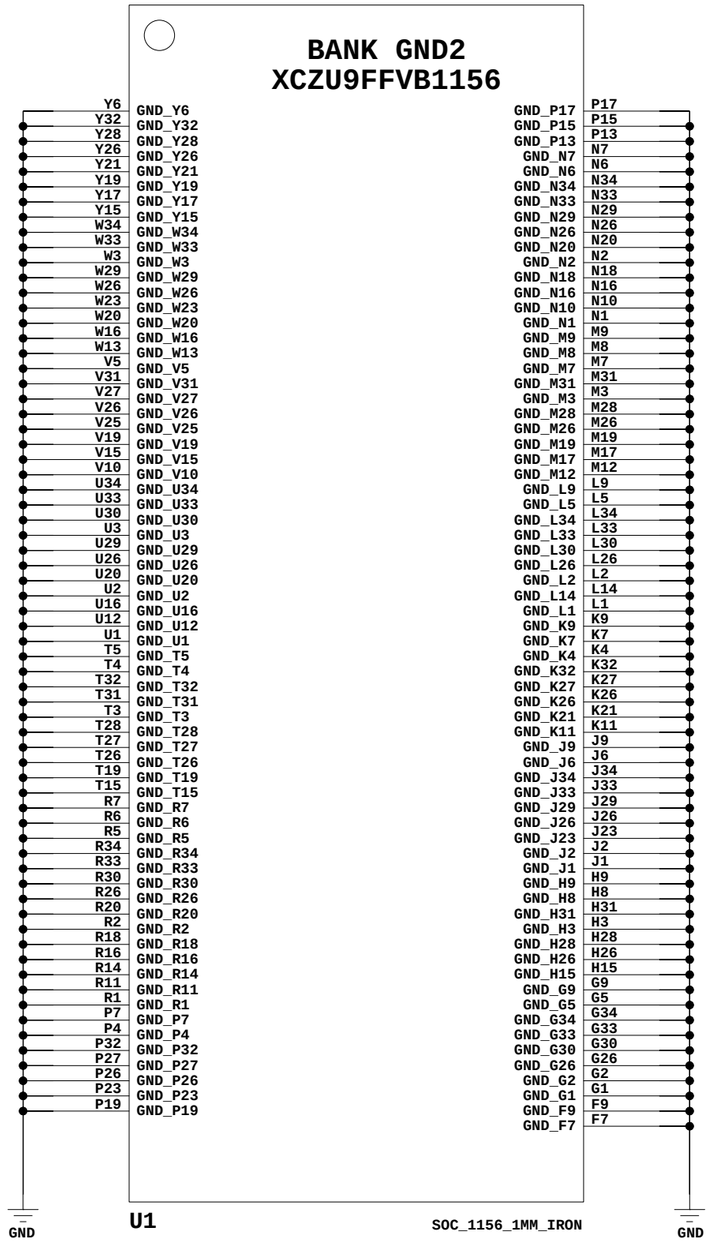
XILINX

TITLE: Zynq Power 3 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 17 OF 87	DRAWN BY: BF

SOC_DA7_FFVB1156_IRONWOOD



SOC_DA7_FFVB1156_IRONWOOD

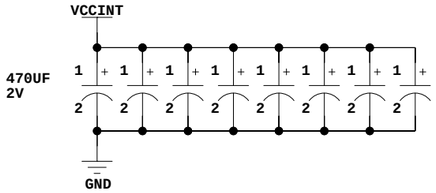


Zynq GND

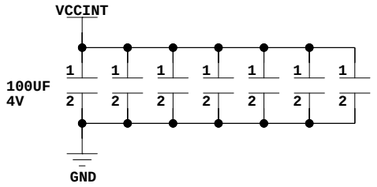
XILINX

TITLE: Zynq GND SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 18 OF 87	DRAWN BY: BF

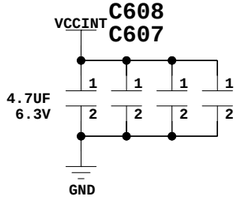
C696 C700
C697 C701
C698 C702
C699 C703



C424 C428
C425 C431
C426 C432
C427

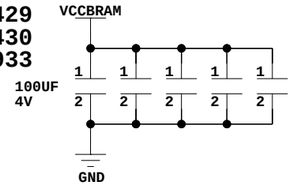


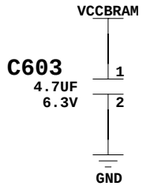
C602
C606
C608
C607



VCCINT

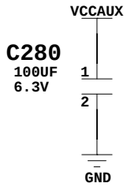
C934 C429
C935 C430
C933

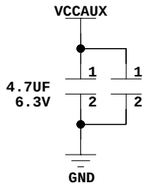




VCCBRAM

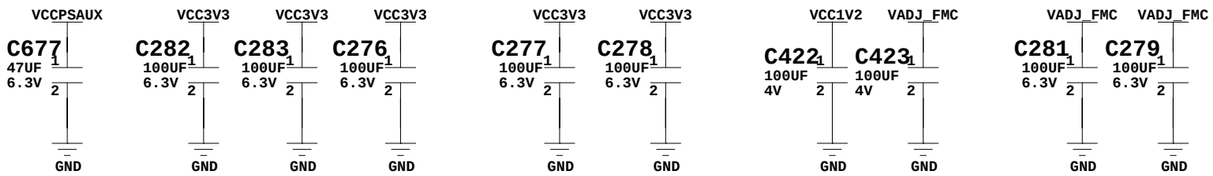
C604
C605





VCCAUX / VCCAUX_IO

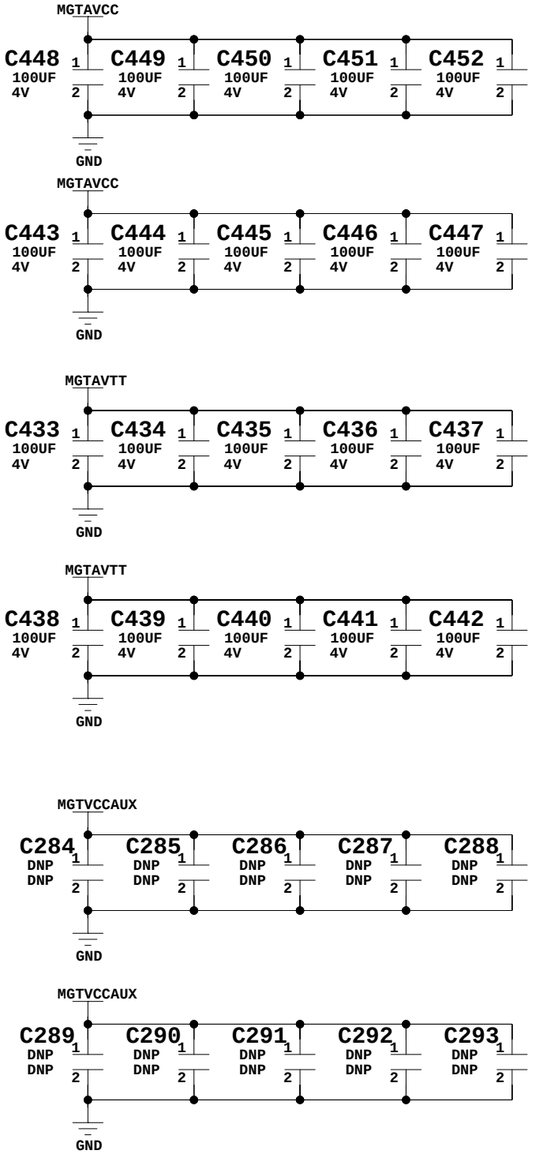
VCCO BANKS 0 44 47 48 49 50 64 65 66 67

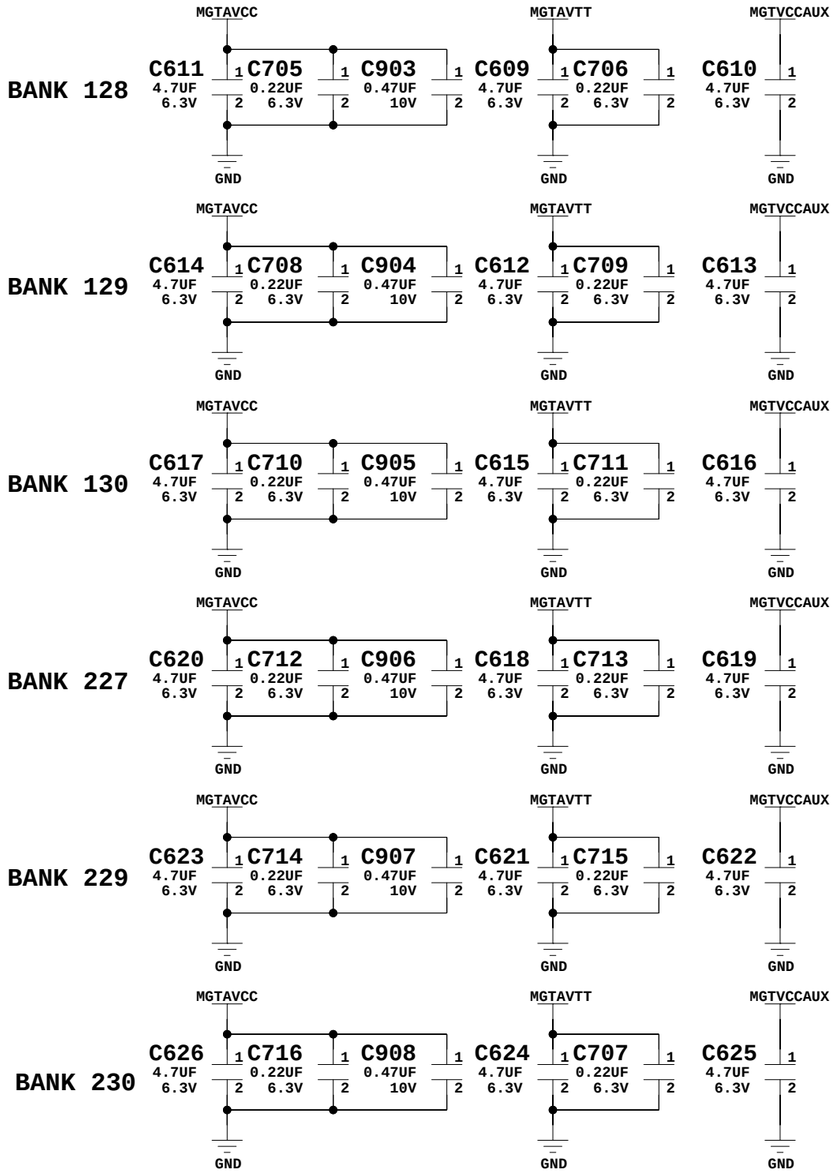


Zynq Decoupling 1

XILINX

TITLE: Zynq Decoupling 1 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 19 OF 87	DRAWN BY: BF

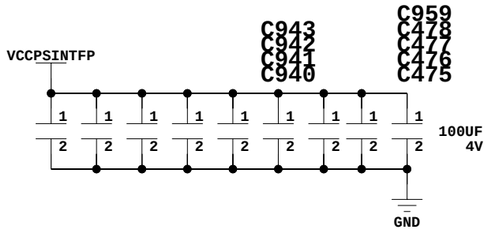


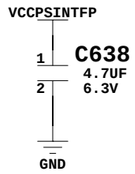


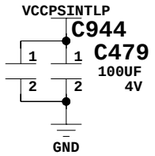
Zynq Decoupling 2

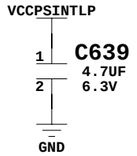
XILINX

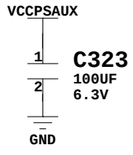
TITLE: Zynq Decoupling 2 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:35	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 20 OF 87	DRAWN BY: BF

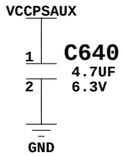


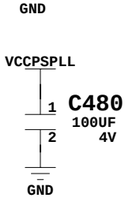


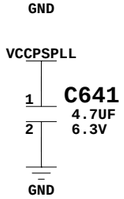


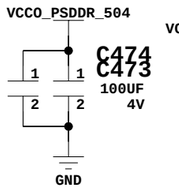


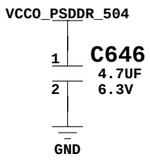


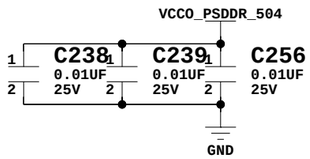


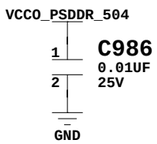


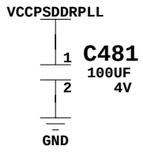


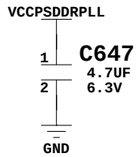


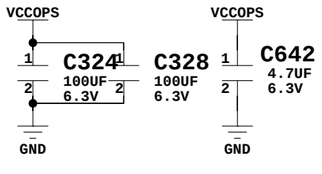


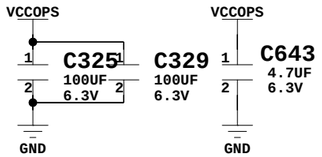


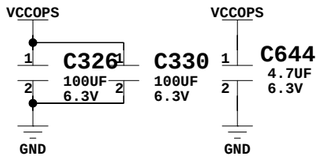


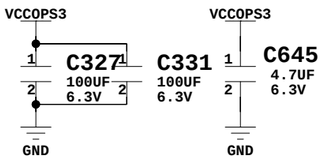




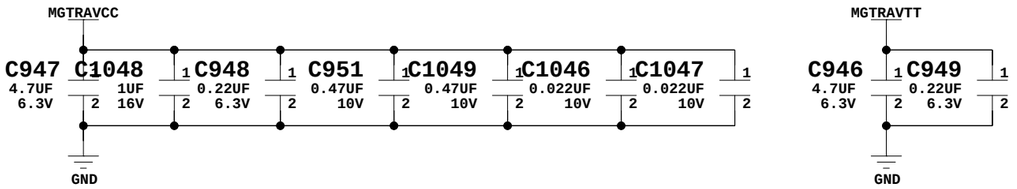








BANK 505

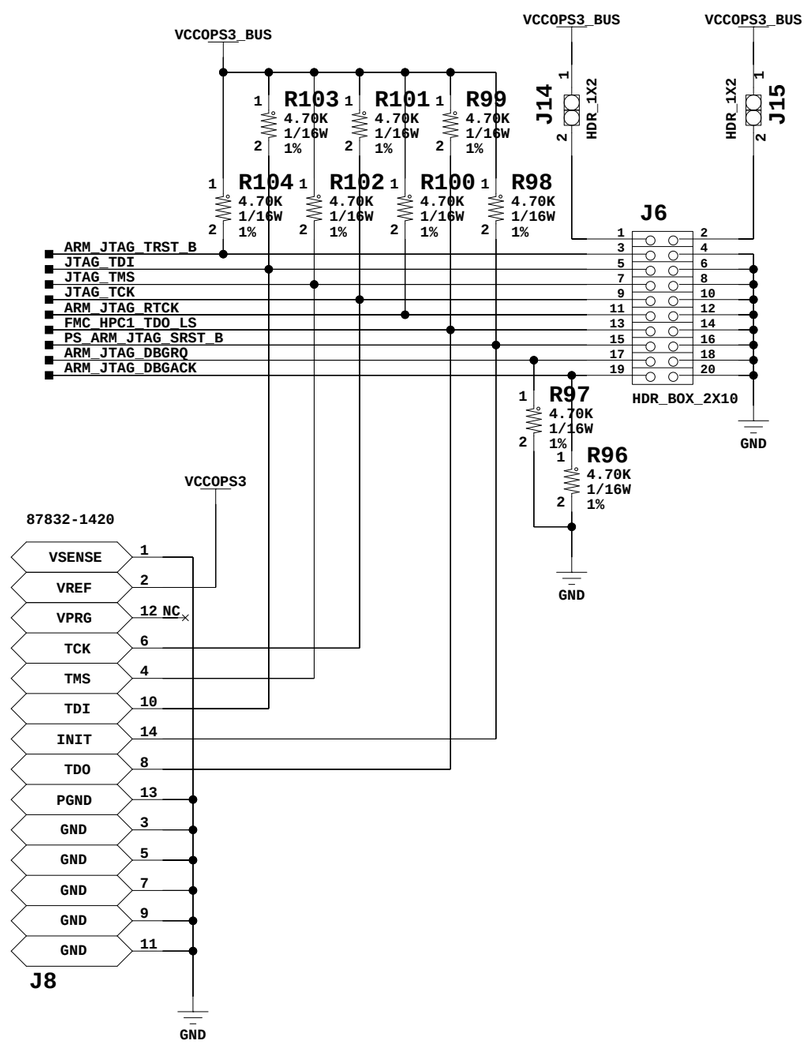


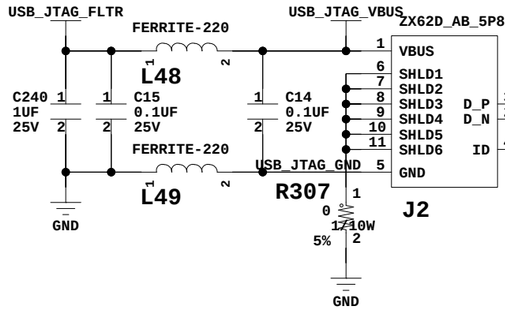
Place this round pad resistor directly under U1

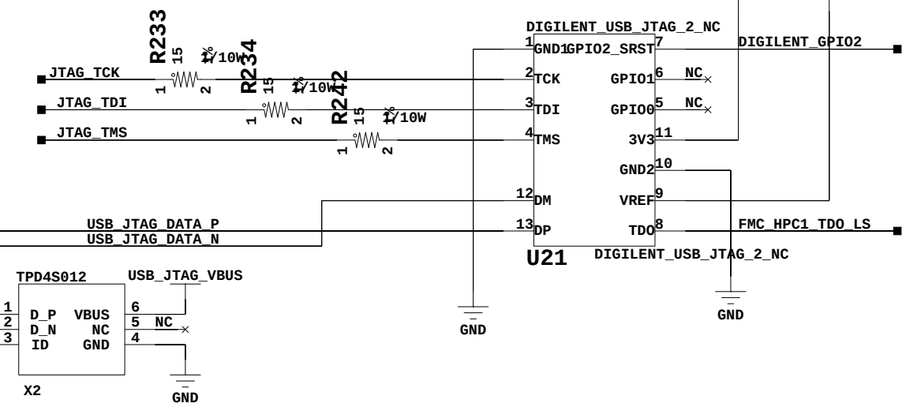
Zynq Decoupling 3

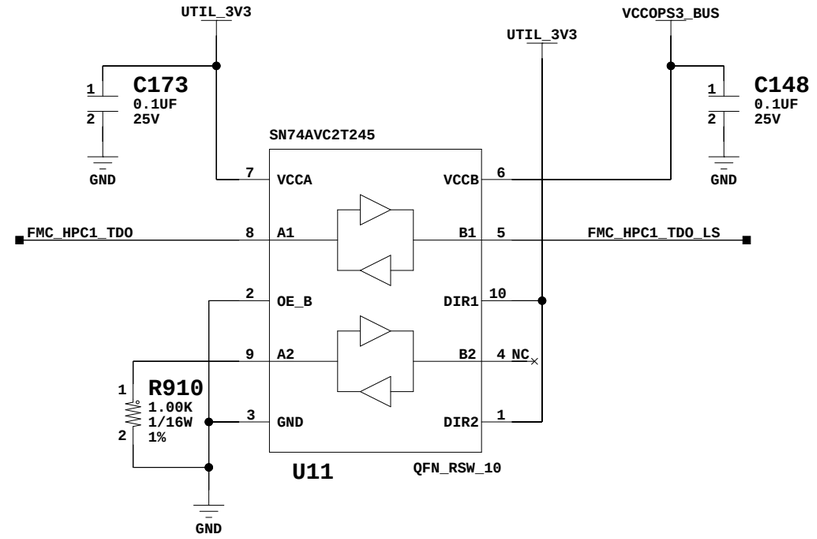
XILINX

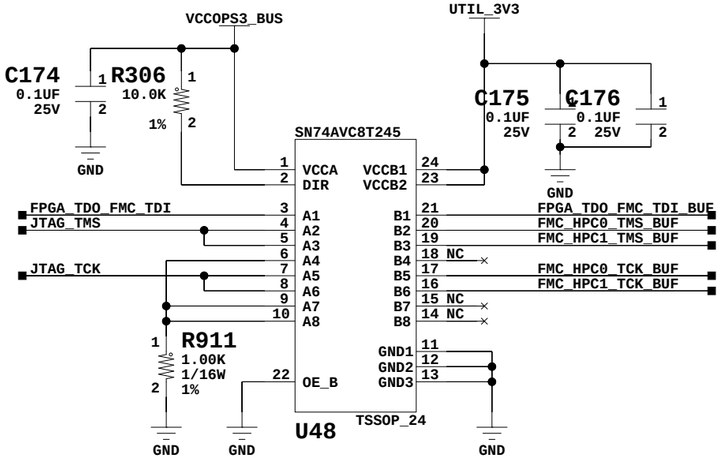
TITLE: Zynq Decoupling 3 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 21 OF 87	DRAWN BY: BF

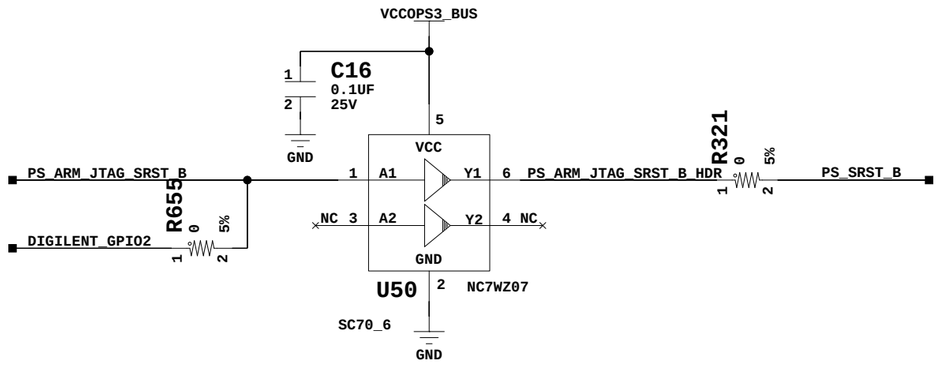








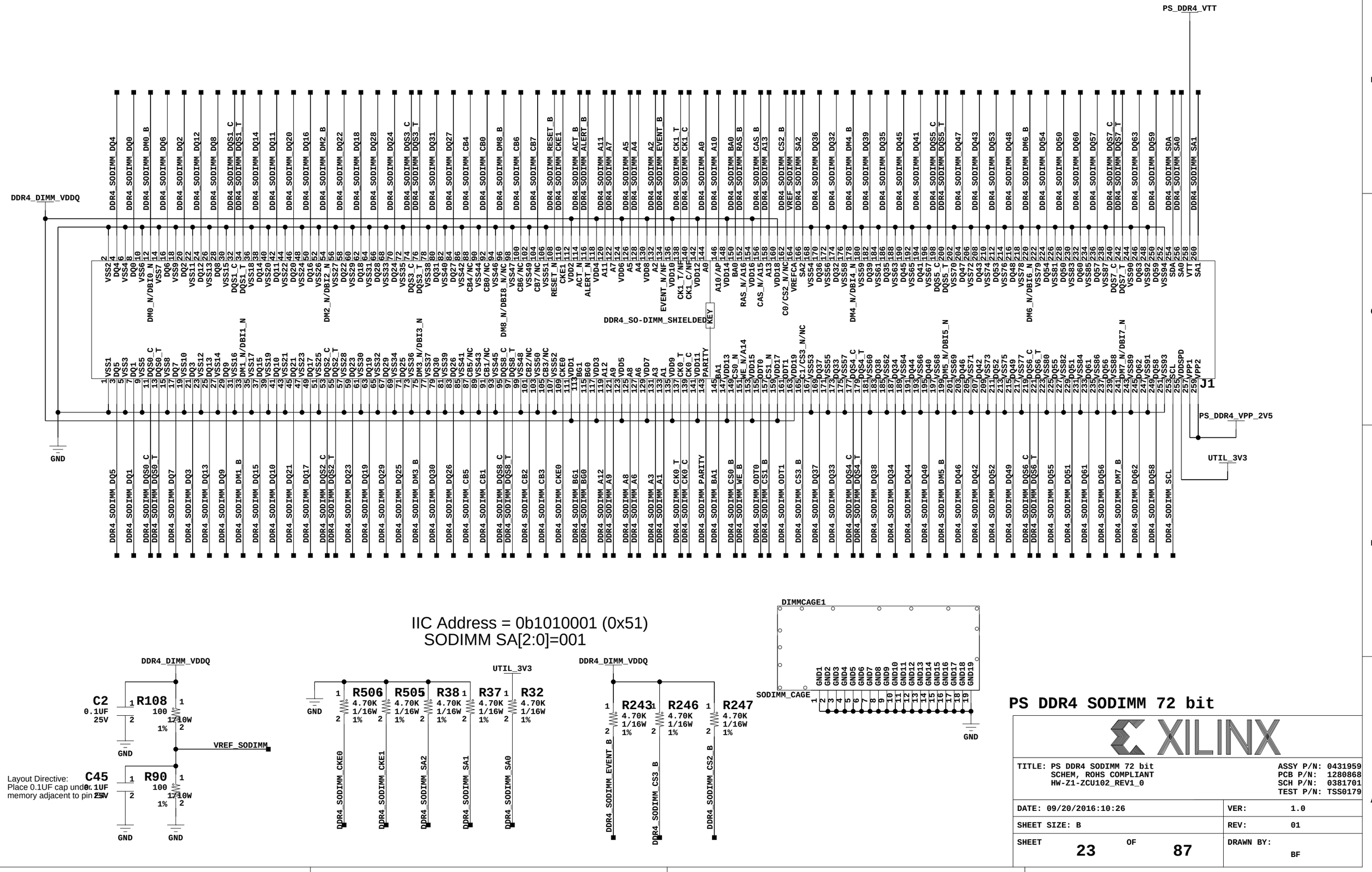




JTAG Headers

XILINX

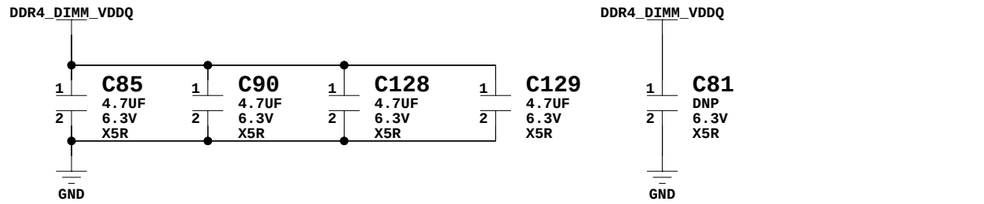
TITLE: JTAG Headers SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 22 OF 87	DRAWN BY: BF

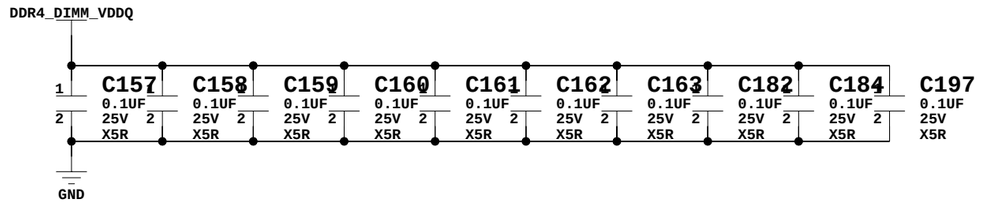


PS DDR4 SODIMM 72 bit

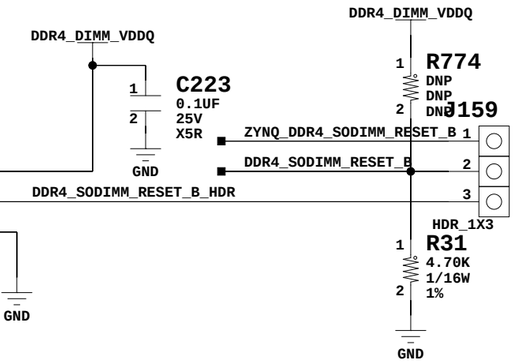
XILINX

TITLE: PS DDR4 SODIMM 72 bit SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 23 OF 87	DRAWN BY: BF

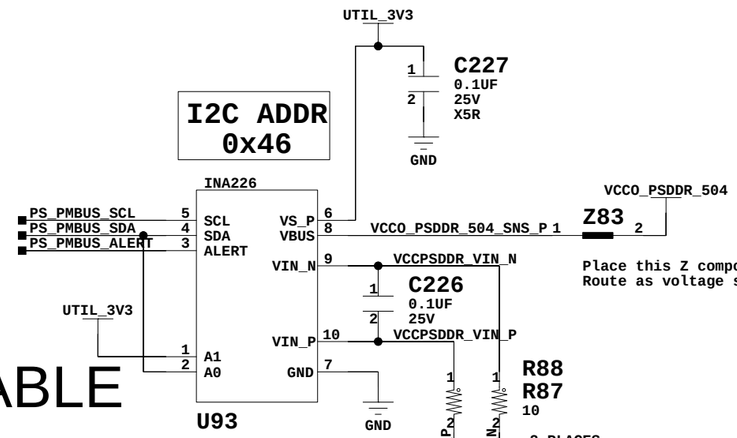




PLACE ABOVE CAPS BENEATH/CLOSE TO DIMM SOCKET

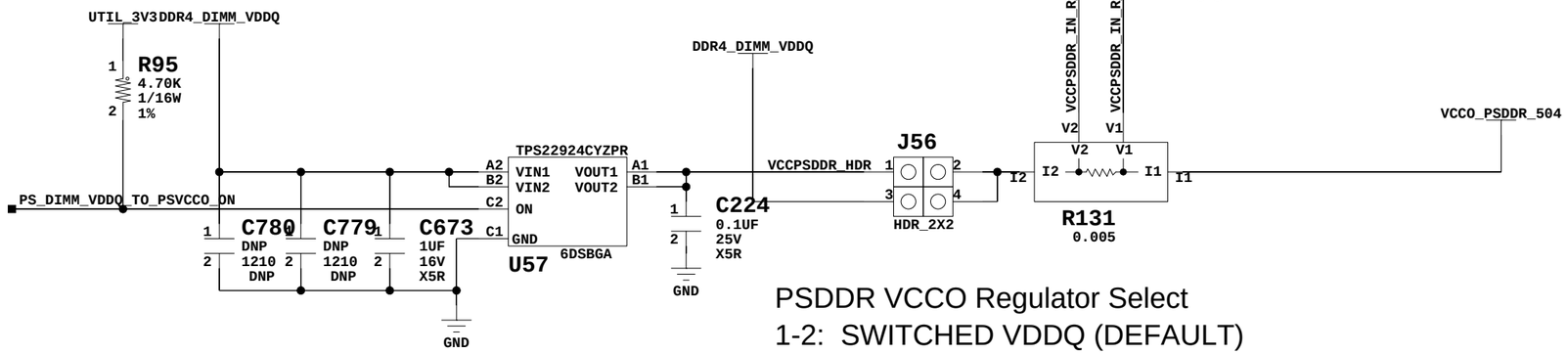


DDR DIMM RESET_B CONTROL



Place this Z component near U1
Route as voltage sense line directly to power via

DDR DIMM VCCO DISABLE



PSDDR VCCO Regulator Select
1-2: SWITCHED VDDQ (DEFAULT)
3-4: DIRECT VDDQ

PS DDR4 SODIMM Decoupling

TITLE: PS DDR4 SODIMM Decoupling SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 24 OF 87	DRAWN BY: BF

Layout: Place 0.1UF cap in via matrix at M1

PL_DDR4_VPP_2V5

PL_DDR4_VTT

VCC1V2

DDR4_VREFB

DDR4_ZQB

DDR4_TEN

DDR4_ALERT_B

C66 0.1UF 25V X5R

C67 0.1UF 25V X5R

R357 1.00K 1/16W 1%

R358 1.00K 1/16W 1%

R349 240 1/10W 1%

R478 R477 R491 R493 R494 R495 R492 R482 R483 R480 R484 R485 R481 R486 R487 R488 R489 R496 R497 R498 R499 R500 R501 39.2 1% 1/16W

R499 39.2 1% 1/10W

U2

MT40A256M16GE-075E:B

MT40A256M16GE-075E

MT40A256M16GE-075E

DDR4_A0	P3	A0	
DDR4_A1	P7	A1	
DDR4_A2	R3	A2	
DDR4_A3	N7	A3	
DDR4_A4	N3	A4	
DDR4_A5	P8	A5	
DDR4_A6	P2	A6	
DDR4_A7	R8	A7	
DDR4_A8	R2	A8	
DDR4_A9	R7	A9	
DDR4_A10	M3	A10/AP	
DDR4_A11	T2	A11	
DDR4_A12	M7	A12/BC_B	
DDR4_A13	T8	A13	
DDR4_BA0	N2	BA0	
DDR4_BA1	N8	BA1	
DDR4_BG0	M2	BG0	
DDR4_A14_WE_B	L2	WE_B/A14	
DDR4_A16_RAS_B	L8	RAS_B/A16	
DDR4_A15_CAS_B	M8	CAS_B/A15	
DDR4_CK_T	K7	CK_T	
DDR4_CK_C	K8	CK_C	
DDR4_CKE	K2	CKE	
DDR4_ACT_B	L3	ACT_B	
	N9	TEN	
	P9	ALERT_B	
DDR4_PAR	T3	PAR	
DDR4_RESET_B	P1	RESET_B	
DDR4_ODT	K3	ODT	
DDR4_CS_B	L7	CS_B	

DQL0	G2	DDR4_DQ0
DQL1	F7	DDR4_DQ1
DQL2	H3	DDR4_DQ2
DQL3	H7	DDR4_DQ3
DQL4	H2	DDR4_DQ4
DQL5	H8	DDR4_DQ5
DQL6	J3	DDR4_DQ6
DQL7	J7	DDR4_DQ7
DQU0	A3	DDR4_DQ8
DQU1	B8	DDR4_DQ9
DQU2	C3	DDR4_DQ10
DQU3	C7	DDR4_DQ11
DQU4	C2	DDR4_DQ12
DQU5	C8	DDR4_DQ13
DQU6	D3	DDR4_DQ14
DQU7	D7	DDR4_DQ15
DQSL_T	G3	DDR4_DQS0_T
DQSL_C	F3	DDR4_DQS0_C
DQSU_T	B7	DDR4_DQS1_T
DQSU_C	A7	DDR4_DQS1_C
DML_B/DBIL_B	E7	DDR4_DM0
DMU_B/DBIU_B	E2	DDR4_DM1
NC	T7	NC

C580 0.01UF 25V X5R

R144 36 1%

R145 36 1%

R156 499 1/10W 1%

R402 1.00K 1/16W 1%

R764 4.70K 1/16W 1%

C631 C630 C629 C64 C63 C62 C61 C60 4.7UF 6.3V X5R / 0.1UF 25V X5R

C628 4.7UF 6.3V X5R

C912 C911 0.47UF 10V X5R

C757 0.068UF 16V X7R

C758 0.068UF 16V X7R

C627 4.7UF 6.3V X5R

C910 C909 0.47UF 10V X5R

C756 0.068UF 16V X7R

C755 0.068UF 16V X7R

C632 4.7UF 6.3V X5R

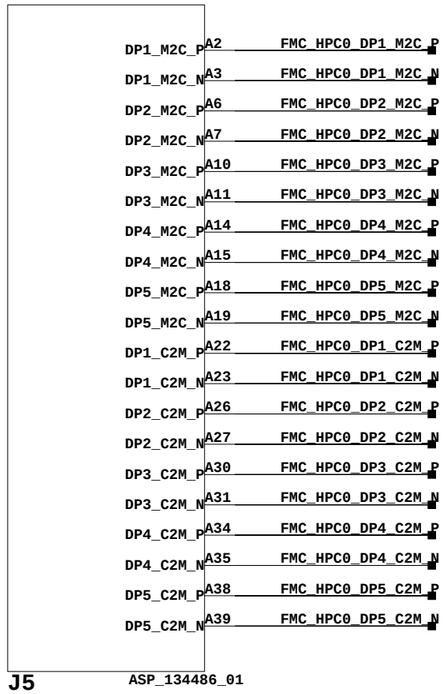
C65 0.1UF 25V X5R

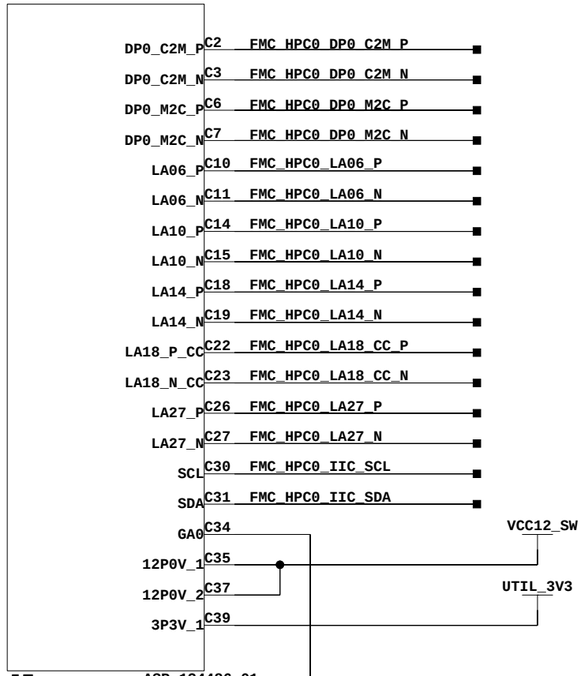
GND

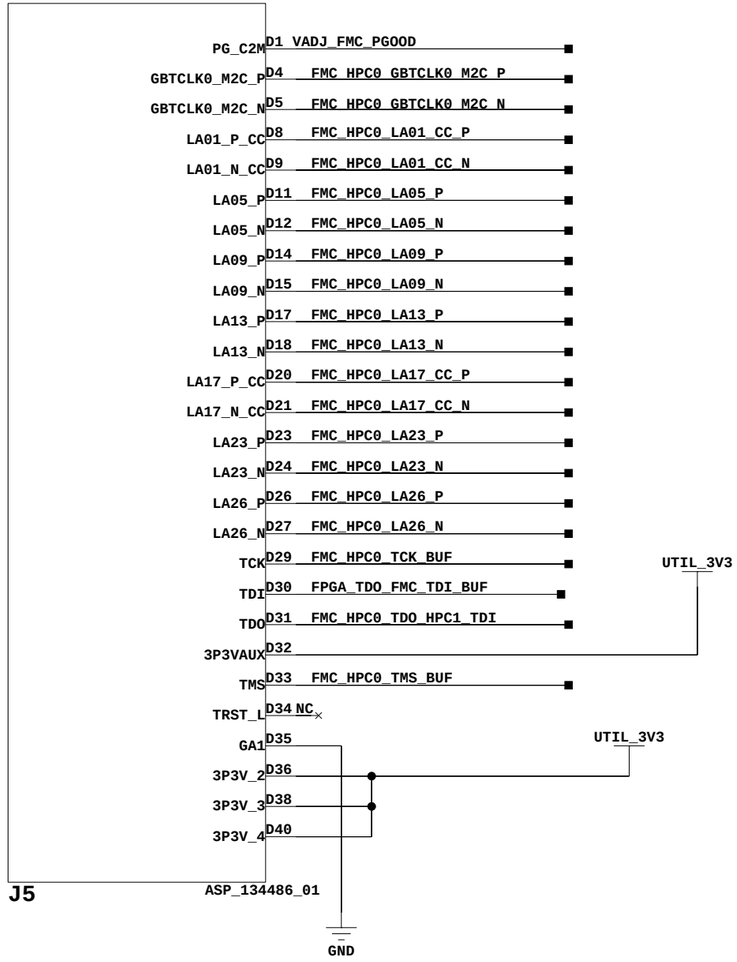
PL Component DDR4 [15-0]

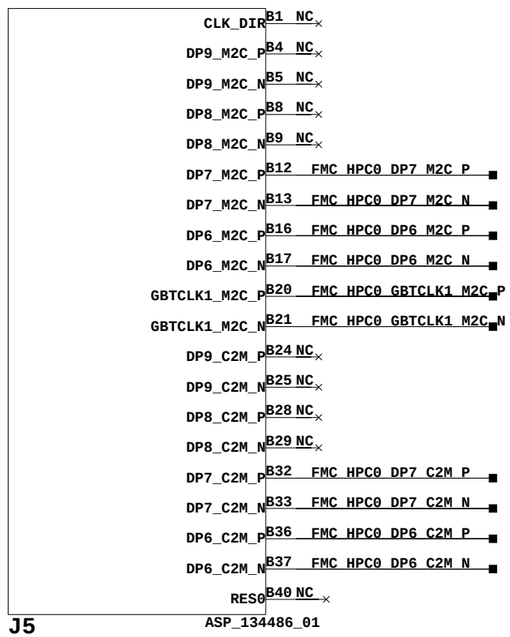
XILINX

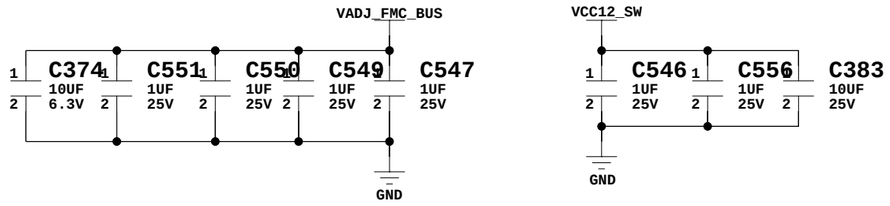
TITLE: PL Component DDR4 [15-0] SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 25 OF 87	DRAWN BY: BF

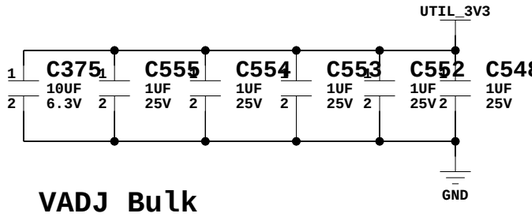


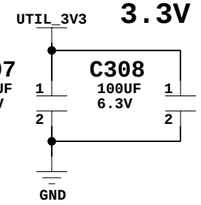






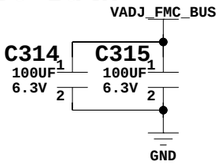


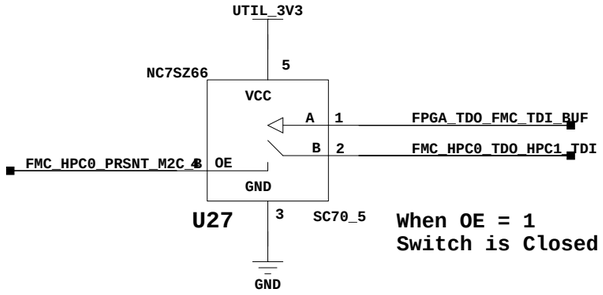




3.3V Bulk

VADJ Bulk

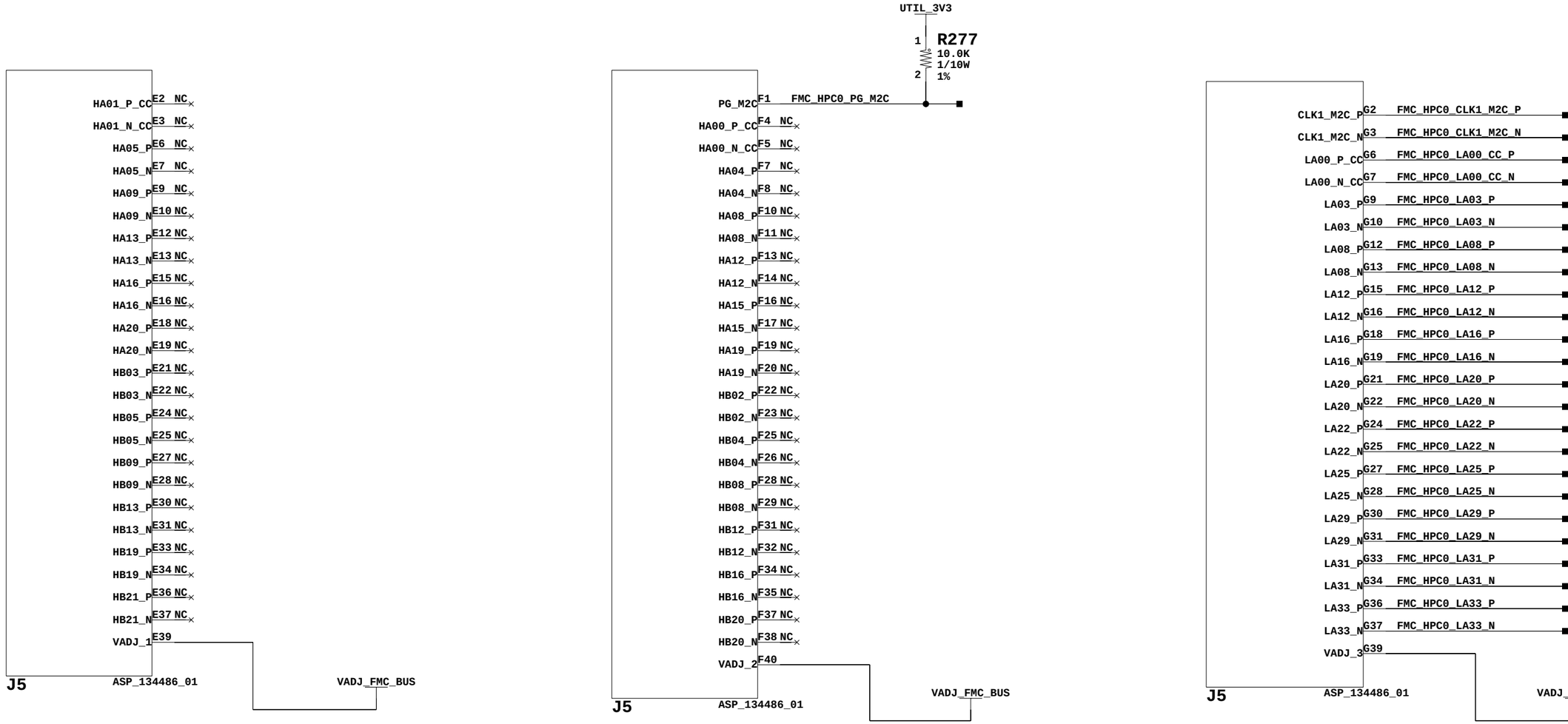




ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows A B C D

XILINX

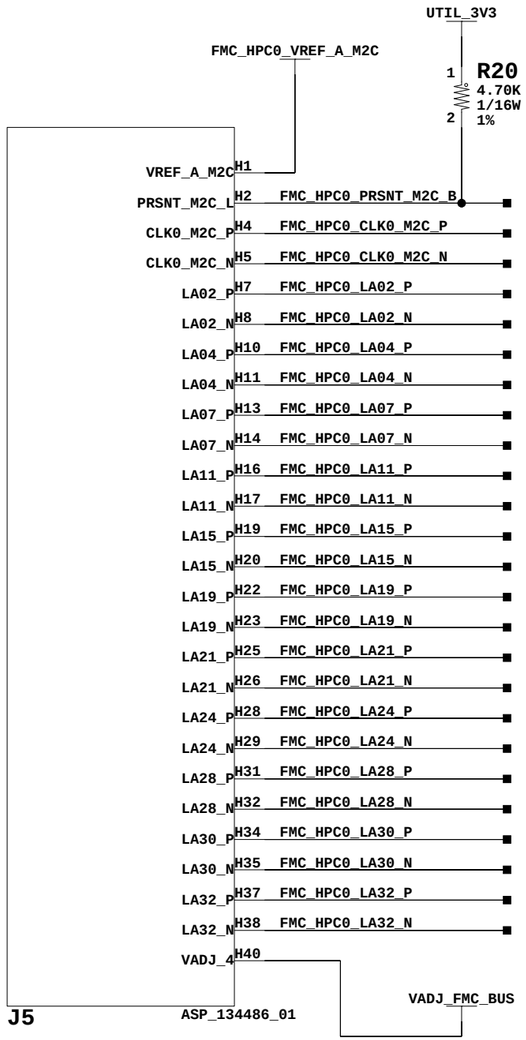
TITLE: PL FMC HPC0 Header Rows A B C D SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 26 OF 87	DRAWN BY: BF

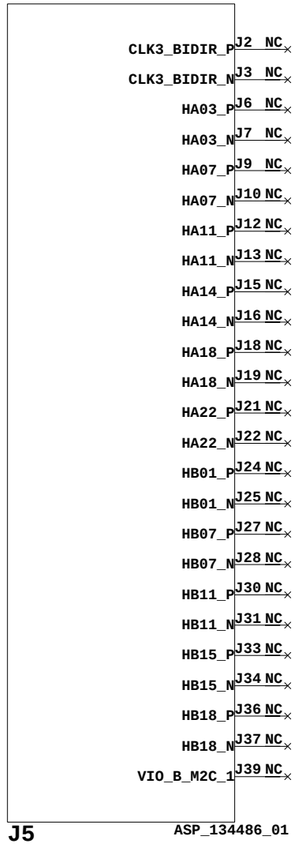


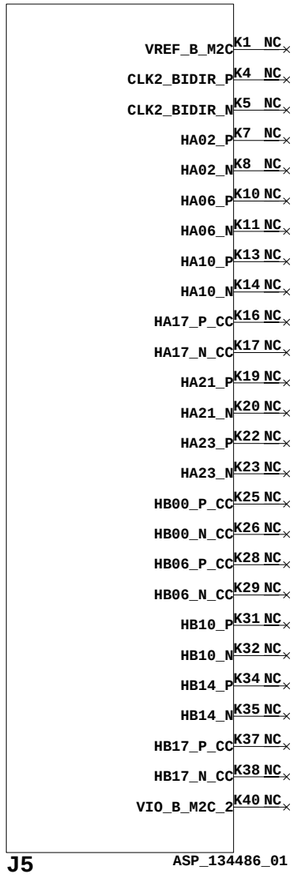
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows E F G

XILINX

TITLE: PL FMC HPC0 Header Rows E F G SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 27 OF 87	DRAWN BY: BF



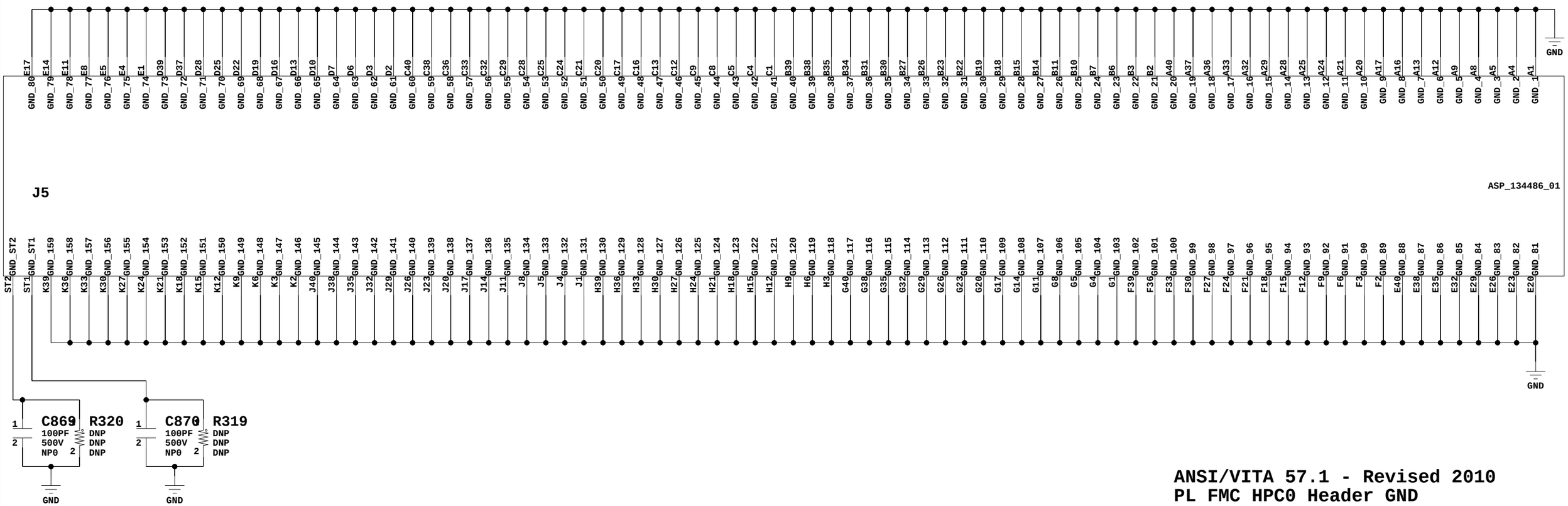




ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows H J K

XILINX

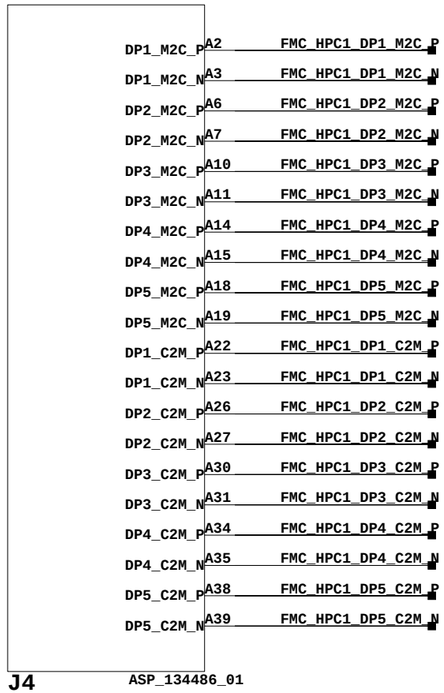
TITLE: PL FMC HPC0 Header Rows H J K SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 28 OF 87	DRAWN BY: BF

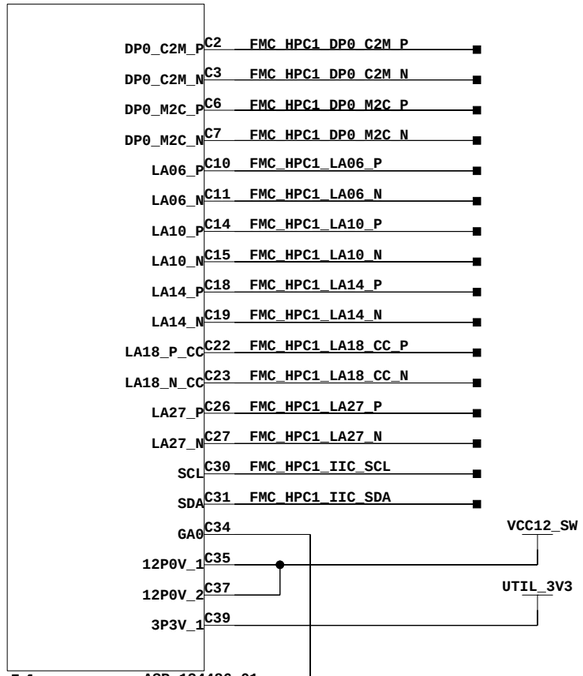


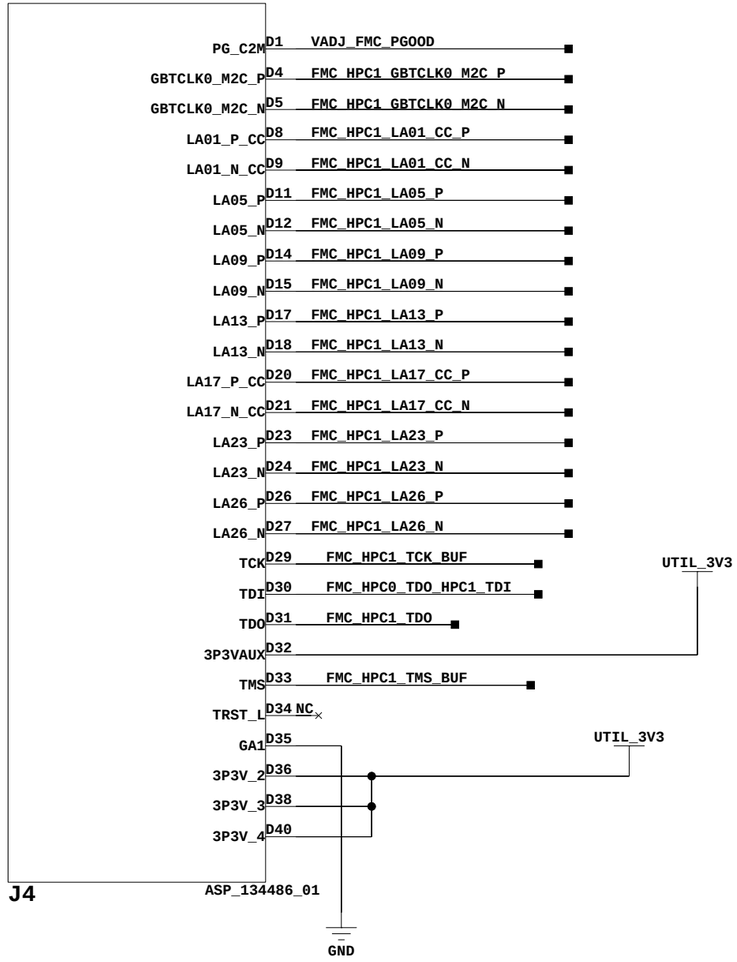
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header GND

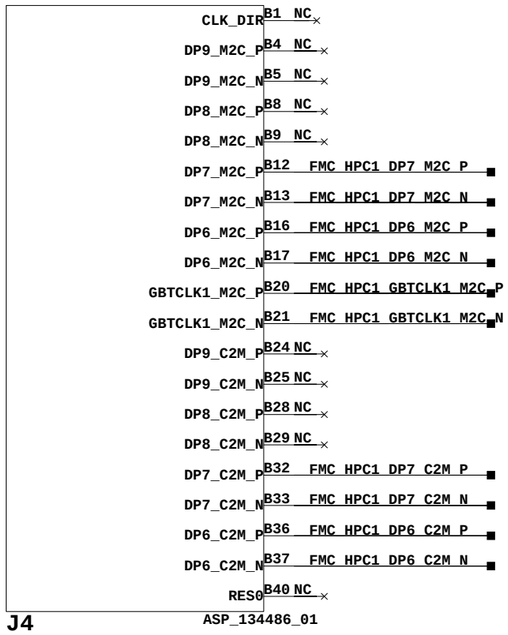
XILINX

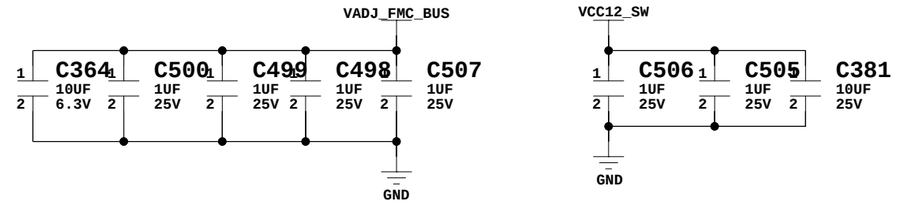
TITLE: PL FMC HPC0 Header GND SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 29 OF 87	DRAWN BY: BF

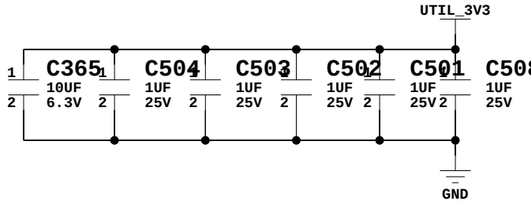


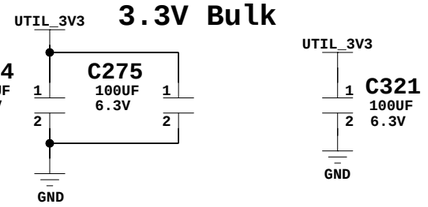


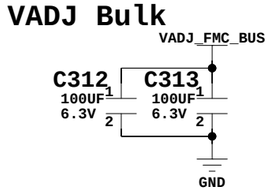


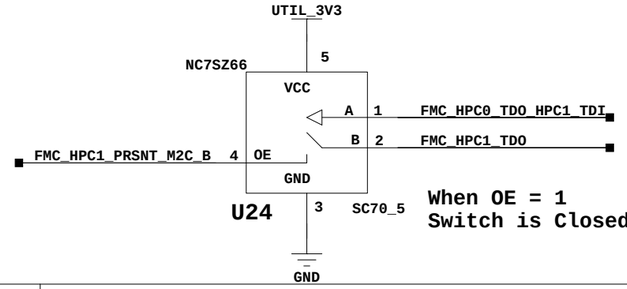












ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows A B C D

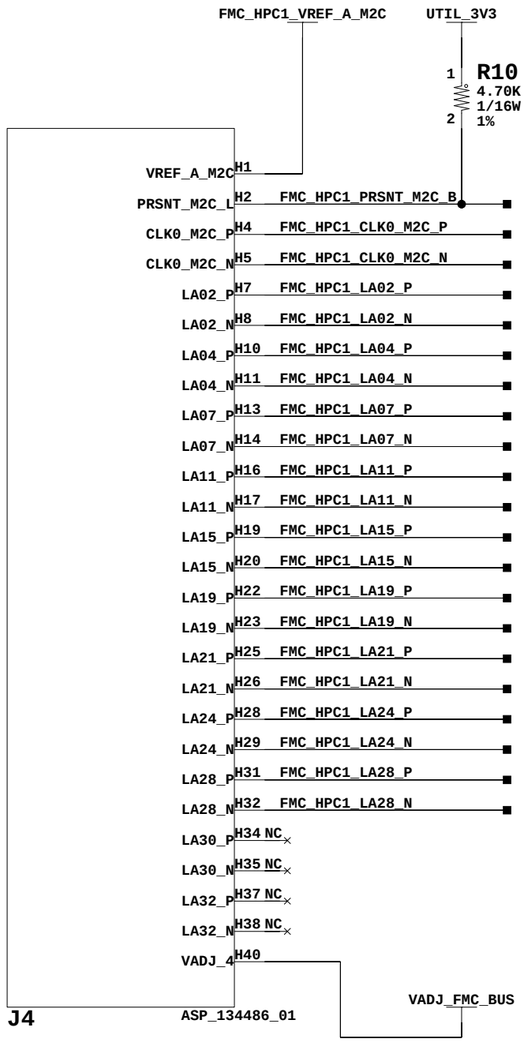
XILINX

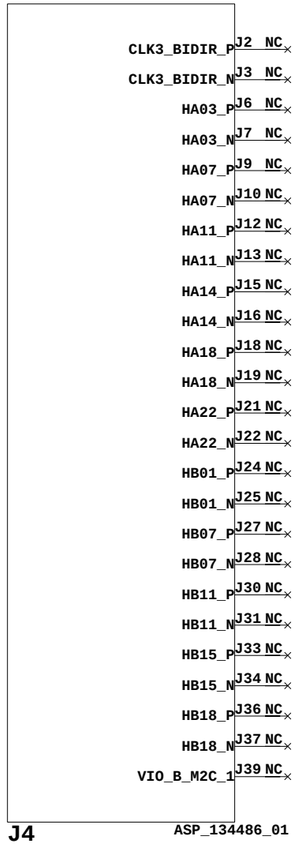
TITLE: PL FMC HPC1 Header Rows A B C D SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 30 OF 87	DRAWN BY: BF

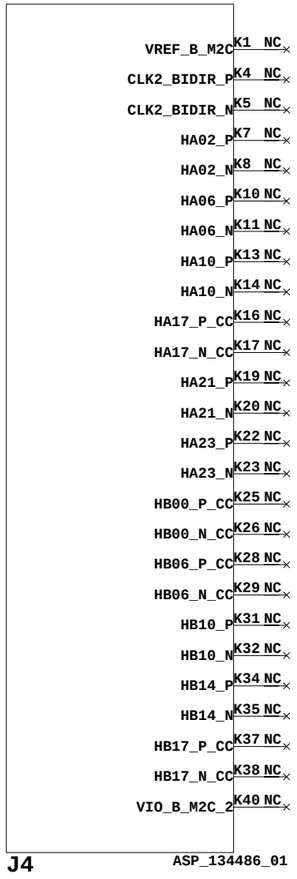
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows E F G

XILINX

TITLE: PL FMC HPC1 Header Rows E F G SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 31 OF 87	DRAWN BY: BF

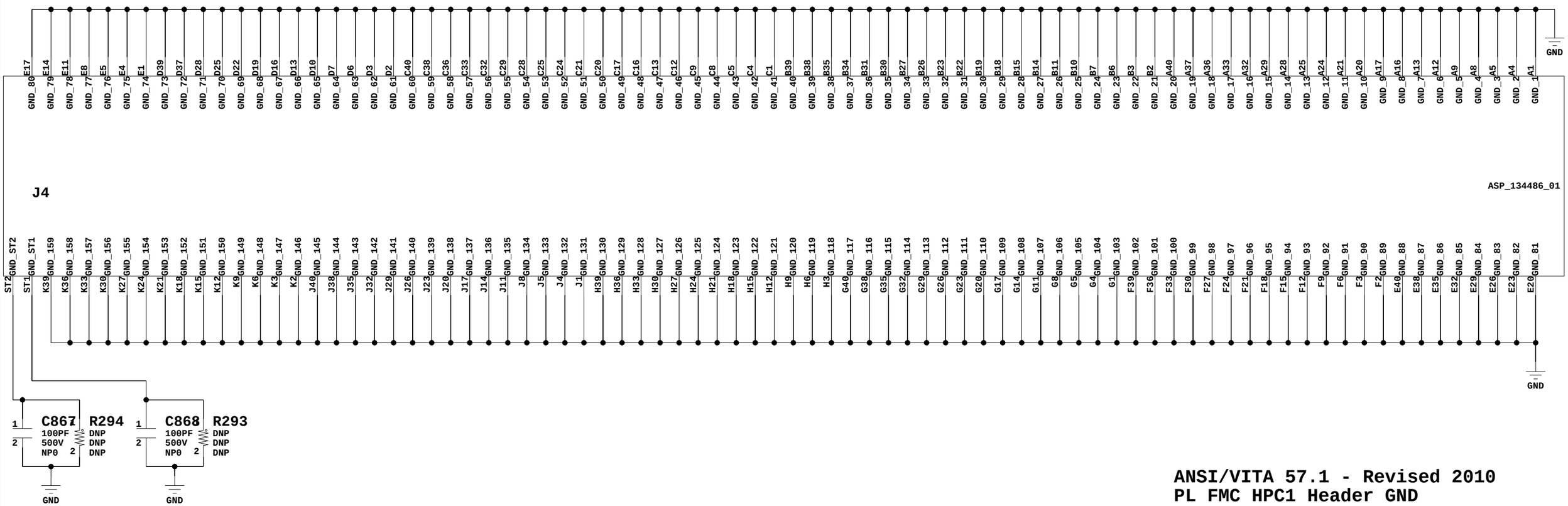






ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows H J K

TITLE: PL FMC HPC1 Header Rows H J K SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 32 OF 87	DRAWN BY: BF



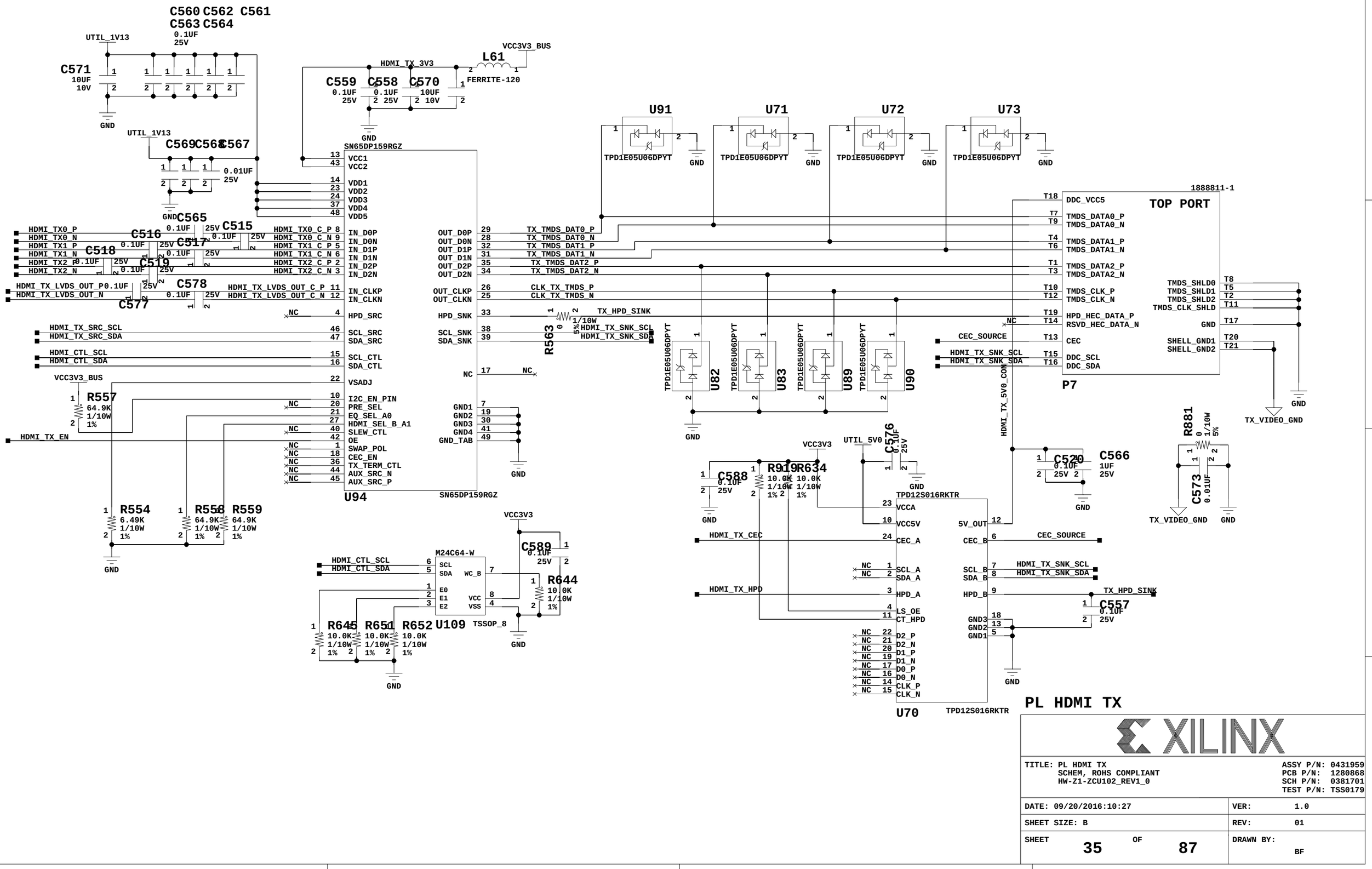
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header GND

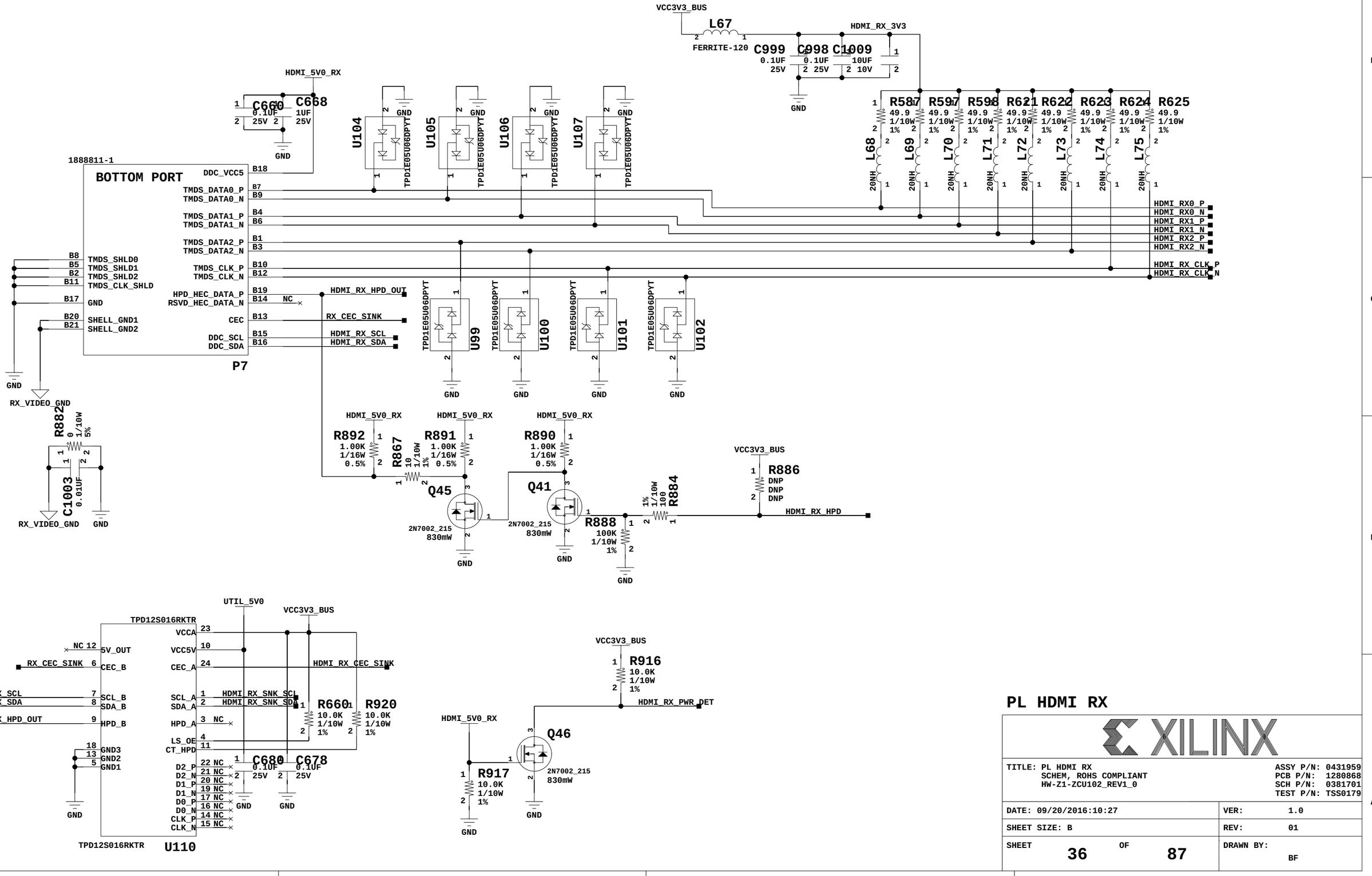
XILINX

TITLE: PL FMC HPC1 Header GND SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 33 OF 87	DRAWN BY: BF

PL SFP+ 2x2 Cage

TITLE: PL SFP+ 2x2 Cage SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 34 OF 87	DRAWN BY: BF

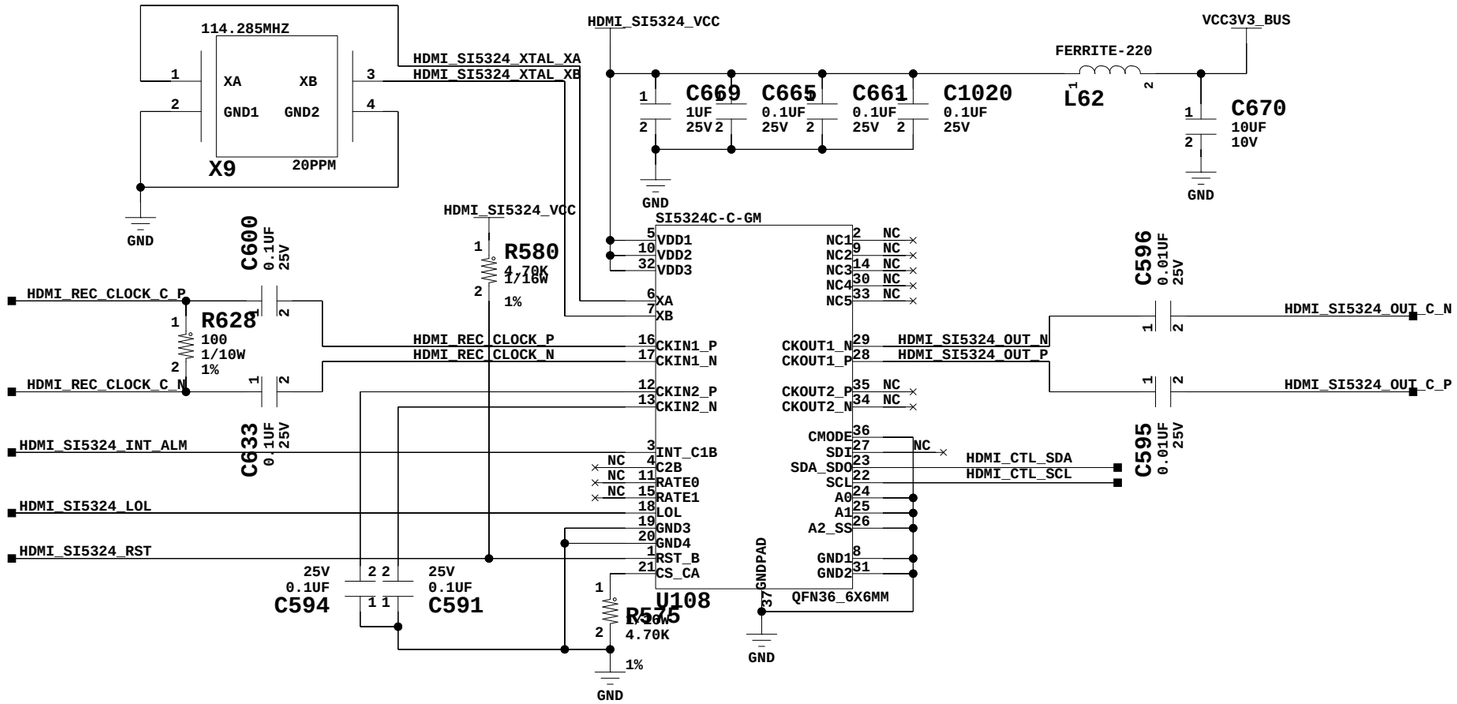

C560 C562 C561
C563 C564
0.1UF
25V
UTIL_1V13
C571
10UF
10V
GND
HDMI_TX_3V3
L61
VCC3V3_BUS
FERRITE-120
C559 C558 C570
0.1UF 0.1UF 10UF
25V 2 25V 2 10V
C569 C568 C567
0.01UF
25V
C565
C516 C515
C517
C518
C519
C578
C577
HDMI_TX0_P
HDMI_TX0_N
HDMI_TX1_P
HDMI_TX1_N
HDMI_TX2_P
HDMI_TX2_N
HDMI_TX_LVDS_OUT_P
HDMI_TX_LVDS_OUT_N
SN65DP159RGZ
VCC1
VCC2
VDD1
VDD2
VDD3
VDD4
VDD5
IN_D0P
IN_D0N
IN_D1P
IN_D1N
IN_D2P
IN_D2N
IN_CLKP
IN_CLKN
HDMI_TX0_C_P
HDMI_TX0_C_N
HDMI_TX1_C_P
HDMI_TX1_C_N
HDMI_TX2_C_P
HDMI_TX2_C_N
HDMI_TX_LVDS_OUT_C_P
HDMI_TX_LVDS_OUT_C_N
NC
HPD_SRC
SCL_SRC
SDA_SRC
SCL_CTL
SDA_CTL
VSADJ
I2C_EN_PIN
PRE_SEL
EQ_SEL_A0
HDMI_SEL_B_A1
SLEW_CTL
OE
SWAP_POL
CEC_EN
TX_TERM_CTL
AUX_SRC_N
AUX_SRC_P
GND1
GND2
GND3
GND4
GND_TAB
U94
HDMI_TX_SRC_SCL
HDMI_TX_SRC_SDA
HDMI_CTL_SCL
HDMI_CTL_SDA
HDMI_TX_EN
R557
64.9K
1/10W
1%
R554
6.49K
R558
R559
64.9K
M24C64-W
SCL
SDA
WC_B
E0
E1
E2
VCC
VSS
TSSOP_8
U109
C589
0.1UF
R644
10.0K
R645
R651
R652
10.0K
OUT_D0P
OUT_D0N
OUT_D1P
OUT_D1N
OUT_D2P
OUT_D2N
OUT_CLKP
OUT_CLKN
HPD_SNK
SCL_SNK
SDA_SNK
TX_TMDS_DAT0_P
TX_TMDS_DAT0_N
TX_TMDS_DAT1_P
TX_TMDS_DAT1_N
TX_TMDS_DAT2_P
TX_TMDS_DAT2_N
CLK_TX_TMDS_P
CLK_TX_TMDS_N
TX_HPD_SINK
R563
1/10W
5%
HDMI_TX_SNK_SCL
HDMI_TX_SNK_SDA
U91
U71
U72
U73
TPD1E05U06DPYT
U82
U83
U89
U90
1888811-1
TOP PORT
P7
DDC_VCC5
TMDS_DATA0_P
TMDS_DATA0_N
TMDS_DATA1_P
TMDS_DATA1_N
TMDS_DATA2_P
TMDS_DATA2_N
TMDS_CLK_P
TMDS_CLK_N
HPD_HEC_DATA_P
RSVD_HEC_DATA_N
CEC_SOURCE
CEC
DDC_SCL
DDC_SDA
TMDS_SHLD0
TMDS_SHLD1
TMDS_SHLD2
TMDS_CLK_SHLD
GND
SHELL_GND1
SHELL_GND2
TX_VIDEO_GND
HDMI_TX_5V0_CON
R881
0
1/10W
5%
C573
0.01UF
C576
C588
R919 R634
10.0K
1/10W
1%
VCC3V3
UTIL_5V0
C520
0.1UF
C566
1UF
25V
TPD12S016RKTR
VCCA
VCC5V
CEC_A
SCL_A
SDA_A
HPD_A
LS_OE
CT_HPD
D2_P
D2_N
D1_P
D1_N
D0_P
D0_N
CLK_P
CLK_N
5V_OUT
CEC_B
SCL_B
SDA_B
HPD_B
GND3
GND2
GND1
HDMI_TX_CEC
HDMI_TX_HPD
C557
U70
PL HDMI TX
XILINX
TITLE: PL HDMI TX
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU102_REV1_0
ASSY P/N: 0431959
PCB P/N: 1280868
SCH P/N: 0381701
TEST P/N: TSS0179
DATE: 09/20/2016:10:27
VER: 1.0
SHEET SIZE: B
REV: 01
SHEET 35 OF 87
DRAWN BY: BF



PL HDMI RX

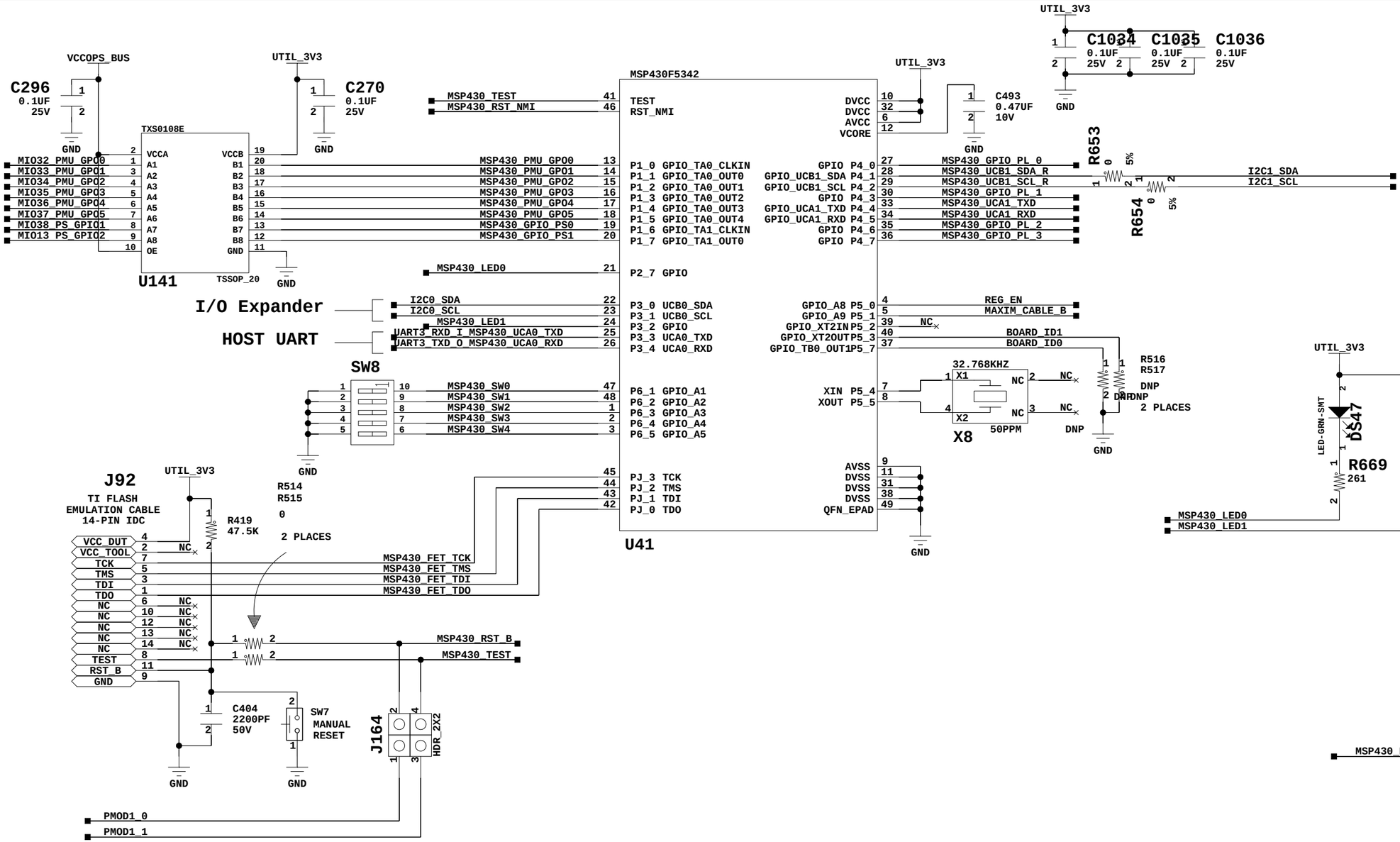
XILINX

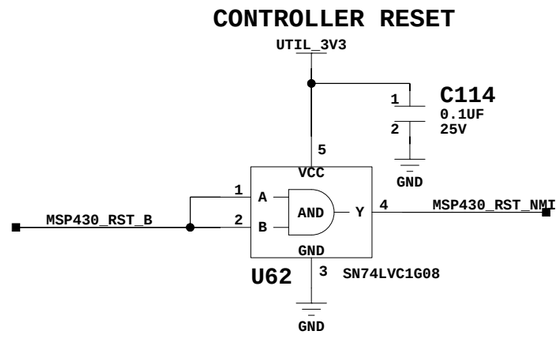
TITLE: PL HDMI RX SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 36 OF 87	DRAWN BY: BF



PL HDMI Clock Recovery

TITLE: PL HDMI Clock Recovery SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 37 OF 87	DRAWN BY: BF

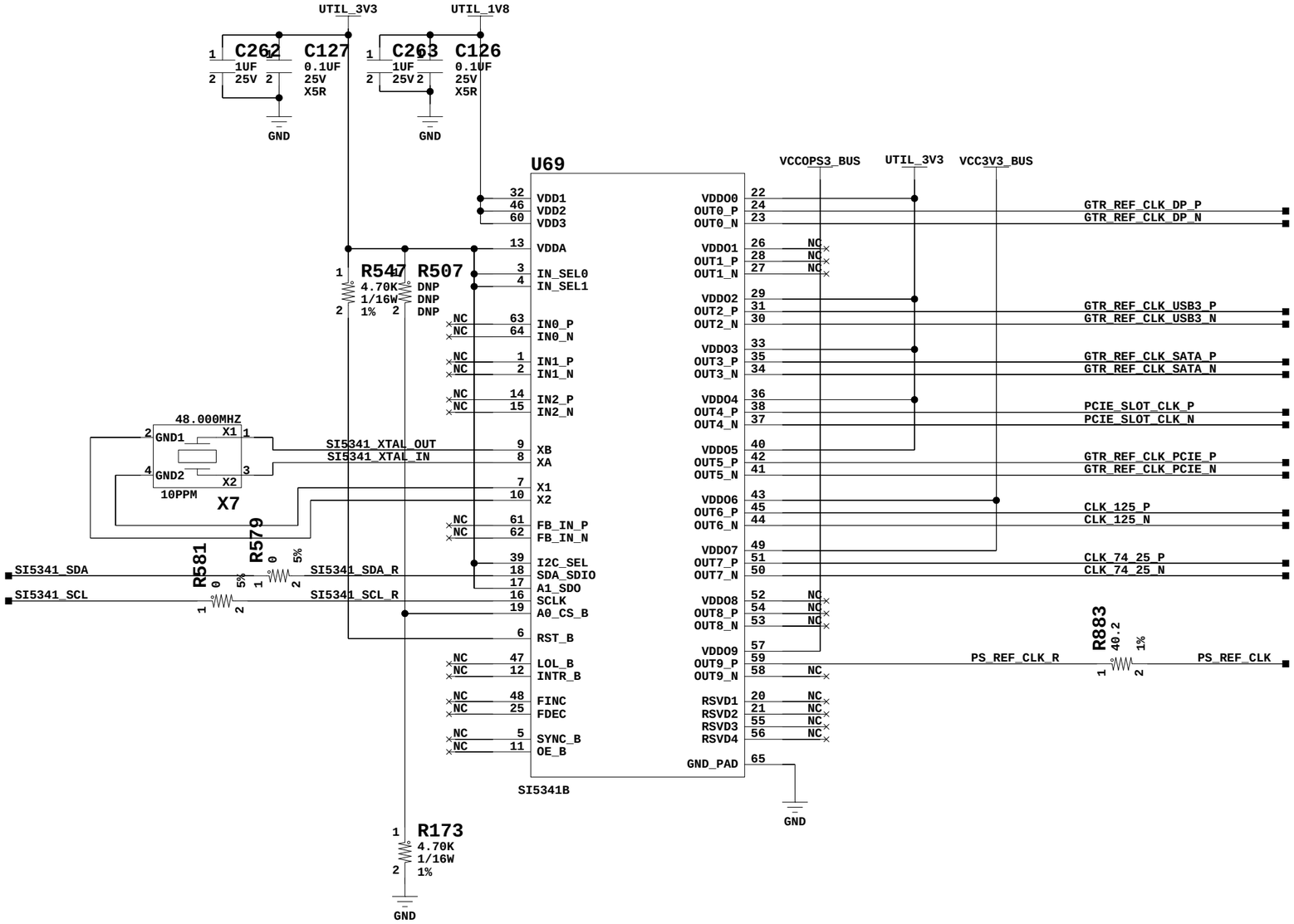




System Controller

XILINX

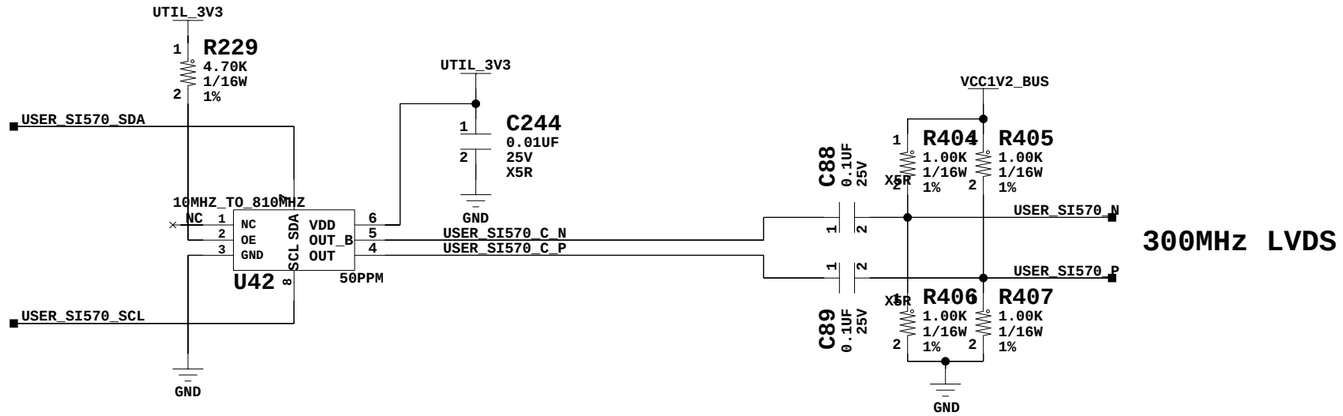
TITLE: System Controller SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 38 OF 87	DRAWN BY: BF



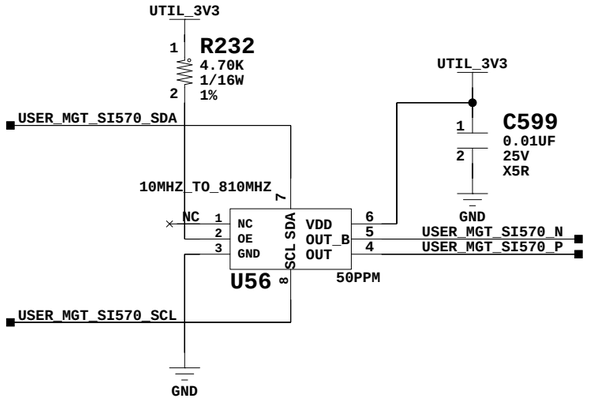
Fixed Clocks

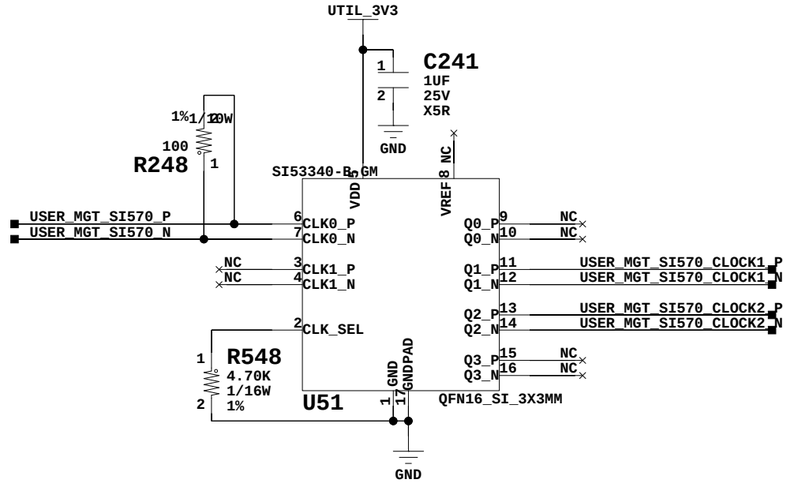
XILINX

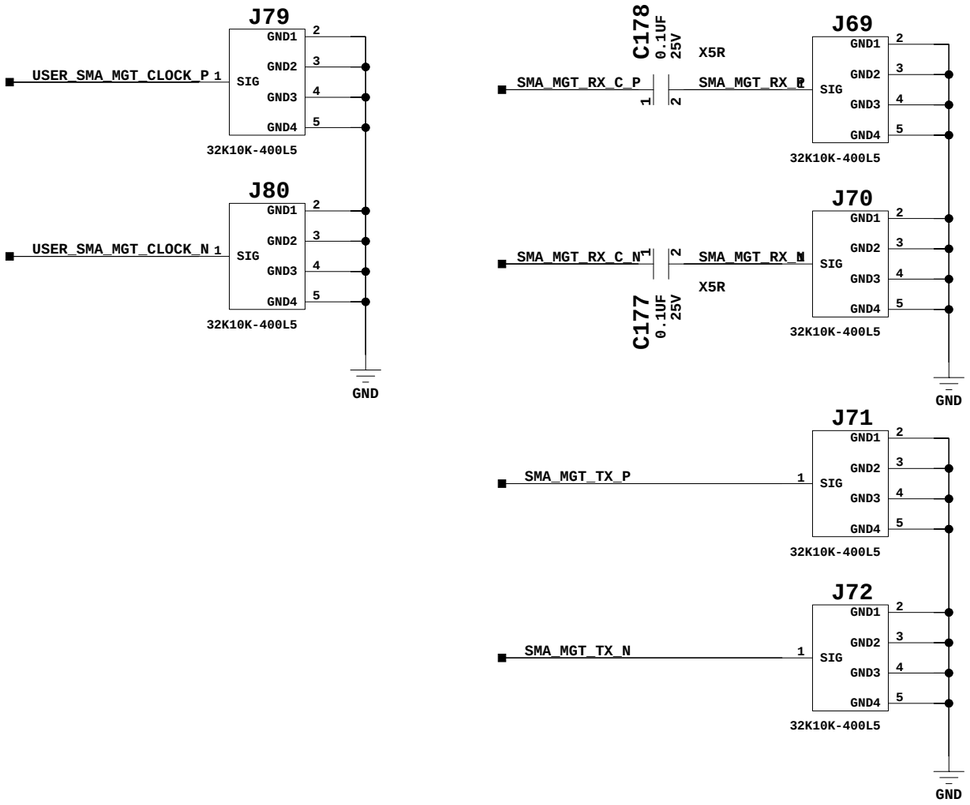
TITLE: Fixed Clocks SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 39 OF 87	DRAWN BY: BF



300MHz LVDS



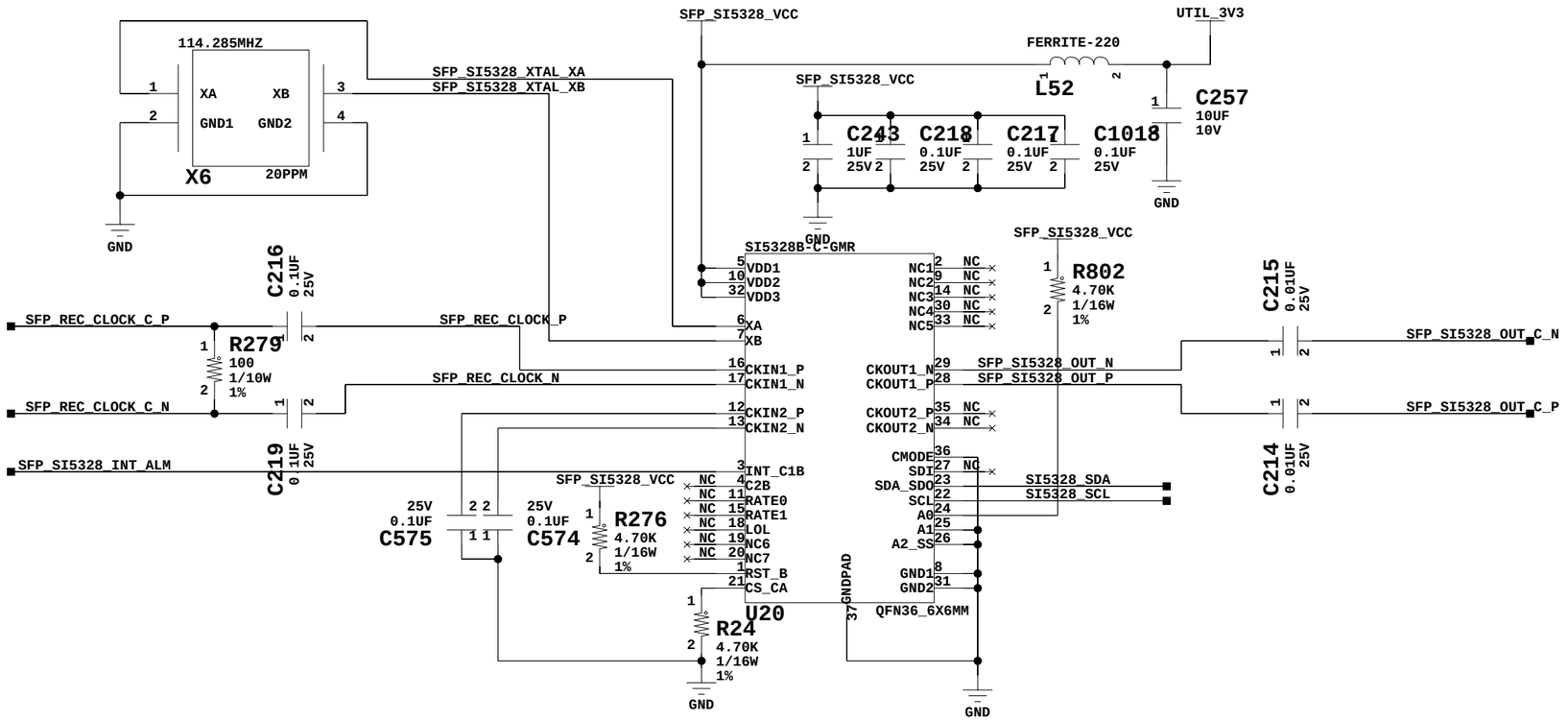




PL Programmable Clocks - SMAs

XILINX

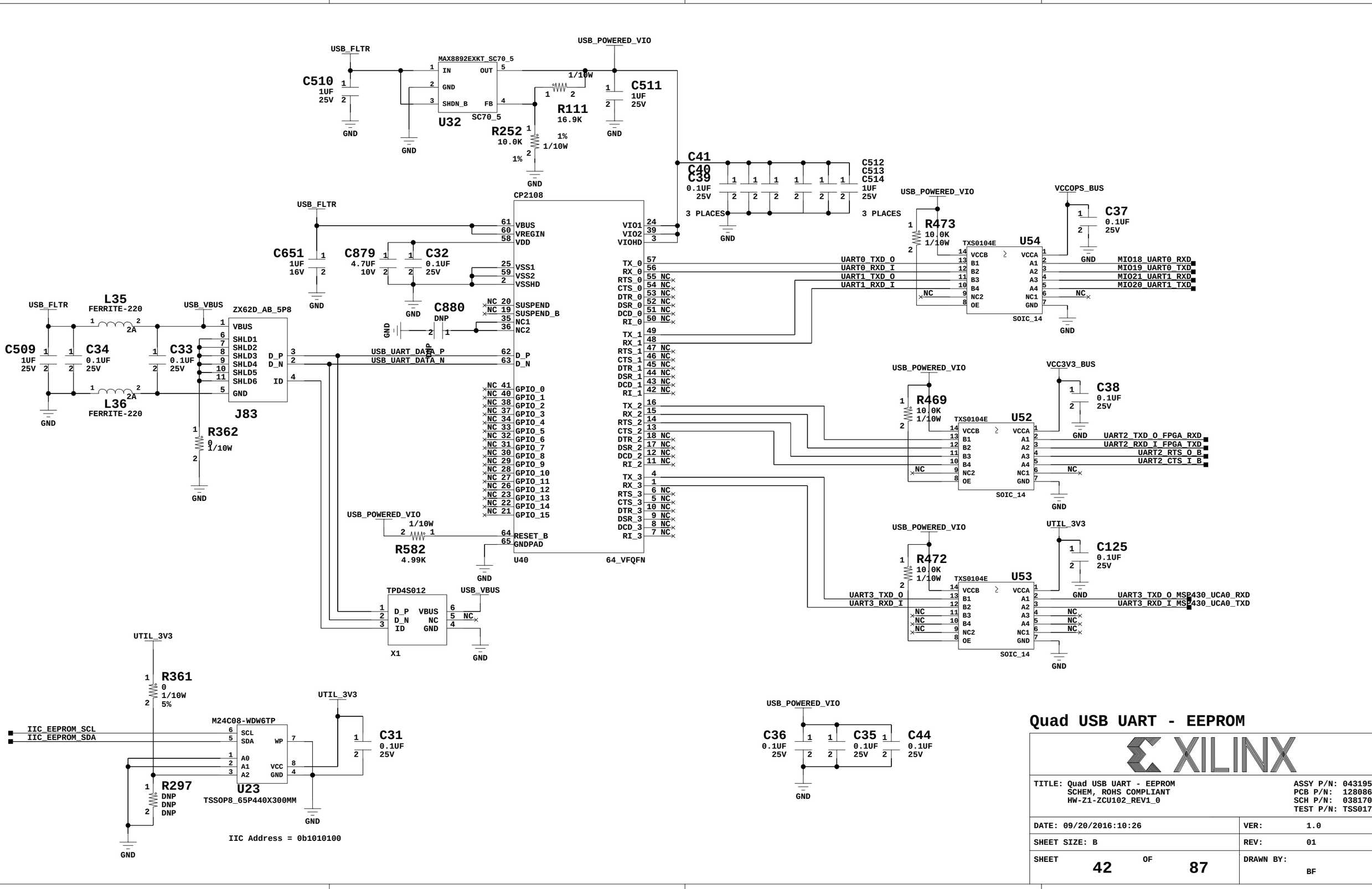
TITLE: PL Programmable Clocks - SMAs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 40 OF 87	DRAWN BY: BF



PL SFP Clock Recovery

XILINX

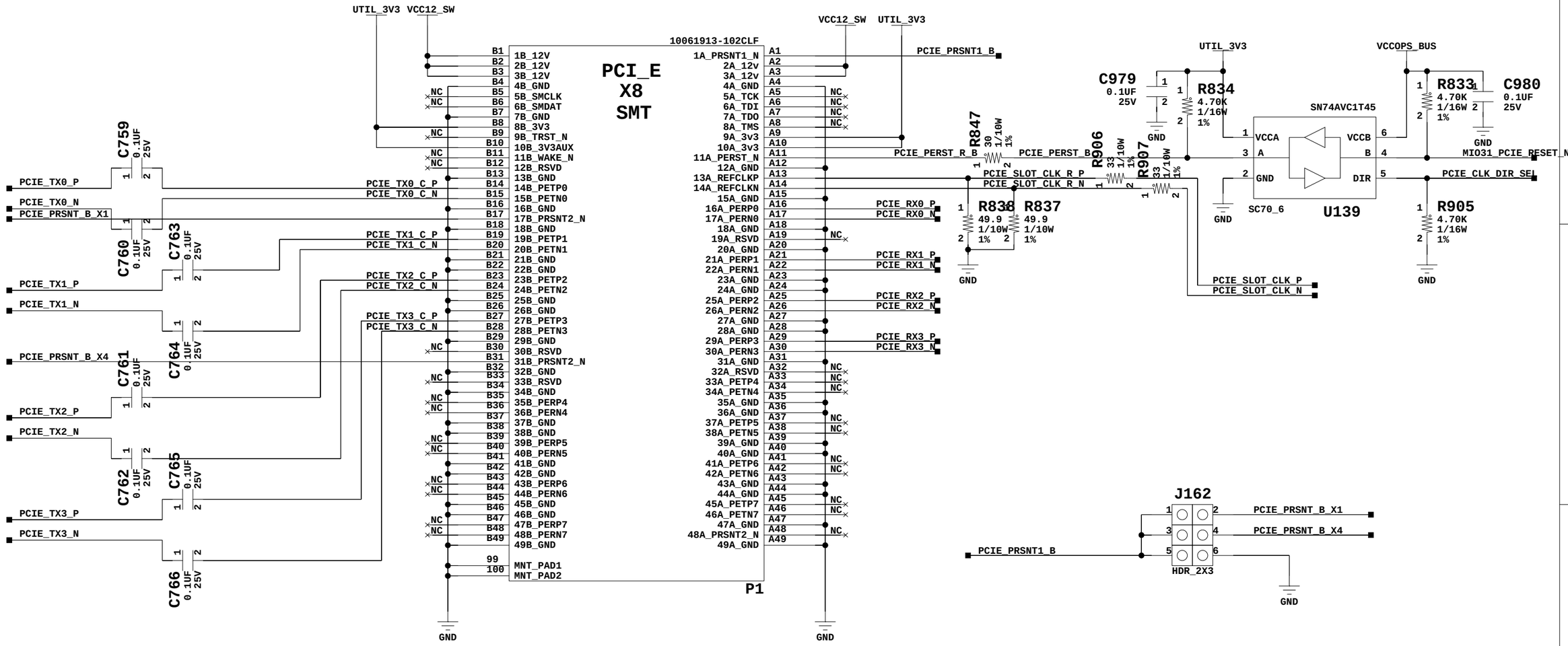
TITLE: PL SFP Clock Recovery SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 02
SHEET 41 OF 87	DRAWN BY: BF



Quad USB UART - EEPROM

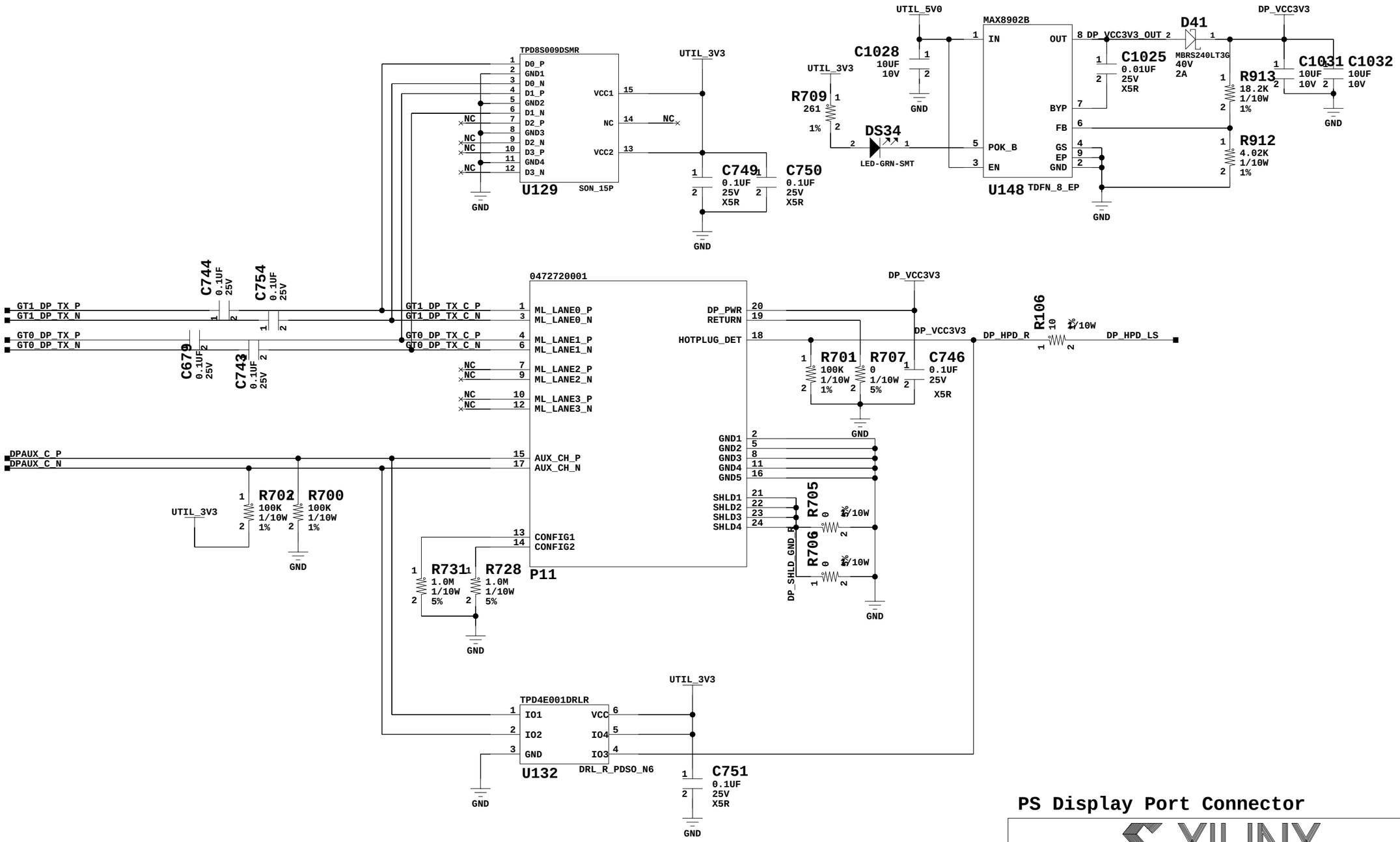
XILINX

TITLE: Quad USB UART - EEPROM SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 42 OF 87	DRAWN BY: BF



PS PCIe x4 Slot - x8 Connector

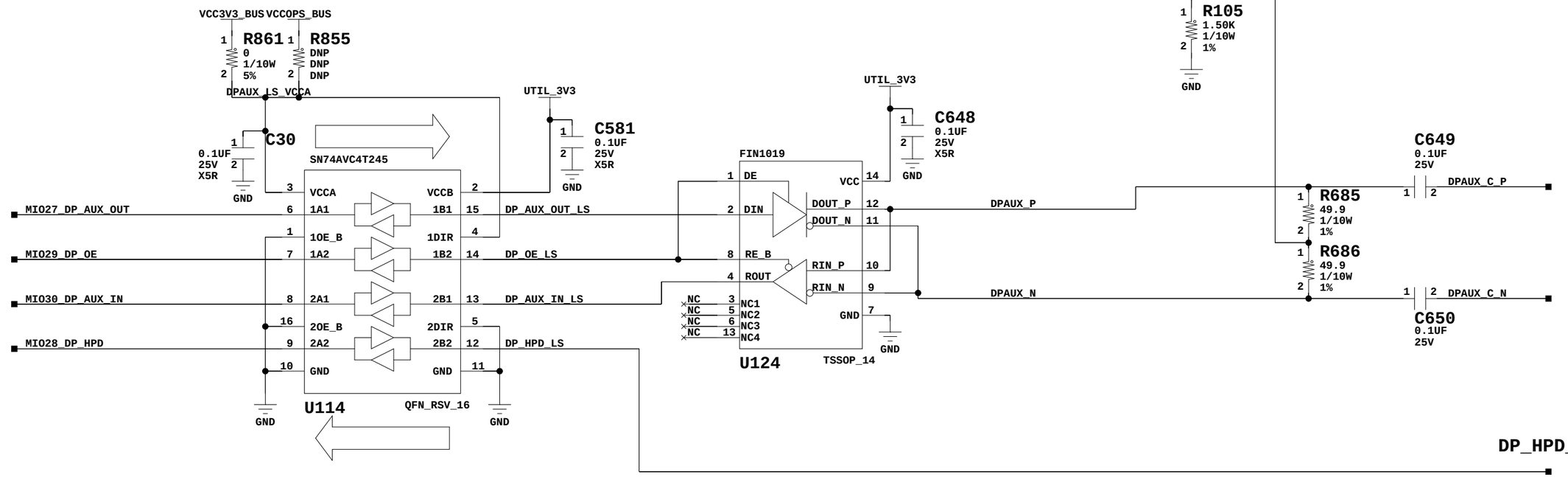
TITLE: PS PCIe x4 Slot - x8 Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 43 OF 87	DRAWN BY: BF



PS Display Port Connector

XILINX

TITLE: PS Display Port Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 44 OF 87	DRAWN BY: BF

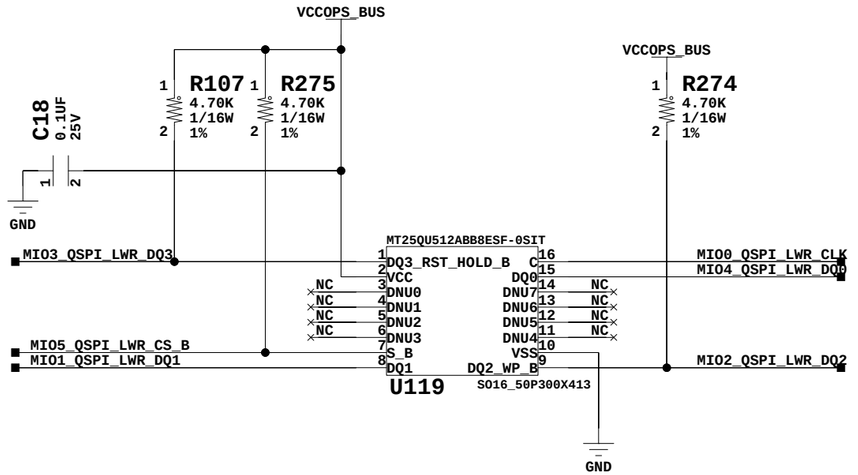


DP_HPD_LS

PS Display Port IO

XILINX

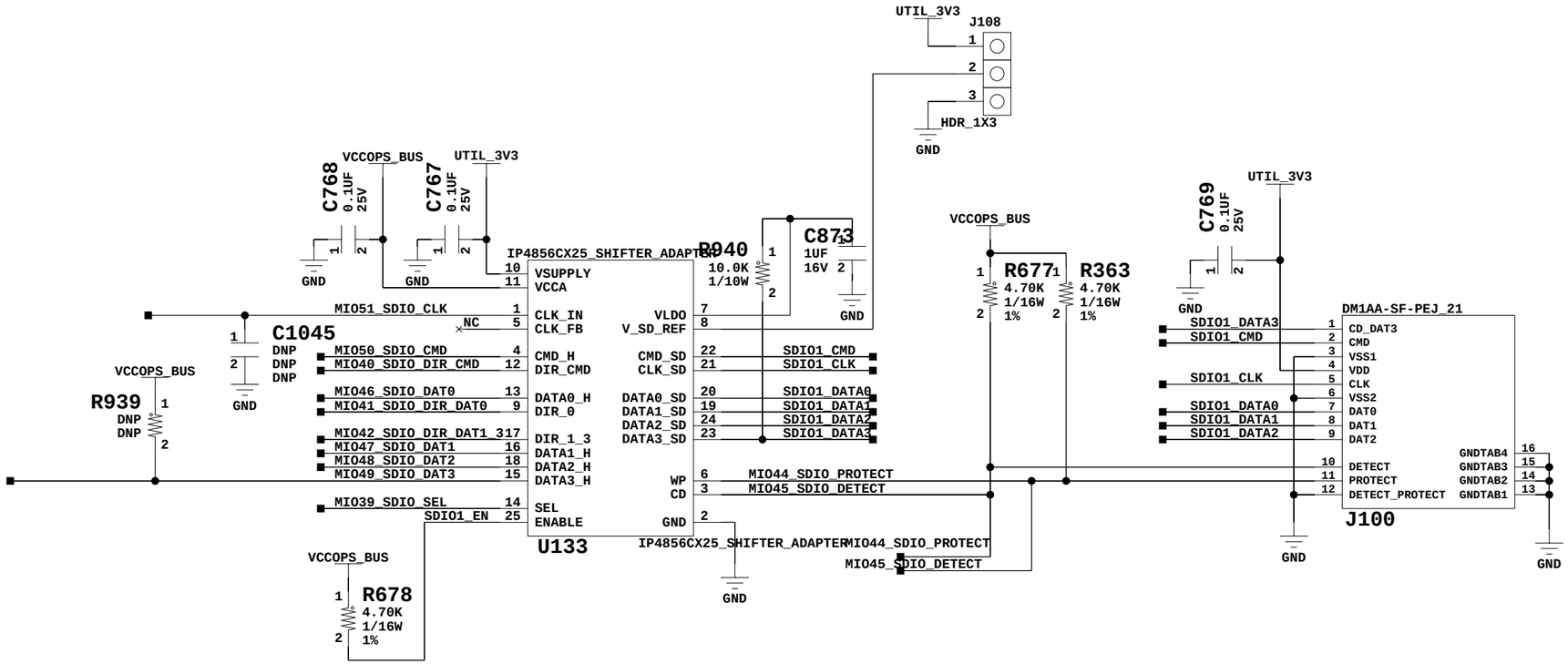
TITLE: PS Display Port IO SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 45 OF 87	DRAWN BY: BF



PS QSPI

XILINX

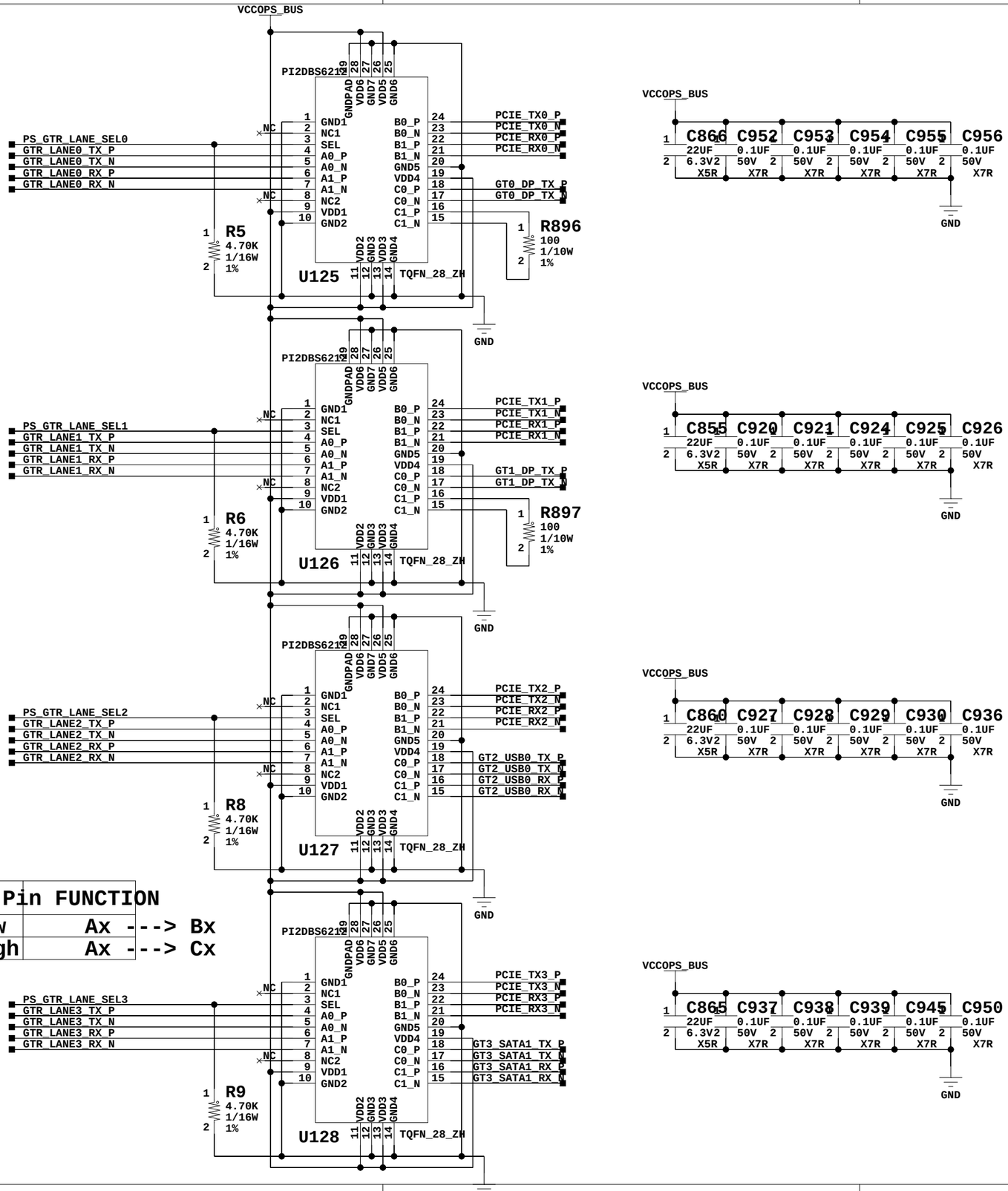
TITLE: PS QSPI SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 46 OF 87	DRAWN BY: BF



PS SD Card Connector

XILINX

TITLE: PS SD Card Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 47 OF 87	DRAWN BY: BF



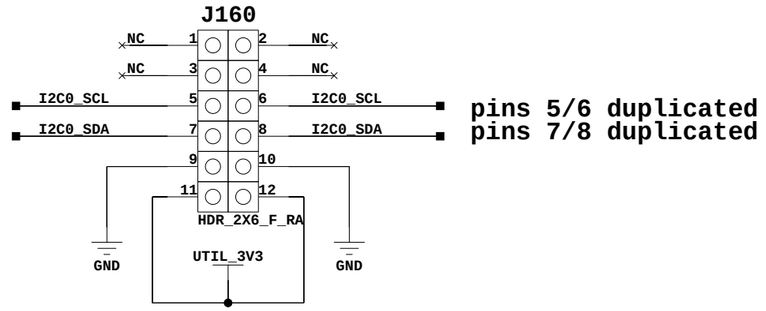
SEL Pin	FUNCTION
Low	Ax --> Bx
High	Ax --> Cx

PS GTR MUX - SATA

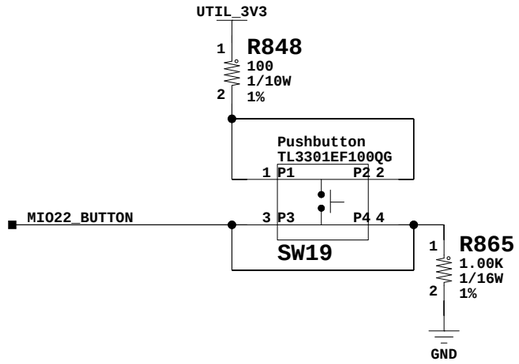
XILINX

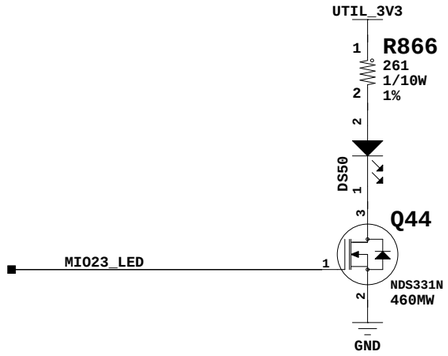
TITLE: PS GTR MUX - SATA SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 48 OF 87	DRAWN BY: BF

Connects to R.A. Female 2x6 PMOD receptacle



pins 5/6 duplicated
pins 7/8 duplicated

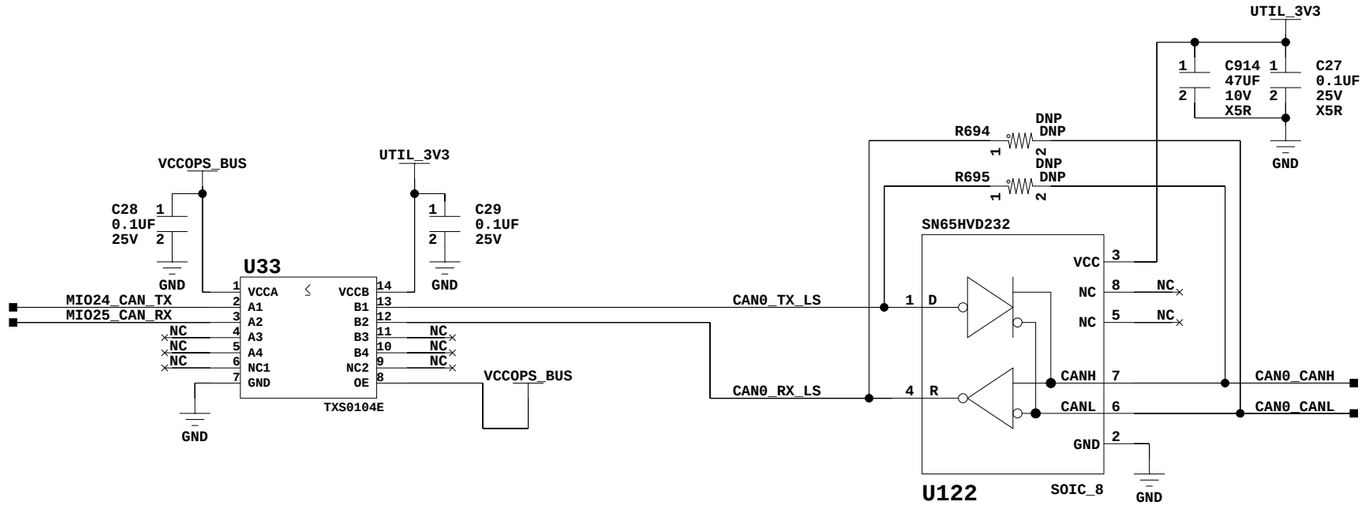


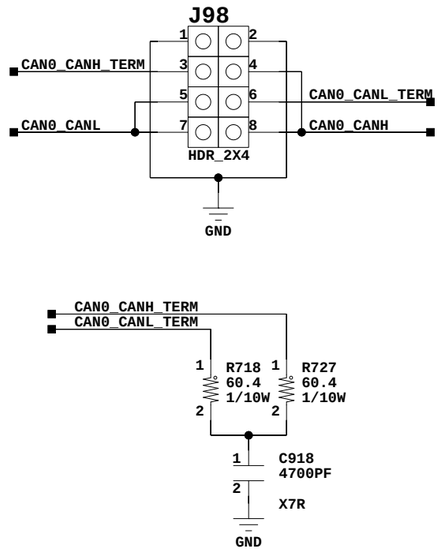


PS MIO PMOD - Button - LED

XILINX

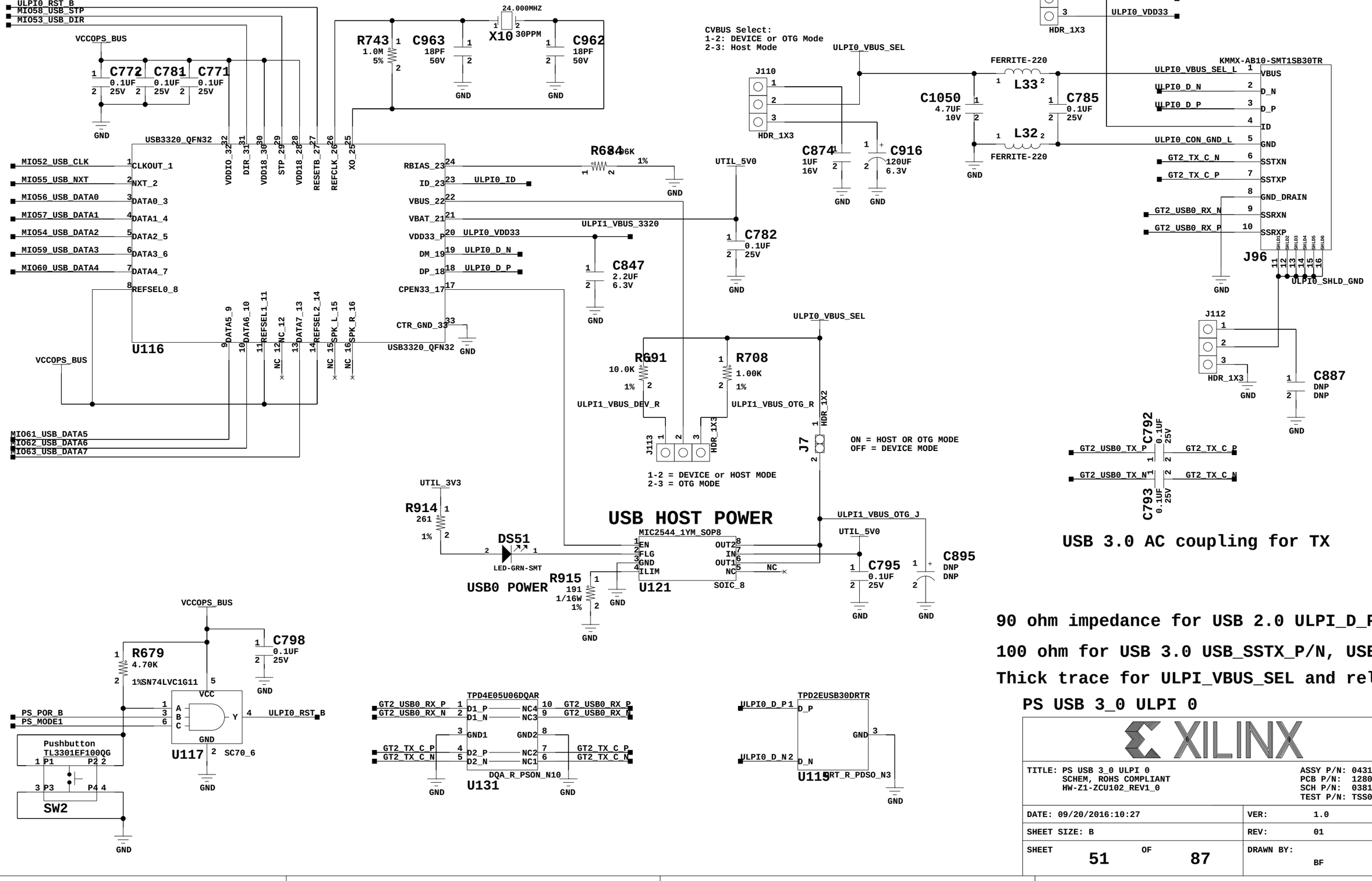
TITLE: PS MIO PMOD - Button - LED SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 49 OF 87	DRAWN BY: BF



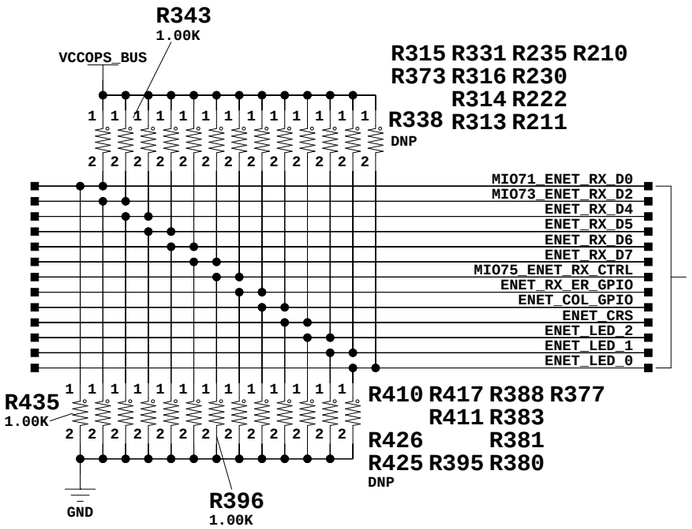


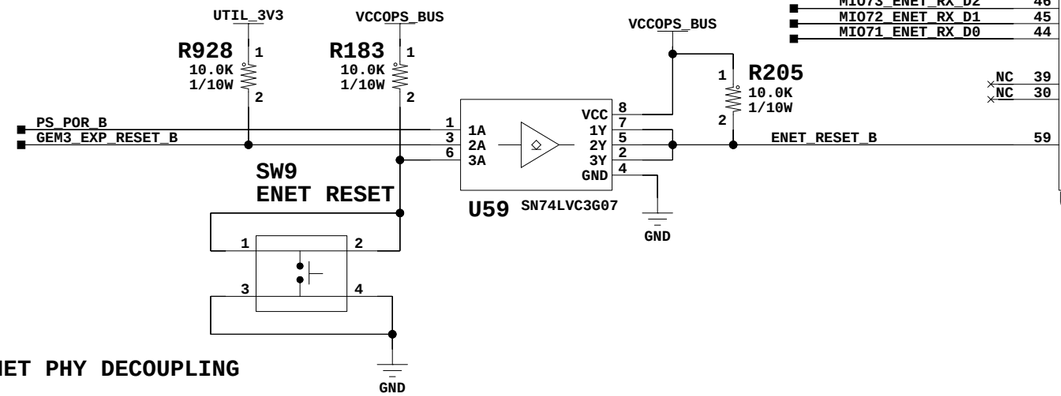
PS CAN Bus

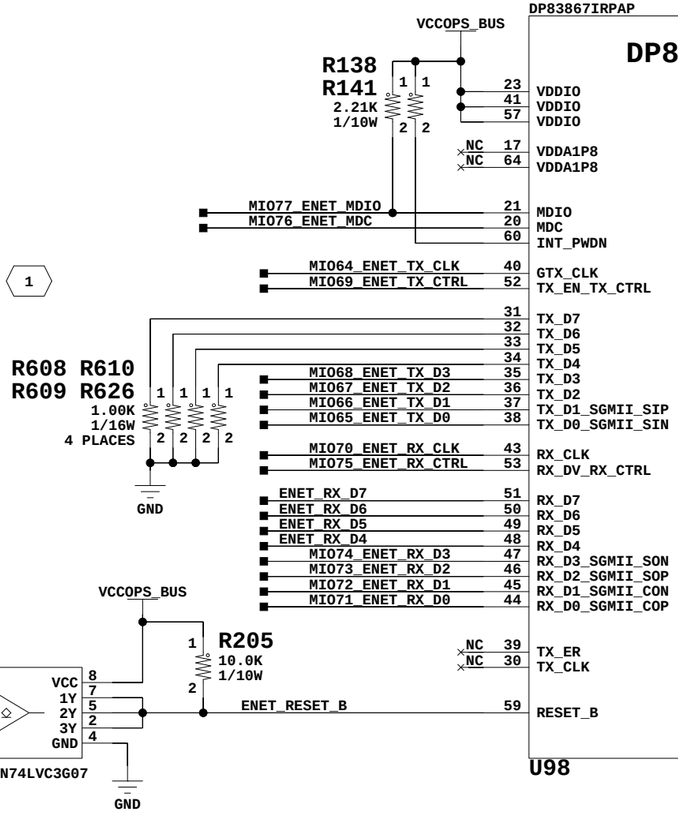
TITLE: PS CAN Bus SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 50 OF 87	DRAWN BY: BF

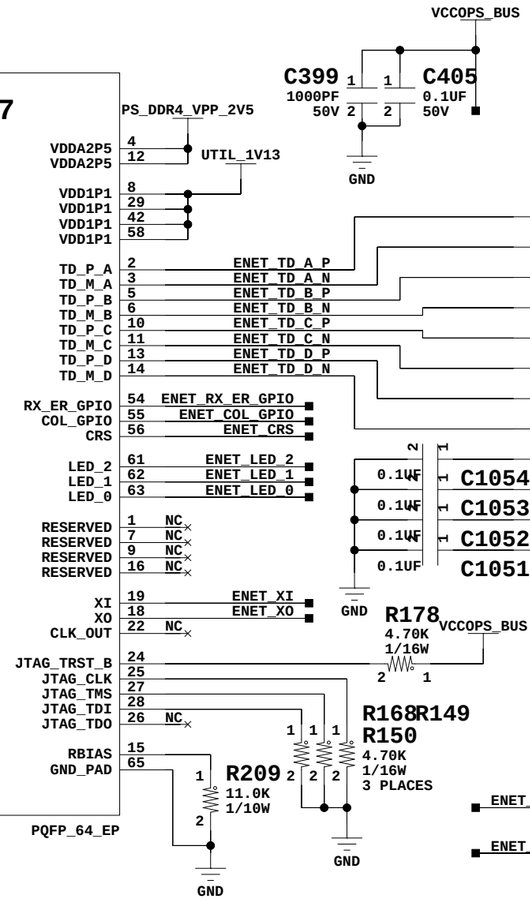


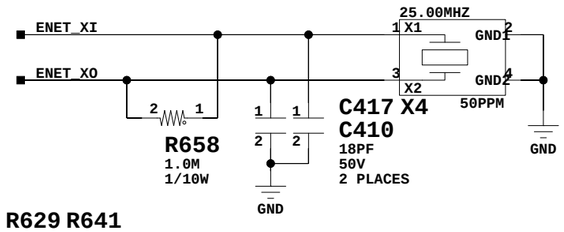
TITLE: PS USB 3_0 ULPI 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 51 OF 87	DRAWN BY: BF



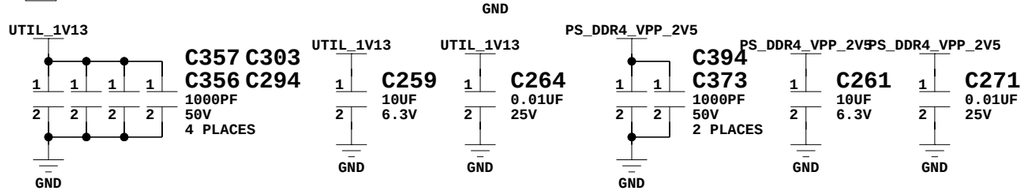


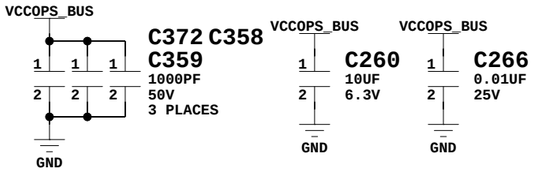




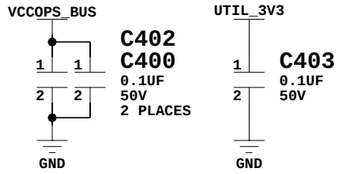


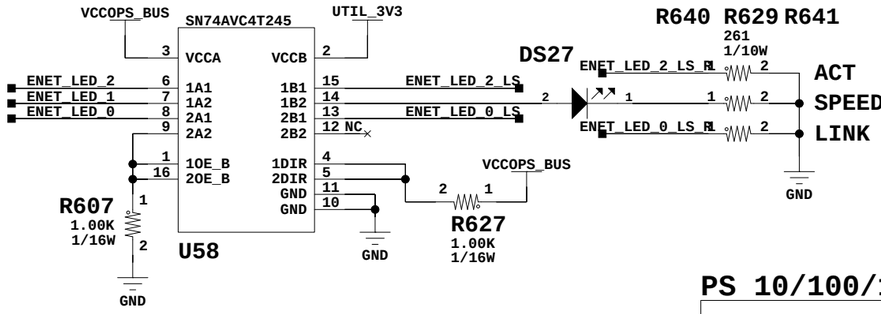
2 ENET PHY DECOUPLING





PERIPHERAL DECOUPLING





2 THESE CAPACITORS ARE PLACED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PINS ON THE DP83867.

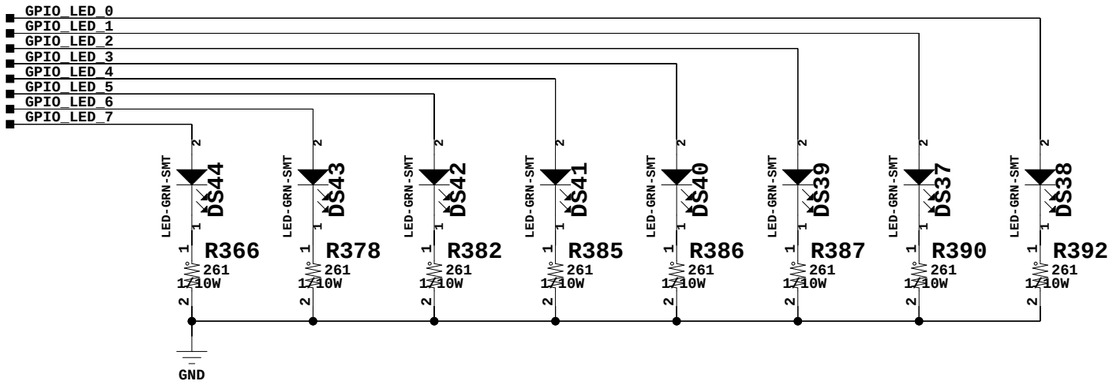
1 STRAP CONFIGURATION RESISTORS. SEE DP83867 DATASHEET FOR DETAILS.

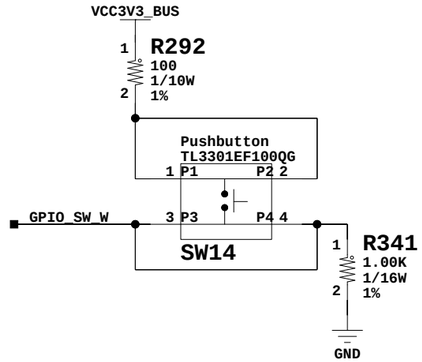
PS 10/100/1000 Ethernet PHY

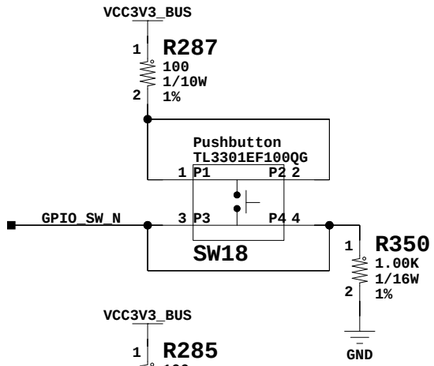
XILINX

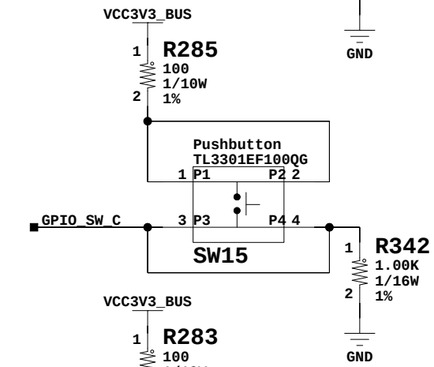
TITLE: PS 10/100/1000 Ethernet PHY SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 52 OF 87	DRAWN BY: BF

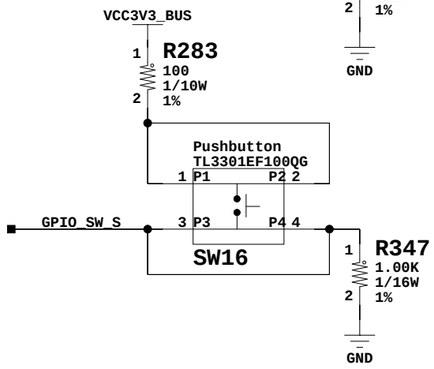
LEDs near top right edge

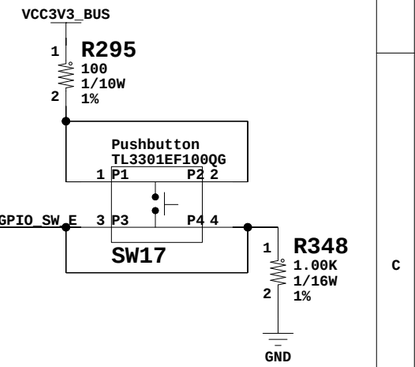


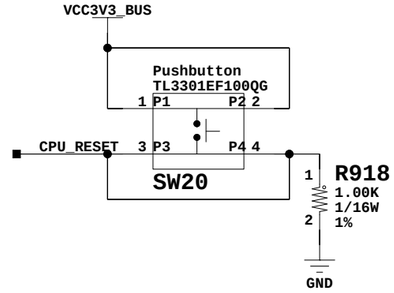


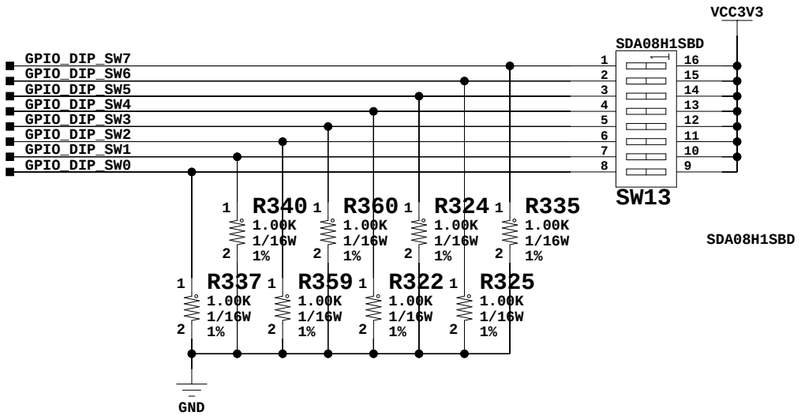










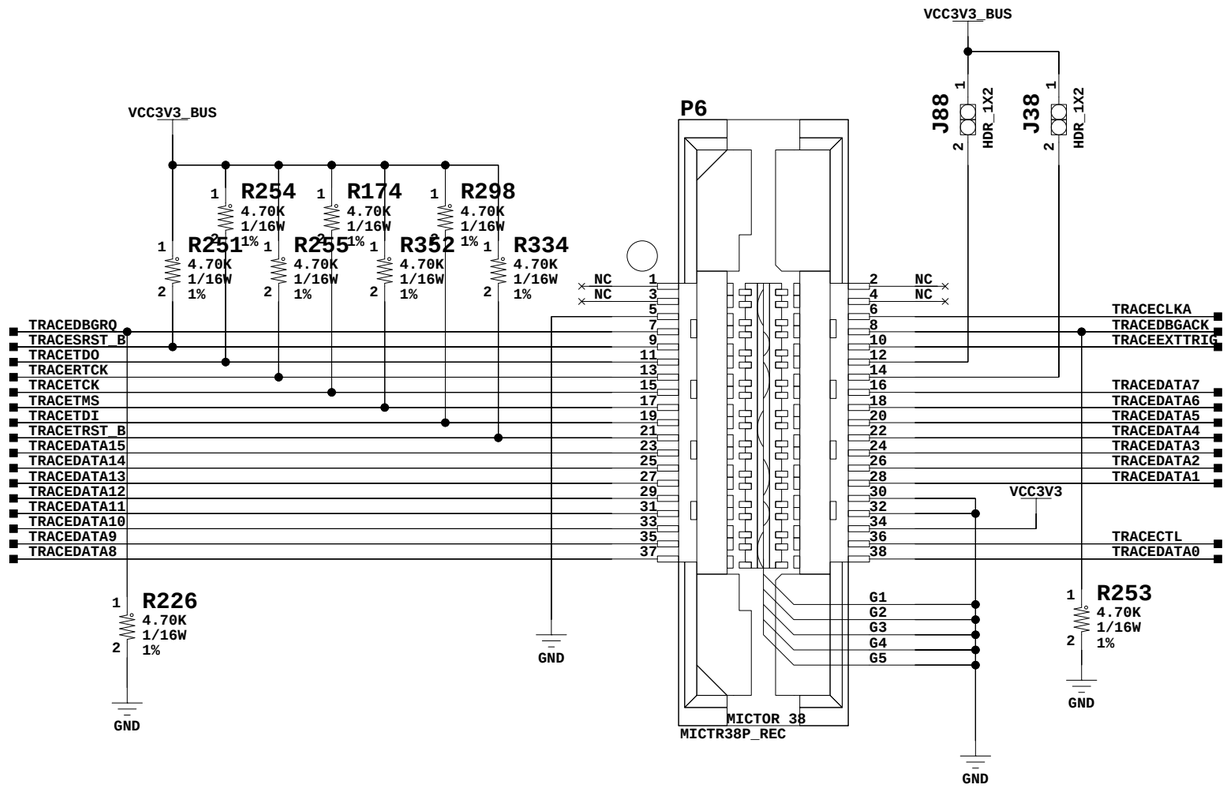


PL Buttons - Switches - LEDs

XILINX

TITLE: PL Buttons - Switches - LEDs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 53 OF 87	DRAWN BY: BF

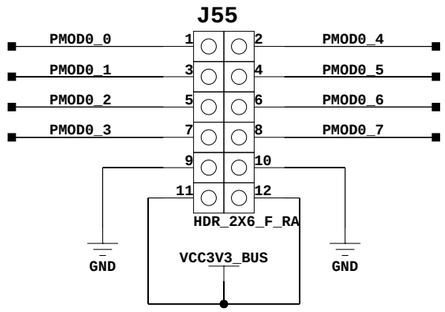
EMIO ARM Trace/Debug

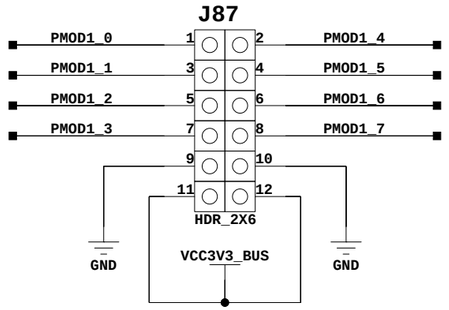


PL EMIO ARM Trace Debug

XILINX

TITLE: PL EMIO ARM Trace Debug SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 54 OF 87	DRAWN BY: BF



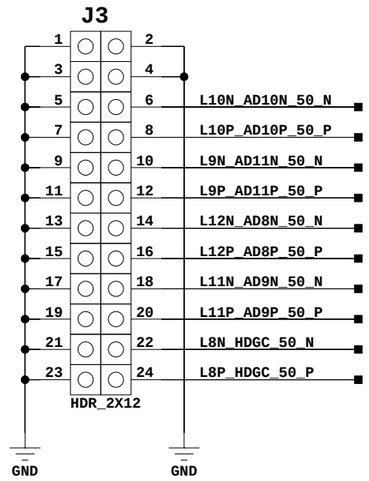


PL PMODs

XILINX

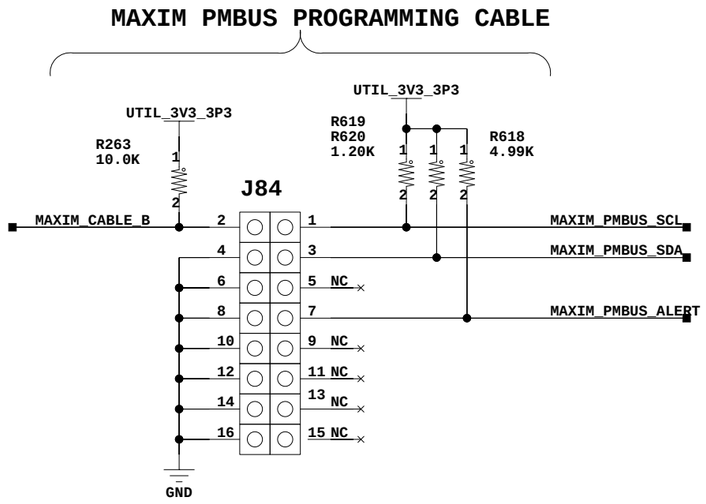
TITLE: PL PMODs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 55 OF 87	DRAWN BY: BF

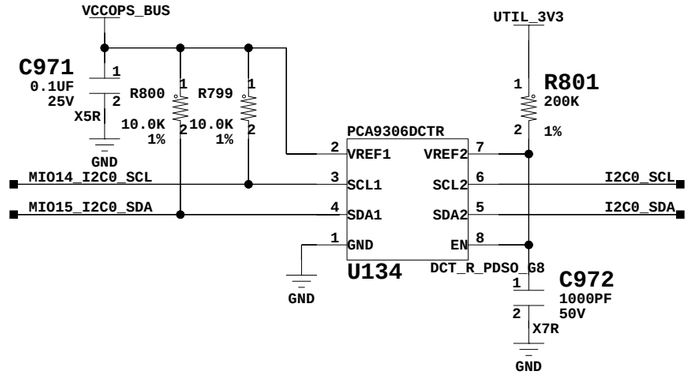
Prototype Header

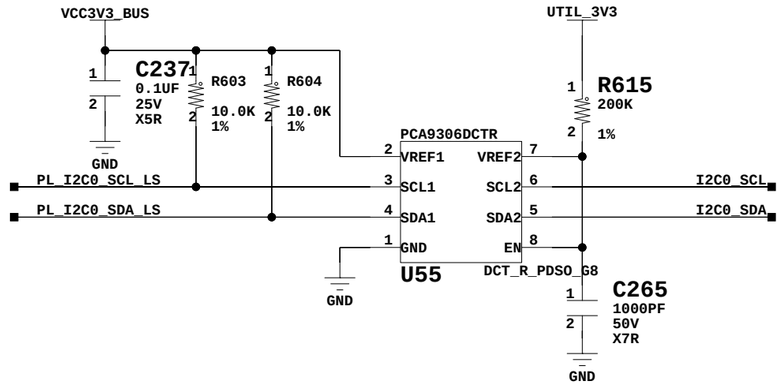


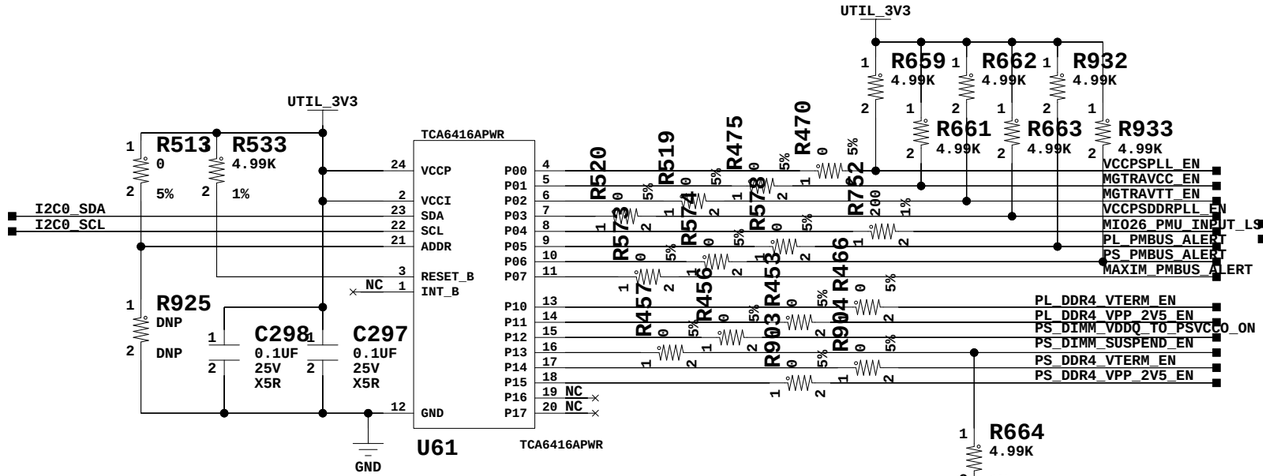
PL SYSMON Prototype Header

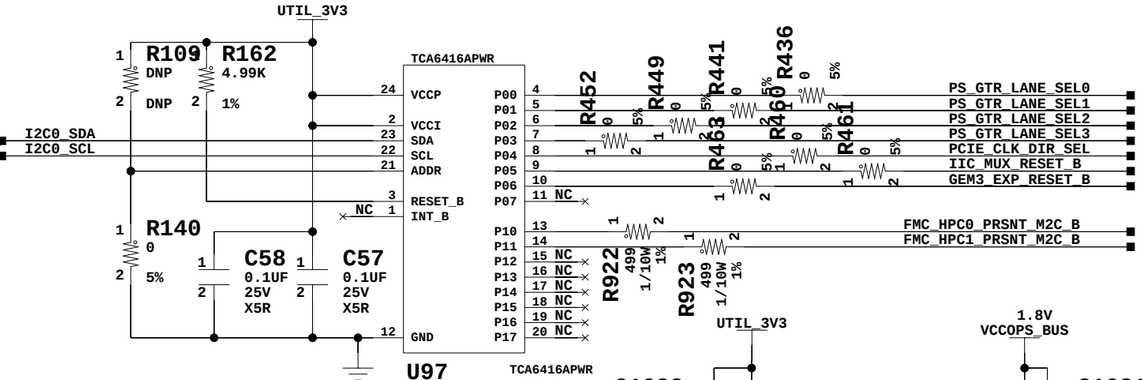
TITLE: PL SYSMON Prototype Header SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 02
SHEET 56 OF 87	DRAWN BY: BF

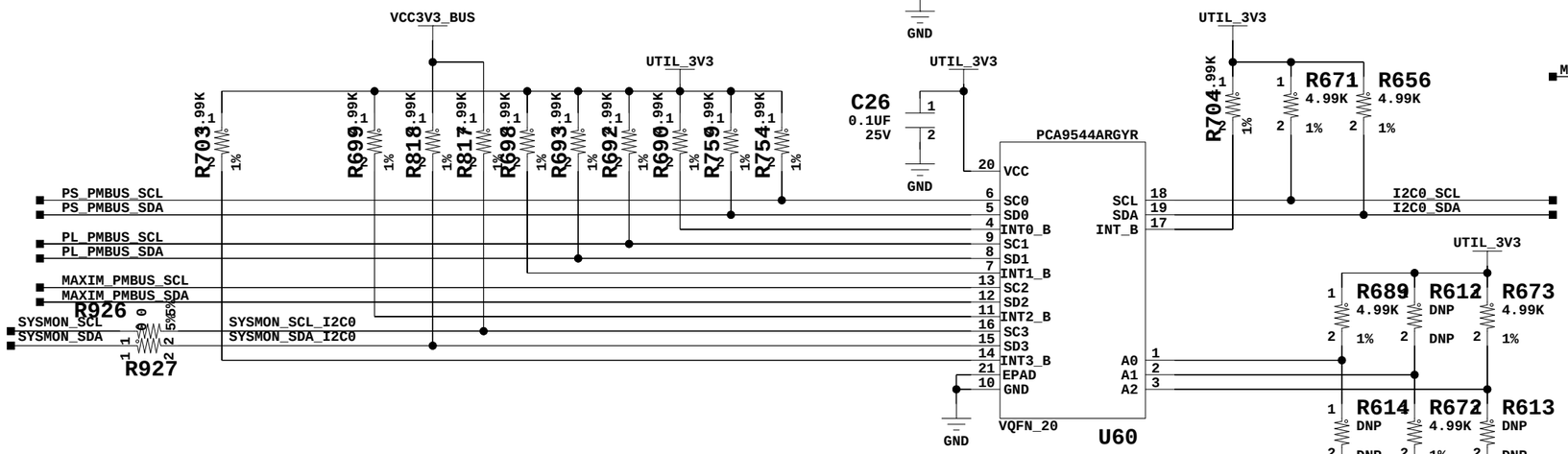


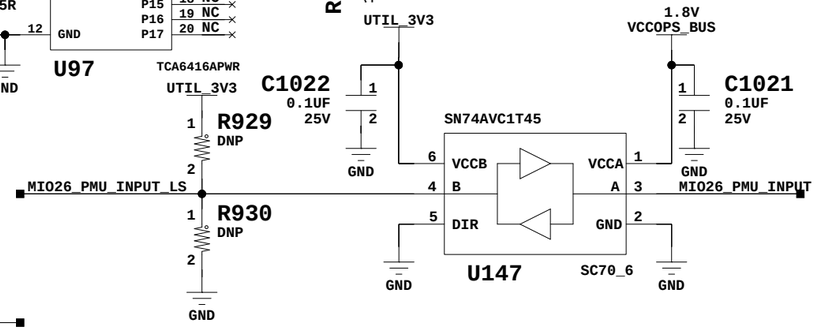






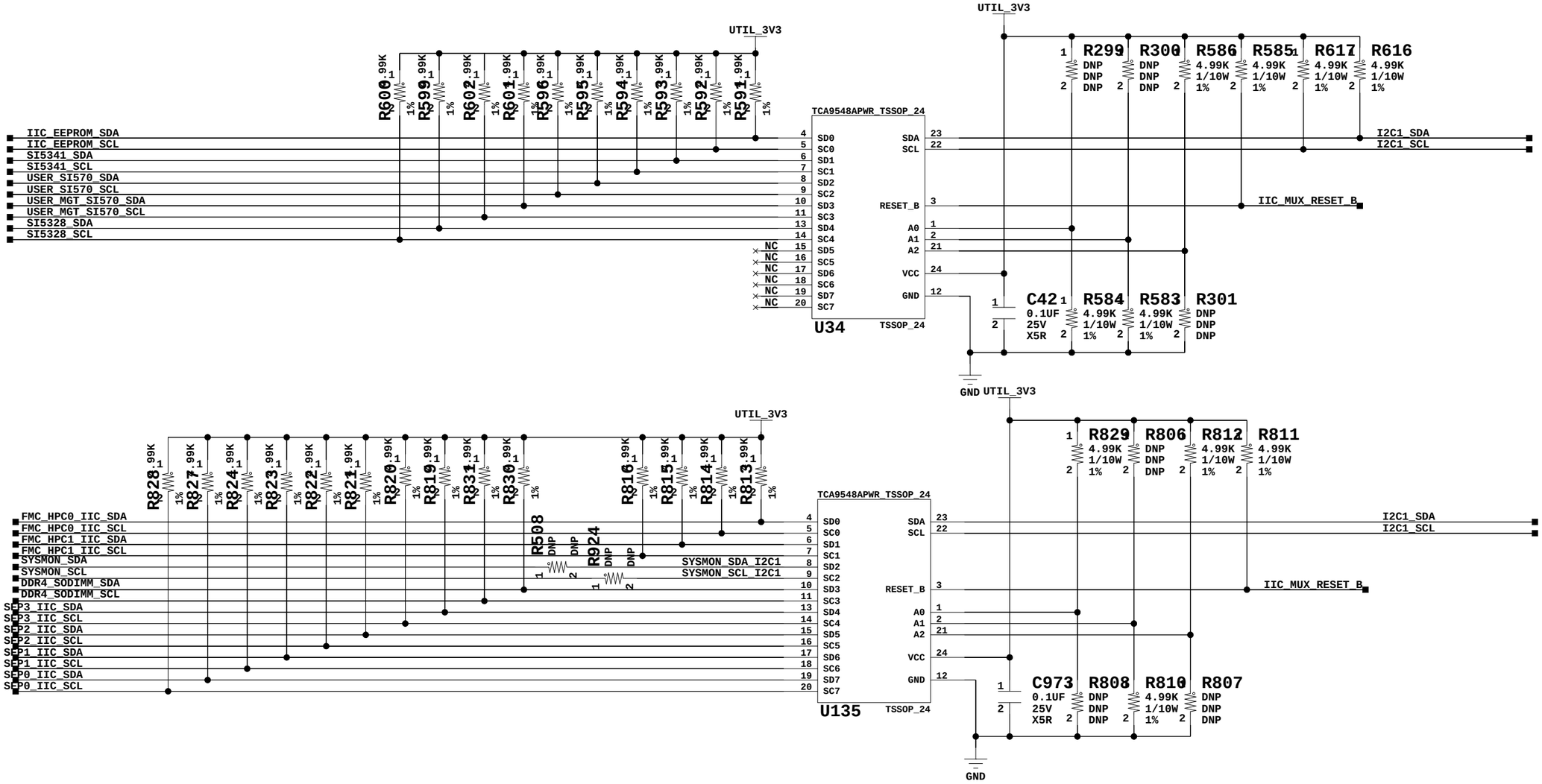




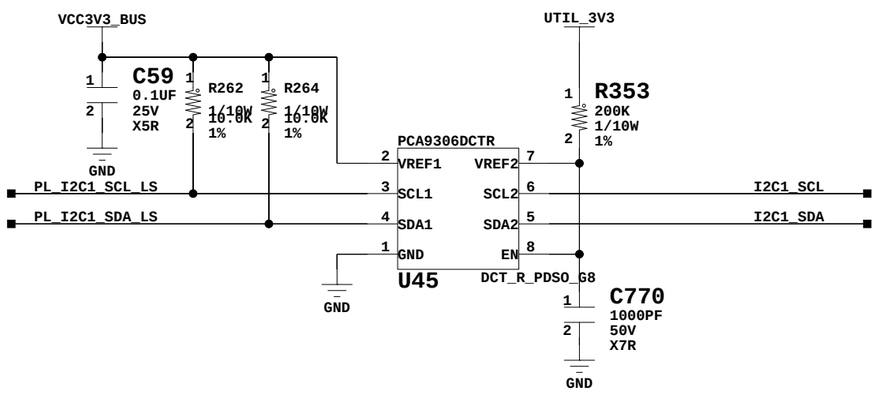


I2C0 MUXes Expanders Level Shifters PMBUS He

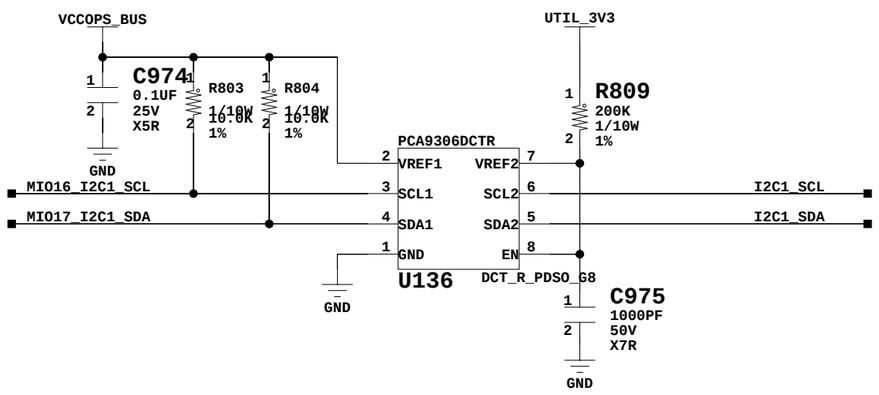
TITLE: I2C0 MUXes Expanders Level Shifters PMBUS Hea SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 57 OF 87	DRAWN BY: BF



PL I2C Level Shifter (disabled if VCC3V3 is off)



PS I2C Level Shifter (I2C1)

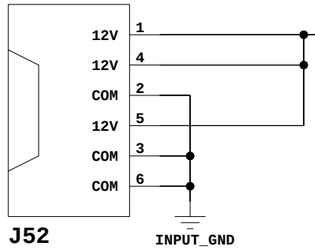


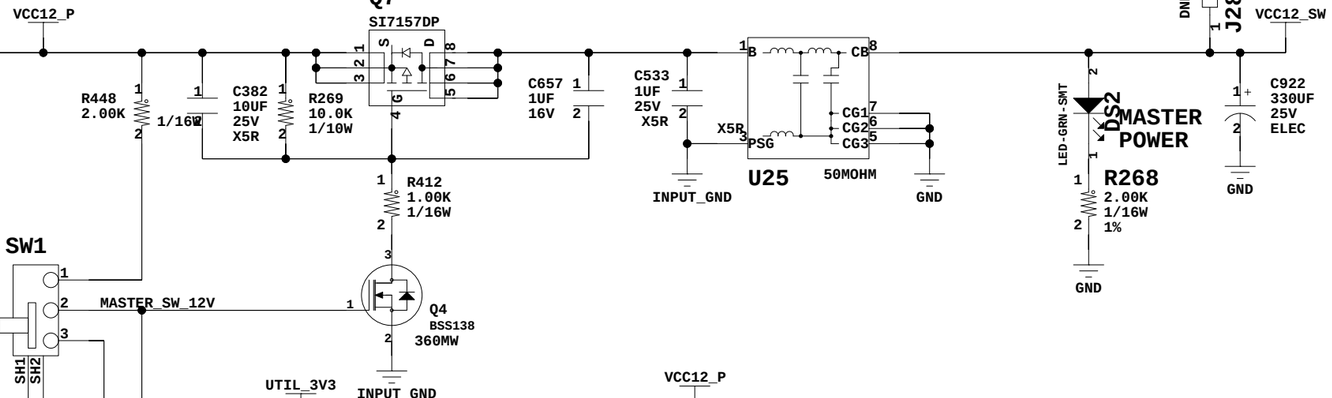
I2C1 MUXes and Level Shifters

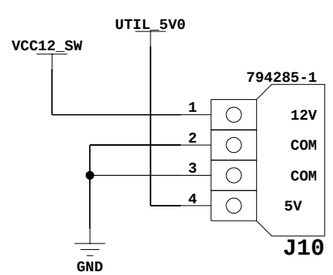
XILINX

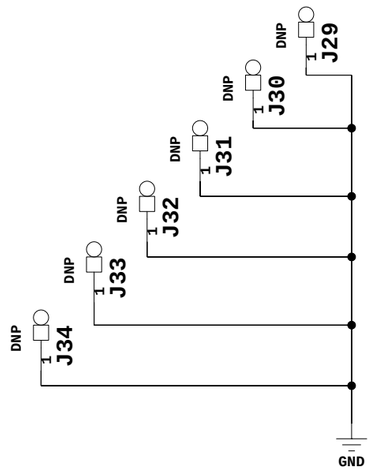
TITLE: I2C1 MUXes and Level Shifters SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 58 OF 87	DRAWN BY: BF

6-PIN MINI-FIT AC ADAPTER (BRICK)

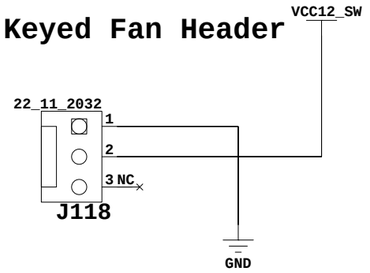








GND Test points

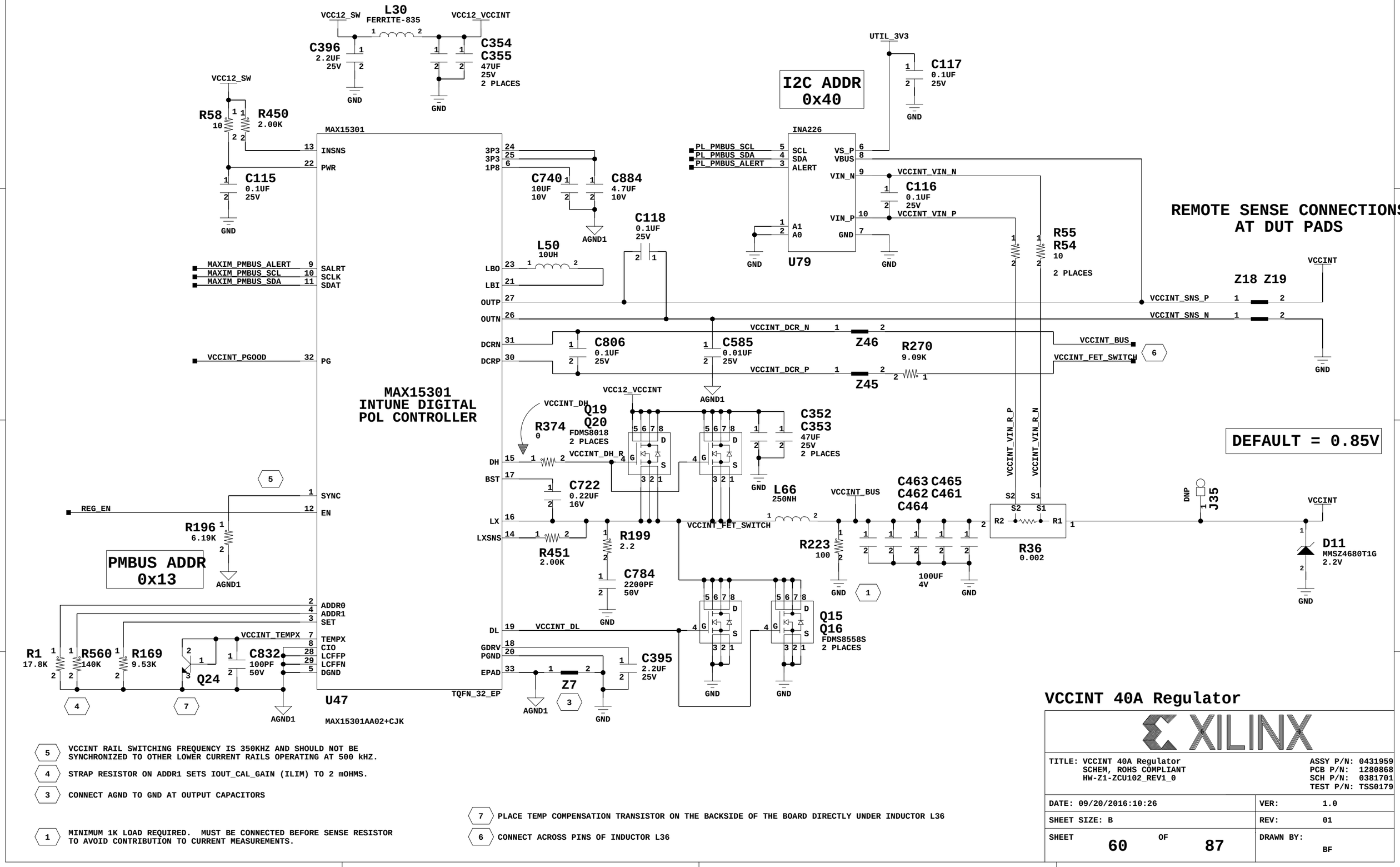


12V Power Connectors Switch

1 Maxim Regulator Inhibit Jumper

XILINX

TITLE: 12V Power Connectors Switch SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 59 OF 87	DRAWN BY: BF



5 VCCINT RAIL SWITCHING FREQUENCY IS 350KHZ AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 500 kHZ.

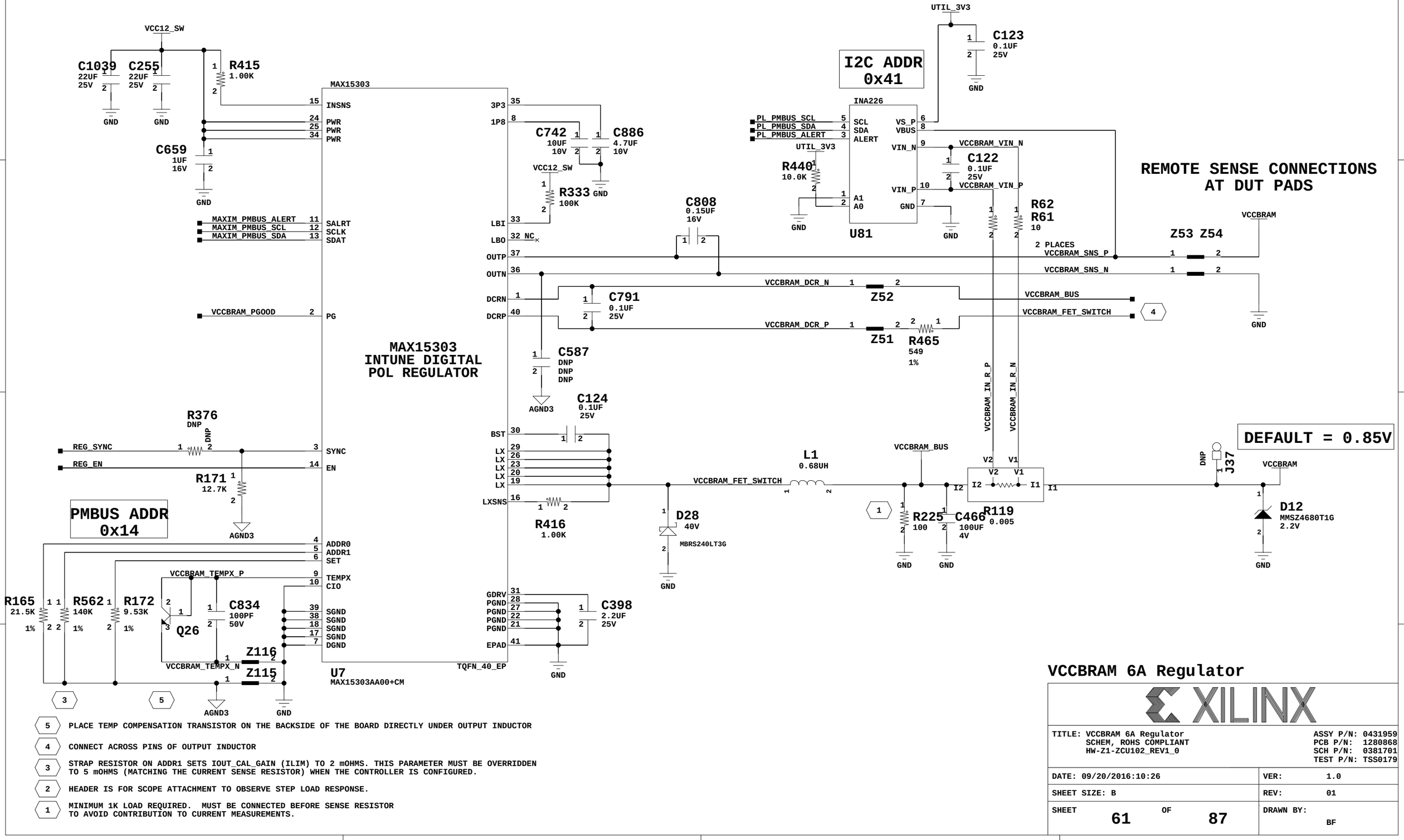
4 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS.

3 CONNECT AGND TO GND AT OUTPUT CAPACITORS

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

7 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L36

6 CONNECT ACROSS PINS OF INDUCTOR L36



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

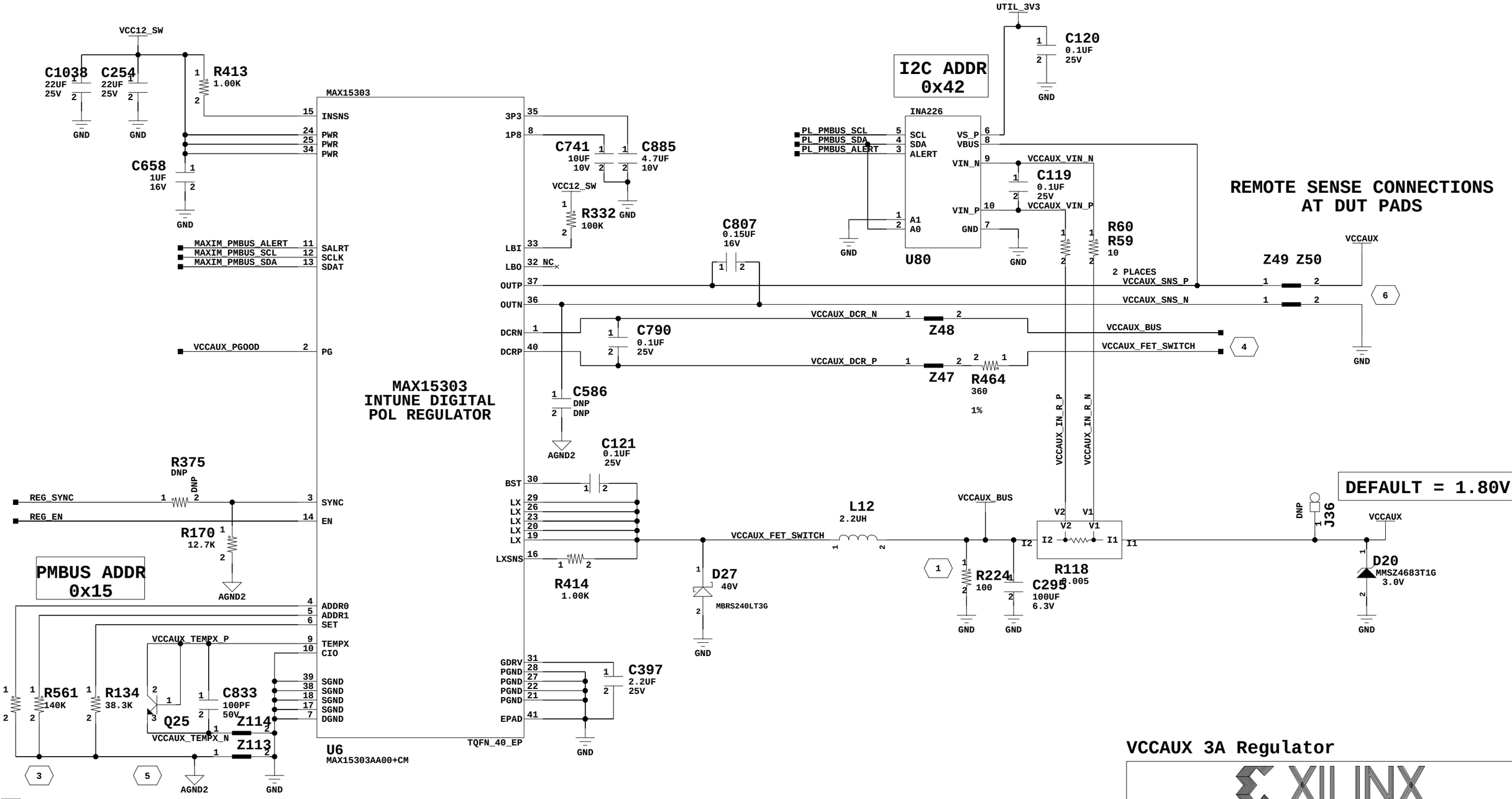
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCBRAM 6A Regulator

XILINX

TITLE: VCCBRAM 6A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 61 OF 87	DRAWN BY: BF



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

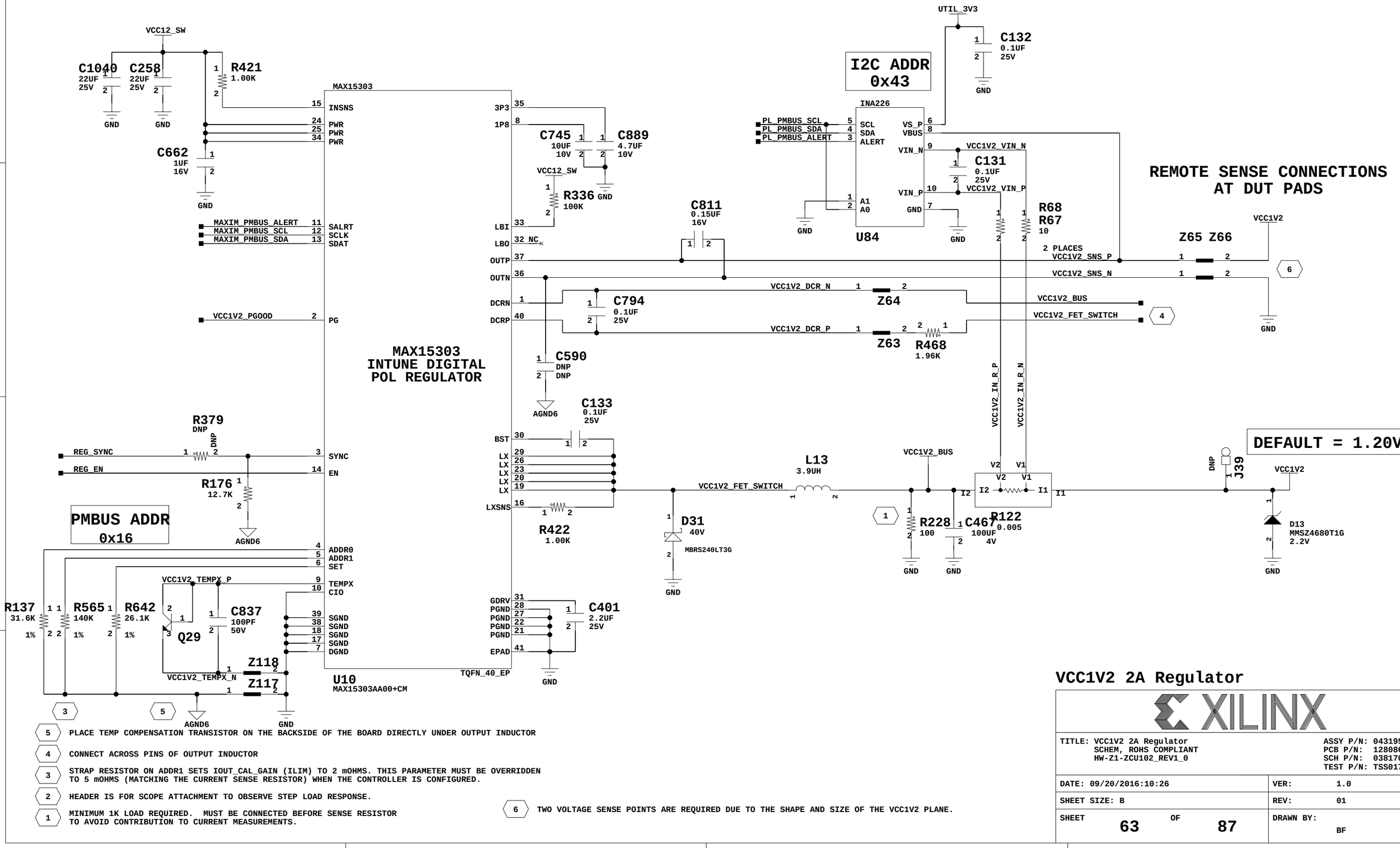
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCAUX PLANE.

VCCAUX 3A Regulator

XILINX

TITLE: VCCAUX 3A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 62 OF 87	DRAWN BY: BF



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

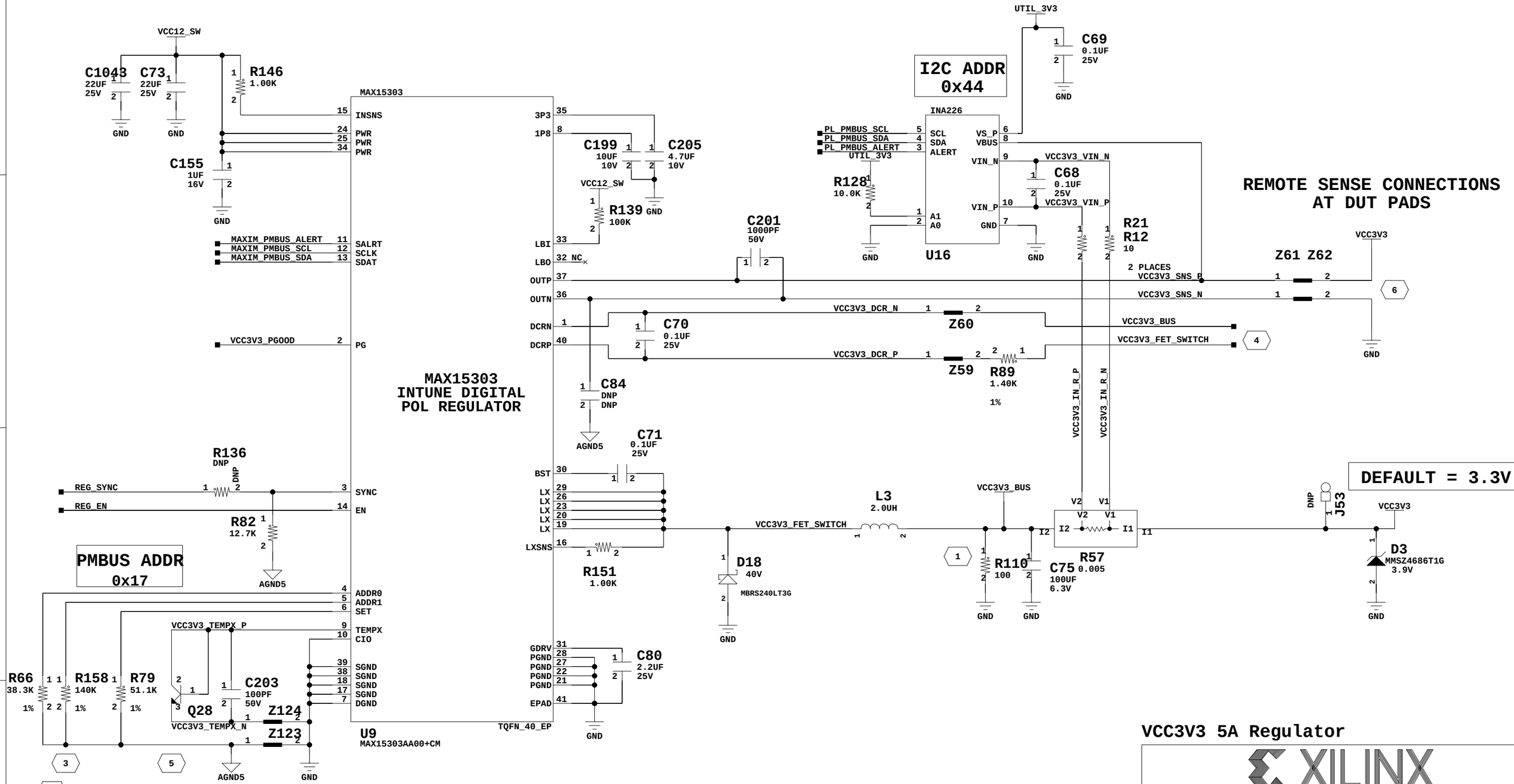
4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC1V2 PLANE.



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

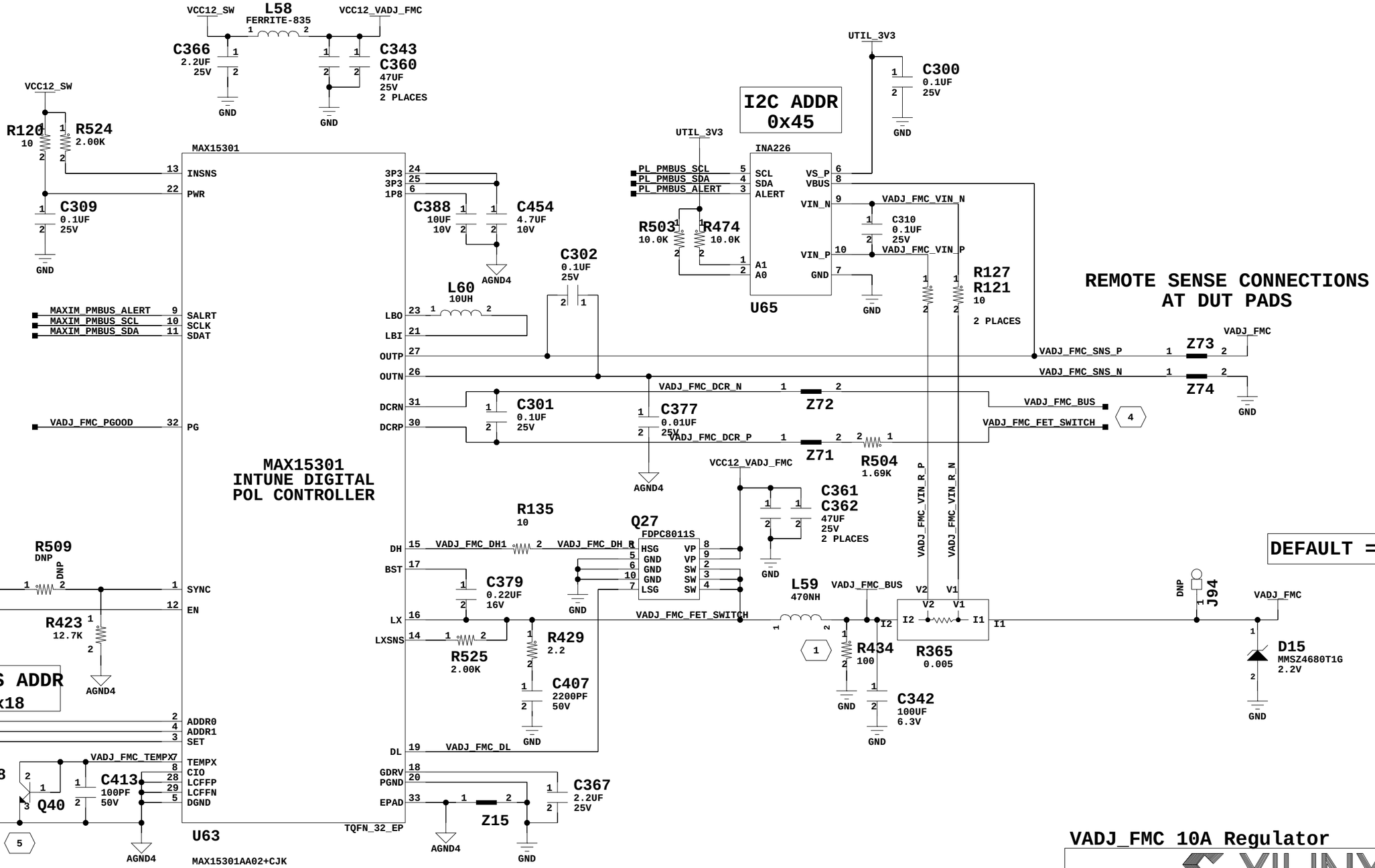
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC3V3 PLANE.

VCC3V3 5A Regulator

XILINX

TITLE: VCC3V3 5A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 64 OF 87	DRAWN BY: BF



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L3

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

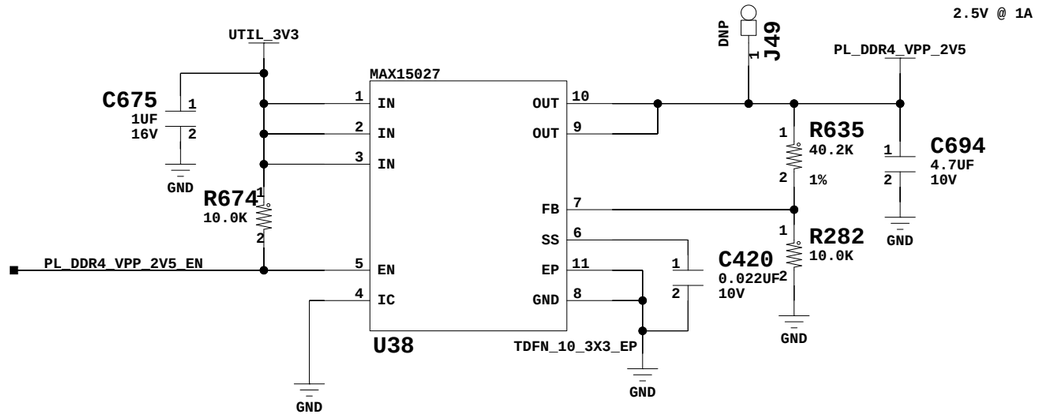
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VADJ_FMC 10A Regulator

XILINX

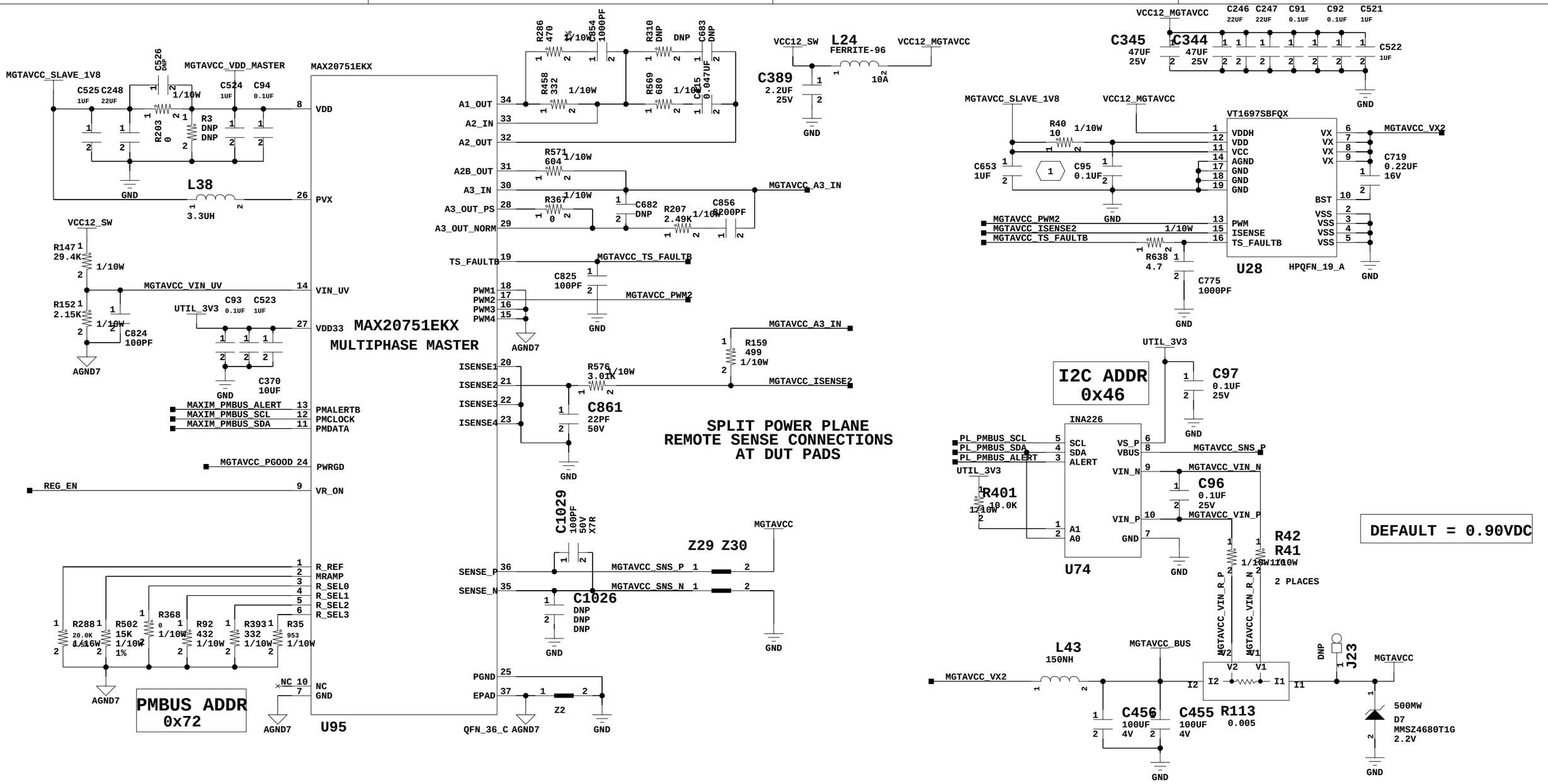
TITLE: VADJ_FMC 10A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 65 OF 87	DRAWN BY: BF



PL_DDR4_VPP_2V5 1A Regulator

XILINX

TITLE: PL_DDR4_VPP_2V5 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 66 OF 87	DRAWN BY: BF



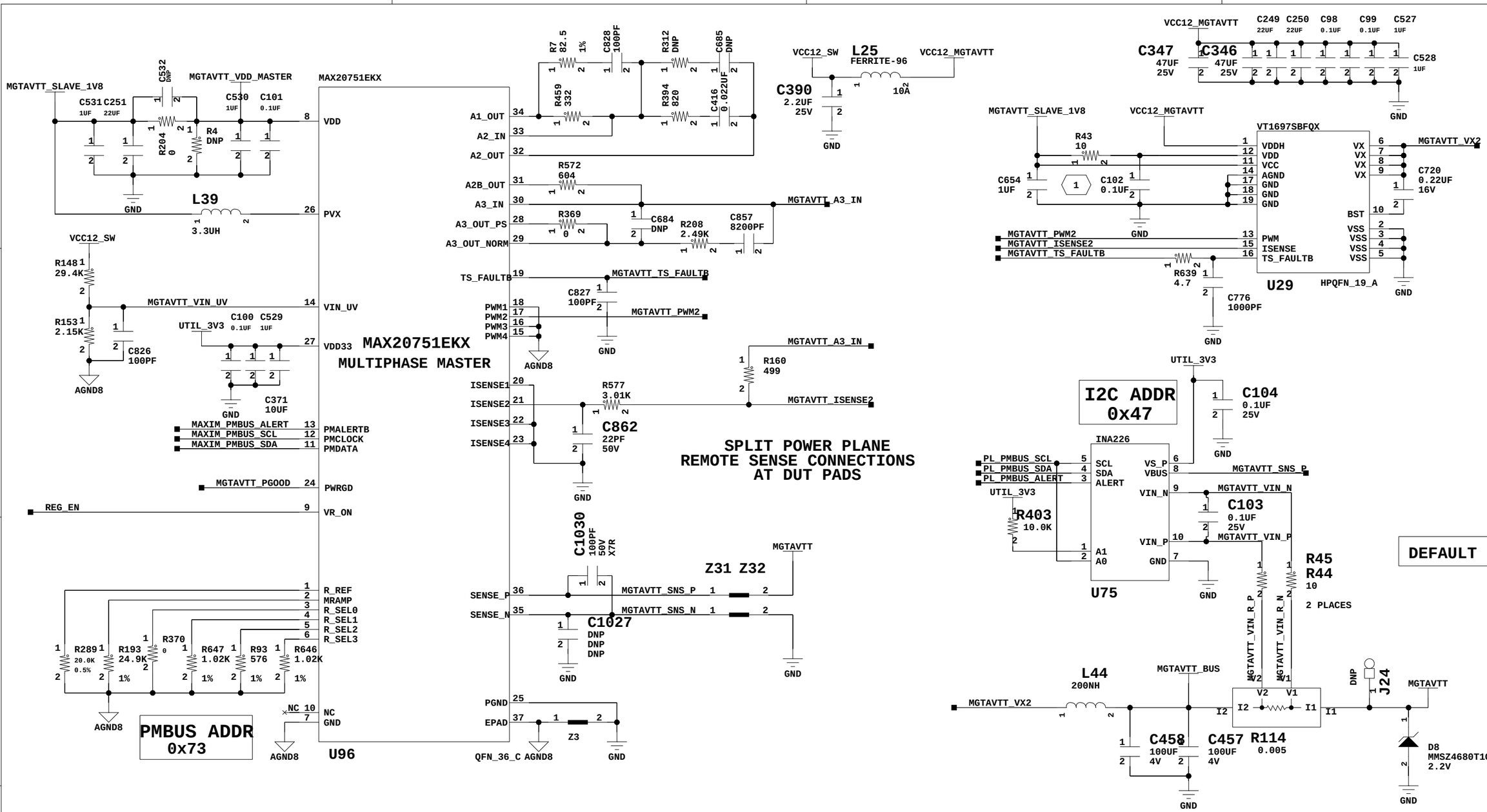
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVCC 6A Regulator

XILINX

TITLE: MGTAVCC 6A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 67 OF 87	DRAWN BY: BF



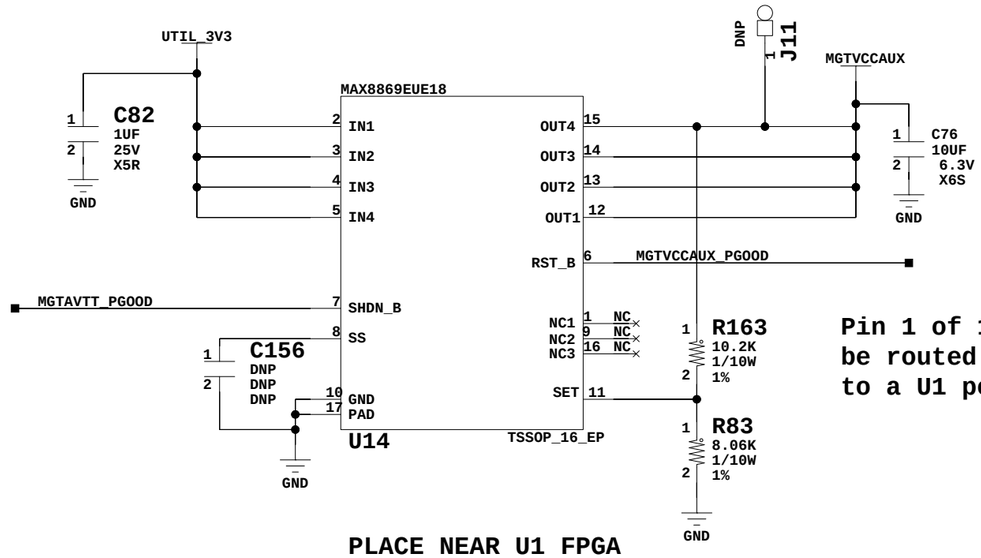
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVTT 6A Regulator

XILINX

TITLE: MGTAVTT 6A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 68 OF 87	DRAWN BY: BF



Pin 1 of 10.2K resistor must be routed as a sense line directly to a U1 power pin

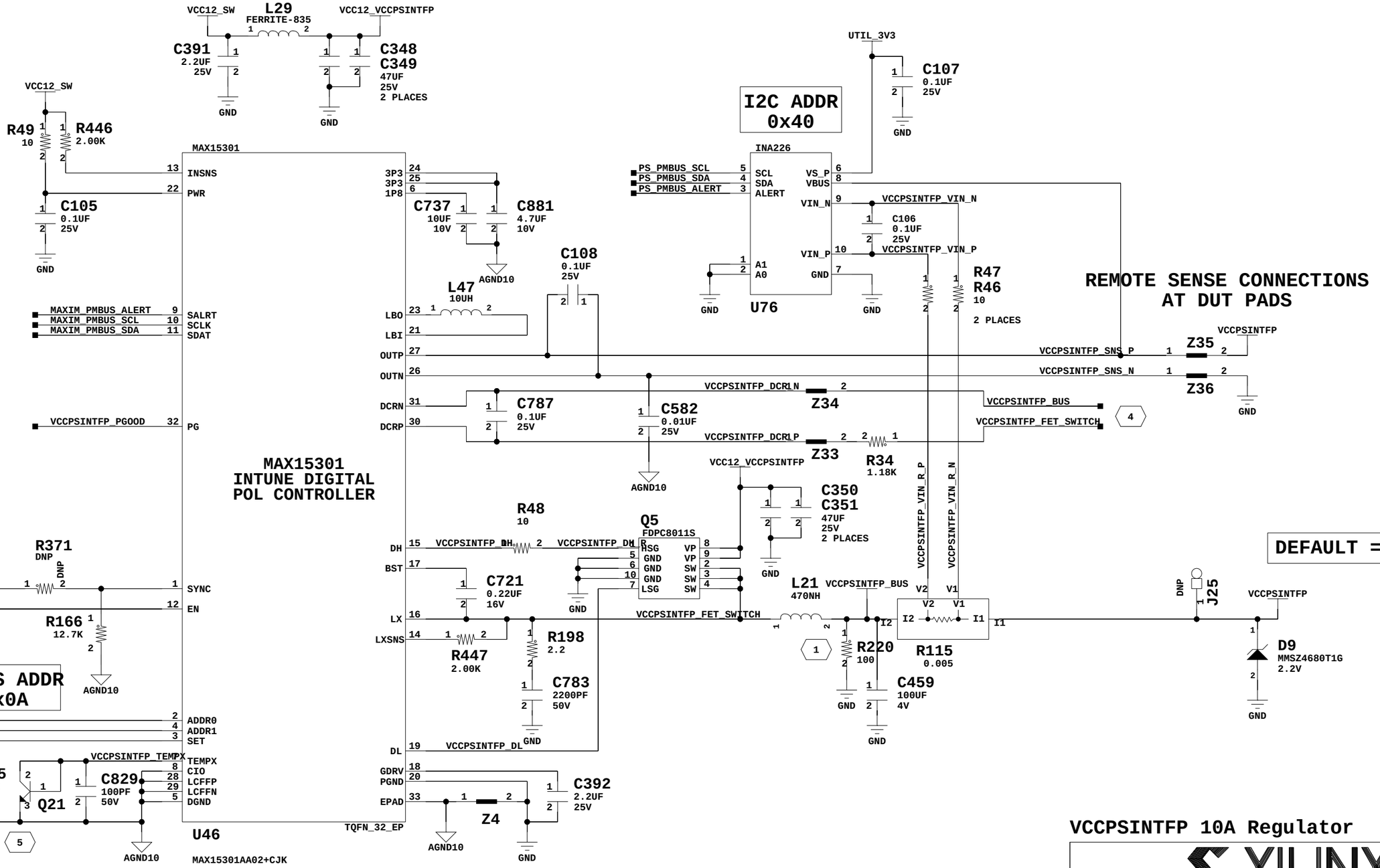
PLACE NEAR U1 FPGA

DEFAULT = 1.81VDC

MGTVCCAUX 1A Regulator

XILINX

TITLE: MGTVCCAUX 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 69 OF 87	DRAWN BY: BF

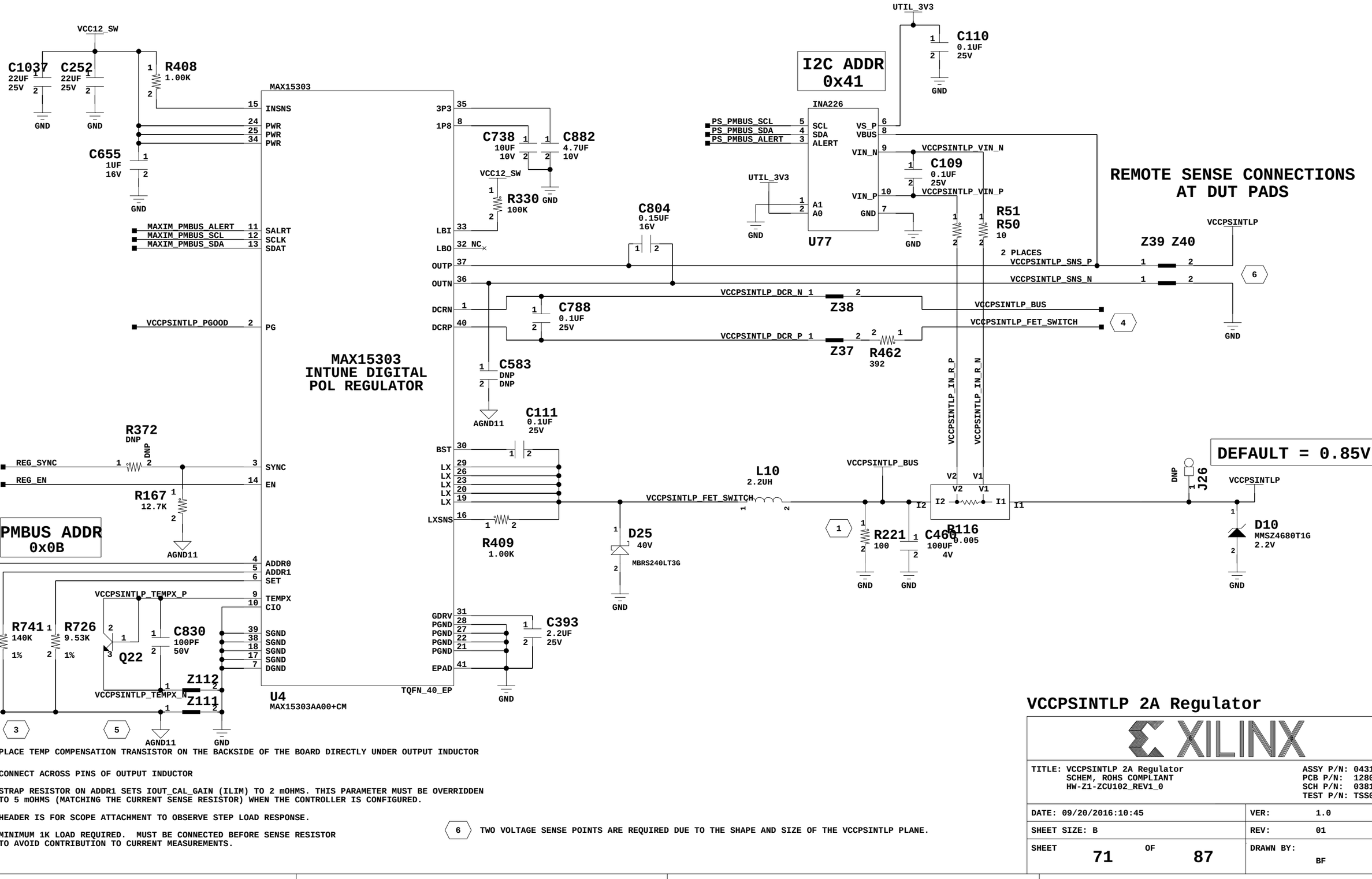


5. PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L3
4. CONNECT ACROSS PINS OF INDUCTOR L3
3. STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
2. HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
1. MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCPSINTFP 10A Regulator

XILINX

TITLE: VCCPSINTFP 10A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431087 PCB P/N: 1280219 SCH P/N: 0381582 TEST P/N: TSS0166
DATE: 09/20/2016:10:26	VER: A.0
SHEET SIZE: B	REV: 01
SHEET 70 OF 87	DRAWN BY: BN



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

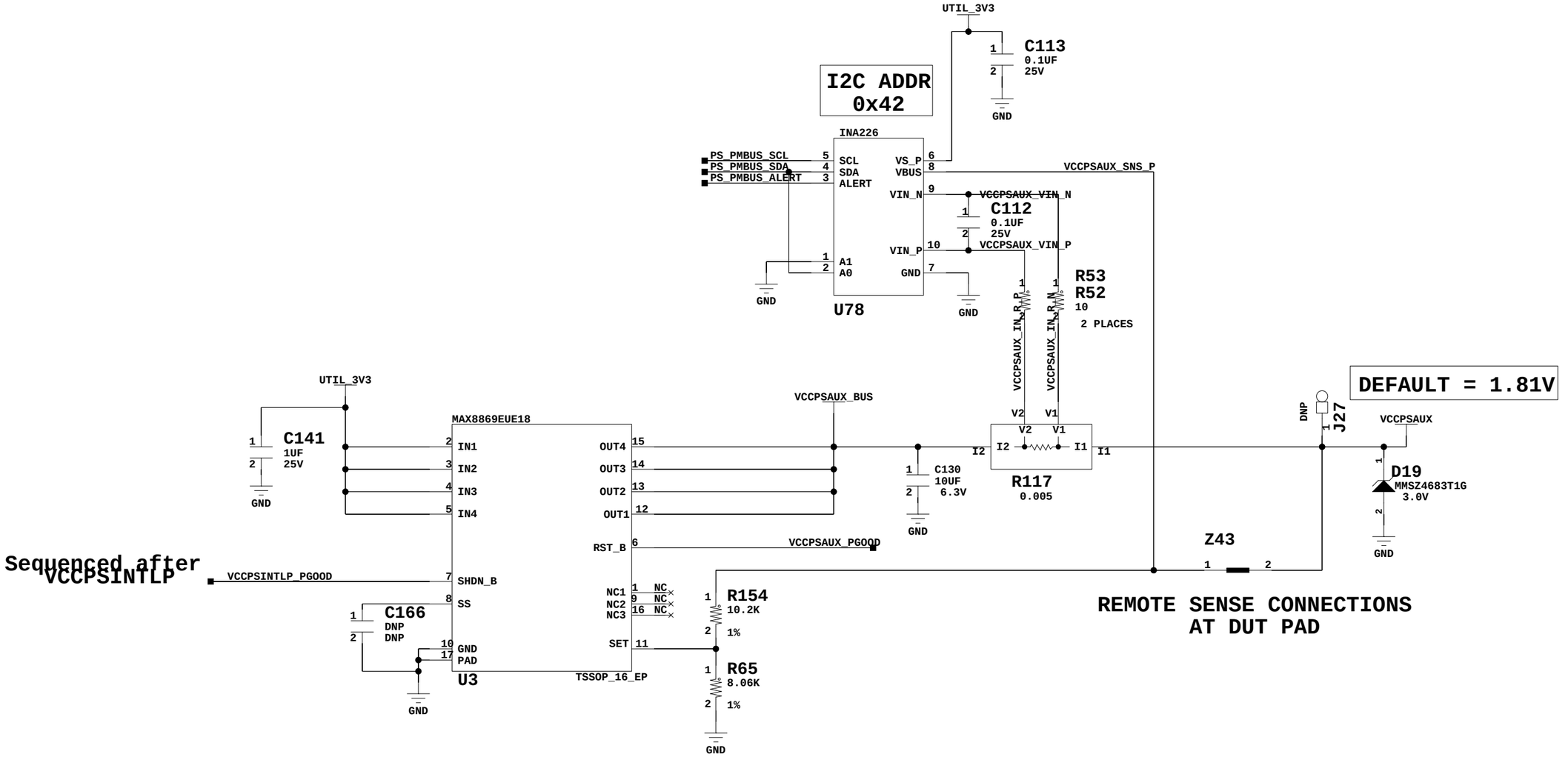
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCPSINTLP PLANE.

VCCPSINTLP 2A Regulator

XILINX

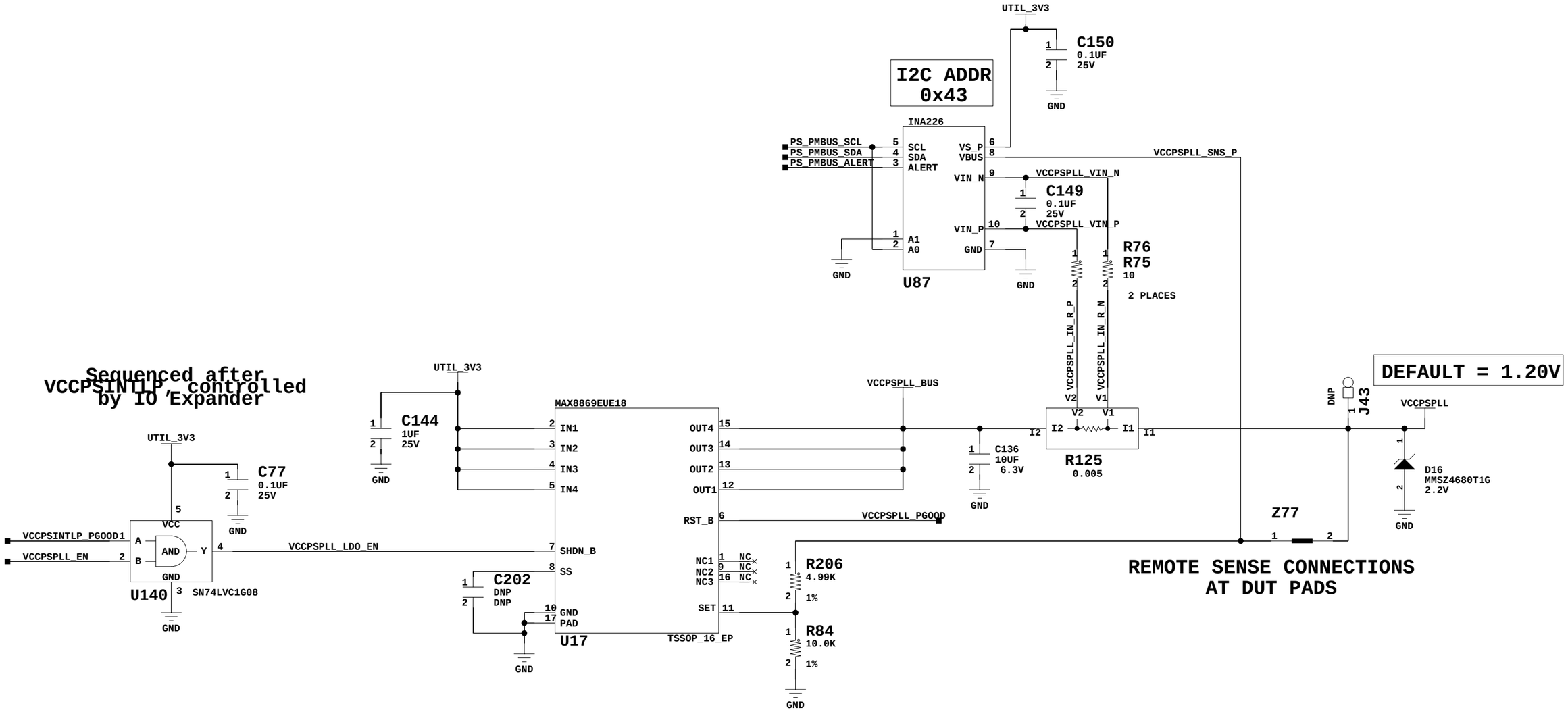
TITLE: VCCPSINTLP 2A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 71 OF 87	DRAWN BY: BF



VCCPSAUX 500MA Regulator

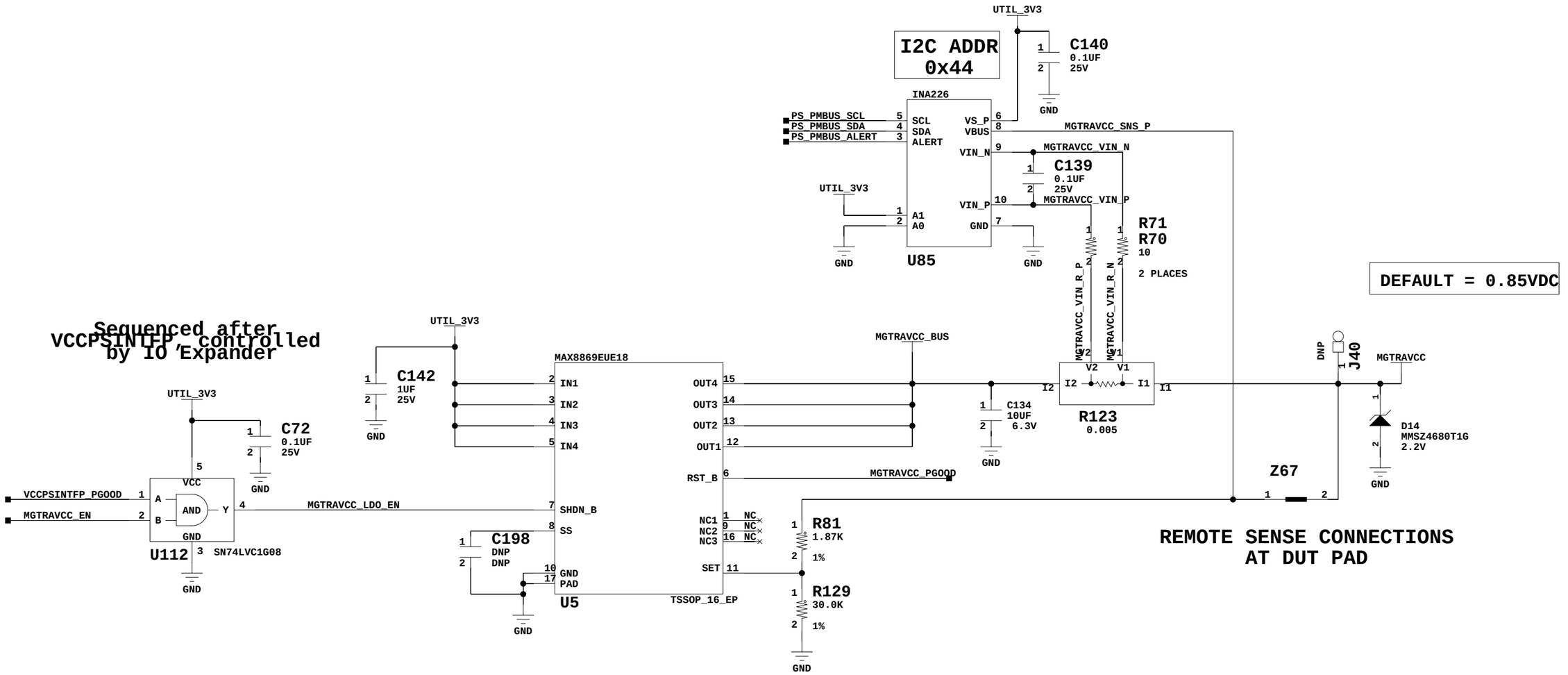
XILINX

TITLE: VCCPSAUX 500MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 72 OF 87	DRAWN BY: BF



VCCPSPLL 200MA Regulator

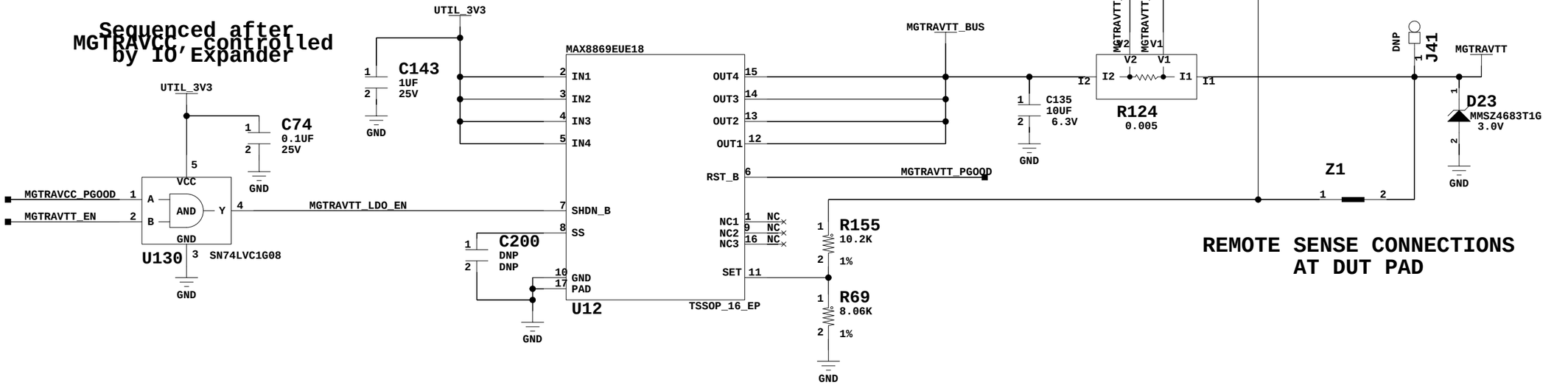
TITLE: VCCPSPLL 200MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 73 OF 87	DRAWN BY: BF



MGTRAVCC 400MA Regulator

XILINX

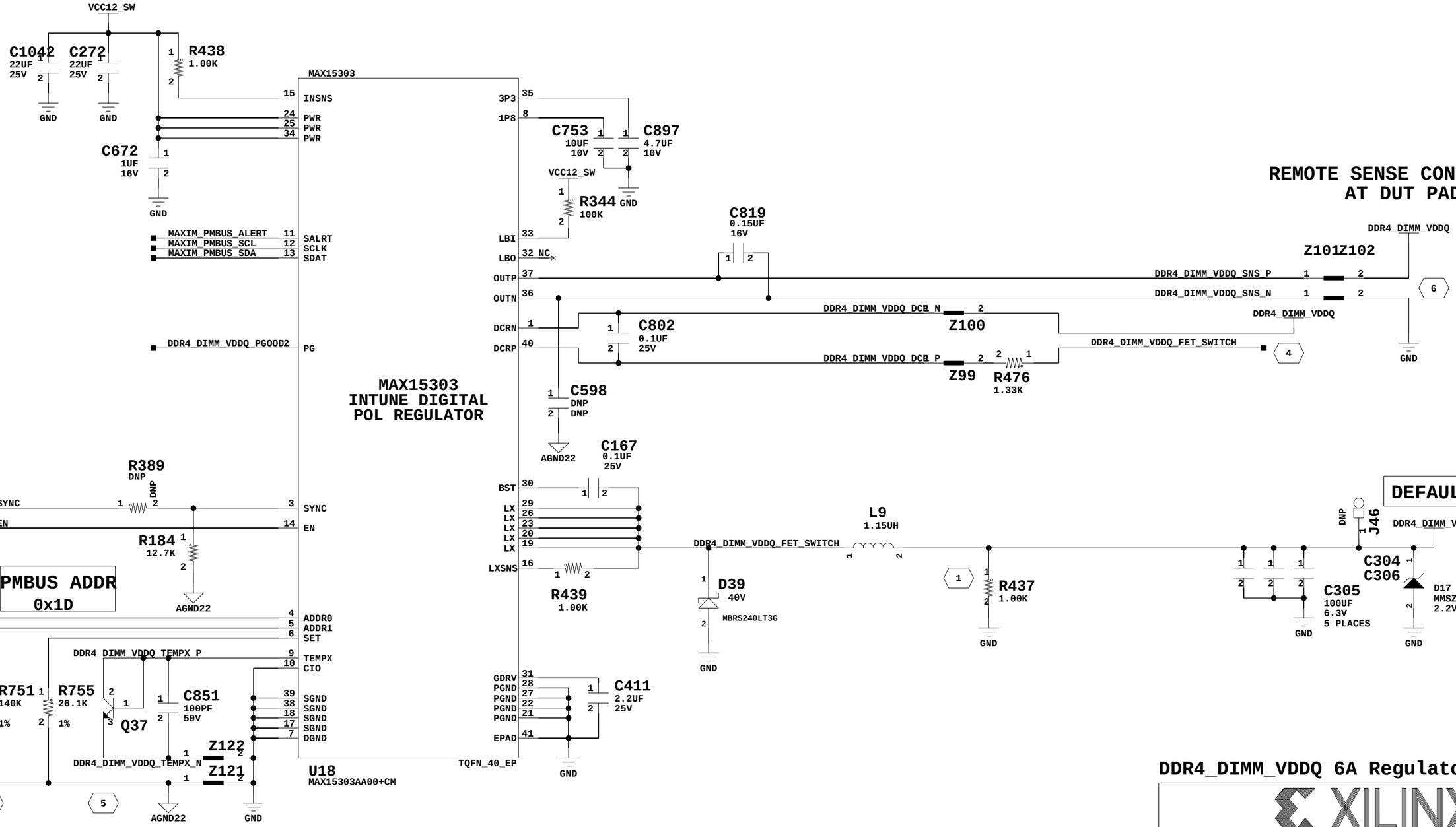
TITLE: MGTRAVCC 400MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 74 OF 87	DRAWN BY: BF



MGTRAVTT 100MA Regulator

XILINX

TITLE: MGTRAVTT 100MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 75 OF 87	DRAWN BY: BF



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

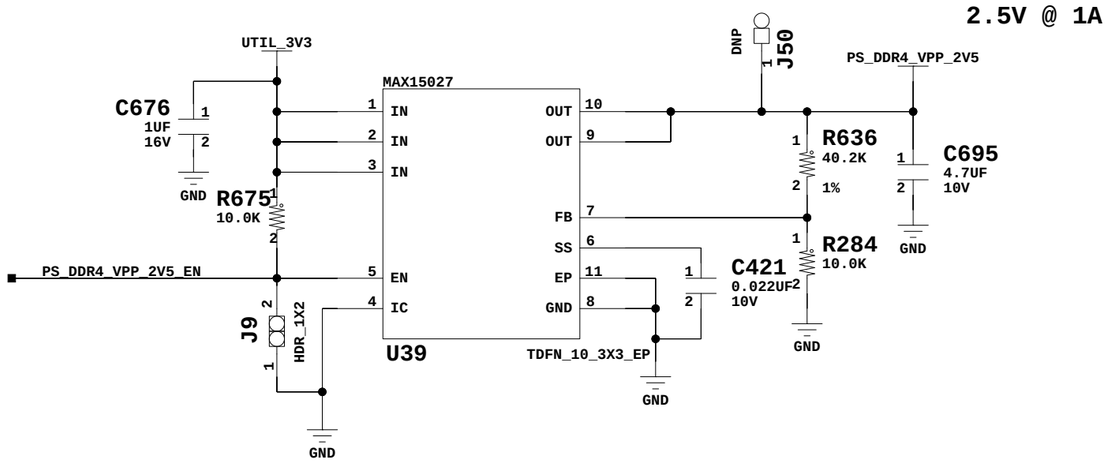
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE DDR4_DIMM_VDDQ PLANE.

DDR4_DIMM_VDDQ 6A Regulator

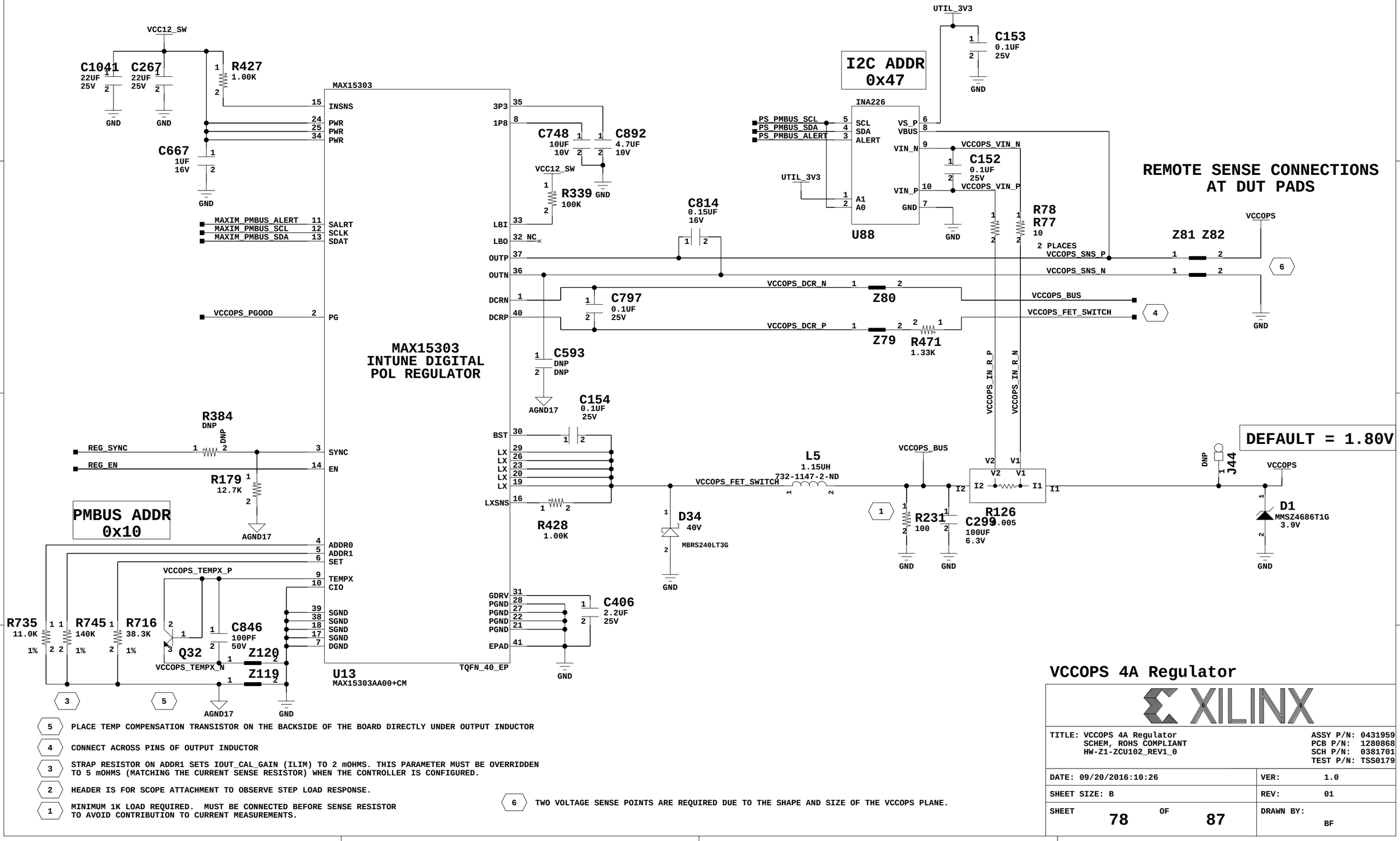
XILINX

TITLE: DDR4_DIMM_VDDQ 6A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 76 OF 87	DRAWN BY: BF



PS_DDR4_VPP_2V5 1A Regulator

TITLE: PS_DDR4_VPP_2V5 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 77 OF 87	DRAWN BY: BF



MAX15303
INTUNE DIGITAL
POL REGULATOR

5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

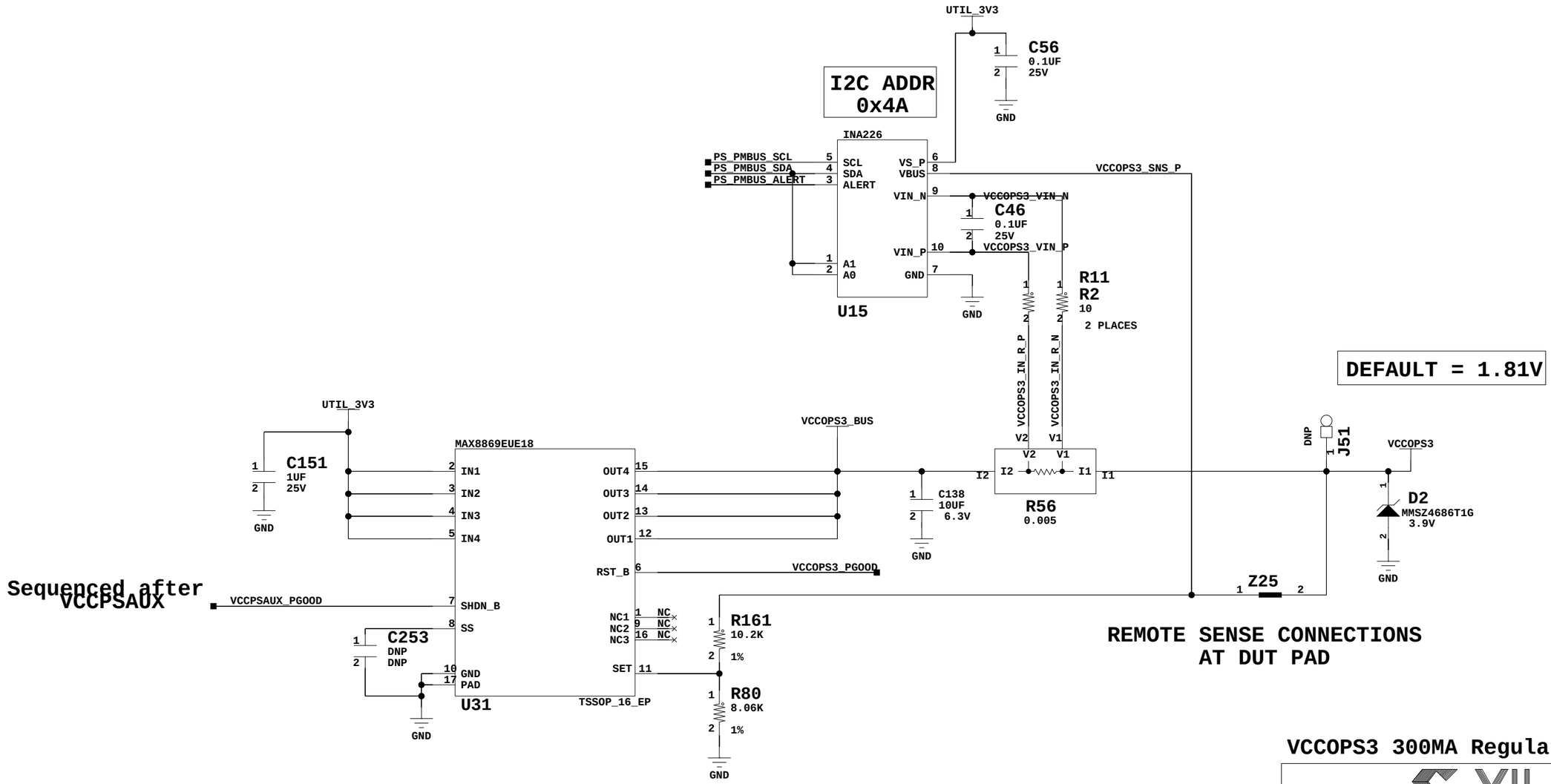
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCOPS PLANE.

VCCOPS 4A Regulator

XILINX

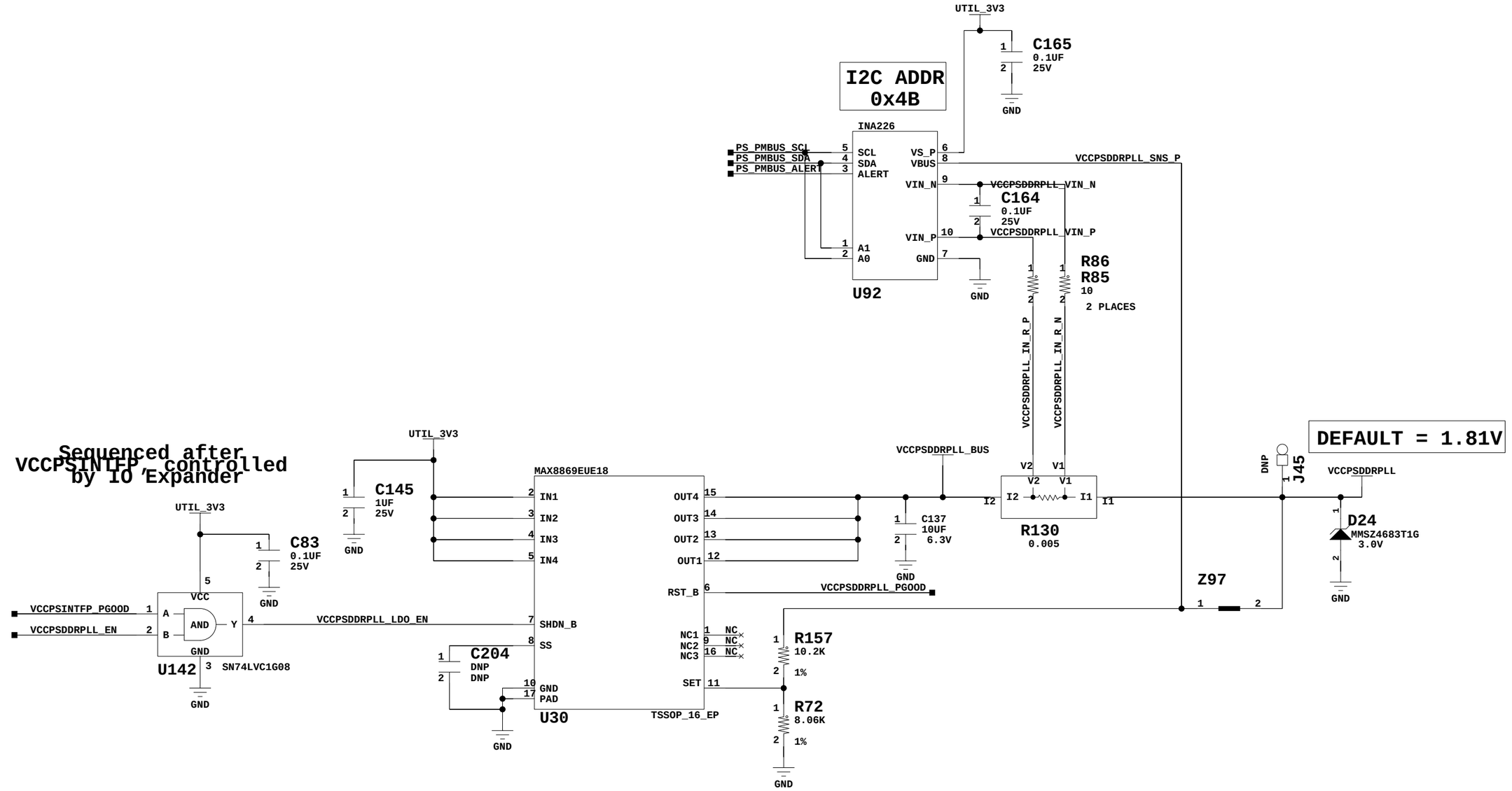
TITLE: VCCOPS 4A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 78 OF 87	DRAWN BY: BF



VCCOPS3 300MA Regulator

XILINX

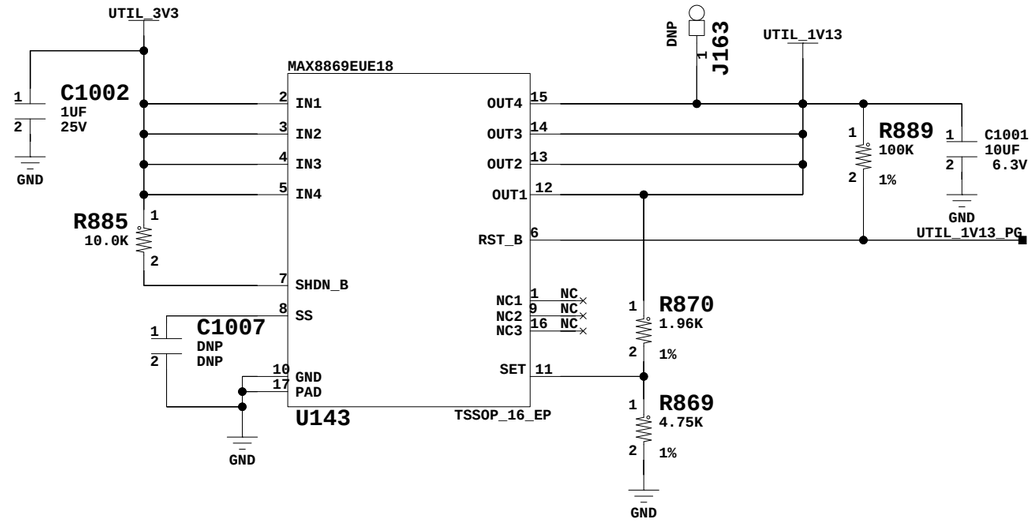
TITLE: VCCOPS3 300MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 79 OF 87	DRAWN BY: BF



VCCPSDDRPLL 100MA Regulator

TITLE: VCCPSDDRPLL 100MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 80 OF 87	DRAWN BY: BF

1.13V @ 1A

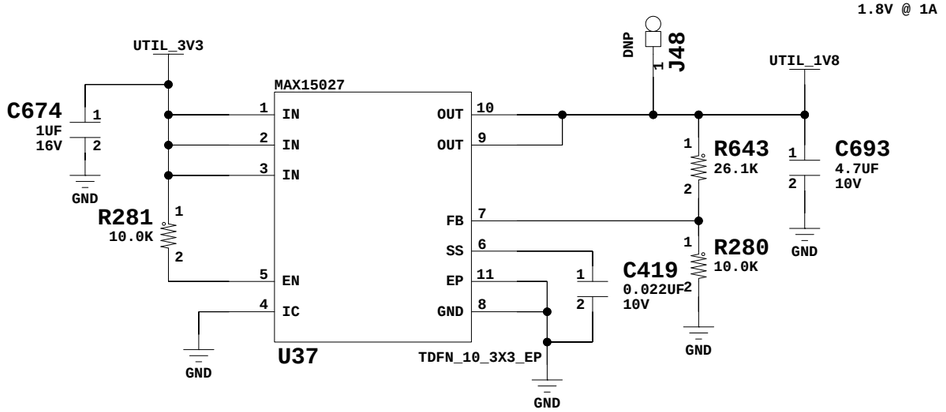


1.13V @ 1A satisfies voltage and total current requirements for TI ENET PHY, as well as HDMI TX and RX transcievers

UTIL_1V13 1A Regulator

XILINX

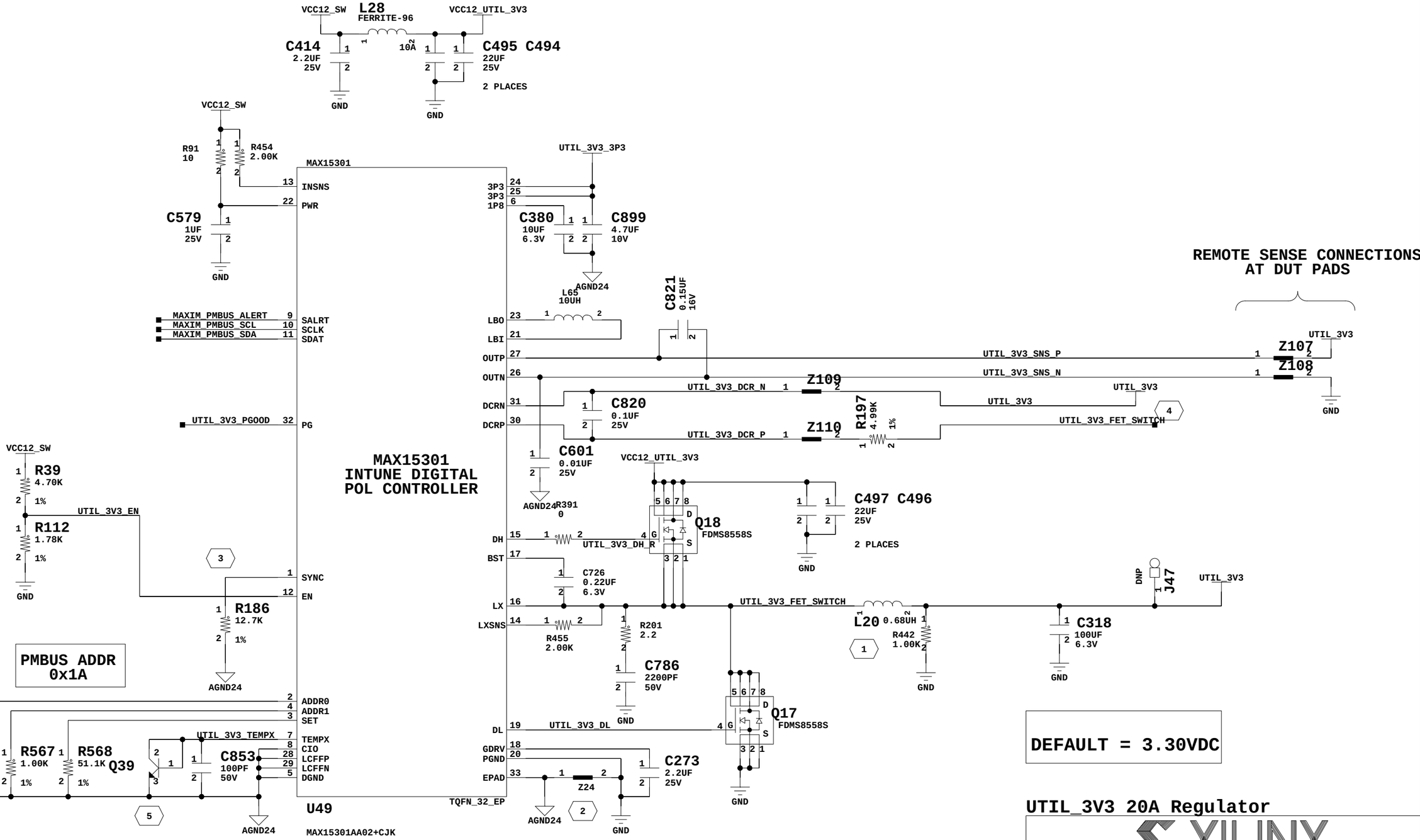
TITLE: UTIL_1V13 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 81 OF 87	DRAWN BY: BF



UTIL_1V8 1A Regulator

XILINX

TITLE: UTIL_1V8 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 82 OF 87	DRAWN BY: BF



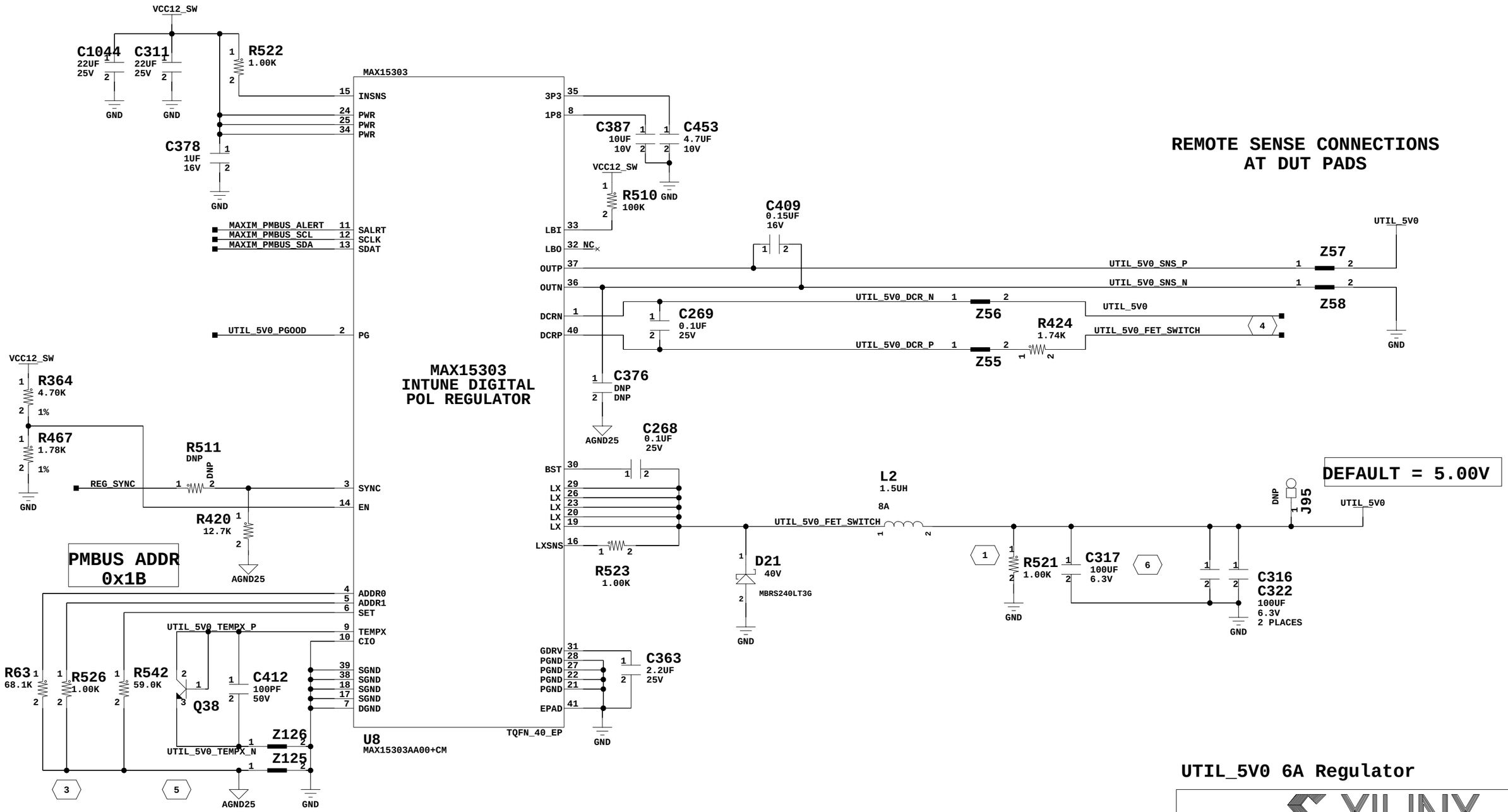
3 UTIL_3V3 RAIL SWITCHING FREQUENCY IS 400kHz AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 600 kHZ.

2 CONNECT AGND TO GND AT OUTPUT CAPACITORS

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

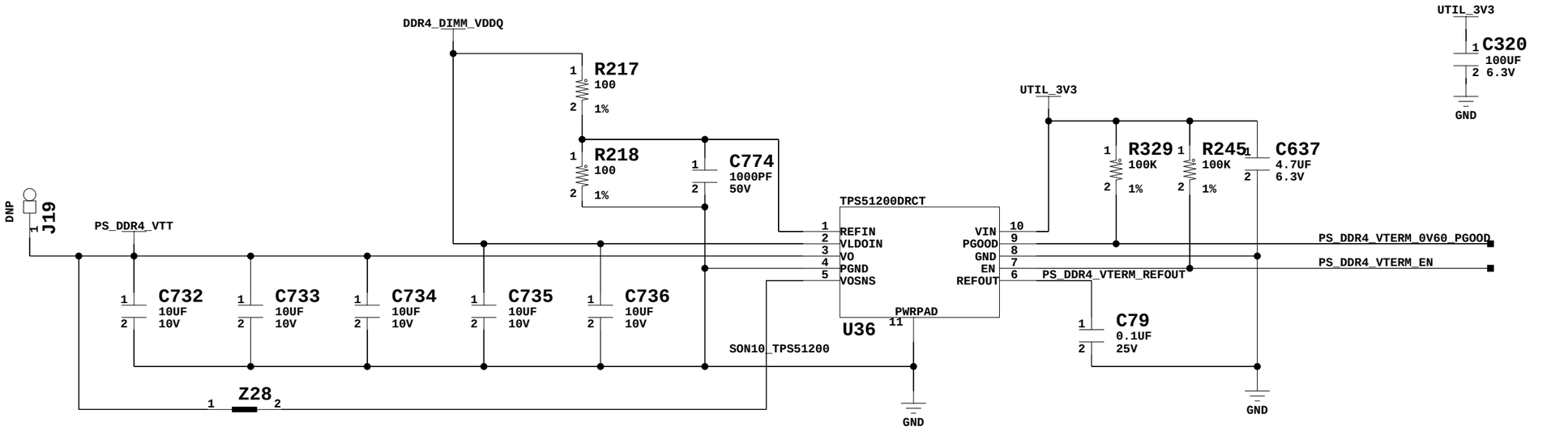
6 PLACE ONE 100uF CLOSE TO THE INDUCTOR, THE REST 100uF SHOULD BE PLACED CLOSE TO THE HEAVY LOAD SIDE

UTIL_5V0 6A Regulator

XILINX

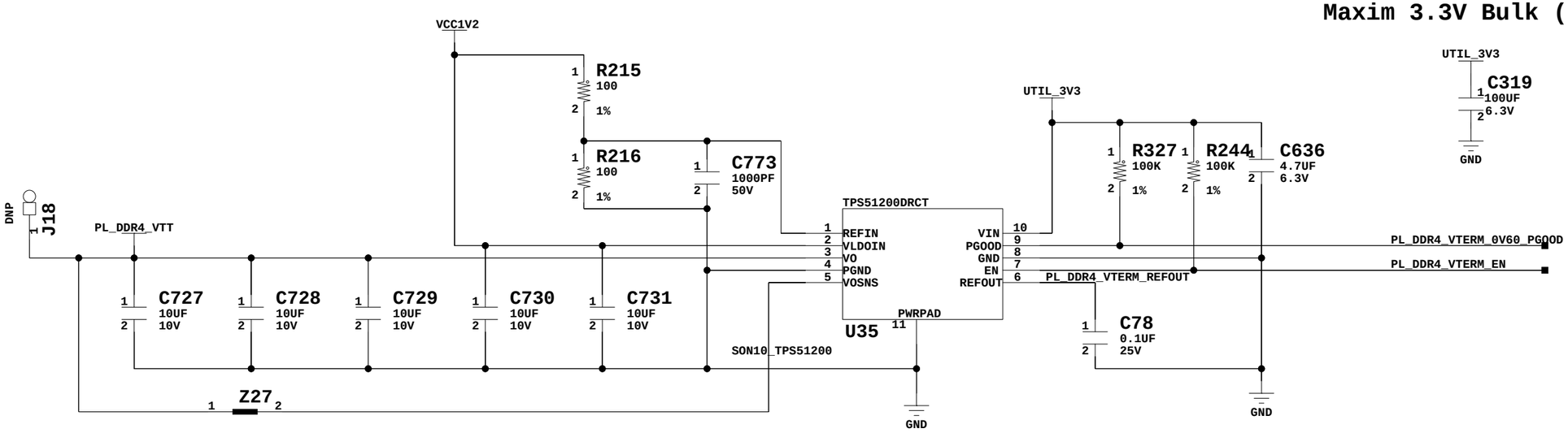
TITLE: UTIL_5V0 6A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:27	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 84 OF 87	DRAWN BY: BF

Maxim 3.3V Bulk (near PS VTT)



Place sense near DDR4 DIMM

Maxim 3.3V Bulk (near PL VTT)

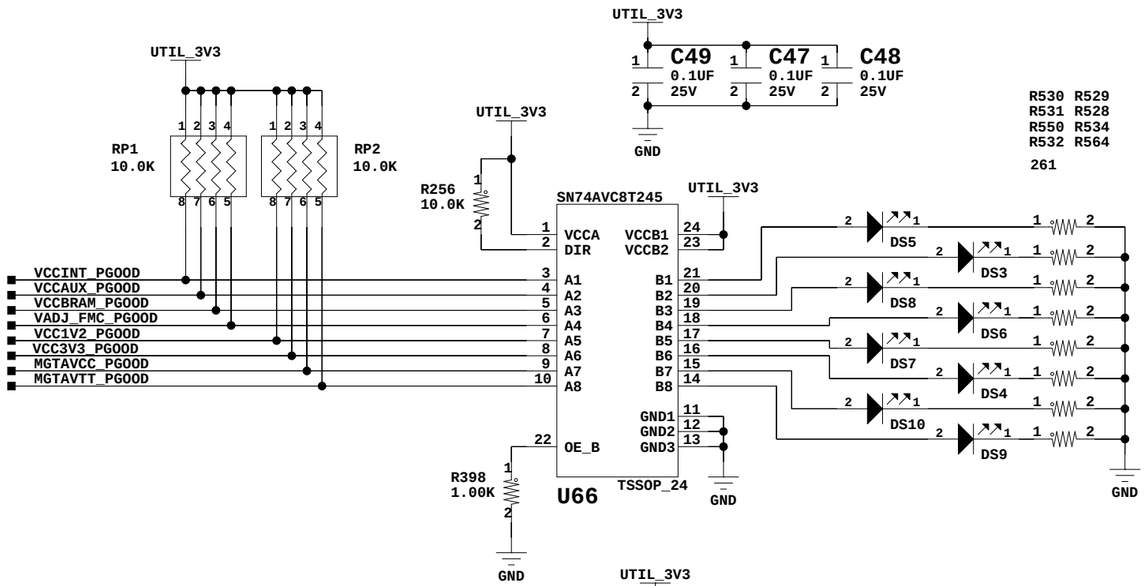


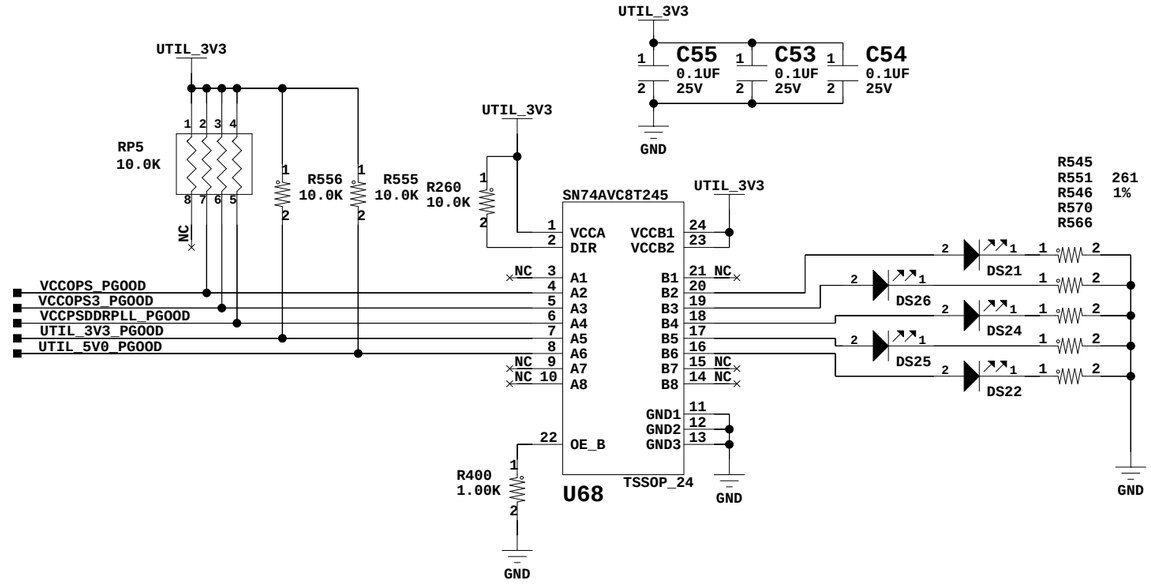
Place sense near DDR4 components

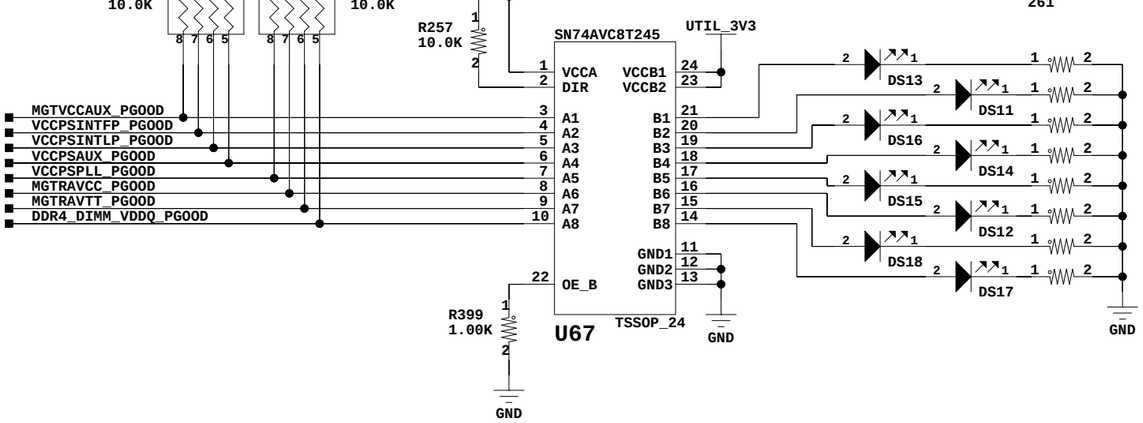
DDR4 Termination Supply

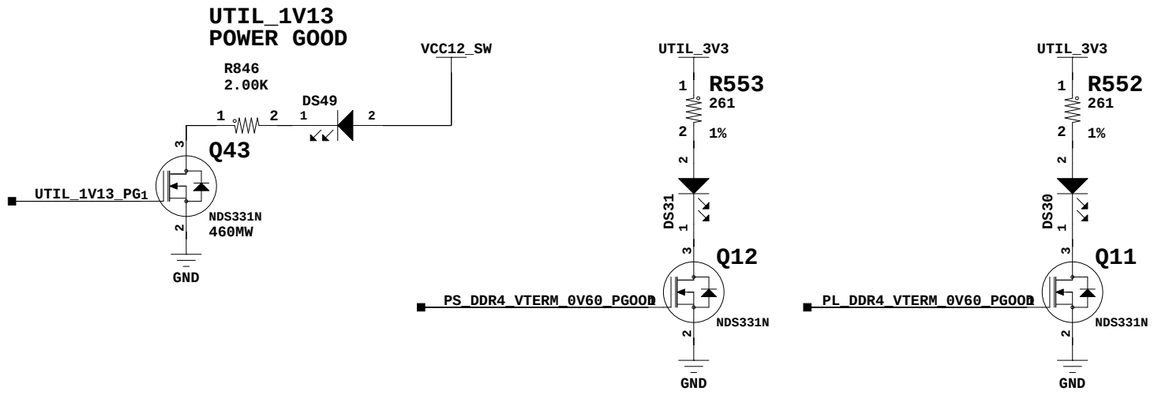
XILINX

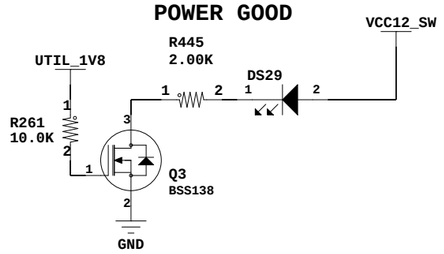
TITLE: DDR4 Termination Supply SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:45	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 85 OF 87	DRAWN BY: BF

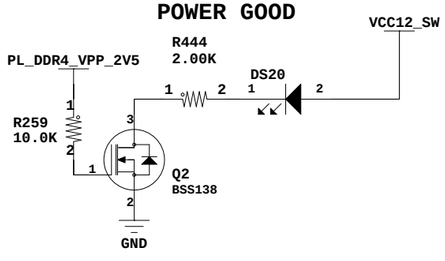


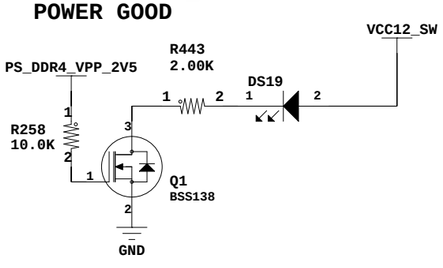








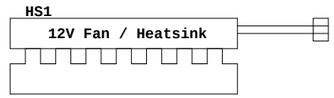




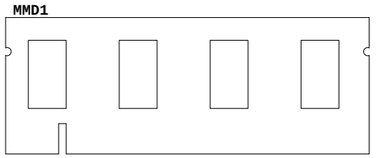
Power Status LEDs

XILINX

TITLE: Power Status LEDs SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 86 OF 87	DRAWN BY: BF



12VDC



DDR4_SODIMM

CBL1

PC_POWER_CABLE

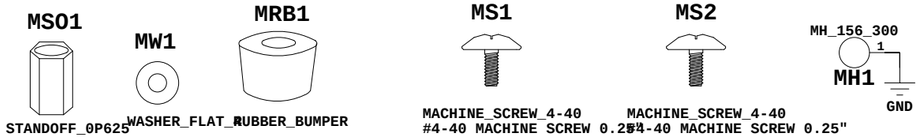
Power Cord

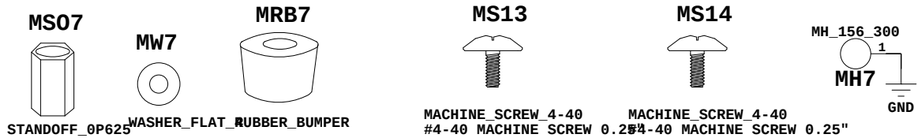
PWR_BRICK_12V

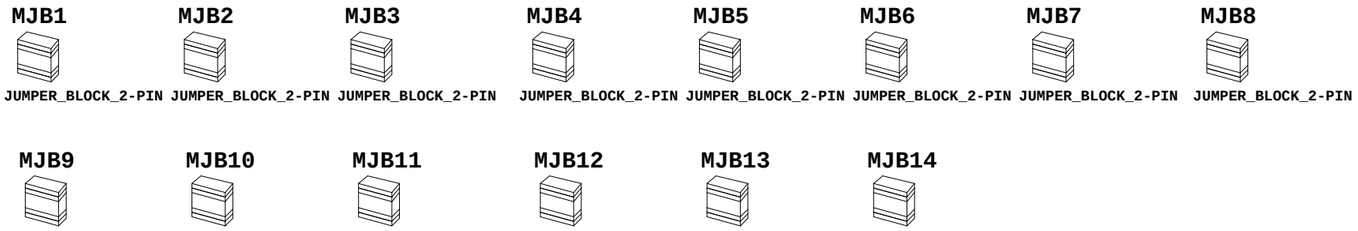
CBL2

USB Micro-B Cable

USB_MICRO_CABLE







Mechanical Components

TITLE: Mechanical Components SCHEM, ROHS COMPLIANT HW-Z1-ZCU102_REV1_0	ASSY P/N: 0431959 PCB P/N: 1280868 SCH P/N: 0381701 TEST P/N: TSS0179
DATE: 09/20/2016:10:26	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 87 OF 87	DRAWN BY: BF