RVC Manual

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# Revision History

| Date | Change |
|---|---|
| June 3, 2019 | Pre-release |

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# 1  Overview

TBD

# 2  Tools

The RVC project uses a design and verification flow based on open source EDA tools. Table 2-1 summarizes the tools, used forthis project.

Table 2-1: Tool Summary

| Tool | Version | Usage |
|---|---|---|
| Verrilator[2] | 3.874 | Linting |
| Icarus Verilog[4] | 0.9.7 | Linting |
| Yosys[6] | 0.7+627 | Linting, Formal Verification |
| SymbiYosys[5] | Sep. 12, 2018 | Formal Verification |
| GTKWave[1] | 3.3.95 | Waveform Viewer |
| Verilog-Perl[3] | 3.418-1 | Gerneration of design data for GTKWave[1] |

# 3 References

[1] BSI. Gtkwave. http://gtkwave.sourceforge.net.

[2] Wilson Snyder. Verilator. http://www.veripool.org/verilator.

[3] Wilson Snyder. Verilog-perl. http://www.veripool.org/verilog-perl.

[4] Stephen Williams. Icarus verilog. http://iverilog.icarus.com.

[5] Clifford Wolf. Symbiyosys. https://github.com/cliffordwolf/SymbiYosys.

[6] Clifford Wolf. Yosys open synthesis suite. http://www.clifford.at/yosys.