DIGITAL DESIGN

LAB13 REGISTER(MEMORY), COUNTER, DON'TS IN VERILOG CODE OF CIRCUIT

2022 FALL TERM @ CSE . SUSTECH

LAB13

- Register
  - Register
  - Shift register
  - Register and Memory in Verilog
- Counter
  - Ring counter
  - Johnson-counter
- DON’Ts in Verilog code of Circuit
- Practice

How to implement 1s

REGISTER(1)

one ff can only store 1 bit information

- In digital electronics, especially computing, **hardware registers** are circuits typically composed of **flip flops**, often with many characteristics similar to memory, such as: The ability to **read** or **write** multiple bits at a time, and using an address to select a particular register in a manner similar to a memory address.

- Hardware registers are used in the interface between software and peripherals. Software writes them to send information to the device, and reads them to get information from the device. Some hardware devices also include registers that are not visible to software, for their internal use.

REGISTER(2)

Read: register on the right

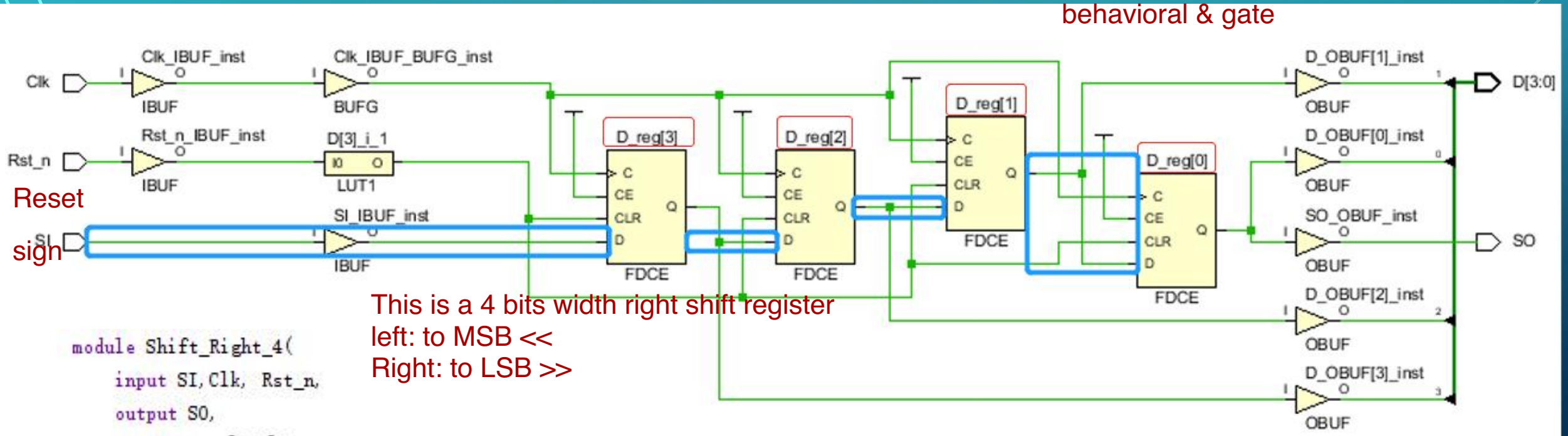
- In its broadest definition, a register consists of a group of flip-flops together with gates that affect their operation. The flip-flops **hold the binary information**, and the gates determine how the information is transferred into the register.

- A register capable of **shifting the binary information held in each cell to its neighboring cell, in a selected direction**, is called a ***shift register***.

SHIFT REGISTER(1) - SHIFT RIGHT(1)

Implement can use 2 way:

behavioral & gate



This is a 4 bits width right shift register

left: to MSB <<

Right: to LSB >>

```
module Shift_Right_4(
    input SI,Clk, Rst_n,
    output SO,
    output reg[3:0] D
    );
    assign SO = D[0];
    always @(posedge Clk, negedge Rst_n)
        if (!Rst_n)
            D<=4'b0000;
        else
            D <= {SI, D[3:1]};
endmodule
```

The data shift from MSB to LSB (shift right)

SI -> D[3], D[3] ->D[2], D[2]->D[1], D[1]->D[0]

D[0] will be removed

The circuit is different from >>, as >> will let D[3]=0,

but this circuit will assign the new input into D[3]

SHIFT REGISTER(1) - SHIFT RIGHT(2)

serial/parallel :

to enlarge the length of parallel output,

2 way: make D longer, use more shift right at one time.

feature: The register can read input while do right shift

```
module Shift_Right_4(
    input SI,Clk, Rst_n,
    output SO,
    output reg[3:0] D
    );
    assign SO = D[0];
    always @(posedge Clk, negedge Rst_n)
        if (!Rst_n)
            D<=4'b0000;
        else
            D <= {SI, D[3:1]};
endmodule
```

input

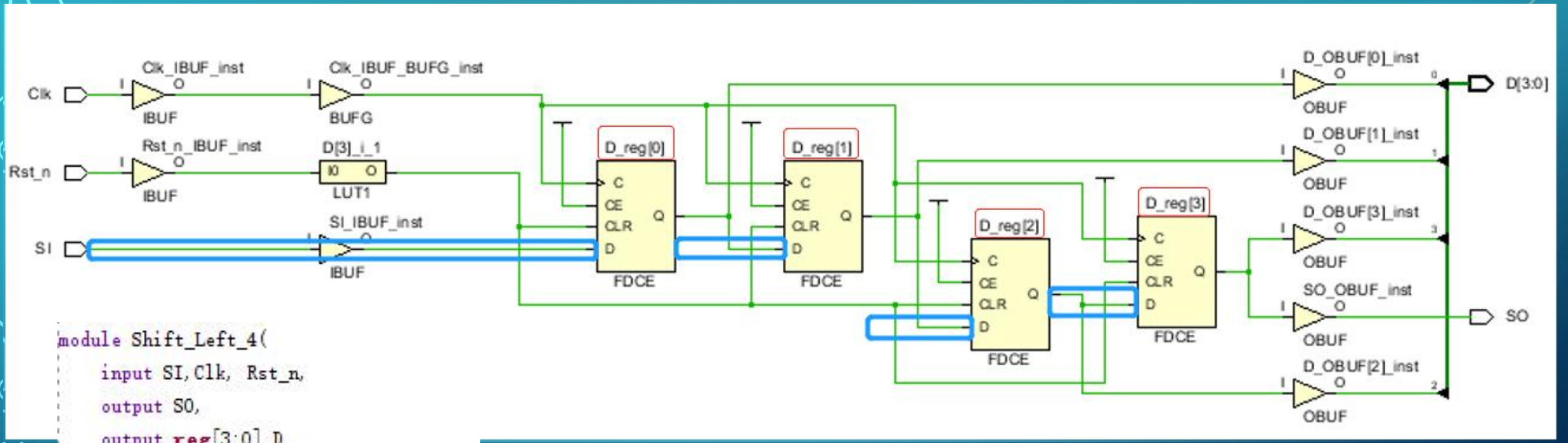
In register, we can do a postponed process:
the input of previous time will be stored on more significant bits

when t=0 reset

when t=5 ns, read the input , right shift, assign MSB

the operation done at t=5 ns will maintained until next positive edge.

SHIFT REGISTER(2) - SHIFT LEFT(1)



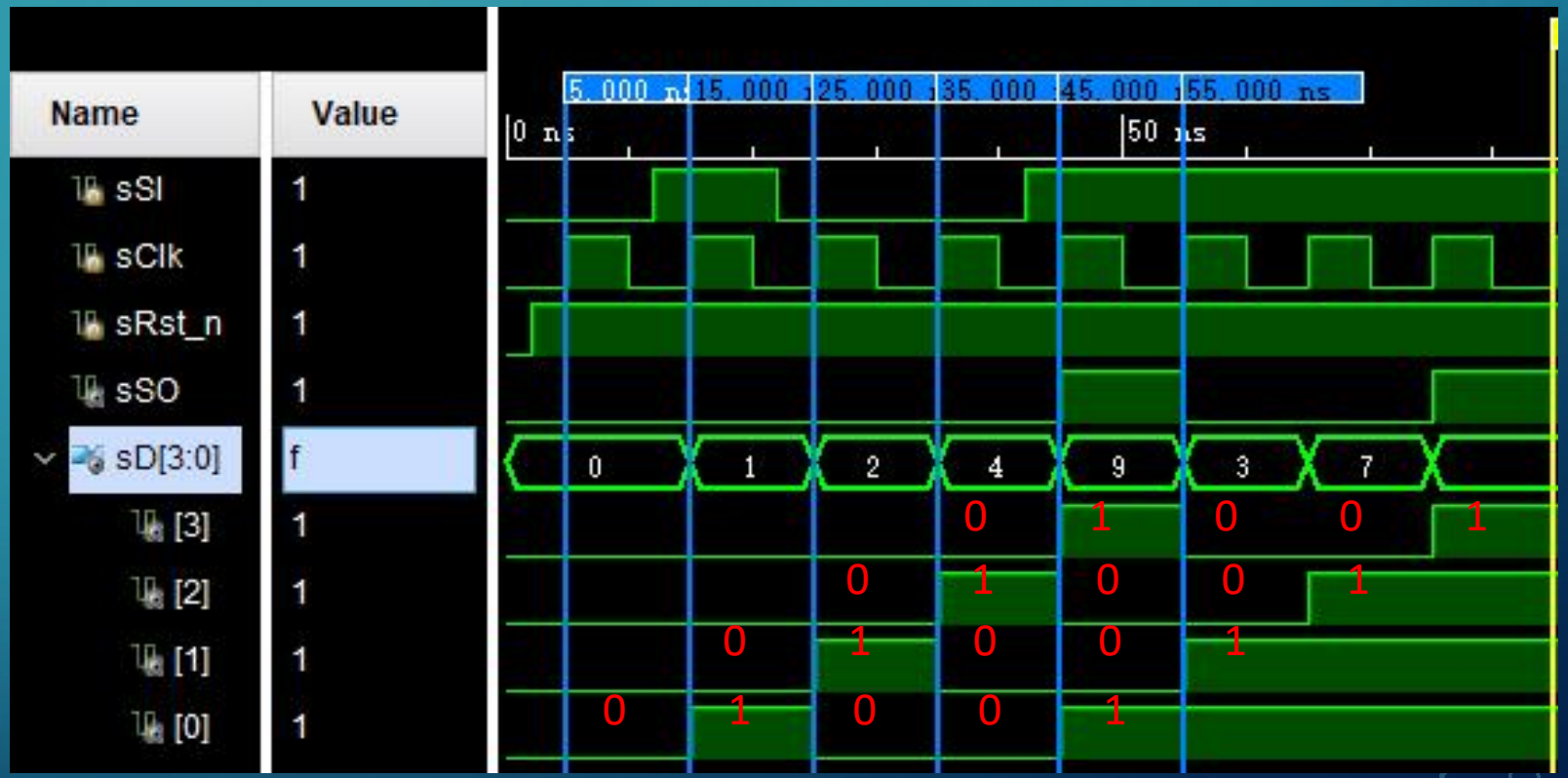

```
module Shift_Left_4(
    input SI,Clk, Rst_n,
    output SO,
    output reg[3:0] D
    );
    assign SO = D[3];
    always @(posedge Clk, negedge Rst_n)
        if (!Rst_n)
            D<=4'b0000;
        else
            D <= {D[2:0], SI};
endmodule
```

The data shift from LSB to MSB (shift left)

D[3] <- D[2], D[2] <- D[1], D[1] <- D[0] , D[0]<-S1

SHIFT REGISTER(2) - SHIFT LEFT(2)

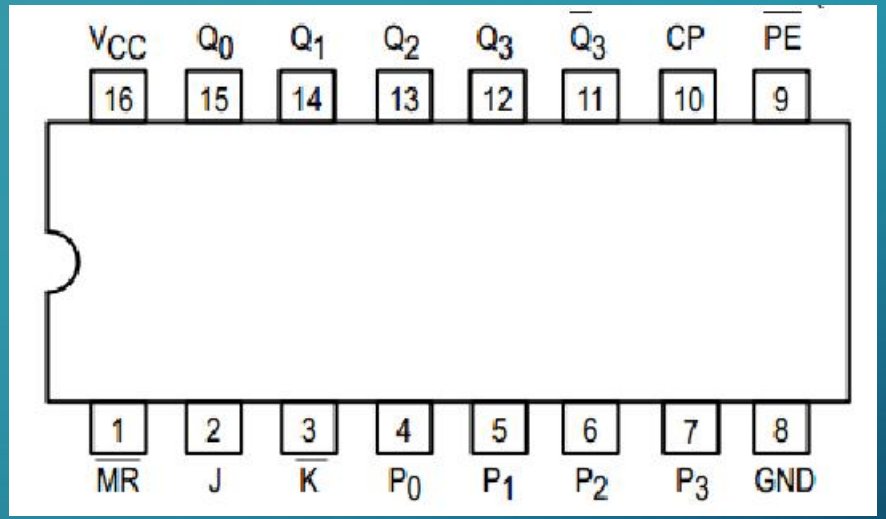
```
module Shift_Left_4(
    input SI,Clk, Rst_n,
    output SO,
    output reg[3:0] D
    );
    assign SO = D[3];
    always @(posedge Clk, negedge Rst_n)
        if (!Rst_n)
            D<=4'b0000;
        else
            D <= {D[2:0], SI};
endmodule
```



SHIFT REGISTER - 74195

Pin names

- $\overline{PE}$ Parallel Enable Input
- $P_0 \sim P_3$ Parallel Data Inputs
- J First Stage J Input
- $\overline{K}$ First Stage K Input
- CP Clock Input
- $\overline{MR}$ Master Reset Input
- $Q_0 \sim Q_3$ Parallel Outputs, Q0 is MSB
- $\overline{Q_3}$ Complementary Last Stage Output

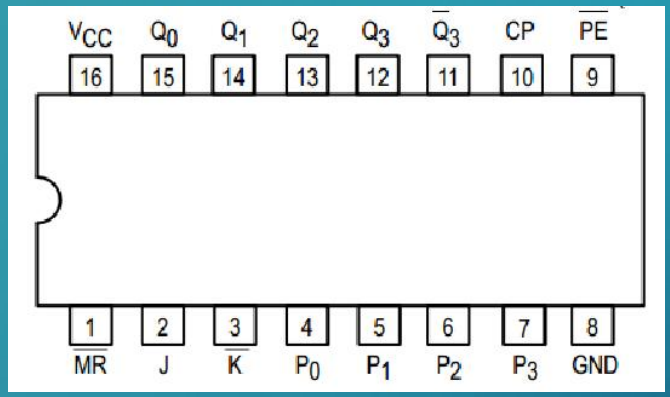


UNIVERSAL 4-BIT SHIFT REGISTER

The SN54/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications.

SHIFT REGISTER - 74195

```
module Shift_Register_74195(
    input MR_n, CP, PE_n, J, K_n,
    input D3, D2, D1, D0,
    output reg Q3, Q2, Q1, Q0,
    output Q0_n
    );
    assign Q0_n = ~Q0;
    assign K = ~K_n;
    always @(posedge CP, negedge MR_n)
        if (!MR_n)
            {Q3, Q2, Q1, Q0}<=4'b0000;
        else
            if(!PE_n)//parallel load
                {Q3, Q2, Q1, Q0}<={D3, D2, D1, D0};
            else
                case ({J, K})
                    2'b00:{Q3, Q2, Q1, Q0}<={Q2, Q1, Q0, Q0};
                    2'b01:{Q3, Q2, Q1, Q0}<={Q2, Q1, Q0, 1'b0};
                    2'b10:{Q3, Q2, Q1, Q0}<={Q2, Q1, Q0, 1'b1};
                    2'b11:{Q3, Q2, Q1, Q0}<={Q2, Q1, Q0, ~Q0};
                endcase;
endmodule
```

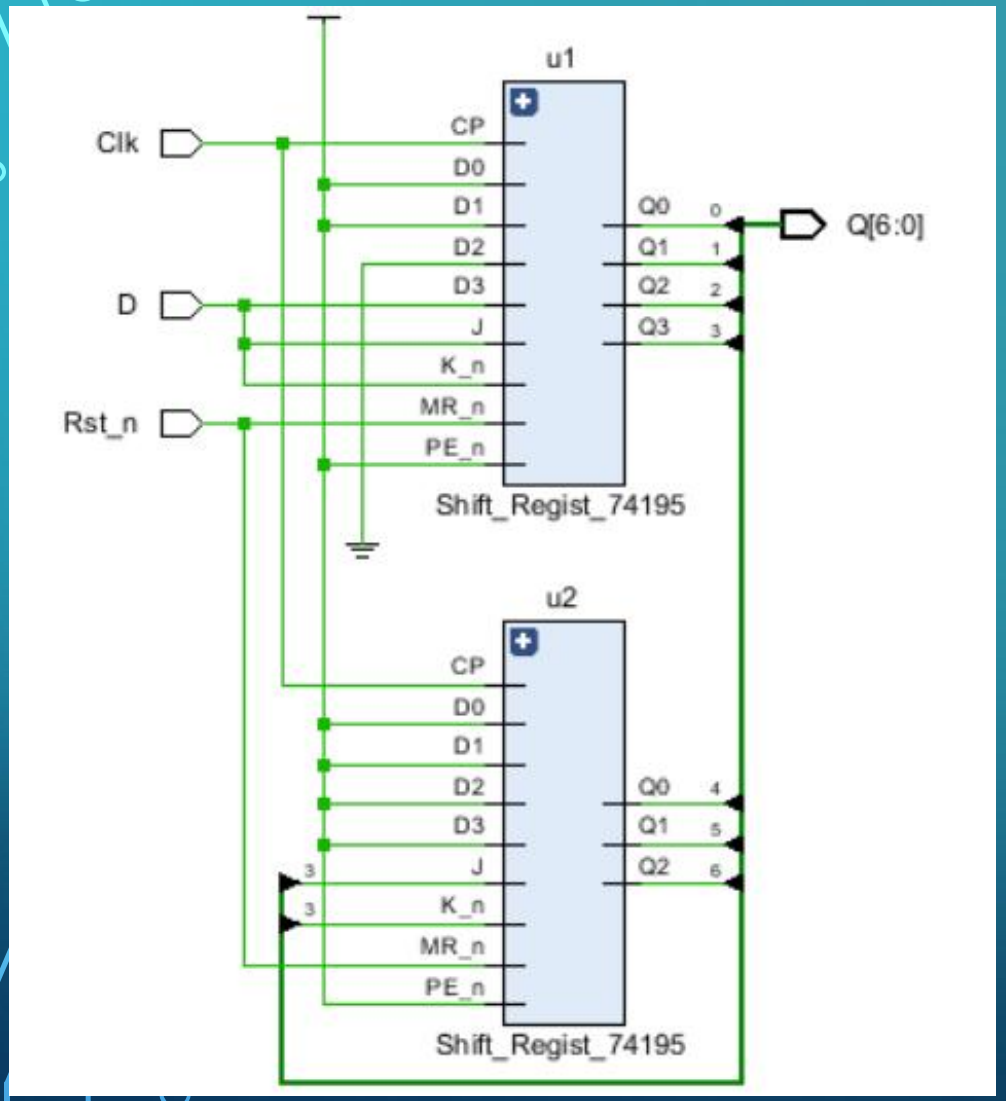


J and K' determined the output Q0

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to HIGH clock transition.

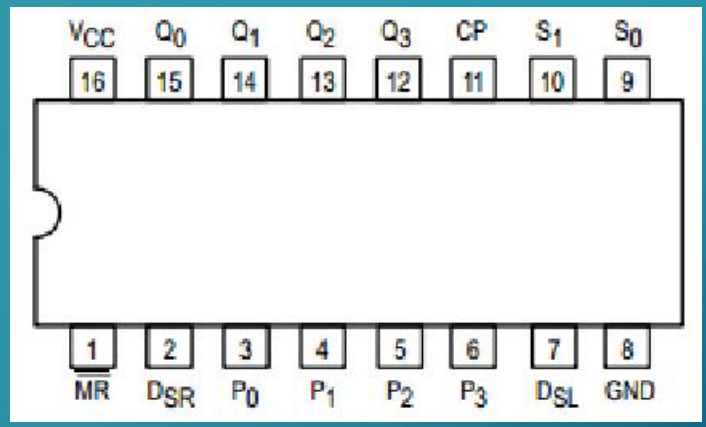
SERIAL-PARALLEL CONVERTER WITH TWO 74195 CHIPS



SHIFT REGISTER - 74194(1)

The most different between 74195 and 74194 is the output direction.

- S_0, S_1 Mode Control inputs
- $P_0 \sim P_3$ Parallel Data Inputs
- D_{SR} Serial(Shift Right) Data Input
- D_{SL} Serial(Shift Left) Data Input
- CP Clock Input
- $\overline{MR}$ Master Reset Input
- $Q_0 \sim Q_3$ Parallel Outputs, Q0 is MSB



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The SN54/74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

SHIFT REGISTER - 74194(2)

```
module Shift_Register_74194(
    input MR_n, CP, DSR, DSL,// Clear, Clock, Serial input
    input [1:0] S,//Select input
    input D3, D2, D1, D0,//Parallel input
    output reg Q3, Q2, Q1, Q0//Parallel output
    );
    always @(posedge CP, negedge MR_n)
        if(!MR_n)
            {Q3, Q2, Q1, Q0} <= 4'b0000;
        else
            case (S)
            2'b00:{Q3, Q2, Q1, Q0}<={Q3, Q2, Q1, Q0};
            2'b01:{Q3, Q2, Q1, Q0}<={DSR, Q3, Q2, Q1};
            2'b10:{Q3, Q2, Q1, Q0}<={Q2, Q1, Q0, DSL};
            2'b11:{Q3, Q2, Q1, Q0}<={D3, D2, D1, D0};
            endcase

endmodule
```

01 and 10 represent different shift direction

OPERATING MODES	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	XXXXX					LLLL			
hold ("do nothing")	X	H	I	I	X	X	X	q_0	q_1	q_2	q_3
shift left	↑	H	h	I	X	I	X	q_1	q_2	q_3	L
	↑	H	h	I	X	h	X	q_1	q_2	q_3	H
shift right	↑	H	I	h	I	X	X	L	q_0	q_1	q_2
	↑	H	I	h	h	X	X	H	q_0	q_1	q_2
parallel load	↑	Hh		h	X	X	d_n	d_0	d_1	d_2	d_3

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

COUNTER

- In digital logic and computing, a **counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the *clock* and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter.

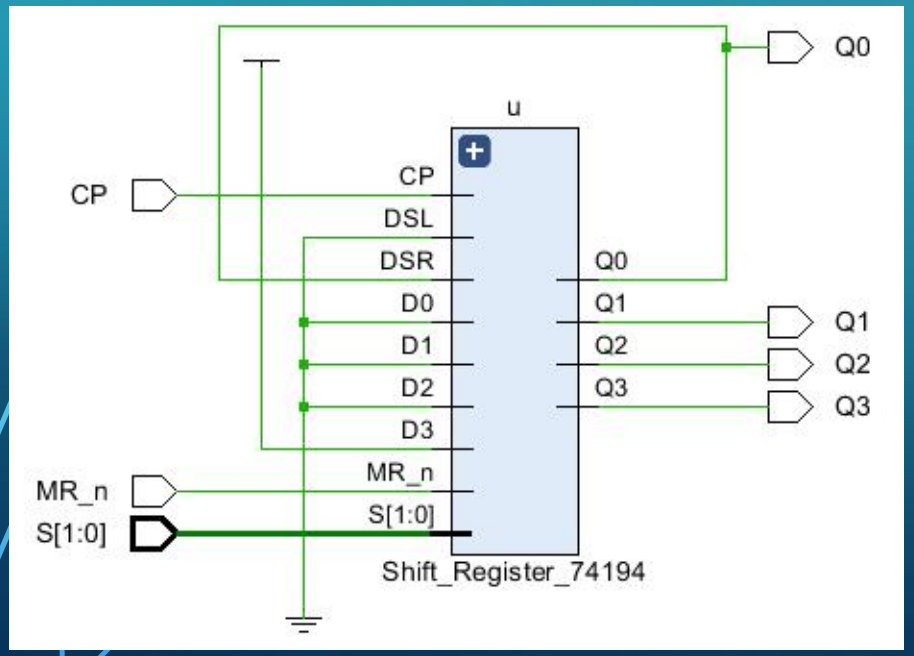
- A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits

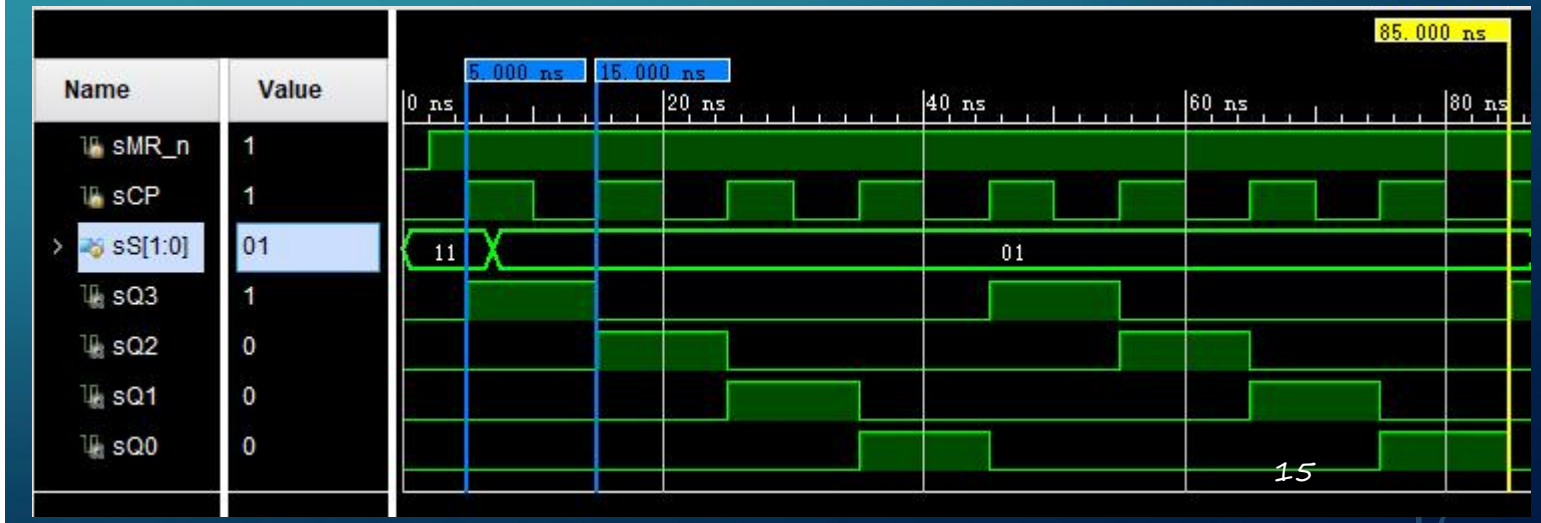
RING COUNTER—USING 74194

it has 4 state. Every state is a one-hot code.

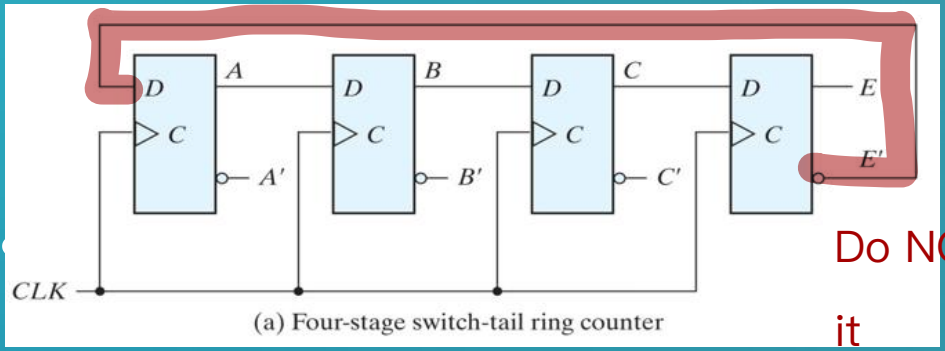
OPERATING MODES	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	XXXXX					LLLL			
hold ("do nothing")	X	H	I	I	X	X	X	q_0	q_1	q_2	q_3
shift left	↑	H	h	I	X	I	X	q_1	q_2	q_3	L
	↑	H	h	I	X	h	X	q_1	q_2	q_3	H
shift right	↑	H	I	h	I	X	X	L	q_0	q_1	q_2
	↑	H	I	h	h	X	X	H	q_0	q_1	q_2
parallel load	↑	Hh		h	X	X	d_n	d_0	d_1	d_2	d_3

sequence number	Q3	Q2	Q1	Q0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1





JOHNSON-COUNTER(1)

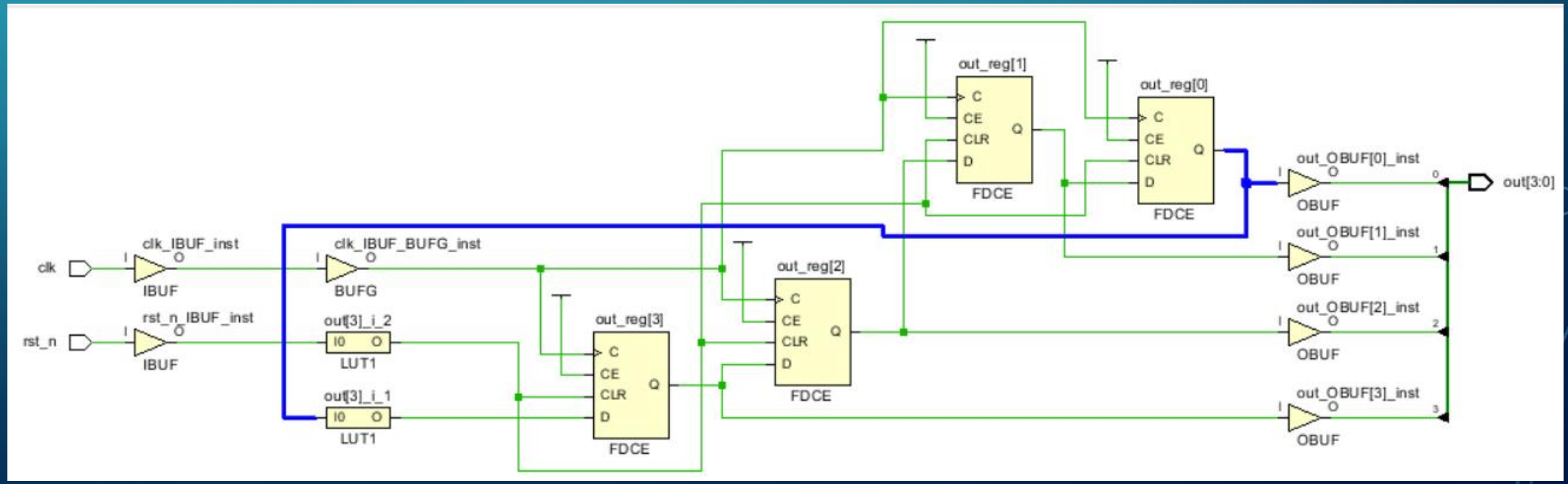


(a) Four-stage switch-tail ring counter

Do NOT operation then input it

```
module johoson_counter(
input clk,rst_n,output reg [3:0] out);
always @(posedge clk,negedge rst_n) begin
    if(~rst_n)
        out<=4'b0;
    else
        out<={~out[0],out[3:1]};
end
endmodule
```

Comma in the sensitive lists means OR



Cell Properties

out[3]_i_1

I0	O=!I0
0	1
1	0

JOHNSON-COUNTER(2)

```
module johoson_counter(
input clk,rst_n,output reg [3:0] out);
always @(posedge clk,negedge rst_n) begin
    if(~rst_n)
        out<=4'b0;
    else
        out<={~out[0],out[3:1]};
end
endmodule
```

```
module johnsonCounterTb( );
reg clk,rst_n;
wire [3:0] out;
johoson_counter jc1(clk,rst_n,out);
initial begin
    clk = 1'b0;
    rst_n = 1'b0;
    #3 rst_n = 1'b1;
    forever #5 clk=~clk;
    #160 $finish;
end
endmodule
```

MEMORY IN VERILOG

- Memory can be seen as a set of registers with the same bit width.

  Modeling memory by building arrays of reg variables, and addressing each unit of the array by array index

- Definition:

  Memory: the proper noun of an array of register

  reg [n-1:0] memory name **[m-1:0]**; // there are **m** units in memory, the size of each unit in the memory is **n** .

- Notes:
  - A n-bit register can be assigned in an assignment statement, but **a full memory CAN NOT**.
  - If you need to read and write a storage unit in memory, you must specify the **address** of the unit in memory.

To define a memory named **Mema** which has **5** memory units, each with a bit width of **3** bits.

reg [**2**:0] **Mema** [**4**:0];

To assign 3'b101 to Mema [1] unit in Mema

Mema [1]= 3'b101;

DON'TS IN VERILOG(1)

can ONLY be recognized by the simulation syntax

- **Non-Synthesizable Verilog** which **is NOT suggested** in your design
  - initial Use reset
  - Task, function sign
  - System task:$display, $monitor, $strobe, $finish NO output device can print output This is used to finish simulation
  - fork... join put statement you want to execute parallelly to a always block
  - **U**ser**D**efined**P**rimitive Also NO delay like #10

1 assign

2 A a1(, , ,)

3 always

123 are both parallel.

DON'TS IN VERILOG(2)

No incomplete if-else, incomplete case and embedded if-else, BUT case is okay.

- **Incomplete "if else" block or Incomplete "case" in combinational logical block** which are **NOT suggested** in your design.
  - a unexpected latch would be generated by EDA tool while finish the systhesis, the latch is not good for the combinational logic.

```
module updown_counter(D,CLK,CR,LD,UP,Q);
input [3:0]D;
input CLK,CR,LD,UP;
output reg [3:0] Q;

always @(posedge CLK )

if(!CR)
    Q=0;
    else if(!LD)
    Q=D;
    else if(UP)
    Q=Q+1;


endmodule
```

not a great example

```
module decorder(cln,data,addr);
input cln;
input [1:0] addr;
output reg [3:0] data;

always @(cln or addr )

begin

if(0==cln)
    data=4'b0000;
else
    case(addr)
    2'b00:data=4'b1110;
    2'b01:data=4'b1101;
    2'b10:data=4'b1011;
    endcase

end

endmodule
```

DON'TS IN VERILOG(3)

- **NOT suggested**
  - Embedded 'if-else'

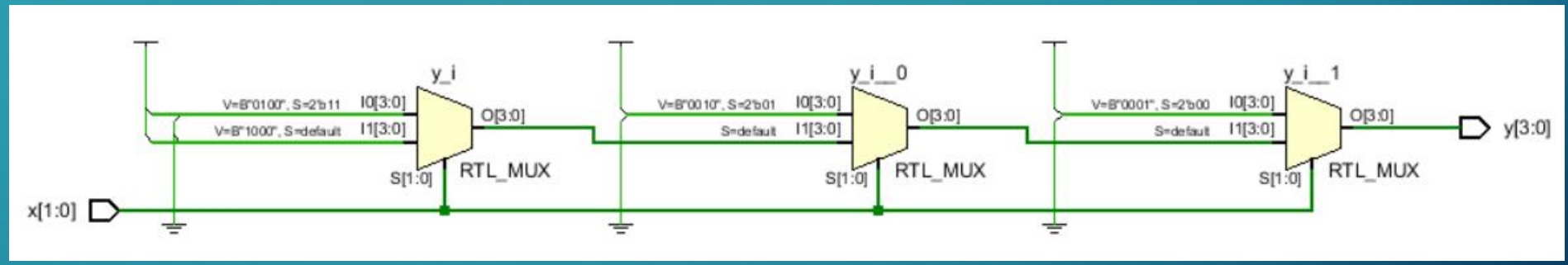
There are priority between conditions

- **Suggested**
  - Using an asynchronous reset to make your system go to initial state
  - Using 'case' instead of embedded 'if-else' to avoid unwanted priority and longer delay

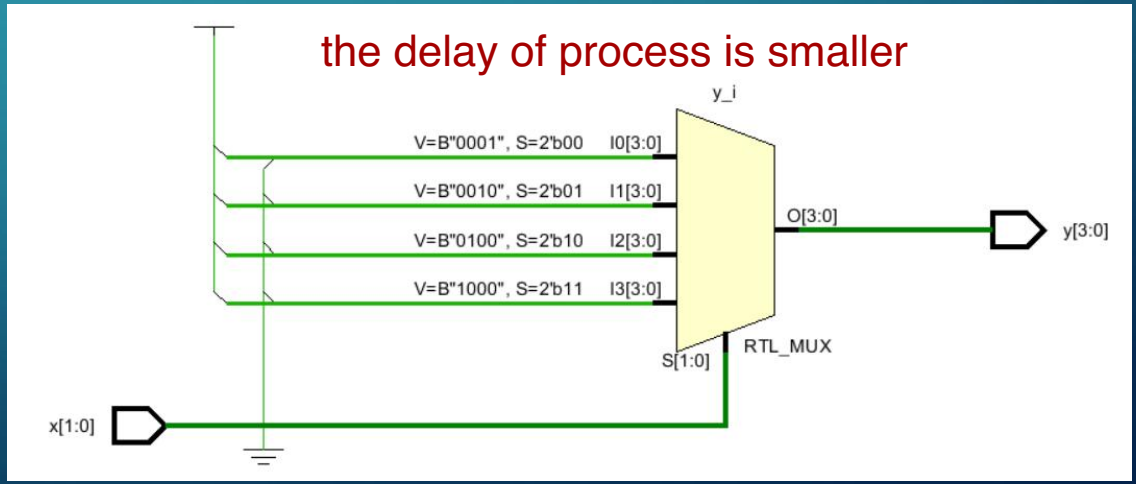
VERILOG (BE CAREFUL WITH EMBEDDED IF-ELSE)

- Embedded 'if-else' circuit brings priority and more latency compared to 'case'

```
always @*
    if( 2'b00 == x)
        y = 4'b0001;
    else if( 2'b01 == x)
            y = 4'b0010;
        else if( 2'b11 == x)
                y = 4'b0100;
            else
                y = 4'b1000;
```




```
always @*
    case(x)
        2'b00: y=4'b0001;
        2'b01: y=4'b0010;
        2'b10: y=4'b0100;
        2'b11: y=4'b1000;
    endcase
```



DON'TS IN VERILOG(4)

- **NOT suggested**
  - Two different edge trigger for one always block

NO!!!!!

  - (!!!) **a signal/port is assigned in more than one always block** (it won't report error while synthesized but its behavior maybe wrong after synthesize, pay special attention about the critical warning: **multipe driver**)

It will generate a uncertain condition

!

  - Mix-use blocking assignment and non-blocking assignment in one always block.

NO

See FSM

DON'TS IN VERILOG(5)

- **NOT suggested**
  - Two different edge trigger for one always block
  - (!!!) **a signal/port is assigned in more than one always block** (it won't report error while synthesized but its behavior maybe wrong after synthesize, pay special attention about the critical warning: **multipe driver**)
  - Mix-use blocking assignment and non-blocking assignment in one always block.

TIPS ON PROJECT(1)

Reference on internet how to implement it.

it is easy to implement.

- Using button on the developing board, notice the shaking of button while it is pressed and released.
- Avoid assigning to a variable in several always block, or it would cause conflicts
- Notice on the sensitive list of always block :
  - Suggested: '*' is suggested in combinational logic
  - NOT suggested:
    - (posedge clk, negedge clk) // there is no corresponding component in FPGA
    - (posedge in1) is not suggested to find a posedge of an input signal

TIPS ON PROJECT(2-1)

Don't using posege or negedge of a normal signal except 'clock' or 'reset' in the sensitive list of the 'always' statement block .

DON'Ts:

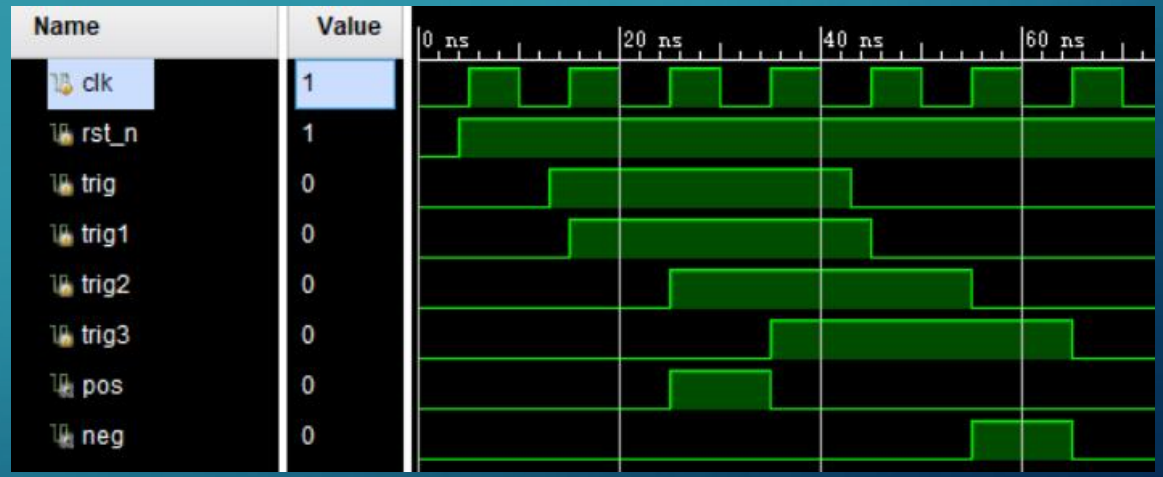
```
always @(posedge trig) begin
    x < = y;
end
```

Do Using following description instead

```
always @(pos) begin
    if(pos)
        x = y;
    else
        x = x;
end

//here pos is a new signal while it's 1'b1
means there is a posedge of trig
```

pos is generate by myself



TIPS ON PROJECT(2)

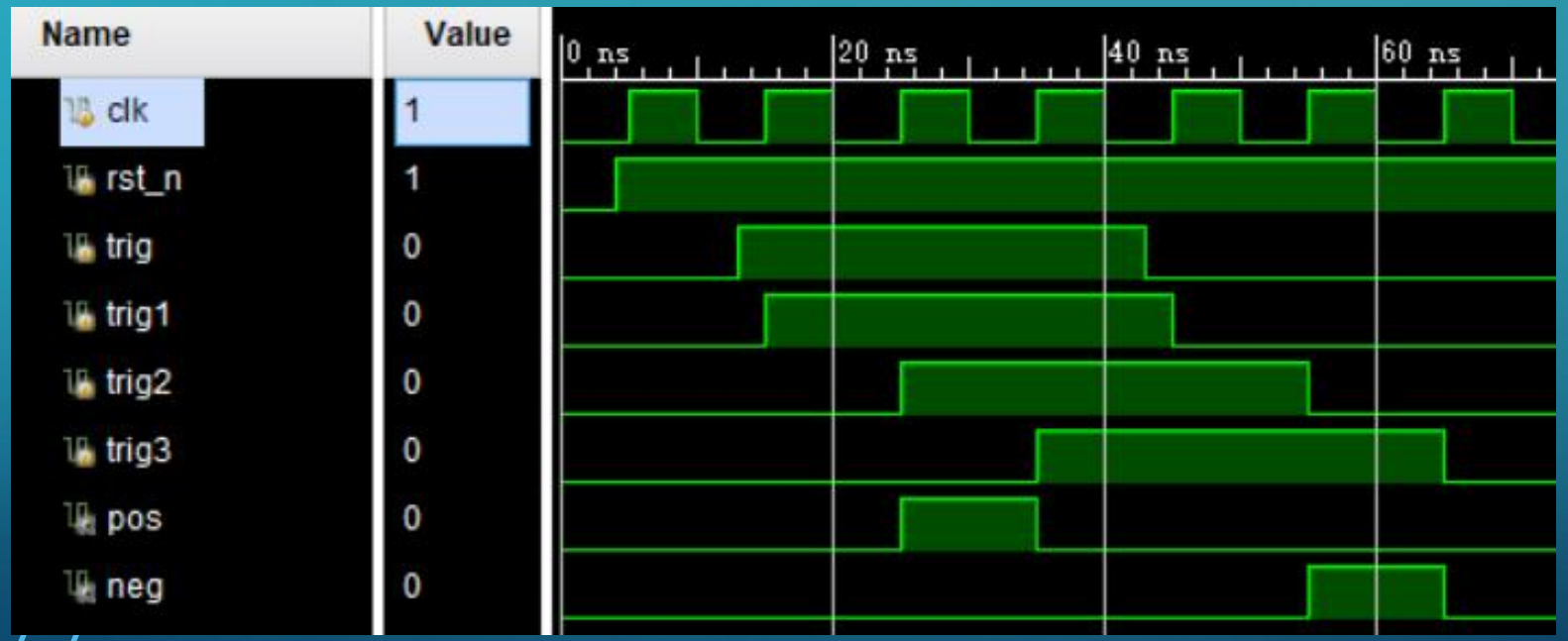
To find the posedge or negedge of input signal ‘trig’
Following method is suggested

First use clk to take sample of trigger:

trig1 is the result of 1 clk delay of trig

trig2 is the result of 1 clk delay of trig1

to get a more static sign, we use trig2 and 3.



Step1:
Sample the ‘trig’ at the rising edge(posedge) of clk to obtain ‘trig1’

Step2:
Delay the ‘trig1’ by one clk cycle to obtain ‘trig2’

Step3:
Delay the ‘trig1’ by one clk cycle to obtain ‘trig3’

Step4:
a) After negating ’ trig3’ , do logic and operation with ‘trig2’ to obtain ‘pos’

b) After negating ’ trig2’ , do logic and operation with ‘trig3’ to obtain ‘neg’

When pos=1 there is a posedge(now=0 next=1) appear

neg=1 negedge

to get the now and then, use the register previous mentioned

PRACTICE

1. Use 74195 chip realize a four-bit ring counter.
   - Do the design and verify its function using test-bench.

sequence number	Q3	Q2	Q1	Q0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

2. Use Two 74194 to implement a 8-bits serial-parallel Converter.

3. Plan the register and memory which would be used in your project?
   - Which modules needs register or memory
   - How to define, read and write them?
     - parameters are suggested to be used here