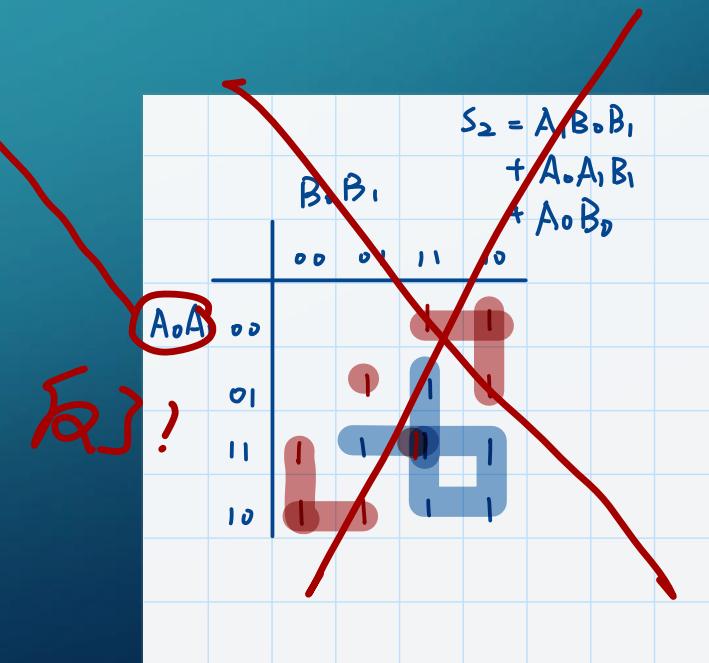


PRACTICE2

- Design a circuit to get the addition of two two-bit unsigned numbers:
 - In the design, the operator “+” in verilog is not allowed here.
 - Build a test bench to verify the function of your design.
 - Program the FPGA chip with the bitstream file, then test the design.

a[1]	a[0]	b[1]	b[0]	sum[2]	sum[1]	sum[0]
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0



$$S_1 = A_0' A_1 B_0 B_1' + A_0' A_1' B_0 + A_0' B_0 B_1' + A_0 A_1 B_0 B_1 + A_0 B_0 B_1' + A_0 A_1' B_0'$$

11

TIPS1

- List the Truth-table of the circuit.
- Recode it's logical expression about every bit of output and the inputs.

sum[0] = ...; sum[1]=....; sum[2]=....;

$$\text{sum}[2] = a[1]' a[0] b[1] b[0] +$$

$$a[1] a[0]' b[1] b[0]' + a[1] a[0] 'b[1] b[0] +$$

$$a[1] a[0] b[1]' b[0] + a[1] a[0] b[1]' b[0] + a[1] a[0] b[1] b[0]' + a[1] a[0] b[1] b[0];$$

- Using bitwise operator “&” ,“|” and “~” to express the logical expression in verilog(Don't forget the keyword “assign” in verilog).

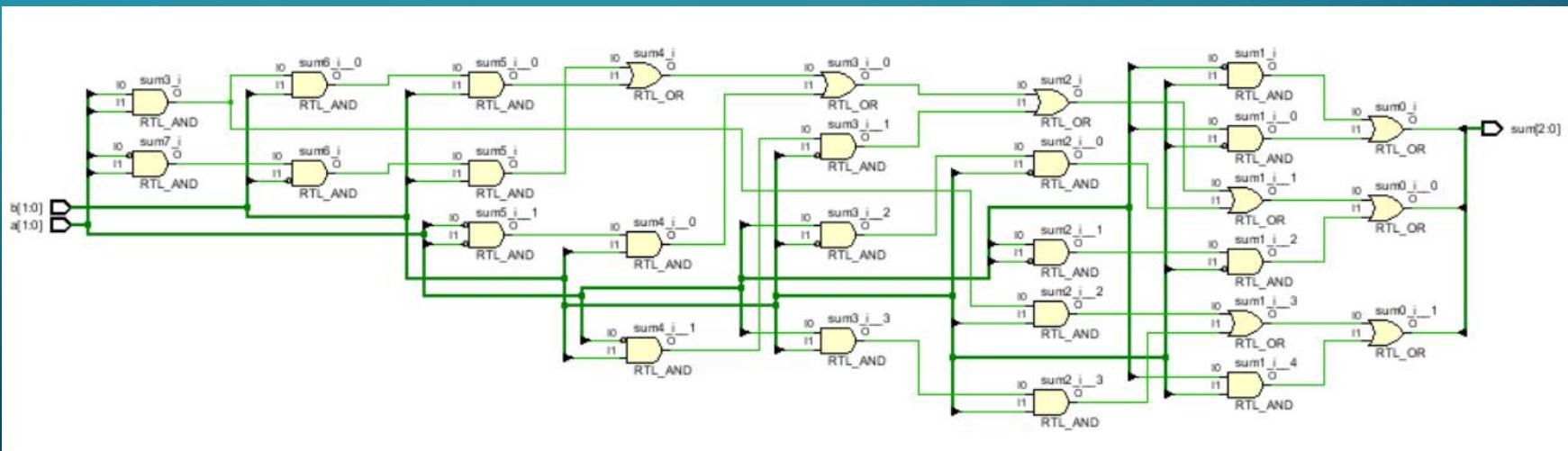
assign sum[2] = ~a[1] & a[0] & b[1] & b[0] | a[1] & ~a[0] & b[1] & ~b[0] | ...

a[1]	a[0]	b[1]	b[0]	sum[2]	sum[1]	sum[0]
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Q: How many gates needed in this circuit ? is it too much ?

PRACTICE3

- Design a circuit to get the addition of two two-bit unsigned numbers:
 - In the design:
 - the operator “+” in verilog is not allowed here.
 - using gates as less as possible.
 - Build a test bench to verify the function of your design.



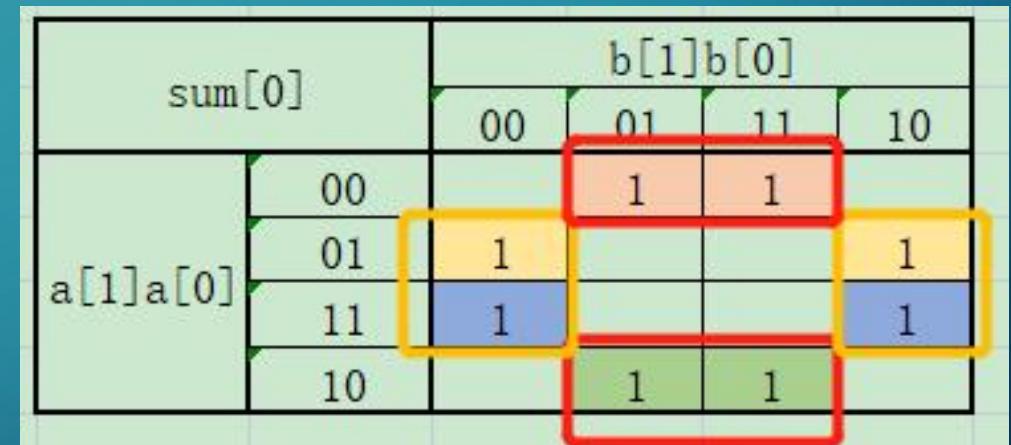
TIP2

- Simplify the circuit by using karnaugh map.

a[1]	a[0]	b[1]	b[0]	sum[0]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Before the simplification, there are only ? not gate(s), ? and gate(s) and ? or gate(s) in the circuit.

sum[0]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00		1	1	
	01	1			1
	11	1			1
	10		1	1	



After simplified by using karnaugh map, the circuit about sum[0] and a,b in Verilog is:
assign sum[0]= ~a[0]&b[0] + ~b[0]&a[0];

There are only ? not gate(s), ? and gate(s) and ? or gate(s).

$$\begin{aligned}
 S_1 = & A_o^1 A_1 B_o^1 R_1 \\
 + & A_o^1 A_1^1 B_o \\
 + & A_o^1 B_o B_1^1 \\
 + & A_o A_1 B_o B_1 \\
 + & A_o B_o^1 B_1^1 \\
 + & A_o A_1^1 B_o^1
 \end{aligned}$$

a[1]	a[0]	b[1]	b[0]	sum[1]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

sum[1]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00			1	1
	01		1		1
	11	1		1	
	10	1	1		

sum[1]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00			1	1
	01		1		1
	11	1		1	
	10	1	1		

$$\begin{aligned}
 \text{SUM}[1] = & (\sim a[1] \& a[0] \& \sim b[1] \& b[0]) \mid (a[1] \& a[0] \& b[1] \& b[0]) \mid \\
 & (\sim a[1] \& \sim a[0] \& b[1]) \mid (\sim a[1] \& b[1] \& \sim b[0]) \mid \\
 & (a[1] \& \sim b[1] \& \sim b[0]) \mid (a[1] \& \sim a[0] \& \sim b[1]);
 \end{aligned}$$

a[1]	a[0]	b[1]	b[0]	sum[2]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

sum[2]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00				
	01			1	
	11		1	1	1
	10			1	1

sum[2]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00				
	01			1	
	11	1	1	1	1
	10			1	1

$$\text{sum}[2] = (a[1]\&a[0]\&b[0]) \mid (a[0]\&b[1]\&b[0]) \mid (a[1]\&b[1])$$

a[1]	a[0]	b[1]	b[0]	sum[2]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

sum[2]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00				
	01			1	
	11		1	1	1
	10			1	1

sum[2]		b[1]b[0]			
		00	01	11	10
a[1]a[0]	00				
	01			1	
	11	1	1	1	1
	10			1	1

$$\text{sum}[2] = (a[1]\&a[0]\&b[0]) \mid (a[0]\&b[1]\&b[0]) \mid (a[1]\&b[1])$$

SYNTHESIZED DESIGN - xc7a35tcsg324-1 (active)

Sources

- Design Sources (2)
 - lab3_dv (lab3_dv)
 - addition2bit (addition2bit.v)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - lab2_addition_sim (lab2_addition_sim.v) (2)
 - lab3_dv (lab3_dv)

Hierarchy Libraries Compile Order

Source File Properties

lab2_addition_sim.v

- Enabled
- Location: C:/Users/Administrator/project_1/lab2_addition.scr
- Type: Verilog
- Library: xil_defaultlib

General Properties

Tcl Console Messages Log Reports Design Runs

```
INFO: [Project 1-479] Netlist was created with Vivado 2017.4
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

Project Summary Device addition2bit.v lab2_addition_sim.v lab3_dv.v

```
timescale 1ns / 1ps
module lab2_addition_sim();
    reg [1:0] in1_sim,in2_sim;
    wire [2:0] out1_sim,out2_sim;
    addition2bit ual(.add_in1(in1_sim),.add_in2(in2_sim),.add_out(out1_sim));
    addition2bit_operator ual2(.a(in1_sim),.b(in2_sim),.sum(out2_sim));
    initial begin
        in1_sim = 2'b0; in2_sim = 2'b0;
        repeat(15) #10 {in1_sim,in2_sim} = {in1_sim,in2_sim} + 1;
        #10 $finish();
    end
endmodule
```

③ Size: 1-0+1 bits

① initial begin & end

② initial input

④ 已分全半角符号

⑤ , <--> .

Create Block Design
Open Block Design
Generate Block Design

SIMULATION
Run Simulation

RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic

SYNTHESIS

IMPLEMENTATION
Run Implementation
Open Implemented Design

PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager

Simulation Sources (2)
sim_1 (2)
lab2_addition_sim (lab2_addition_sim.v) (2)
lab3_df (lab3_df.v)

Hierarchy Libraries Compile Order

Source File Properties

lab2_addition_sim.v
 Enabled
Location: C:/Users/Administrator/project_1/lab2_addition.sv
Type: Verilog
Library: xil_defaultlib

General Properties

Tcl Console X **Message** Log Reports Design Runs

报错及警告

```
ERROR: [XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.  
INFO: [USF-XSim-69] 'elaborate' step finished in '1' seconds  
INFO: [USF-XSim-99] Step results log file: 'C:/Users/Administrator/project_1/project_1.sim/sim_1/behav/xsim/elaborate.log'  
ERROR: [USF-XSim-62] 'elaborate' step failed with error(s). Please check the Tcl console output or 'C:/Users/Administrator/project_1/project_1.sim/sim_1/behav/xsim/elaborate.log'  
ERROR: [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.  
ERROR: [Common 17-39] 'launch_simulation' failed due to earlier errors.
```

Type a Tcl command here

22 module lab2_addition_sim();
23 Critical Messages

There were two error messages while Run Simulation.

Messages

[USF-XSim-62] 'elaborate' step failed with error(s). Please check the Tcl console output or 'C:/Users/Administrator/project_1/project_1.sim/sim_1/behav/xsim/elaborate.log' file for more information.
[Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.

OK Open Messages View

DELL

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Open Elaborated Design

Report Methodology

Report DRC

Report Noise

Schematic

SYNTHESIS

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Open Hardware Manager

lab2_addition_sim.v

Enabled

General Properties

Tcl Console Messages Log Reports Design Rules

Error (4) Warning (2) Info (39) Status (29)

Synthesized Design (2 errors)

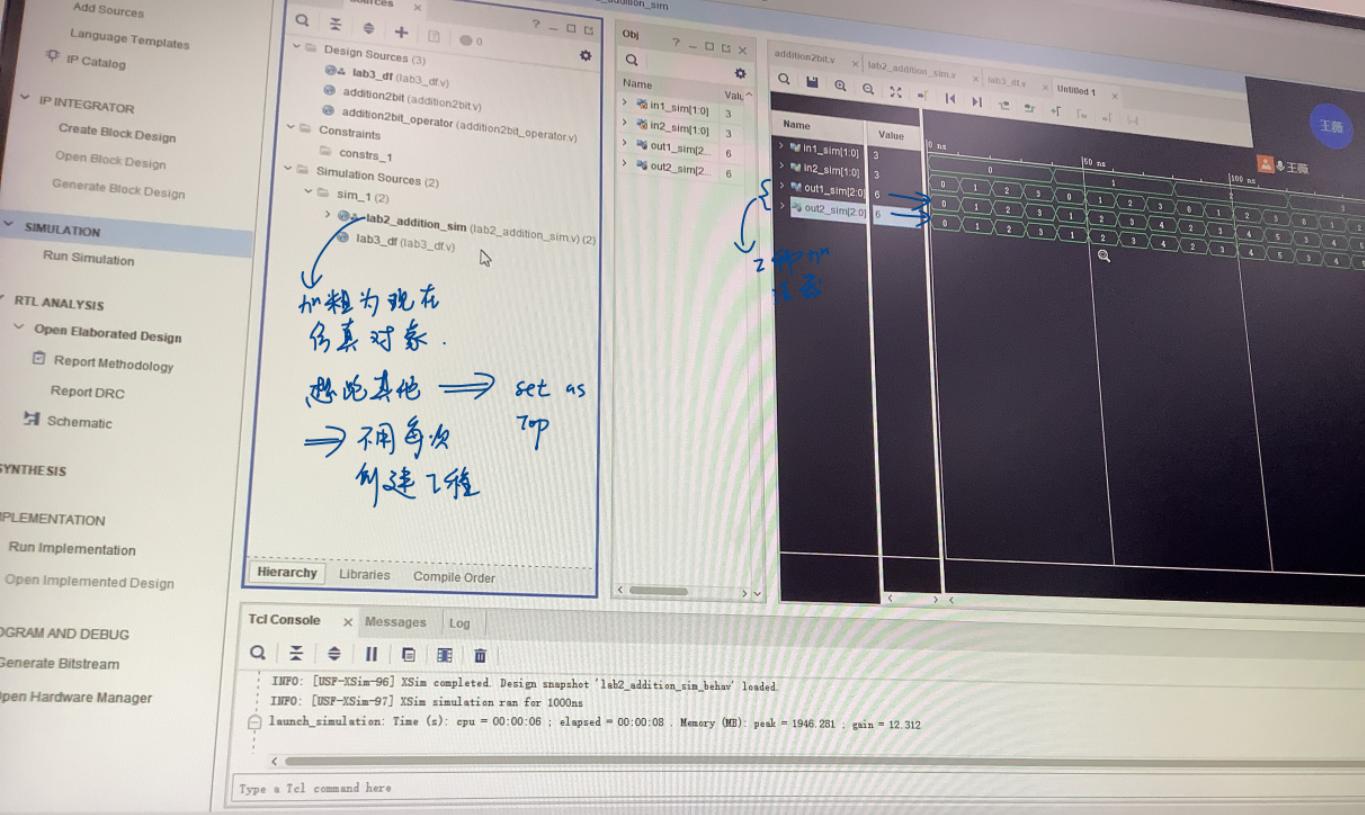
Simulation (2 errors)

initial begin
ini_sim = 2'b0; in2_sim = 2'b0;
repeat(15) #10 {ini_sim,in2_sim} = {ini_sim,in2_sim} + 1;
#10 \$finish();
end

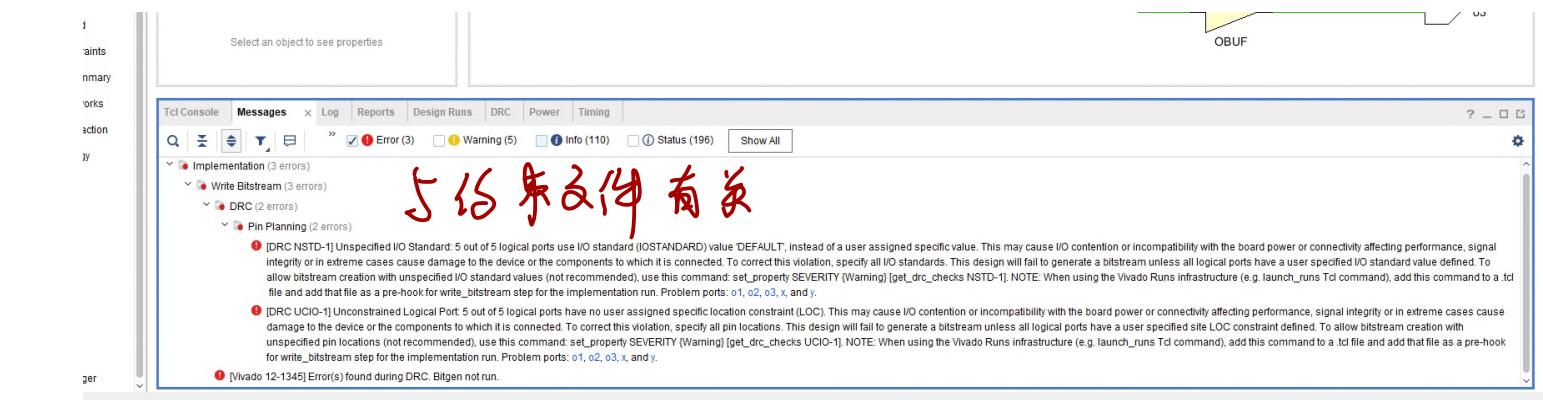
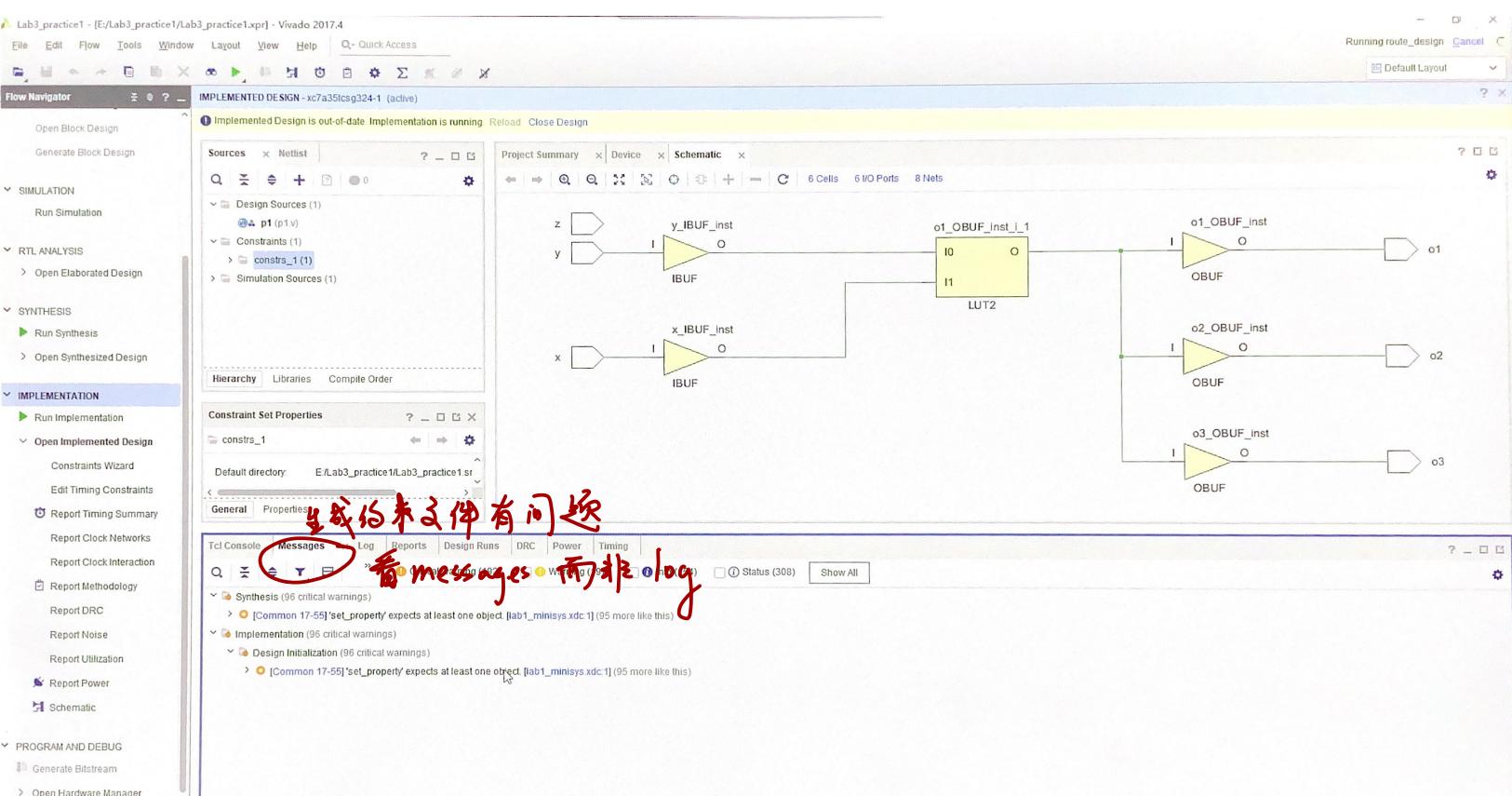
高蓝跑到
报告位置

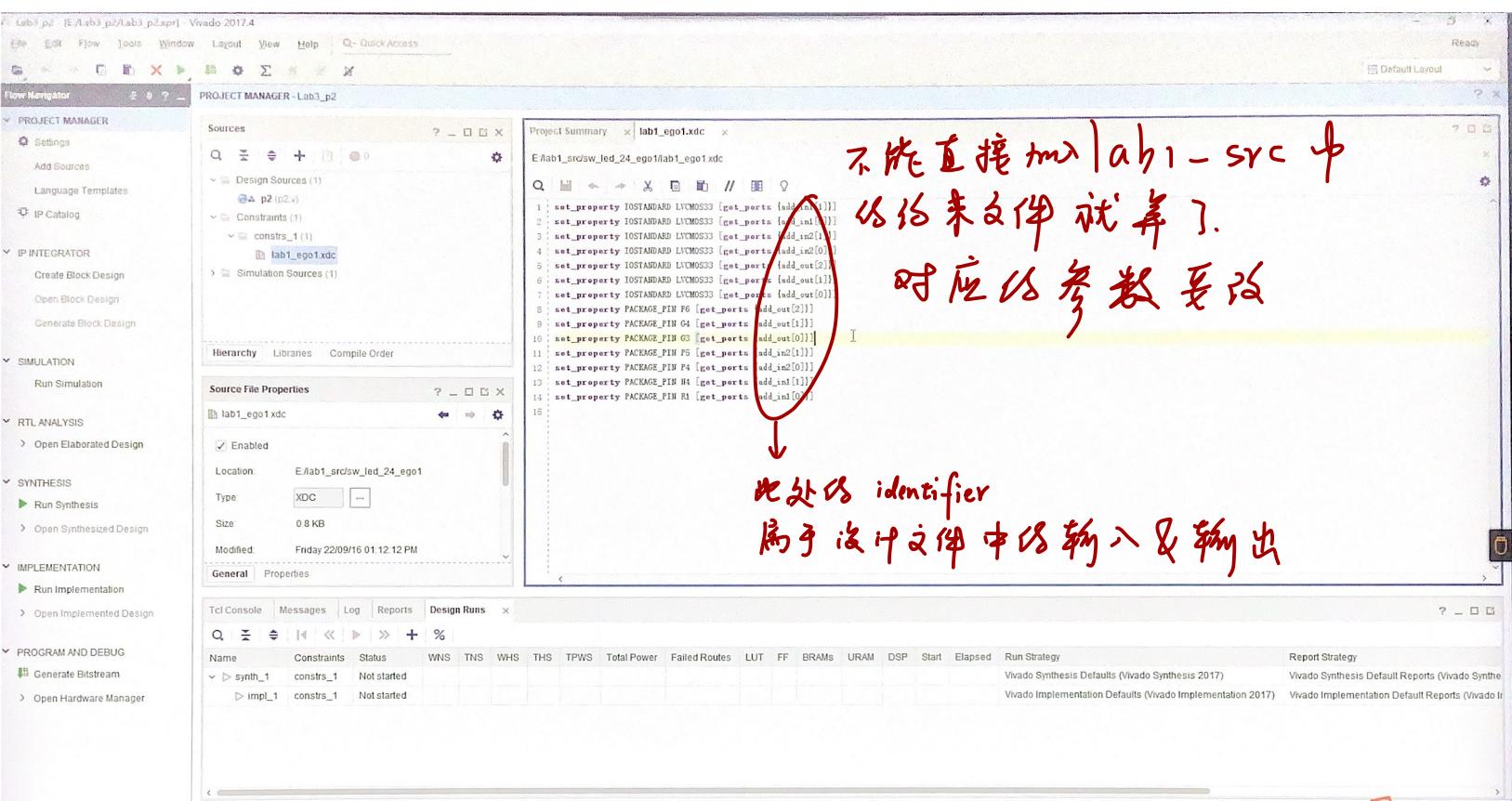
```
initial begin
ini_sim = 2'b0; in2_sim = 2'b0;
repeat(15) #10 {ini_sim,in2_sim} = {ini_sim,in2_sim} + 1;
#10 $finish();
end
```

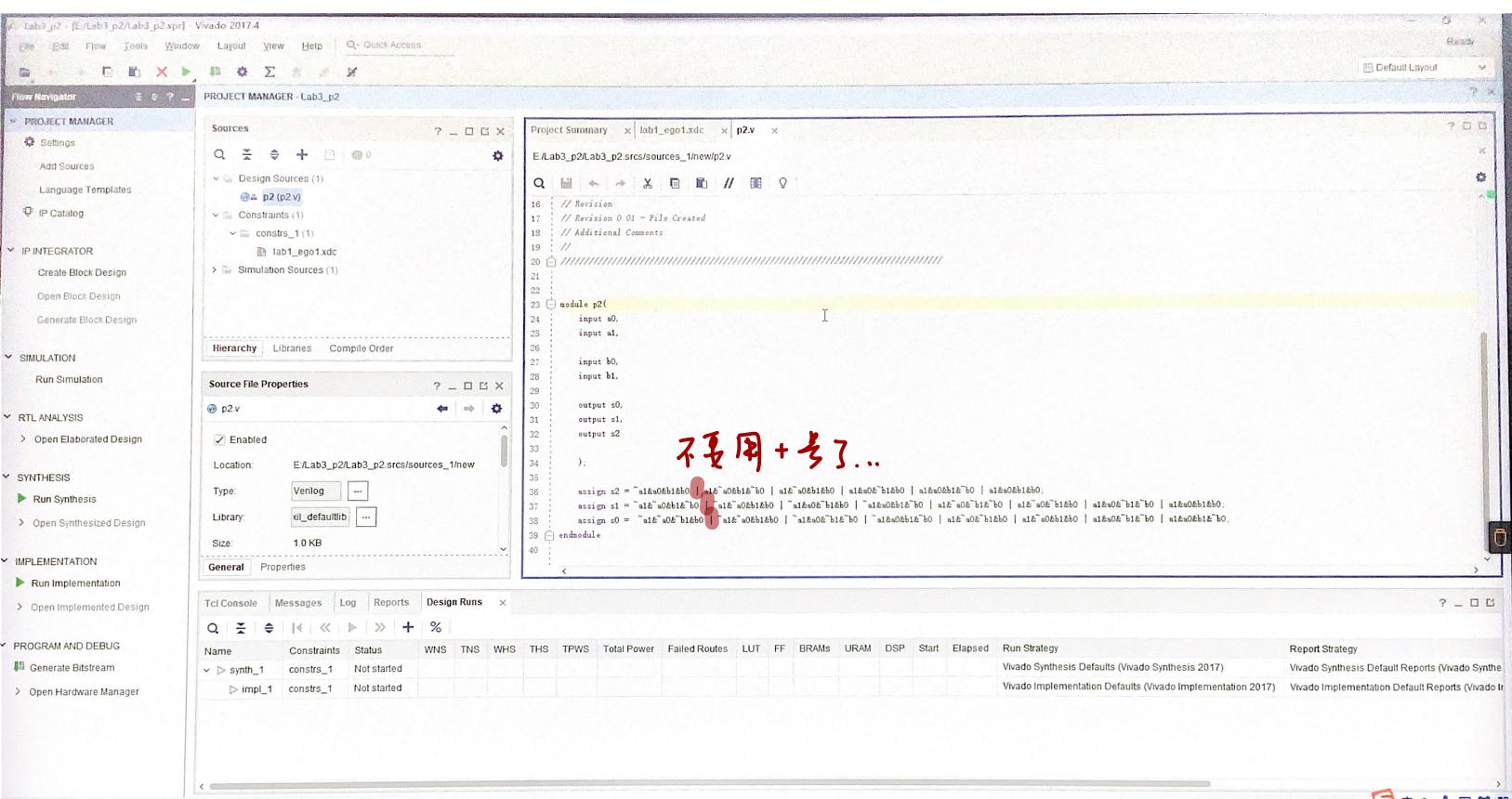
DELL



DELL







Lab3_p3 [E:/Lab3_p3/Lab3_p3.xpr] Vivado 2017.4

File Edit Flow Tools Window Layout View Help Quick Access

Default Layout

PROJECT MANAGER - Lab3_p3

Sources

Design Sources (1) @ A p3 (p3.v)

Constraints (1) conststrs_1 (1) lab1_ego1.xdc

Simulation Sources (1)

Hierarchy Libraries Compile Order

Source File Properties

p3.v

Enabled Location: E:/Lab3_p3/Lab3_p3.srsc/sources_1/new/p3.v

Type: Verilog Library: xl_defaultlib Size: 0.5 KB

General Properties

Tcl Console Messages Log Reports Design Runs

Name Constraints Status WNS TNS WHS THS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Run Strategy

synth_1 conststrs_1 Not started
impl_1 conststrs_1 Not started

Report Strategy
Vivado Synthesis Defaults (Vivado Synthesis 2017)
Vivado Implementation Defaults (Vivado Implementation 2017)

Vivado Synthesis Default Reports (Vivado Synthesis 2017)
Vivado Implementation Default Reports (Vivado Implementation 2017)

ASSIGN
Spelling !!!

代表某变量有几位
而非数组.

```

6 // Create Date: 2022/09/30 09:28:21
7 // Design Name:
8 // Module Name: p3
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20
21
22
23 module p3();
24   input [1:0] a;
25   input [1:0] b;
26   output [2:0] sum;
27
28
29 assign sum[2] = a[1] & b[1];
30 assign sum[1] = a[1] | b[1];
31 endmodule

```