

Synchronous Sequential Logic

CS207 Chapter 7

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Analysis of clocked sequential circuits

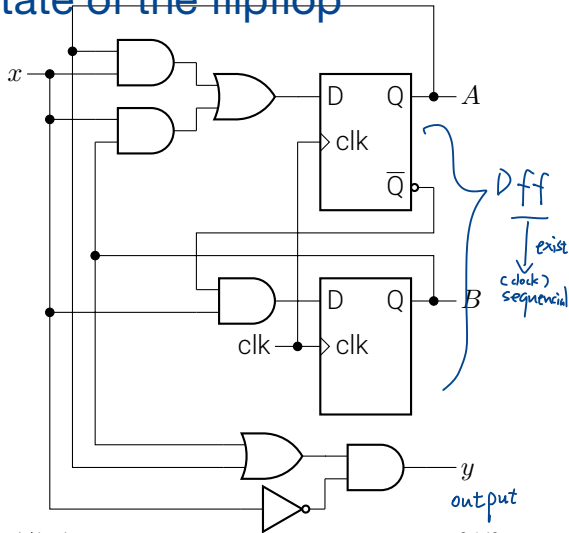


- Describes what a given circuit will do under certain operating conditions.
 - Obtaining a table or a diagram for the time sequence of inputs, outputs, and internal states.
 - Or obtain the Boolean expressions that describes the behavior of the circuit.
- A diagram is a clock sequential circuit, if it includes flip-flops and clock inputs.

diagram
map
loop
input & output

The state of Q is called the **present state** of the flipflop.

- ① sequential / combination circuit
↑↑
flip-flops



Analysis of clocked sequential circuits

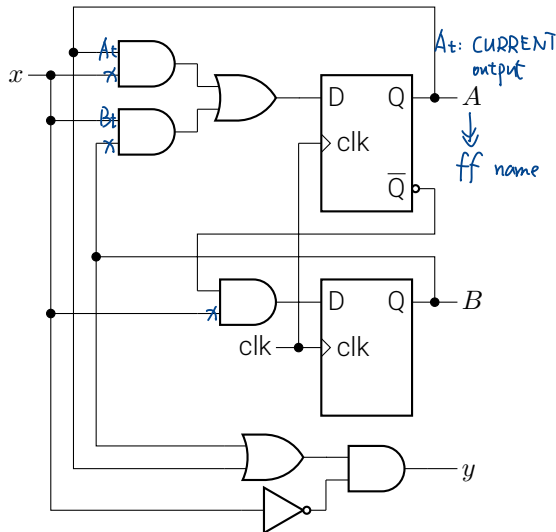


- Two D flip-flops:
 - $A(t+1) = A(t)x(t) + B(t)x(t)$,
 - $B(t+1) = A'(t)x(t)$.
- The output:
 - $y(t) = [A(t) + B(t)]x(t)'$.
 - Since all signals are labeled by t , we can also write $y = (A + B)x'$.

② look into ff

ff name \leftarrow output name

\Rightarrow B ff. Aff

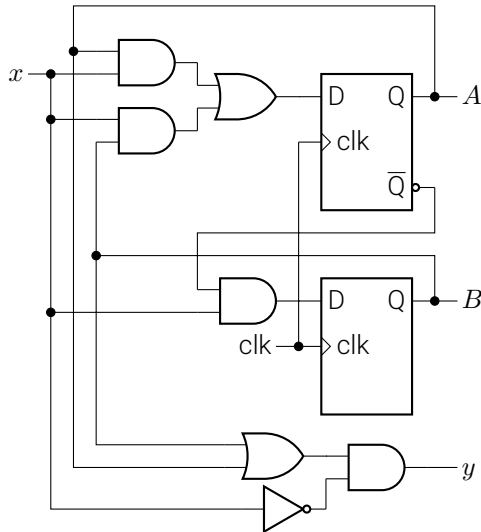


Analysis of clocked sequential circuits



- Time-sequence of inputs, outputs, FFs can be enumerated in a *state table*.

Present		Input	Next		Output
<i>A</i>	<i>B</i>	<i>x</i>	<i>A</i>	<i>B</i>	<i>y</i>
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0



Analysis of clocked sequential circuits



- State table has 2^{m+n} rows for m flip-flops and n inputs, which is very long.
- Or with three sections, with input in the next state and output column.

Present		Next				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

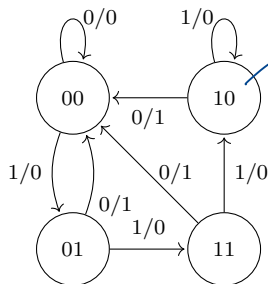
Analysis of clocked sequential circuits



- State diagram:

- Each state as a circle.
- Transitions between states are directed lines connecting the circles.

≥ every



circle's
different type
of internal state

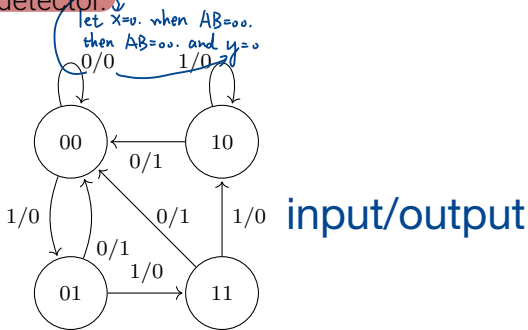
Present		Next				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

any arrangement of circle
is okay, but by default is like this

Analysis of clocked sequential circuits



- Circuit diagram \rightarrow Equations \rightarrow State table \rightarrow State diagram.
 - State table is easier to derived from circuit diagram and state equations.
 - State diagram gives a pictorial view of state transitions.
- The shown diagram is a 1-detector.



Analysis of clocked sequential circuits



- The logic diagram of a sequential circuit consists of flip-flops and gates.
- The interconnections among the gates form a combinational circuit and may be specified algebraically with Boolean expressions.
- The part of the combinational circuit that generates external outputs is described algebraically by a set of Boolean functions called *output equations*. *eg. y*
- The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean functions called *flip-flop input equations* (or, sometimes, *excitation equations*). *optional. sequential circuit may no in/output*
drive sth. to happen

Analysis of clocked sequential circuits

- We will adopt the convention of using the flip-flop input symbol to denote the input equation variable and a subscript to designate the name of the flip-flop output.
 - For example, the following input equation specifies an OR gate with inputs x and y connected to the D input of a flip-flop whose output is labeled with the symbol Q :

Diagram illustrating the input equation $D_Q = x + y$ for a flip-flop:

- The variable D_Q is the input to the flip-flop, labeled "port (in D ff)".
- The output of the flip-flop is labeled Q , with a note "output of ff (D_a, D_b)".
- The equation $D_Q = x + y$ specifies an OR gate with inputs x and y .
- A downward arrow from D_Q is labeled "current input".

Analysis of clocked sequential circuits



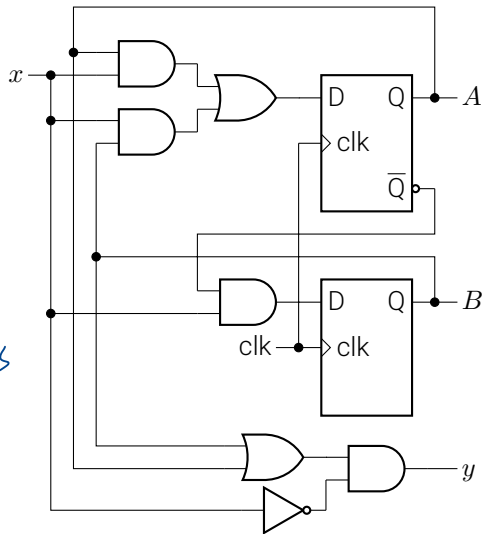
- The sequential circuit consists of two D flip-flops *A* and *B*, an input *x*, and an output *y*.
transparent ff.
- The logic diagram of the circuit can be expressed algebraically with two flip-flop input equations and an output equation:

$$D_A = Ax + Bx,$$

$$D_B = A'x,$$

$$y = (A + B)x'.$$

instantaneous



Analysis with JK/T flip-flops



$input = output$

- JK flip-flops and T flip-flops are different from D flip-flops whose state equation is the same as the input equation.
 - Refer to the corresponding characteristic equation.
- Next-state values can be derived by
 - Determining input equations.
 - Listing binary values for each input equation.
 - Using the corresponding flip-flop characteristic table to determine next state values.

An example

no output



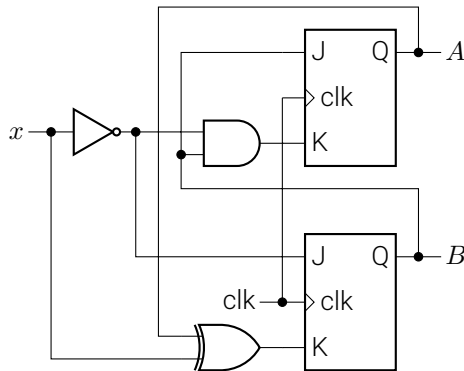
- Determine input equations:

$$J_A = B, K_A = Bx',$$

① check $J_B = x', K_B = A \oplus x$.
has ff \Rightarrow is sequential circuit

② clarify boolean equations

4 inputs: J_A, K_A, J_B, K_B



input equation is the equation that to determine the input of ff or latches. the digit on the left hand side is something like J/K/T..... it is different from the state of the ff(or latches), but the

An example



- List binary values for each input equation.
- Use the corresponding flip-flop characteristic table to determine next state values.
 - $Q(t+1) = JQ' + K'Q$. characteristic equation of JK ff
- $A(t+1) = J_AA' + K'_AA = A'B + A(Bx')'$.
- $B(t+1) = J_BB' + K'_BB = x'B + B(A \oplus x)'$.

An example



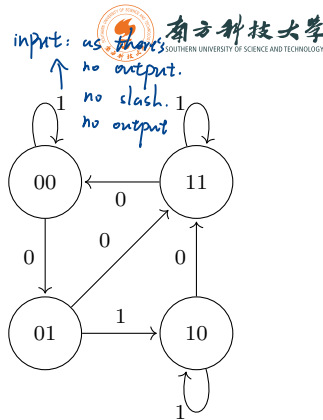
- $A(t+1) = J_A A' + K'_A A = A'B + A(Bx')'$.
- $B(t+1) = J_B B' + K'_B B = x'B + B(A \oplus x)'$. *Just for interpretation*

Present		Input	Next		FF Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Not part of
the state table

An example

Present		Input	Next		FF Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0



Another example

- Determine input equations:

$$T_A = Bx, T_B = x$$

$$y = AB.$$

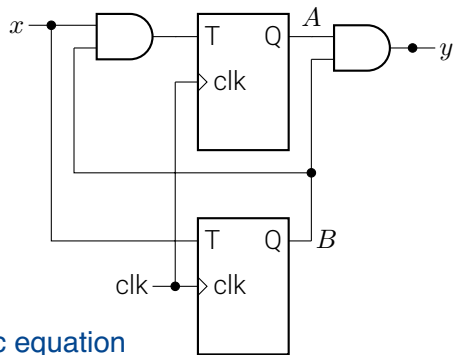
- List binary values for each input equation.
- Use the corresponding flip-flop characteristic table to determine next state values.

- $Q(t+1) = T \oplus Q = T'Q + TQ'$.

- $A(t+1) = (Bx)'A + (Bx)A'$
 $AB' + Ax' + A'Bx.$

- $B(t+1) = x \oplus B$.

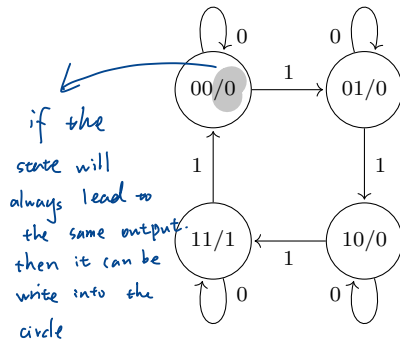
The characteristic equation
of T_{ff}



Another example



Present		Input	Next		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



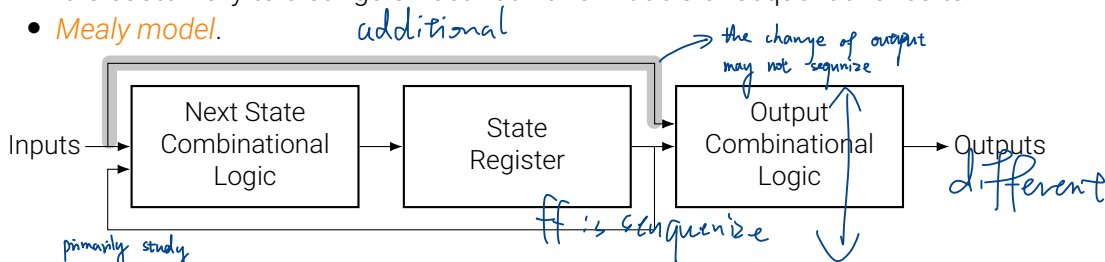
if the
state will
always lead to
the same output.
then it can be
write into the
circle

BUT this type is
NOT recommended.

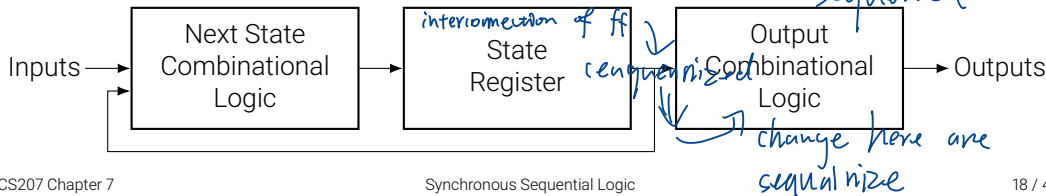


Finite state machine logic system

- The most general model of a sequential circuit has inputs, outputs, and internal states.
- It is customary to distinguish between two models of sequential circuits:
- *Mealy model.*



- *primarily study*
Moore model.



Design of clocked sequential circuits

state
diagram
description

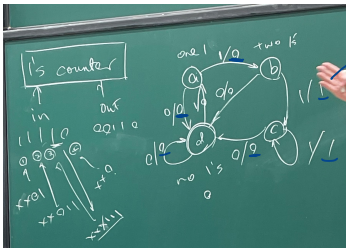


circuit
diagram



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- The *analysis* of sequential circuits starts from a circuit diagram and culminates in a state table or diagram.
- The *design* (synthesis) of a sequential circuit starts from a set of specifications and culminates in a logic diagram.
- Two sequential circuits may exhibit the same input-output behavior, but have a different number of internal states in their state diagram.
 - In general, reducing the number of flipflops reduces the cost of a circuit.
 - *State reduction* and *state assignment*.



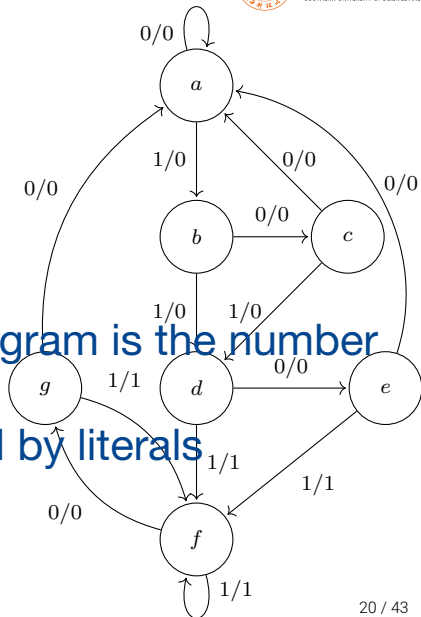
if has ≥ 3
consecutive 1



State reduction

- The reduction in the number of flip-flops in a sequential circuit is referred to as the *state-reduction* problem.
 - Reducing the number of states in a state table, while keeping the external input-output requirements unchanged.
- We illustrate the procedure with an example.

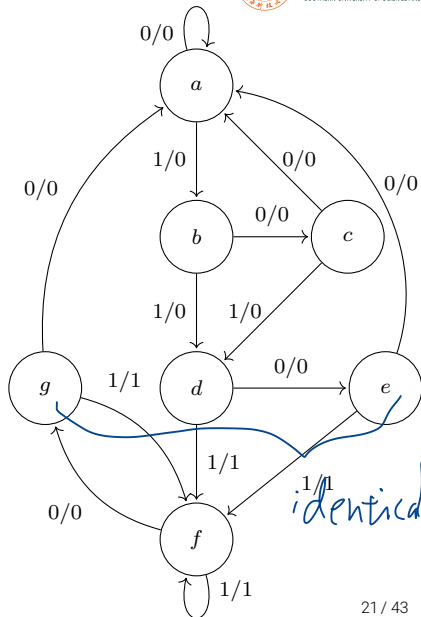
the output sequence of state diagram is the number of output,
rather than the state represented by literals





State reduction

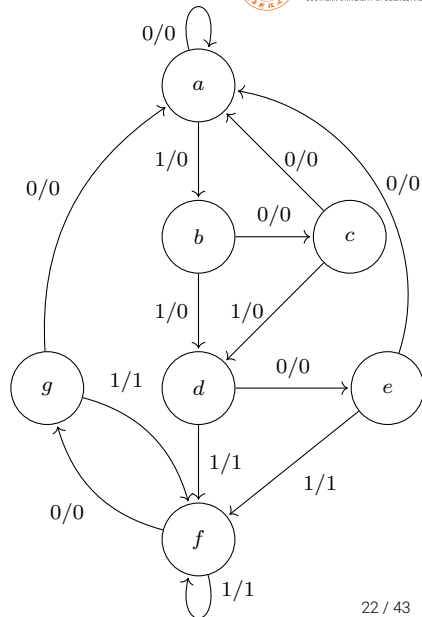
- In our example, only the input-output sequences are important.
 - The internal states are used merely to provide the required sequences.
- There are an infinite number of input sequences that may be applied to the circuit.
 - Each results in a unique output sequence.
 - Example, consider the input sequence **01010110100** starting from state *a*.



State reduction



State	Input	Output
<i>a</i>	0	0
<i>a</i>	1	0
<i>b</i>	0	0
<i>c</i>	1	0
<i>d</i>	0	0
<i>e</i>	1	1
<i>f</i>	1	1
<i>f</i>	0	0
<i>g</i>	1	1
<i>f</i>	0	0
<i>g</i>	0	0
<i>a</i>		



State reduction

- Let us assume that we have found a sequential circuit whose state diagram has fewer than seven states.
 - If identical input sequences are applied to the two circuits and identical outputs occur for all input sequences, then the two circuits are said to be equivalent.
 - One may be replaced by the other.
- The problem of state reduction is to find ways of reducing the number of states in a sequential circuit without altering the input-output relationships.

State reduction

- First, we need the state table:

Present	Next		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

first error?



State reduction

- Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.
 - States g and e are equivalent, and one of these states can be removed.

Present	Next		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1
g	a	f	0	1

\Rightarrow remove
 g . substitute
it to e

State reduction

- Now states f and d are equivalent, and state f can be removed and replaced by d .

Present	Next		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

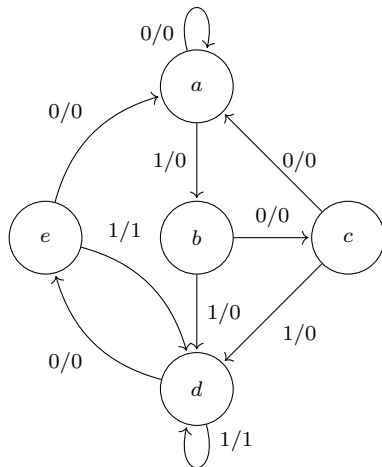
use d replace f

State reduction

- Finally we have

Present	Next		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

- The sequential circuit of this example was reduced from seven to five states.



State assignment

- In order to design a sequential circuit with physical components, it is necessary to assign unique coded binary values to the states.
- For a circuit with m states, the codes must contain n bits, where $2^n \geq m$.
 - Before the state reduction, we must assign binary values to seven states; the remaining state is unused.
 - If the state table after reduction is used, only five states need binary assignment, and we are left with three unused states.
 - Unused states are treated as don't-care conditions during the design.
- Since don't-care conditions usually help in obtaining a simpler circuit, it is more likely but not certain that the circuit with five states will require fewer combinational gates than the one with seven states.

State assignment



State	recommended in assignment		electing 1 line
	Binary	Gray Code	One-Hot
<i>a</i>	000	000	00001
<i>b</i>	001	001	00010
<i>c</i>	010	011	00100
<i>d</i>	011	010	01000
<i>e</i>	100	110	10000

- One-hot encoding usually leads to simpler decoding logic for the next state and output.

Design procedure



- The design of a clocked sequential circuit starts from a set of specifications.
 - Different from combinational circuits, a sequential circuit requires a state table.
- It consists of choosing the flip-flops and combinational gates.
 - Number of flip-flops determined from the number of states.
 - Combinational circuits derived from state table.
- The procedure for designing synchronous sequential circuits can be summarized by a list of recommended steps:

Unique
in clock
sequential
circuit

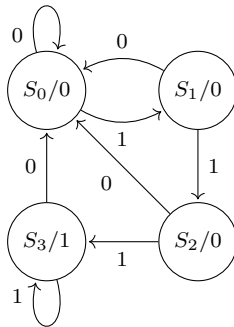
- ① From the word description and specifications of the desired operation, derive a state diagram for the circuit.
- ② Reduce the number of states if necessary.
- ③ Assign binary values to the states.
- ④ Obtain the binary-coded state table.
- ⑤ Choose the type of flip-flops to be used. *if allowed, use D.*
- ⑥ Derive the simplified flip-flop input equations and output equations.
- ⑦ Draw the logic diagram.

Design procedure

- The first step is a critical part of the process, because succeeding steps depend on it.
 - We will give one simple example to demonstrate how a state diagram is obtained from a word specification.

Design procedure

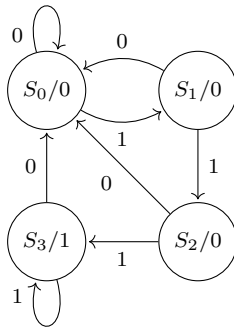
- Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line.
- Starting with state S_0 , the reset state.
 - If the input is 0, the circuit stays in S_0 .
 - If the input is 1, it goes to state S_1 to indicate that a 1 was detected.
- If the next input is 1, the change is to state S_2 to indicate the arrival of two consecutive 1's, but if the input is 0, the state goes back to S_0 .
- The third consecutive 1 sends the circuit to state S_3 . If more 1's are detected, the circuit stays in S_3 . Any 0 input sends the circuit back to S_0 .



Design procedure

- Once the state diagram has been derived, the rest of the design follows a straightforward synthesis procedure.

Present		Input	Next		Output
<i>A</i>	<i>B</i>	<i>x</i>	<i>A</i>	<i>B</i>	<i>y</i>
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1



Design procedure

- Once the state diagram has been derived, the rest of the design follows a straightforward synthesis procedure.

Present		Input	Next		Output
<i>A</i>	<i>B</i>	<i>x</i>	<i>A</i>	<i>B</i>	<i>y</i>
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

- We use D flip-flop.
- The flip-flop input equations can be obtained:

$$A(t+1) = D_A(A, B, x)$$

$$= \sum(3, 5, 7),$$

$$B(t+1) = D_B(A, B, x)$$

$$= \sum(1, 5, 7),$$

$$y(A, B, x) = \sum(6, 7).$$

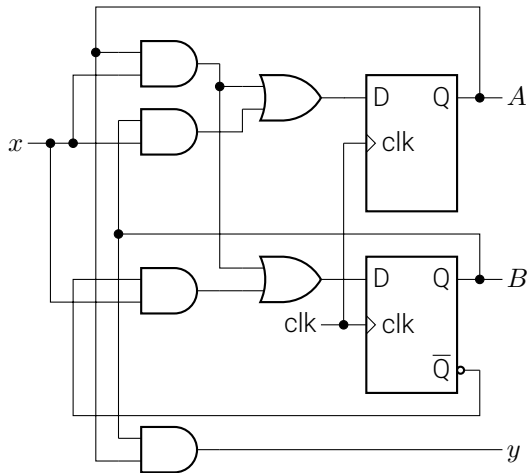
Design procedure

- The equations are simplified by means of K-map:

$$D_A = Ax + Bx,$$

$$D_B = Ax + B'x,$$

$$y = AB.$$



Excitation tables

- The design of a sequential circuit with flip-flops other than the D type is complicated by the fact that the input equations for the circuit must be derived indirectly from the state table.
 - When D-type flip-flops are employed, the input equations are obtained directly from the next state.
 - This is not the case for the JK and T types of flip-flops.
- In order to determine the input equations for these flip-flops, it is necessary to derive a functional relationship between the state table and the input equations.
- During the design process, we usually know the transition from the present state to the next state and wish to find the flip-flop input conditions that will cause the required transition.
- For this reason, we need a table that lists the required inputs for a given change of state: *excitation table*.



Excitation tables

- JK flip-flop: identical to characteristic table, but its inverse

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- T flip-flop:

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Synthesis using JK flip-flops



- The manual synthesis procedure for sequential circuits with JK flip-flops is the same as with D flip-flops.
 - Except that the input equations must be evaluated from the present state to the next-state transition derived from the excitation table.

Present		Input	Next		Flip-flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Synthesis using JK flip-flops



A \ Bx	00	01	11	10
0				1
1	X	X	X	X

A \ Bx	00	01	11	10
0	X	X	X	X
1			1	

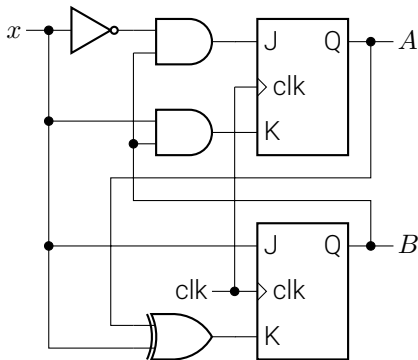
A \ Bx	00	01	11	10
0		1	X	X
1		1	X	X

A \ Bx	00	01	11	10
0	X	X		1
1		X	1	X

Synthesis using JK flip-flops

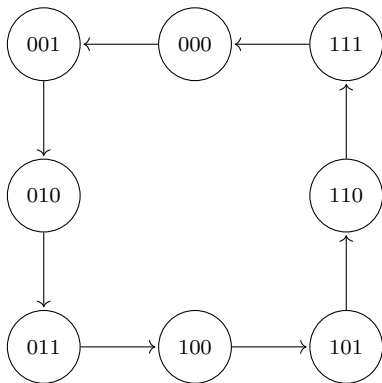


$$\begin{aligned}J_A &= Bx', \\J_B &= x, \\K_A &= Bx, \\K_B &= (A \oplus x)'.\end{aligned}$$



Synthesis using T flip-flops

- The procedure for synthesizing circuits using T flip-flops will be demonstrated by designing a binary counter.
- An n -bit binary counter consists of n flip-flops that can count in binary from 0 to $2^n - 1$.



Synthesis using T flip-flops



Present			Next			Flip-flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Synthesis using T flip-flops



A \ Bx	00	01	11	10
0			1	
1			1	

A \ Bx	00	01	11	10
0		1	1	
1		1	1	

A \ Bx	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$T_{A2} = A_1 A_0,$$

$$T_{A1} = A_0,$$

$$T_{A0} = 1.$$