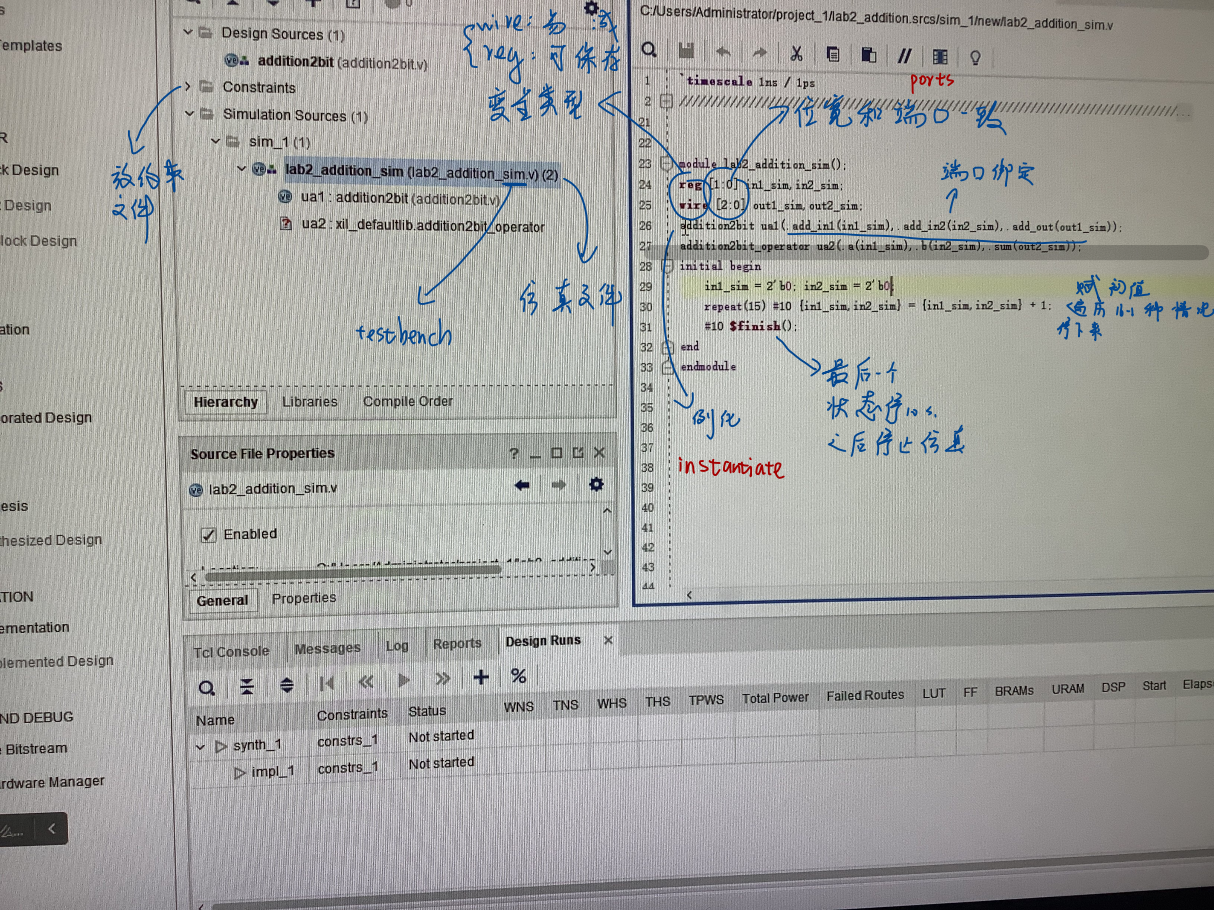
DIGITAL DESIGN

LAB3　BITWISE OPERATION IN VERILOG, GATES IN RTL VS LUT IN FPGA

2022 FALL TERM


Design Sources (1)
addition2bit (addition2bit.v)
Constraints
Simulation Sources (1)
sim_1 (1)
lab2_addition_sim (lab2_addition_sim.v) (2)
ua1 : addition2bit (addition2bit.v)
ua2 : xil_defaultlib.addition2bit_operator
Hierarchy
Libraries
Compile Order
Source File Properties
lab2_addition_sim.v
Enabled
General
Properties
C:/Users/Administrator/project_1/lab2_addition.srcs/sim_1/new/lab2_addition_sim.v
`timescale 1ns / 1ps
module lab2_addition_sim();
reg [1:0] in1_sim,in2_sim;
wire [2:0] out1_sim,out2_sim;
addition2bit ua1(.add_in1(in1_sim), .add_in2(in2_sim), .add_out(out1_sim));
addition2bit_operator ua2(.a(in1_sim), .b(in2_sim), .sum(out2_sim));
initial begin
in1_sim = 2'b0; in2_sim = 2'b0;
repeat(15) #10 {in1_sim,in2_sim} = {in1_sim,in2_sim} + 1;
#10 $finish();
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
synth_1
constrs_1
Not started
impl_1
constrs_1
Not started

LAB3

- Verilog
  - Bitwise and logic operations in Verilog
- Design mode in Verilog
  - 1. data flow
- Vivado
  - Schematic of “TRL analysis” (Gates)
  - Schematic of “Synthesis” (LUT of FPGA chip)

BITWISE AND LOGICAL OPERATIONS IN VERILOG

Four-valued logic (The IEEE 1364 standard): 0, 1, Z (high impedance), and X (unknown logic value).

Operator : ~ & ^ ~^ ^~ | ! && ||

Priority:

~ ! > & > ^ ~^ ^~ > | > && > ||

Operator type	Operator symbols	Operation performed
Bitwise	~	Bitwise NOT (1's complement)
	&	Bitwise AND
	|	Bitwise OR
	^	Bitwise XOR
	~^ or ^~	Bitwise XNOR
Logical	!	NOT
	&&	AND
	||	OR

DESIGN MODE IN VERILOG - DATA FLOW

- 1. Data flow design： using “assign “ as *continuous assignment* , to transfer the data from input ports through variables to the output ports .

logical expression	data flow in Verilog
f(a,b,c) = abc + a’b	assign f = a & b &c | ~a &b;
f(a,b,c) = ∑(2,4,5,6) = a’bc’+ab’c’+ab’c+abc’	assign f = ~a&b&~c | a&~b&~c | a& ~b&c | a&b&~c;

Operator : ~ & ^ ~^ ^~ | ! && ||

Priority:
~ ! > & > ^ ~^ ^~ > | > && > ||

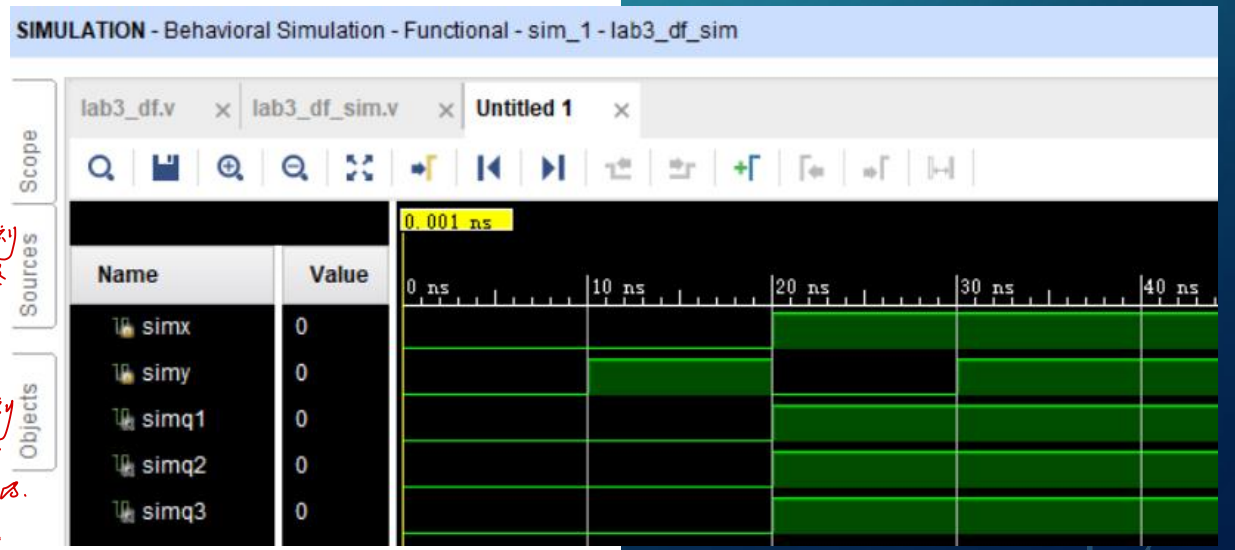
Operator type	Operator symbols	Operation performed
Bitwise	~	Bitwise NOT (1's complement)
	&	Bitwise AND
	|	Bitwise OR
	^	Bitwise XOR
	~^ or ^~	Bitwise XNOR
Logical	!	NOT
	&&	AND
	||	OR

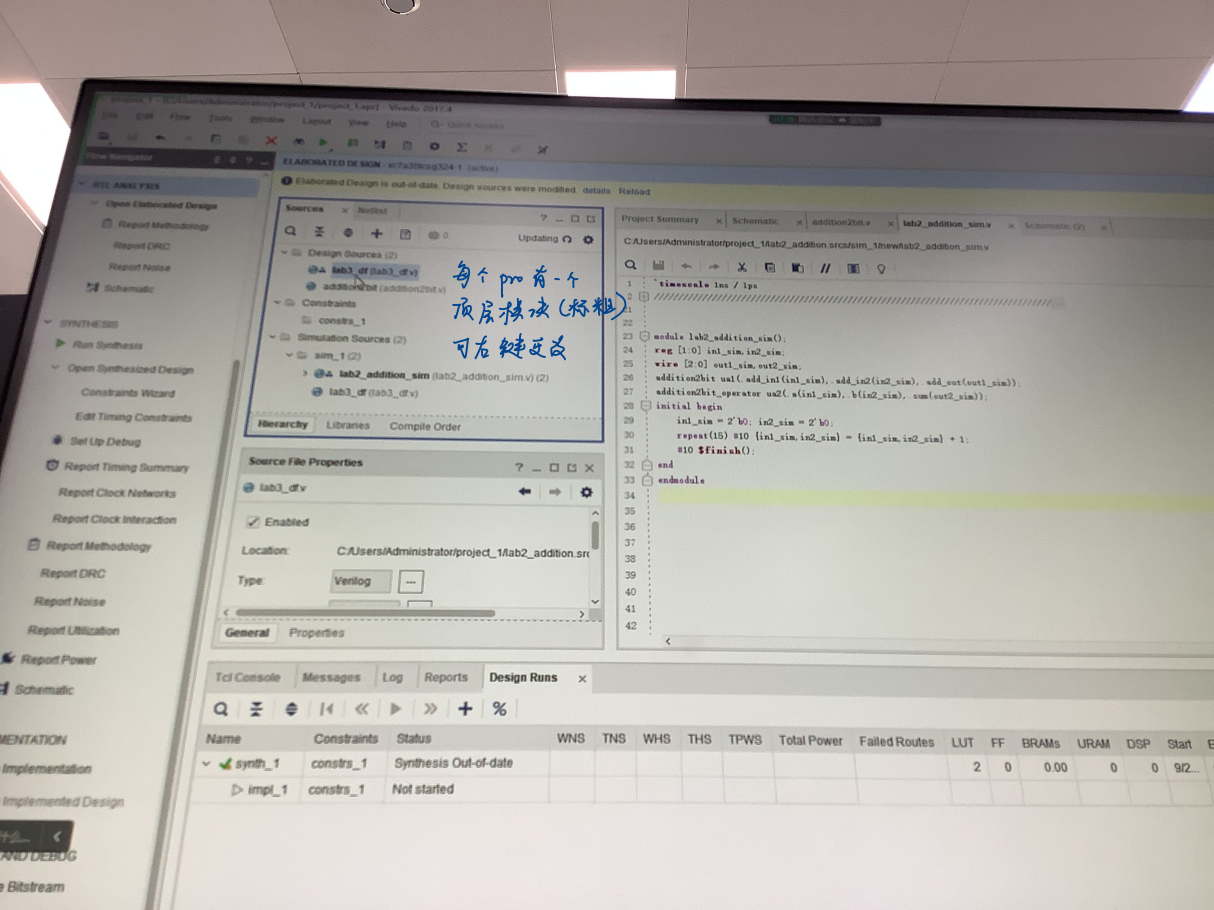
DATA FLOW DESIGN

Demo: a) q1 = x b) q2=x + xy c) q3=x(x + y)

```
module lab3_df(
    input x,
    input y,
    output q1,
    output q2,
    output q3
    );
    assign q1 = x;
    assign q2 = x | (x & y);
    assign q3 = x & (x | y);

endmodule
```

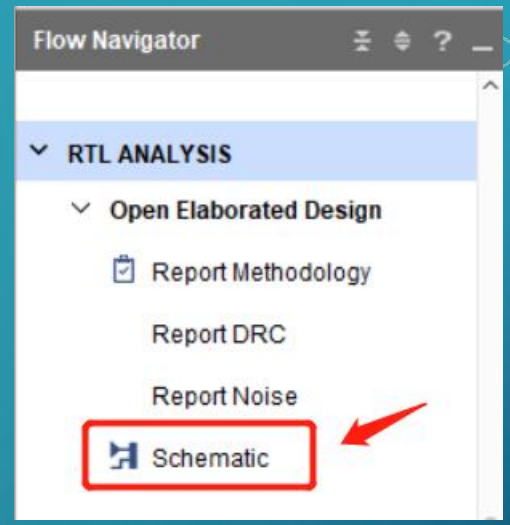
```
module lab3_df_sim( );
    reg simx, simy;
    wire simq1, simq2, simq3;
    lab3_df u_df(
    .x(simx), .y(simy), .q1(simq1), .q2(simq2), .q3(simq3) );

    initial
    begin
        simx=0;
        simy=0;
    #10
        simx=0;
        simy=1;
    #10
        simx=1;
        simy=0;
    #10
        simx=1;
        simy=1;
    end
endmodule
```

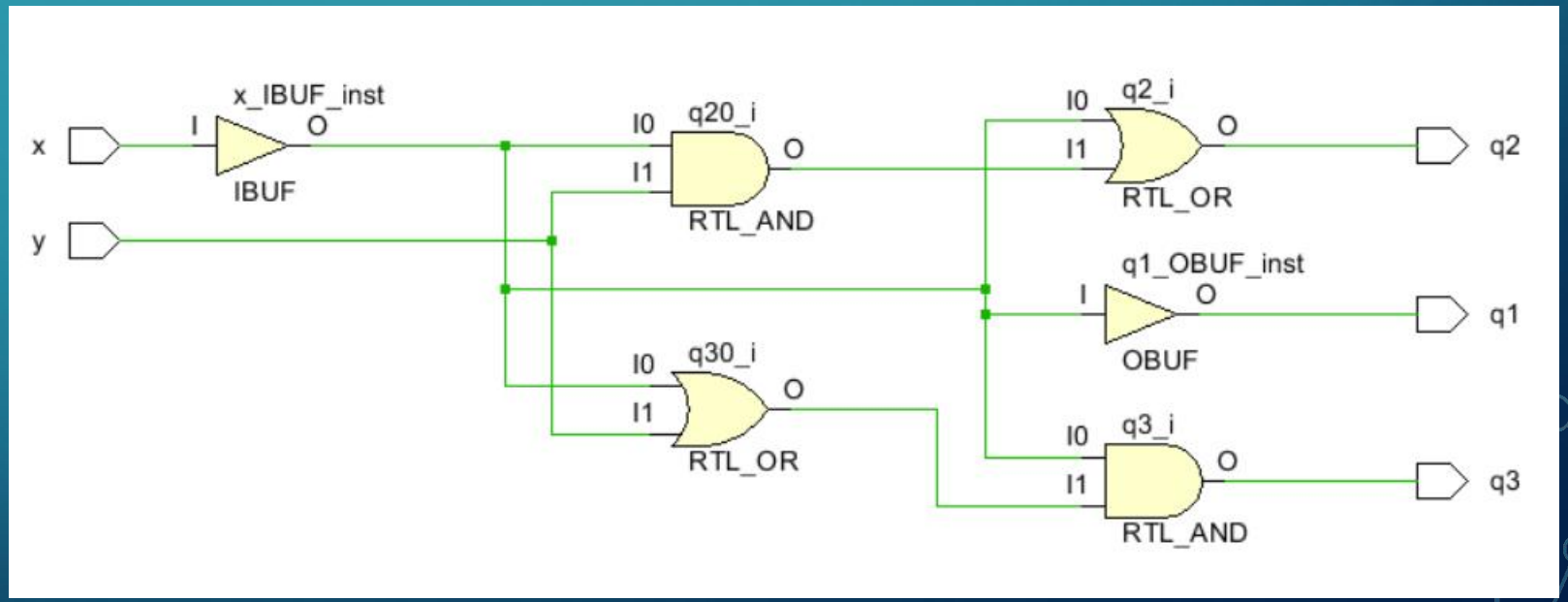



每个 pro 有一个
顶层模块（标粗）
可右键更改
Sources
Design Sources (2)
lab3_df (lab3_df.v)
addition2bit (addition2bit.v)
Constraints
constrs_1
Simulation Sources (2)
sim_1 (2)
lab2_addition_sim (lab2_addition_sim.v) (2)
lab3_df (lab3_df.v)
Hierarchy
Libraries
Compile Order
Source File Properties
lab3_df.v
Enabled
Location:
C:/Users/Administrator/project_1/lab2_addition.sr
Type:
Verilog
General
Properties
Project Summary
Schematic
addition2bit.v
lab2_addition_sim.v
C:/Users/Administrator/project_1/lab2_addition.srcs/sim_1/new/lab2_addition_sim.v
`timescale 1ns / 1ps
module lab2_addition_sim();
reg [1:0] in1_sim,in2_sim;
wire [2:0] out1_sim,out2_sim;
addition2bit ua1(.add_in1(in1_sim), .add_in2(in2_sim), .add_out(out1_sim));
addition2bit_operator ua2(.a(in1_sim), .b(in2_sim), .sum(out2_sim));
initial begin
in1_sim = 2'b0; in2_sim = 2'b0;
repeat(15) #10 {in1_sim,in2_sim} = {in1_sim,in2_sim} + 1;
#10 $finish();
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
synth_1
constrs_1
Synthesis Out-of-date
2
0
0.00
0
0
9/2...
impl_1
constrs_1
Not started

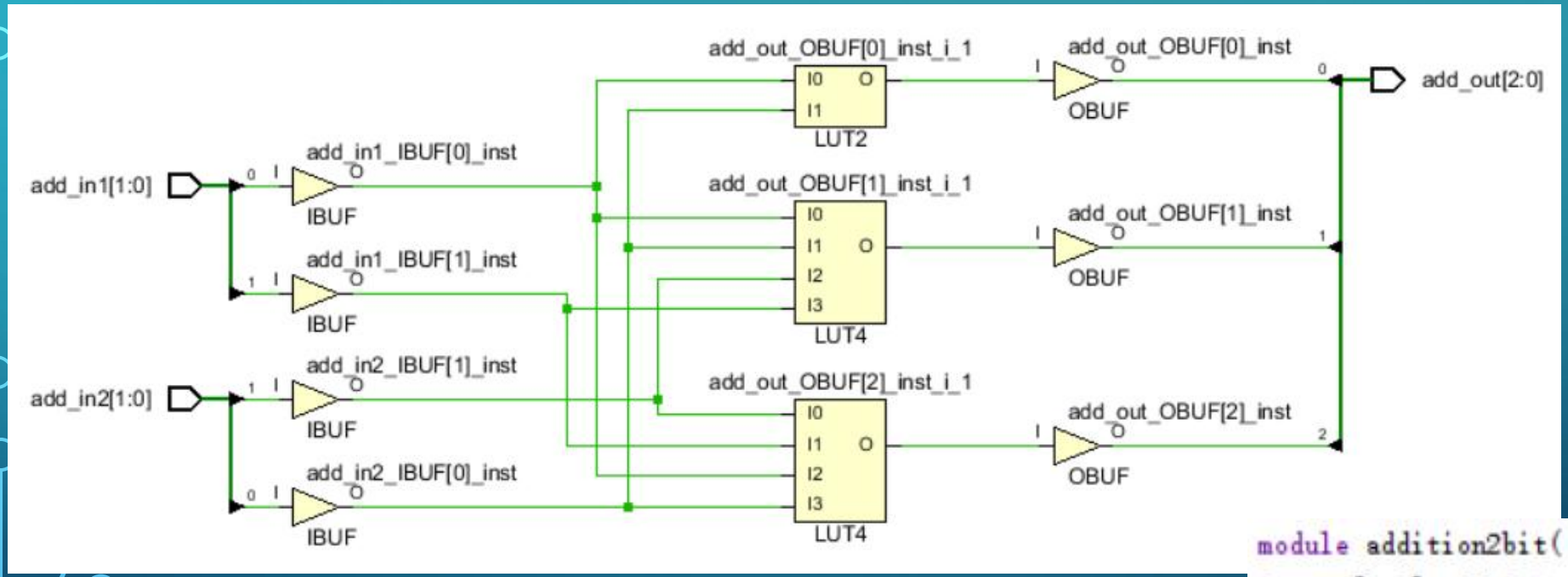
SCHEMATIC IN ‘RTL ANALYSIS’

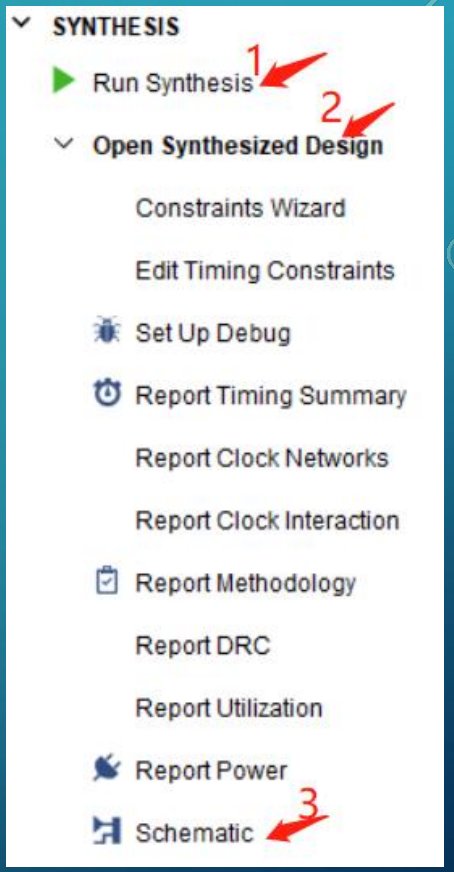
```
module lab3_df(
    input x,
    input y,
    output q1,
    output q2,
    output q3
    );
    assign q1 = x;
    assign q2 = x | (x & y);
    assign q3 = x & (x | y);

endmodule
```





SCHEMATIC IN 'SYNTHESIS'(1)

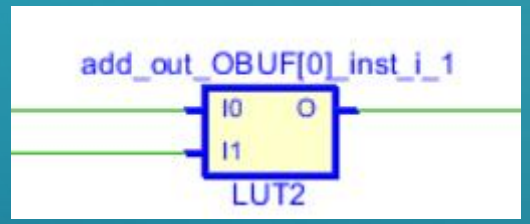




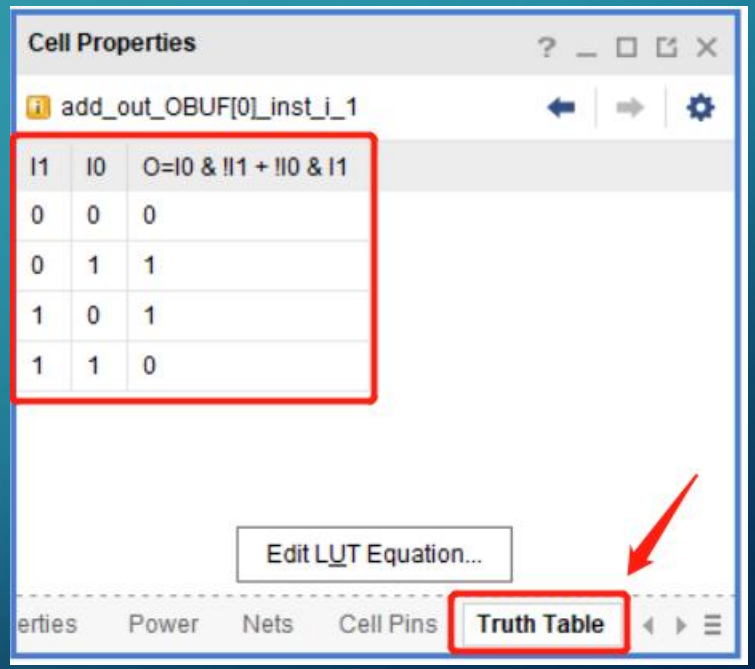

```
module addition2bit(
input [1:0] add_in1,
input [1:0] add_in2,
output [2:0] add_out
    );
    assign add_out = add_in1+add_in2;
endmodule
```

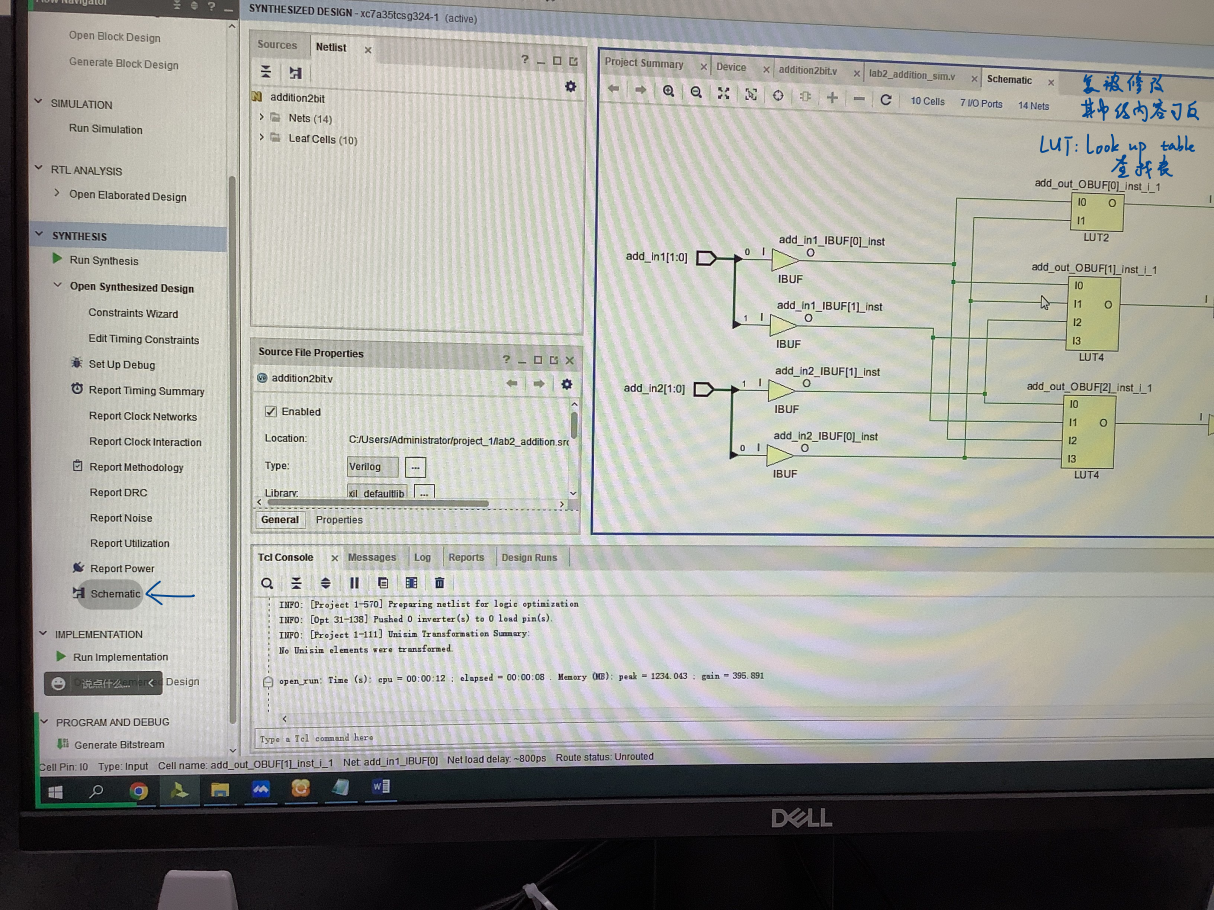
SCHEMATIC IN 'SYNTHESIS'(2)

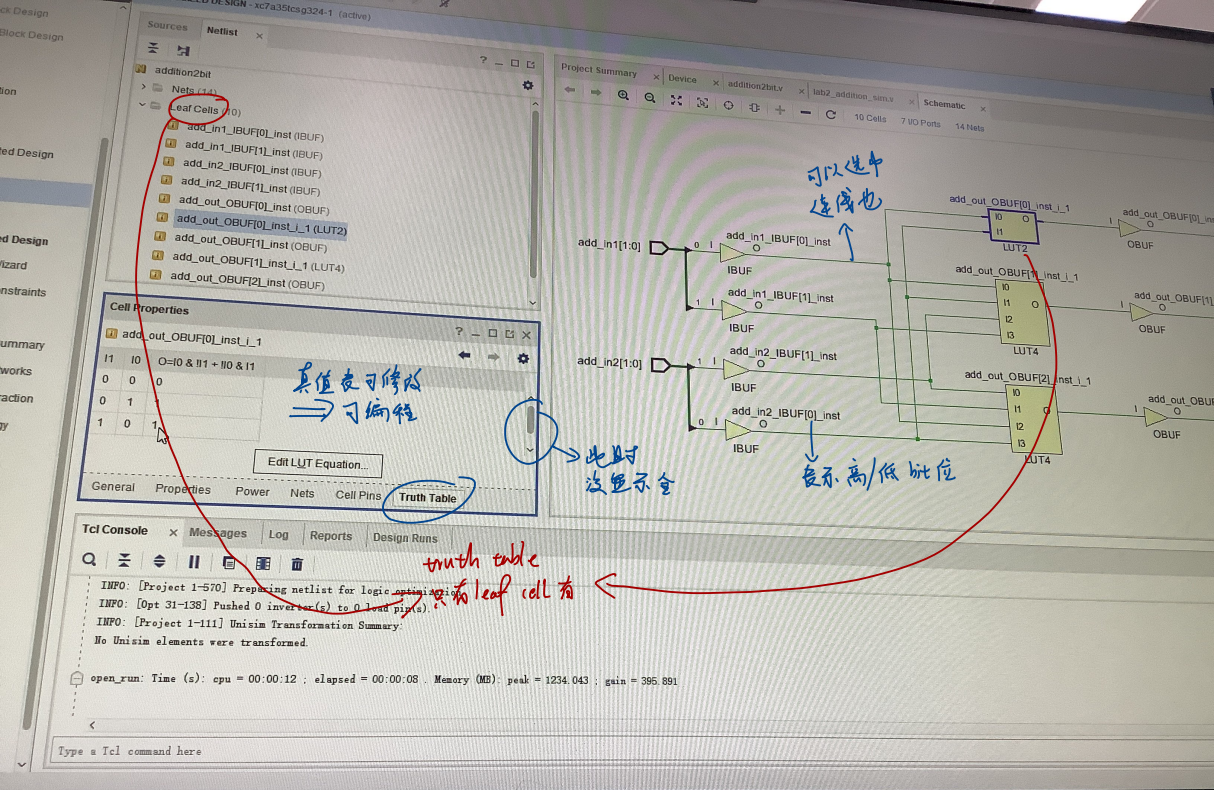
- **Double click** the LUT in schematic window

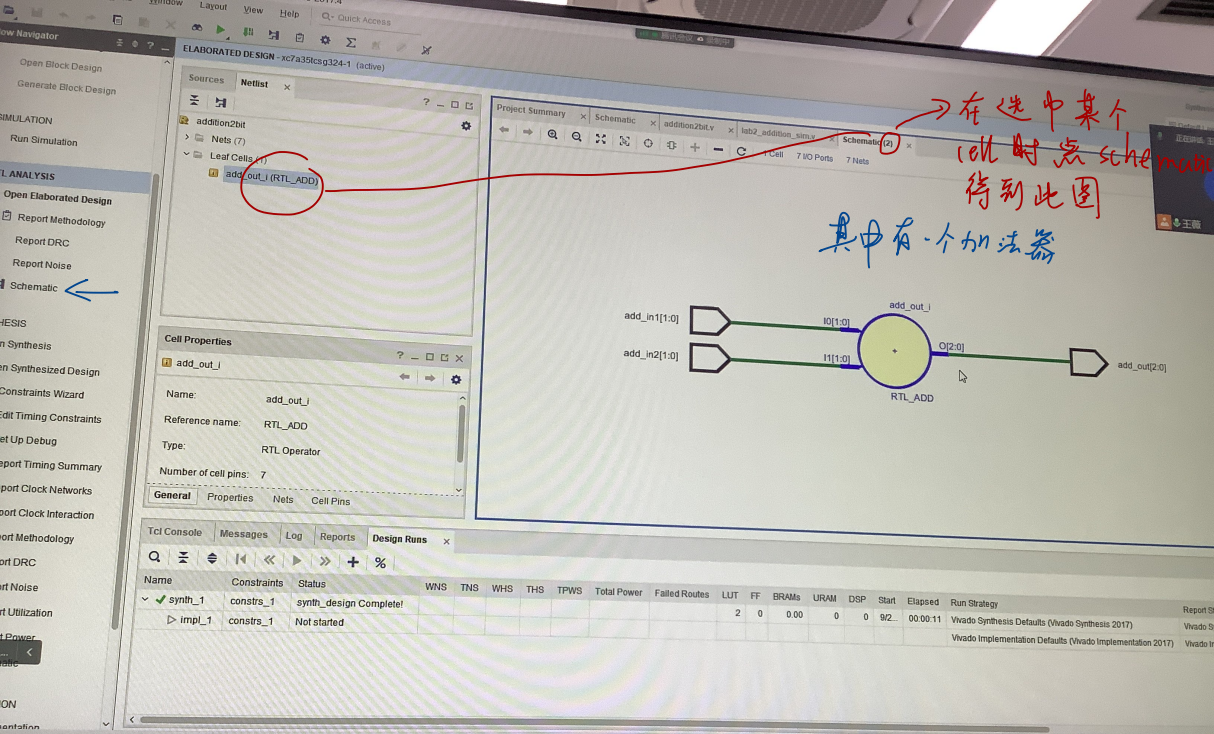


- In the '**Cell Properties**' window , choose '**Truth Table**' , the truth table of the cell is shown




Flow Navigator
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Design
PROGRAM AND DEBUG
Generate Bitstream
SYNTHESIZED DESIGN - xc7a35tcsg324-1 (active)
Sources
Netlist
addition2bit
Nets (14)
Leaf Cells (10)
Source File Properties
addition2bit.v
Enabled
Location:
C:/Users/Administrator/project_1/lab2_addition.sr
Type:
Verilog
Library:
xil_defaultlib
General
Properties
Project Summary
Device
addition2bit.v
lab2_addition_sim.v
Schematic
10 Cells
7 I/O Ports
14 Nets
LUT: Look up table
查找表
add_out_OBUF[0]_inst_i_1
LUT2
add_in1[1:0]
add_in1_IBUF[0]_inst
IBUF
add_in1_IBUF[1]_inst
IBUF
add_out_OBUF[1]_inst_i_1
LUT4
add_in2[1:0]
add_in2_IBUF[1]_inst
IBUF
add_in2_IBUF[0]_inst
IBUF
add_out_OBUF[2]_inst_i_1
LUT4
Tcl Console
Messages
Log
Reports
Design Runs
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
open_run: Time (s): cpu = 00:00:12 ; elapsed = 00:00:08 . Memory (MB): peak = 1234.043 ; gain = 395.891
Type a Tcl command here
Cell Pin: I0 Type: Input Cell name: add_out_OBUF[1]_inst_i_1 Net: add_in1_IBUF[0] Net load delay: ~800ps Route status: Unrouted


Sources
Netlist
addition2bit
Nets (14)
Leaf Cells (10)
add_in1_IBUF[0]_inst (IBUF)
add_in1_IBUF[1]_inst (IBUF)
add_in2_IBUF[0]_inst (IBUF)
add_in2_IBUF[1]_inst (IBUF)
add_out_OBUF[0]_inst (OBUF)
add_out_OBUF[0]_inst_i_1 (LUT2)
add_out_OBUF[1]_inst (OBUF)
add_out_OBUF[1]_inst_i_1 (LUT4)
add_out_OBUF[2]_inst (OBUF)
Cell Properties
add_out_OBUF[0]_inst_i_1
I1 I0 O=I0 & !I1 + !I0 & I1
0 0 0
0 1 1
1 0 1
Edit LUT Equation...
General Properties Power Nets Cell Pins Truth Table
真值表可修改
⇒可编程
此时
没显示全
Project Summary
Device
addition2bit.v
lab2_addition_sim.v
Schematic
10 Cells
7 I/O Ports
14 Nets
可以选中
连线也
add_in1[1:0]
add_in2[1:0]
add_in1_IBUF[0]_inst
add_in1_IBUF[1]_inst
add_in2_IBUF[1]_inst
add_in2_IBUF[0]_inst
IBUF
add_out_OBUF[0]_inst_i_1
add_out_OBUF[1]_inst_i_1
add_out_OBUF[2]_inst_i_1
LUT2
LUT4
OBUF
是否高/低 此位
Tcl Console
Messages
Log
Reports
Design Runs
truth table
和 leaf cell 有
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
open_run: Time (s): cpu = 00:00:12 ; elapsed = 00:00:08 . Memory (MB): peak = 1234.043 ; gain = 395.891
Type a Tcl command here


在选中某个
cell 时点 schematic
得到此图
其中有一个加法器
Sources
Netlist
addition2bit
Nets (7)
Leaf Cells (1)
add_out_i (RTL_ADD)
Project Summary
Schematic
addition2bit.v
lab2_addition_sim.v
Schematic (2)
1 Cell
7 I/O Ports
7 Nets
add_in1[1:0]
add_in2[1:0]
I0[1:0]
I1[1:0]
add_out_i
O[2:0]
add_out[2:0]
RTL_ADD
Cell Properties
add_out_i
Name: add_out_i
Reference name: RTL_ADD
Type: RTL Operator
Number of cell pins: 7
General
Properties
Nets
Cell Pins
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
Run Strategy
synth_1
constrs_1
synth_design Complete!
2
0
0.00
0
0
9/2...
00:00:11
Vivado Synthesis Defaults (Vivado Synthesis 2017)
impl_1
constrs_1
Not started
Vivado Implementation Defaults (Vivado Implementation 2017)
Open Block Design
Generate Block Design
Run Simulation
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic

PRACTICE1

- 1. Do the circuit design:
  - There are 3 inputs: x, y and z, 3 output: o1,o2 and o3(all of them are 1 bit width)
  - The logical expression between inputs and outputs are:

    o1= xyz+xyz’ , o2=xy(z+z’) , o3=xy

  Implement the circuit by using data flow
- 2. Get the schematic of the circuit in “RTL analysis” and “Synthesis” respectively, describe the differences between them.

PRACTICE1

- 3. create testbench, do simulation to verify function of the design.

  make your conclusion about the following the by using the waveform of simluation.

  xyz+xyz’ = xy(z+z’) = xy

- 4. generate bitstream file, test the circuit on the board
- 5. For 3 circuit : o1= xyz+xyz’, o2= xy(z+z’), o3= xy, Which circit is better,why ?