1. Description

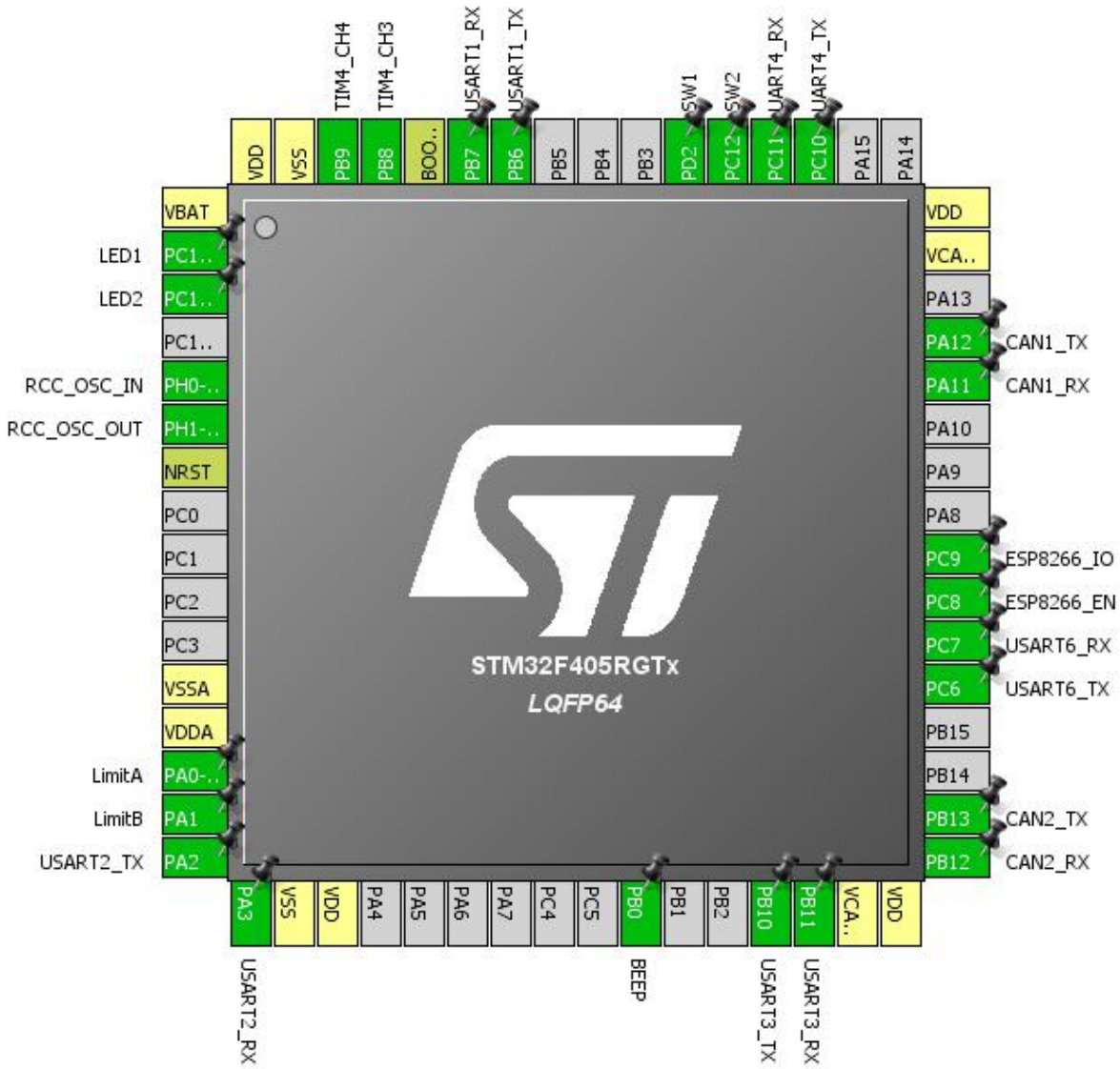
1.1. Project

Project Name	MainCTR
Board Name	MainCTR
Generated with:	STM32CubeMX 4.20.1
Date	07/10/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



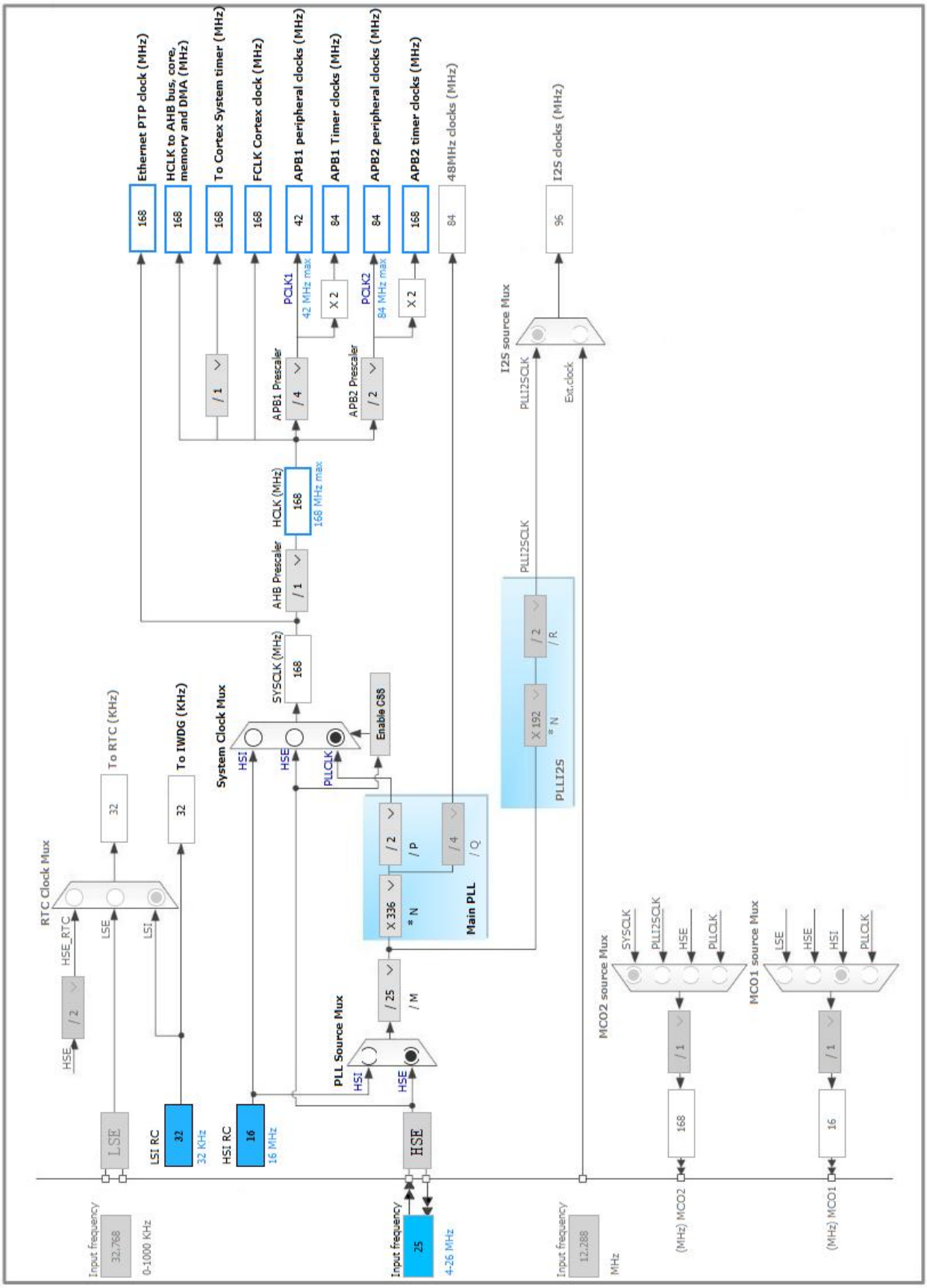
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Output	LED1
3	PC14-OSC32_IN *	I/O	GPIO_Output	LED2
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Input	LimitA
15	PA1 *	I/O	GPIO_Input	LimitB
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
26	PB0 *	I/O	GPIO_Output	BEEP
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VCAP_1	Power		
32	VDD	Power		
33	PB12	I/O	CAN2_RX	
34	PB13	I/O	CAN2_TX	
37	PC6	I/O	USART6_TX	
38	PC7	I/O	USART6_RX	
39	PC8 *	I/O	GPIO_Output	ESP8266_EN
40	PC9 *	I/O	GPIO_Output	ESP8266_IO
44	PA11	I/O	CAN1_RX	
45	PA12	I/O	CAN1_TX	
47	VCAP_2	Power		
48	VDD	Power		
51	PC10	I/O	UART4_TX	
52	PC11	I/O	UART4_RX	
53	PC12 *	I/O	GPIO_Input	SW2
54	PD2 *	I/O	GPIO_Input	SW1
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	PB8	I/O	TIM4_CH3	
62	PB9	I/O	TIM4_CH4	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. CAN1

mode: Mode

5.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
Time for one Bit	1000
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.2. CAN2

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
Time for one Bit	1000

ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.3. IWDG

mode: Activated

5.3.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	**32 ***
IWDG down-counter reload value	**1000 ***

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.5. SYS

Timebase Source: SysTick

5.6. TIM4

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3333-1 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**3332/2 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**3332/2 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM6

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**840-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.8. UART4

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART1

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.10. USART2

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.11. USART3

Mode: Asynchronous

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.12. USART6

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.13. FREERTOS

mode: Enabled

5.13.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.3

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	**30360 ***
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	**Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.13.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	**Enabled ***
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	**Enabled ***
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PC11	UART4_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART6	PC6	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PA0-WKUP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LimitA
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LimitB
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BEEP
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESP8266_EN
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESP8266_IO
	PC12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW2
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW1

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low
USART6_TX	DMA2_Stream6	Memory To Peripheral	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
UART4_RX	DMA1_Stream2	Peripheral To Memory	Low
UART4_TX	DMA1_Stream4	Memory To Peripheral	Low

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART6_TX: DMA2_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte

Memory Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_RX: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream2 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
CAN1 RX0 interrupts	true	5	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
USART3 global interrupt	true	5	0
UART4 global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	5	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
CAN2 RX0 interrupts	true	5	0
DMA2 stream6 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
USART6 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM4 global interrupt	unused		
CAN2 TX interrupts	unused		
CAN2 RX1 interrupt	unused		
CAN2 SCE interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Software Project

7.1. Project Settings

Name	Value
Project Name	MainCTR
Project Folder	F:\\\RM2018\\\MainCTR
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.13.0

7.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No