Lab 1 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Complete VHDL code for the design	_____	_____/05
Adequate commenting of the VHDL code	_____	_____/05
Successful software test bench run	_____	_____/10
Generate clean synthesized net list	_____	_____/05
Successful net list synthesis with synthesized test bench run	_____	_____/05
Total combinational functions = Total registers = Worst case setup time = Worst case delay from clock edge to output time = Worst case hold time = worst case path delay =		
Correct hardware behavior	_____	_____/05