Lab 3 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Initial Single cycle block diagram (use software to draw, dont copy from book or note, should include major blocks, all muxes, critical signal length and name)	_____	_____/12
Code for single cycle blocks (At minimum, you are required to have a complete controller that decodes all instructions which you should finish to recieve points)	_____	_____/10
Program 1: Correct behavior using sim to generate the product.	_____	_____/05
Program 2: Correct behavior using sim to generate multiple products.	_____	_____/05
Program 3: Correct behavior using sim to generate number of days (from December 14, 2012)	_____	_____/05
Program 1: Data stored in hardware memory address: **0x3FFC** is correct.	_____	_____/08
Program 2: Data stored in hardware memory address: **0x3FFC** is correct.	_____	_____/08
Program 3: Data stored in hardware memory address: **0x3FFC** is correct.	_____	_____/08
debug1.vhd successfully compiles	_____	_____/03
debug2.vhd successfully compiles	_____	_____/03

Predicted values of A,B,C,D,E,sel,
and $sel2$ in *debug3.vhd* are:
A=_____ B=_____ C=_____
D=_____ E=_____ sel=_____
$sel2$=_____

Why do the resulting signals have X's and U's
in them? Do any bits of the signal match? Why?

_____ _____/05

which lines can be changed to make it work
(comment what lines do):

_____ _____/03

Cause of the error in *debug4.vhd*:

_____ _____/03

Cause of the error in *debug5.vhd*:

_____ _____/03