Lab 4 Evaluation Sheet

Section:_____
Student Name:_____
Mg:_____

Lab Exercises	TA Initials	Score
Complete VHDL code for all CPU blocks	_____	_____/05
Modular Design	_____	_____/05
Student test benches for all CPU blocks (except controller)	_____	_____/05
Complete CPU block diagram	_____	_____/05
Simulation of source CPU passes tests: *test.loadstore.asm* *test.rtype.asm*	_____	_____/10
CPU synthesizes	_____	_____/10
Simulation of synthesized CPU passes tests: *test.loadstore.asm* *test.rtype.asm*	_____	_____/10
Hardware		
Correct behavior for *test.loadstore.asm*	_____	_____/10
Correct behavior for *test.rtype.asm*	_____	_____/10
Grading of submitted CPU design with TA grading script	_____	_____/50

Optional Bonus Points
use Logic Analyzer to probe one program execution in hardware on top level signals with LAcpu.vhd and LAcpuTest.vhd (provided on course website) as well as explainning the waveform on Logic Analyzer regardless if your Single Cycle is prefect. (note: Logic Analyzer User Manual is under "Links" on course web, it will be required to use Logic Analyzer to probe hardware in next pipeline project) _____/10