## **CprE 381 – Computer Organization and Assembly-Level Programming**

## Lab-03 Report

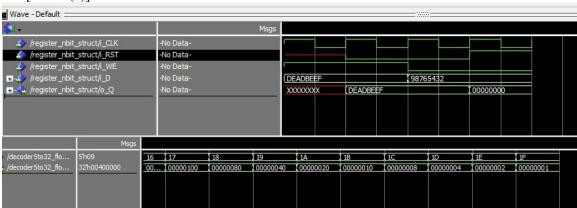
Student Name	
Section / Lab Time	

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

a. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?

3 register select lines each 5 bits 1 write enable 1 bit 1 32 bit input to store in a register 2 32 bit output lines clock

b. [Part 1 (c)] Waveform.

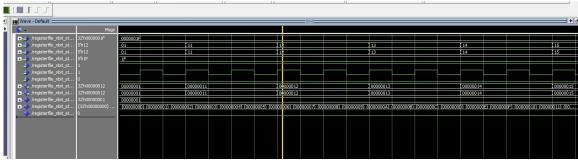


- e. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.
  - I wrote a nbit to 1 multiplexer. I did this so it will hopefully be reusable in furure designs. I did this in structual VHDL having n/2 muxs in a first row controlled by 1 bit that feed into another row which has n/4 muxs controlled by the next input. This is repeated for log2(N) rows. This allows any of the inputs to be selected.
- f. [Part 1 (g)] Waveform.



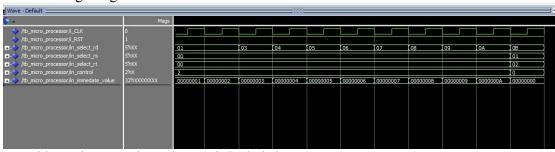
More data is in the corocponding mp4

- g. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).
- h. [Part 1 (i)] Waveform.



Note: a video of the code running the regFile.do is avaluable in the folder

- i. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).
- j. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.



A video going over the entire test is included

k. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	1	
Pencil/paper	1	2hour
design		
VHDL design		10-15
Assembly coding		0
Simulation		3
Debugging		15-20
Report writing		.5-75
Other:		
Total	2	Roughly 35 (3
		complete days)

ii. If you could change one thing about the lab experience, what would it be? Why?

This was 2-3 labs we were expected to do in 1 week. This is a 4 credit class. It is unreasonable to expect us to spend more then 40 hours a week on it. I know I am not the only one putting in such an unreasonable amount of time. This class is harming all of my other classes and I can feel it starting to affect my health.

iii. What was the most interesting part of the lab? I was really interested in getting the seeing the slowly building up of the processor, but after 37 hours I don't really care any more.