# CprE 381 – Computer Organization and Assembly-Level Programming

## Lab-04 Report

Student Name _____

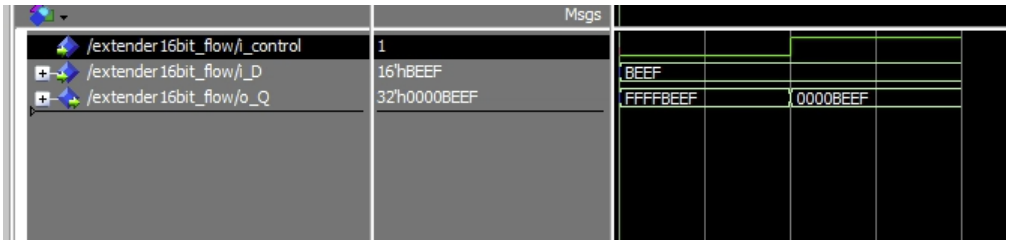
Section / Lab Time _____

***Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the Lab-04 instructions for the context of the following questions.***

a. [Part 1 (a)] What are the MIPS instructions that require some value to be sign extended? What are the MIPS instructions that require some value to be zero extended?
Every value that takes an immediate needs to have an extension of some kind because we are unable to pass in 32 bit immediate and the processor only works on 32 bit numbers. Anything with signed numbers needs to have sign extension and anything with unsigned number needs to have 0 extension.

b. [Part 1 (b)] what are the different 16-bit to 32-bit "extender" components that would be required by a MIPS processor implementation?
There would need to be an extender for the immediate values when they first come into the processor. Another one would also be needed when taking values out of the memory if you can do byte addressable.

c. [Part 1 (d)] Waveform.




d. [Part 2 (b)] Provide a 2-3 sentence description of each of the individual ports (both generic and regular).

Clk - This is just the basic clock signal. It should be plugged into the system clock
addr - This is the address of the 32 we want to write/read from
data - this is the value we are storing in the address
we - this lets us control if we write to the memory or not. 1 means write, 0 disables write
q - This is always the data stored in the address given by addr

e. [Part 2 (c)] Waveform.

See recording in recording folder

f. [Part 2 (d)] Briefly describe how the waveforms for this mem.vhd module differ from those that you analyzed as part of the pre-lab.

These differ in a couple ways. First is we have way more lines of memory so we are obviously better. We also don't have a byteenable because we can only access things in 32 bit chunks.

g. [Part 3 (a)] what control signals will need to be added to the simple processor from Lab #3? How do these control signals correspond to the ports on the mem.vhd component analyzed in problem 2)?

We will need to add 1 more control bit because we are now supporting 6 instructions. The only place where the control signal will directly affect the mem component is for the write enable command. In my implementation the memory will only be written to when ctl == 5. Otherwise the control signals will control the multiplex for the register input data, the add/sub control, register write enable, and the mux before the adder.

h. [Part 3 (b)] Draw a schematic of a simplified MIPS processor consisting only of the base components used in Lab #3, the extender component described in problem (1), and the data memory from problem (2).

see jpg in screenshot folder

i. [Part 3 (c)] Waveform.
Video in attached folder

j. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

| Task | During lab time | Outside of lab time |
|---|---|---|
| Reading lab | | 30 min |
| Pencil/paper design | | 2-4 |
| VHDL design | 2 | 10 |
| Assembly coding | | |
| Simulation | | 2 |
| Debugging | | 5 |
| Report writing | | 45 min |

| | | |
|---|---|---|
| Other: | | |
| Total | 2 | 20 |

ii. If you could change one thing about the lab experience, what would it be? Why?
I was happy with the amount of work for this lab. Still a lot but no longer “no longer care about anything” a lot.

iii. What was the most interesting part of the lab?
I’ve gotten better at efficient debugging which is nice.