CprE 381 – Computer Organization and Assembly-Level Programming

Lab-02 Report

Student Name _____

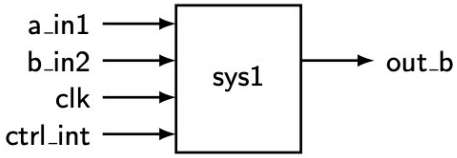
Section / Lab Time _____

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-02 instructions for the context of the following questions.

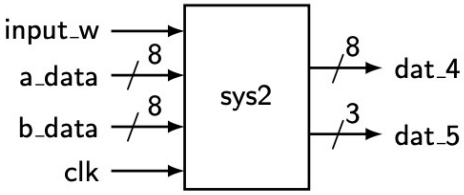
a. [Prelab] At the end of Chapter 3, answer questions 4b), 5a), and 6.

4. Write VHDL entity declarations that describe the following black-box diagrams:

a)



b)

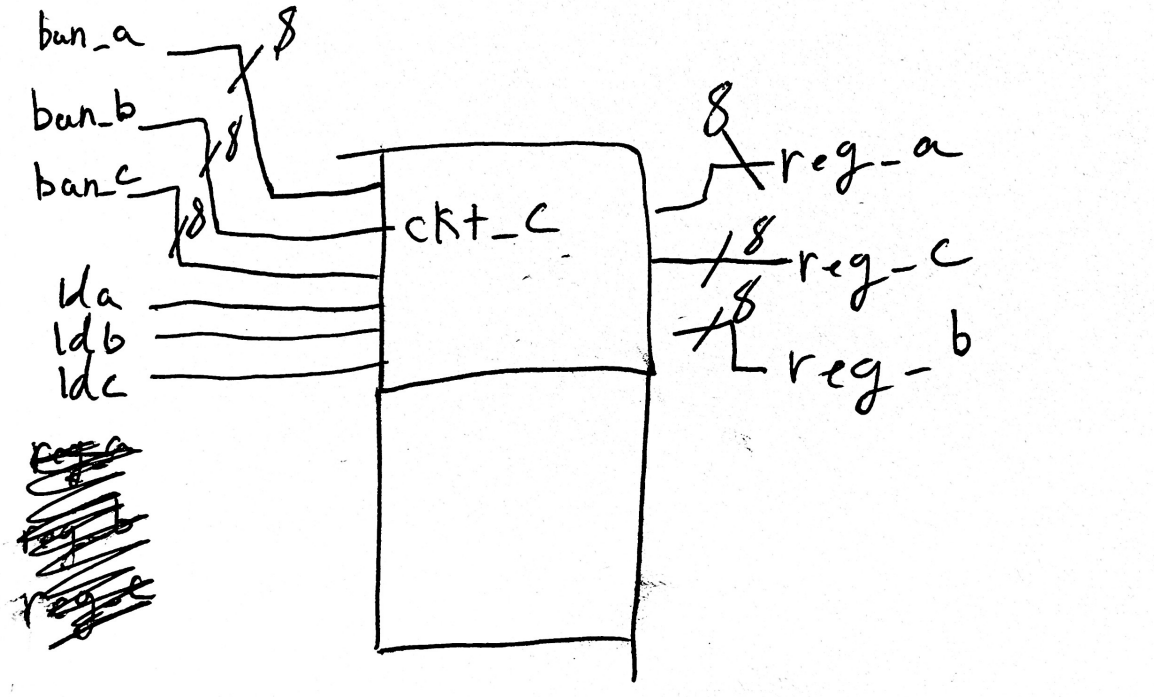



```
entity sys2 is
   port (
      input_w     : in std_logic;
      a_data      : in std_logic_vector(0 to 7);
      b_data      : in std_logic_vector(0 to 7);
      clik        : in std_logic;
      dat_4       : out std_logic_vector(0 to 7);
      dat_4       : out std_logic_vector(0 to 3);
   );
end sys2;
```

5. Provide black-box diagrams that are defined by the following VHDL entity declarations:

a)

```
entity ckt_c is
port (
    bun_a, bun_b, bun_c   : in    std_logic_vector(7 downto 0);
    lda, ldb, ldc         : in    std_logic;
    reg_a, reg_b, reg_c   : out   std_logic_vector(7 downto 0));
end ckt_c;
```



6. The following two entity declarations contain two of the most common syntax errors made in VHDL. What are they?

a)

```
entity ckt_a is
port (
    J,K : in  std_logic;
    CLK : in  std_logic
    Q   : out std_logic;)
end ckt_a;
```

b)

```
entity ckt_b is
port (
mr_fluffy   : in  std_logic_vector(15 downto 0);
mux_ctrl    : in  std_logic_vector(3 downto 0);
byte_out    : out std_logic_vector(3 downto 0);
end ckt_b;
```

A is missing a semicolon on line 4.
B is missing the end). There should be a ");" before the end ckt_b;

b. [Part 1 (c)] Waveform.

c. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux.

d. [Part 2 (e)] Waveform.

e. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder.

f. [Part 3 (e)] Waveform.

g. [Part 4 (a)] Draw a schematic (don't use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the 'nAdd_Sub' bit used?

h. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?

i. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

   i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab		
Pencil/paper design		
VHDL design		
Assembly coding		
Simulation		
Debugging		
Report writing		
Other:		
Total		

   ii. If you could change one thing about the lab experience, what would it be? Why?

   iii. What was the most interesting part of the lab?