

CprE 381 – Computer Organization and Assembly-Level Programming

Lab-02 Report

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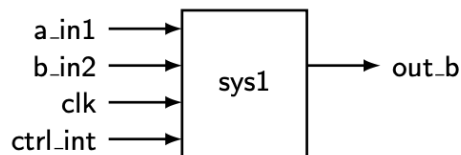
Section / Lab Time S7

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-02 instructions for the context of the following questions.

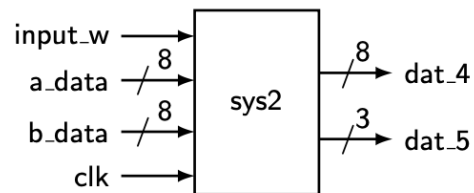
a. [Prelab] At the end of Chapter 3, answer questions 4b), 5a), and 6.

4. Write VHDL entity declarations that describe the following black-box diagrams:

a)



b)

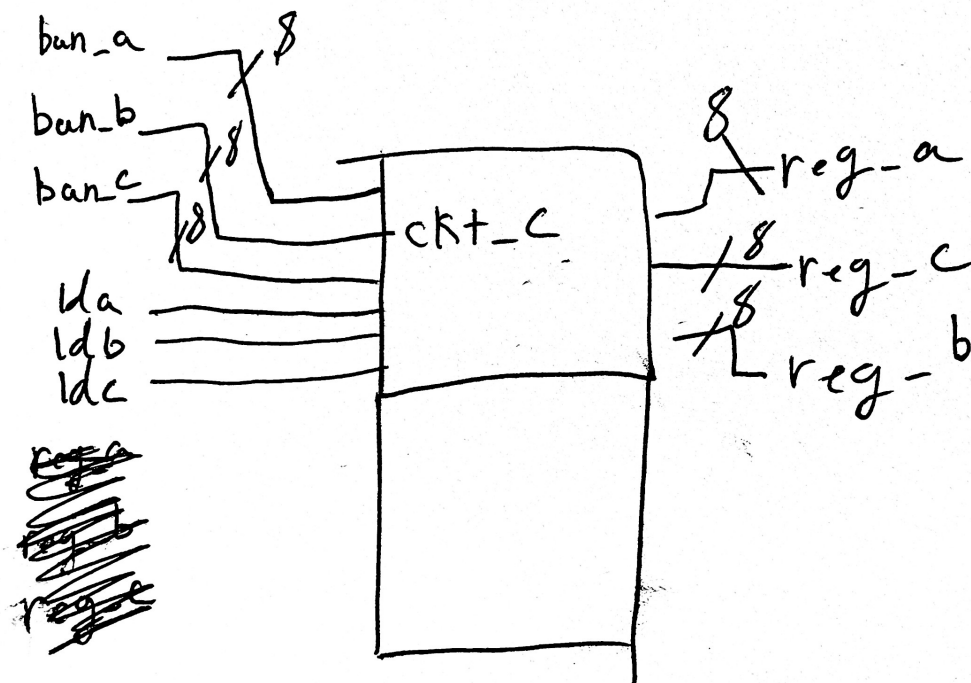


```
entity sys2 is
  port (
    input_w   : in std_logic;
    a_data    : in std_logic_vector(0 to 7);
    b_data    : in std_logic_vector(0 to 7);
    clk       : in std_logic;
    dat_4     : out std_logic_vector(0 to 7);
    dat_5     : out std_logic_vector(0 to 3);
  );
end sys2;
```

5. Provide black-box diagrams that are defined by the following VHDL entity declarations:

a)

```
entity ckt_c is
port (
  bun_a, bun_b, bun_c : in  std_logic_vector(7 downto 0);
  lda, ldb, ldc       : in  std_logic;
  reg_a, reg_b, reg_c : out std_logic_vector(7 downto 0));
end ckt_c;
```



6. The following two entity declarations contain two of the most common syntax errors made in VHDL. What are they?

a)

```
entity ckt_a is
port (
    J,K : in  std_logic;
    CLK : in  std_logic
    Q   : out std_logic;)
end ckt_a;
```

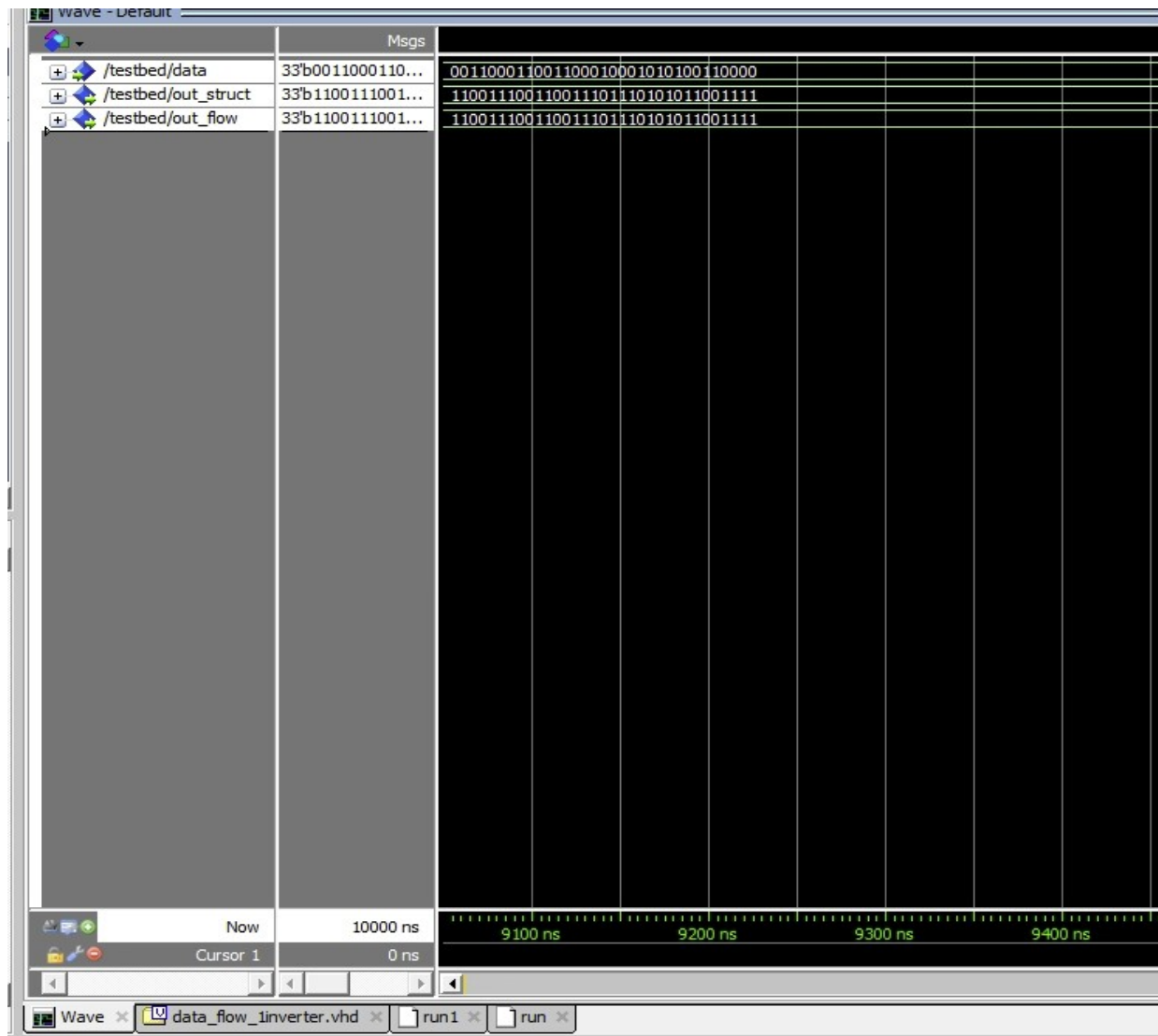
b)

```
entity ckt_b is
port (
mr_fluffy    : in  std_logic_vector(15 downto 0);
mux_ctrl     : in  std_logic_vector(3  downto 0);
byte_out     : out std_logic_vector(3  downto 0);
end ckt_b;
```

A is missing a semicolon on line 4.

B is missing the end). There should be a “);” before the end ckt_b;

b. [Part 1 (c)] Waveform.



- c. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux.

d. [Part 2 (e)] Waveform.

| | Msgs | | | | | |
|-------------------------|---------------|-----------|--|--|--|--|
| /mux_testbed/data_a | 33'h063311530 | 063311530 | | | | |
| /mux_testbed/data_b | 33'h031655765 | 031655765 | | | | |
| /mux_testbed/i_select | 0 | | | | | |
| /mux_testbed/out_struct | 33'h031655765 | 031655765 | | | | |
| /mux_testbed/out_flow | 33'h031655765 | 031655765 | | | | |

| | Msgs | | | | | |
|-------------------------|---------------|-----------|--|--|--|--|
| /mux_testbed/data_a | 33'h063311530 | 063311530 | | | | |
| /mux_testbed/data_b | 33'h031655765 | 031655765 | | | | |
| /mux_testbed/i_select | 1 | | | | | |
| /mux_testbed/out_struct | 33'h063311530 | 063311530 | | | | |
| /mux_testbed/out_flow | 33'h063311530 | 063311530 | | | | |

e. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder.

page 3 & 4 & 5 of drawings

f. [Part 3 (e)] Waveform.

| | | | | | |
|-------------------------------|------------|--------|--|--|--|
| /adder_testbed/i_a | 33'd604197 | 604197 | | | |
| /adder_testbed/i_b | 33'd75331 | 75331 | | | |
| /adder_testbed/i_carry | 1 | | | | |
| /adder_testbed/o_sum_struct | 33'd679529 | 679529 | | | |
| /adder_testbed/o_carry_struct | 0 | | | | |
| /adder_testbed/o_sum_flow | 33'd679528 | 679528 | | | |

- g. [Part 4 (a)] Draw a schematic (don't use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the 'nAdd_Sub' bit used?

Page 6 of drawings

- h. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?
- i.

| | Msgs | |
|-------------------------------|---------|-----|
| /add_sub_struct/i_a | 33'd80 | 80 |
| /add_sub_struct/i_b | 33'd37 | 37 |
| /add_sub_struct/i_select | 0 | |
| /add_sub_struct/o_sum | 33'd117 | 117 |
| /add_sub_struct/o_carry | 0 | |
| /add_sub_struct/inter_carry_1 | -33'd38 | -38 |
| /add_sub_struct/inter_carry_2 | 33'd37 | 37 |

| | Msgs | |
|-------------------------------|---------|-----|
| /add_sub_struct/i_a | 33'd80 | 80 |
| /add_sub_struct/i_b | 33'd37 | 37 |
| /add_sub_struct/i_select | 0 | |
| /add_sub_struct/o_sum | 33'd117 | 43 |
| /add_sub_struct/o_carry | 0 | |
| /add_sub_struct/inter_carry_1 | -33'd38 | -38 |
| /add_sub_struct/inter_carry_2 | 33'd37 | -38 |

| | Msgs | |
|-------------------------------|---------|-------------|
| /add_sub_struct/i_a | 33'd80 | 4294967295 |
| /add_sub_struct/i_b | 33'd37 | 4294967295 |
| /add_sub_struct/i_select | 1 | |
| /add_sub_struct/o_sum | 33'd43 | 0 |
| /add_sub_struct/o_carry | 1 | |
| /add_sub_struct/inter_carry_1 | -33'd38 | -4294967296 |
| /add_sub_struct/inter_carry_2 | -33'd38 | -4294967296 |

| | Msgs | |
|-------------------------------|-----------------|-------------|
| /add_sub_struct/i_a | 33'd4294967295 | 4294967295 |
| /add_sub_struct/i_b | 33'd4294967295 | 4294967295 |
| /add_sub_struct/i_select | 0 | |
| /add_sub_struct/o_sum | -33'd2 | -2 |
| /add_sub_struct/o_carry | 0 | |
| /add_sub_struct/inter_carry_1 | -33'd4294967296 | -4294967296 |
| /add_sub_struct/inter_carry_2 | 33'd4294967295 | 4294967295 |

| | Msgs | |
|-------------------------------|-----------------|---------|
| /add_sub_struct/i_a | 33'd4294967295 | -234887 |
| /add_sub_struct/i_b | 33'd4294967295 | -29521 |
| /add_sub_struct/i_select | 0 | |
| /add_sub_struct/o_sum | -33'd2 | -264408 |
| /add_sub_struct/o_carry | 0 | |
| /add_sub_struct/inter_carry_1 | -33'd4294967296 | 29520 |
| /add_sub_struct/inter_carry_2 | 33'd4294967295 | -29521 |

| | Msgs | |
|-------------------------------|-------------|---------|
| /add_sub_struct/i_a | -33'd234887 | -234887 |
| /add_sub_struct/i_b | -33'd29521 | -29521 |
| /add_sub_struct/i_select | 0 | |
| /add_sub_struct/o_sum | -33'd264408 | -205366 |
| /add_sub_struct/o_carry | 1 | |
| /add_sub_struct/inter_carry_1 | 33'd29520 | 29520 |
| /add_sub_struct/inter_carry_2 | -33'd29521 | 29520 |

- j. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

- i. How many hours did you spend on this lab?

| Task | During lab time | Outside of lab time |
|---------------------|--------------------|---------------------|
| Reading lab | 15 min | 10 min |
| Pencil/paper design | 10 min | 35 min |
| VHDL design | 45 min | 2 hours |
| Assembly coding | 0 | 0 |
| Simulation | 10 | 30 min |
| Debugging | 60 min | 4-5 hours |
| Report writing | 5 min | 15 min |
| Other: | | |
| Total | 2 and a half hours | 8 hours roughly |

- ii. If you could change one thing about the lab experience, what would it be? Why?

Less lab, split it into two.

- iii. What was the most interesting part of the lab?

The slowly building up was nice to see.