CprE 381 – Computer Organization and Assembly-Level Programming

Lab-03 Report

Student Name _____

Section / Lab Time _____

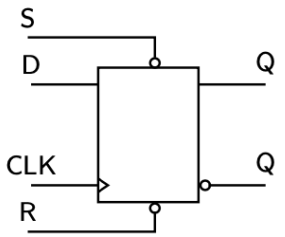
Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

a. [Prelab] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.

Provide a VHDL model of an 8-input OR gate using a process statement.

```
org8to1: process(in_1,in_2,in_3,in_4,in_5,in_6,in_7,in_8,) is
begin
    out <= in_1 or in_2 or in_3 or in_4 or in_5 or in_6 or in_7 or in_8;
end process org8to1;
```

EXERCISE 2. Provide a VHDL behavioral model of the D flip-flop shown on the right. The `S` and `R` inputs are an active low asynchronous preset and clear. Assume the `S` input takes precedence over the `R` input in the case where both are asserted simultaneously.




```
SRFlipFlop: proces (CLK, S,R,D)
begin
    if(S = '0') then
            Q <= '1'
    elseif (R = '0') then
            Q <= '0';
    elseif(rissing_edge(CLK)) then
            Q <= D;
    end if;
end proces SRFlipFlop
```

b. [Prelab, contract due at Lab-03 deadline] Project team assignment and completed contract.

c. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?

d. [Part 1 (c)] Waveform.

e. [Part 1 (d)] What type of decoder would be required by the MIPS register file and why?

f. [Part 1 (e)] Waveform.

g. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

h. [Part 1 (g)] Waveform.

i. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).

j. [Part 1 (i)] Waveform.

k. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).

l. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.

m. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

    i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab		
Pencil/paper design		
VHDL design		
Assembly coding		
Simulation		
Debugging		
Report writing		
Other:		
Total		

ii. If you could change one thing about the lab experience, what would it be? Why?

iii. What was the most interesting part of the lab?