CprE 381 – Computer Organization and Assembly-Level Programming

Lab-01 Report

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Section / Lab Time Thursday 2-4

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-01 instructions for the context of the following questions.

a. [Part 1 (b)] Reference the circuit diagram at the end of this document (some parts simplified). There are 33 labeled areas in the diagram. For 15 of these labels, specify where (VHDL file and line number) these values are located – some will be found in more than one place. Also attempt to explain the functionality of each label as it occurs in the code.

11, 15, & 24 – These are instances of the entire multiplier file. So everything within the file is this. It is also called or referenced in the Quadratic file on line 41, 66 for 11, 72 for 15, and 81 for 24.

6 is the iA input for mult1 and is referenced in the Quadratic file on line 68
7 is the iB input for mult1 and is referenced in the Quadratic file on line 69

12 is the iA input for mult2 and is referenced in the Quadratic file on line 74
13 is the iB input for mult2 and is referenced in the Quadratic file on line 75

16 is the iA input for mult3 and is referenced in the Quadratic file on line 83
17 is the iB input for mult3 and is referenced in the Quadratic file on line 84

8,9,10 are all internal components of the multiplier.

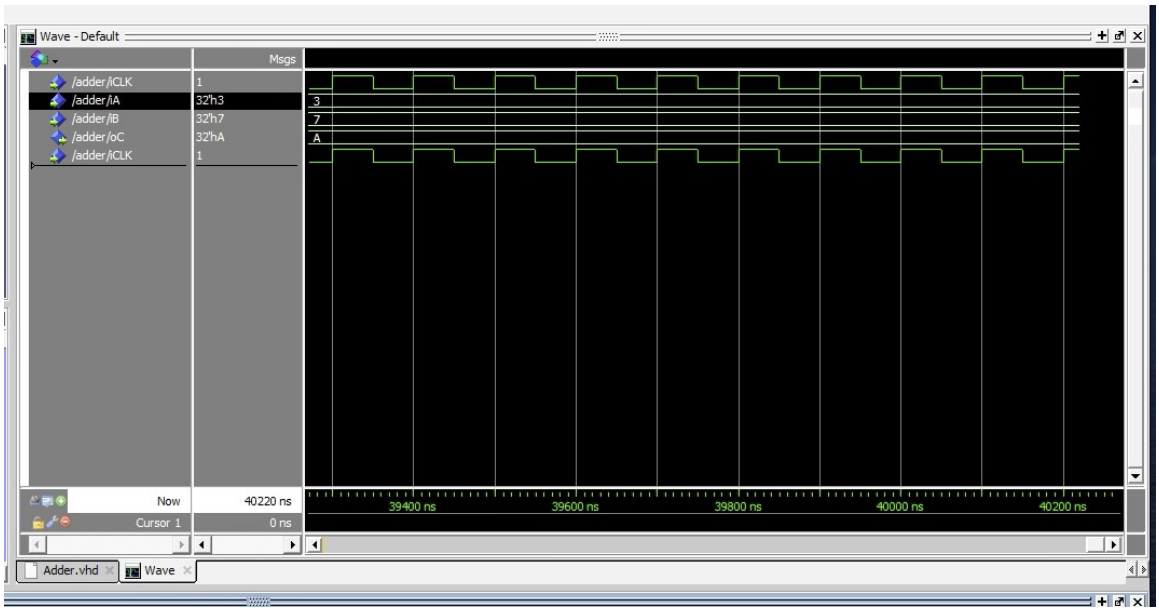
8 is what I think is an XOR gate on the two inputs and is found on line 41
9 is the flipflop so the output (10) only changes on the rising edge and is in the code as a if statement covering lines 40-42
10 is the output and it is created on line 31 and assigned on line 41

1-5 are all found in the quadratic file as inputs
they are declared on
1 is an arbitary constant declared on line 49
2: 25 this is a input
3 is an arbitary constant declared on line 50
4 is an arbitary constant declared on line 51
5 is the internal clock and first declared on line 24

These are then all reference at
1 cA – 68
2 iX – 69
3 cB never seems to be referenced
4 cC never seems to be referenced
5 ICLK – 35,42,67,68,73,82,88,97

b. [Part 1 (h)] In your report, provide a brief explanation of how the timing waveform corresponds to your understanding of the adder design.

This makes scene to me because it is taking my two inputs and adding them together and outputs them as oC. It also doesn't do it until there is a rising edge, which is hard to see from the screenshot. This is exactly what the code for the adder says.



c. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	10 min	15 min
Pencil/paper design	0	5 min
VHDL design	1:00	45 min
Assembly coding	0	0

Simulation	20 min	10
Debugging		
Report writing	5	0
Other:	0	0
Total	1:35	1:15

ii. If you could change one thing about the lab experience, what would it be? Why?
The remote is not great and I want to be able to see if this can be done locally, the problem is that I run mac, but since it is a java file hopefully I can make it work.

iii. What was the most interesting part of the lab?
Nothing hugely interesting, it was nice to figure out how the software works and see the implications for future labs.