CSCE-312 | Summer 2020 | Project3 – SEQUENTIAL CHIPS

Due Date: Submit on eCampus by Thursday, July 16th, 11:59 PM

Grading

(A) Project Execution [100%]:
You will be graded for correctness of the chips you have designed and coded. Your work will be drawn from the codes downloaded from eCampus and exercised using Nand2tetris software (Hardware Simulator). So, make sure to test and verify your codes before finally submitting on eCampus.

Deliverables & Submission

You need to turn in completed HDL, TST, CMP files as applicable for all the designed chips. Put your full name and UIN in the introductory comment present in each HDL code. Use relevant code comments and indentation. Also, include the cover sheet with your signature. Zip all the required files and the signed cover sheet into a compressed file *FirstName-LastName-UIN.zip* . Submit this zip file on eCampus.

Late Submission Policy: Refer to the Syllabus

Full Name: Quy Dao **Section:** 299 **UIN:** 427007909

Any assignment turned in without a fully completed cover page will NOT BE GRADED.

Please list all below all sources (people, books, web pages, etc) consulted regarding this assignment:

CSCE 312 Students	Other People	Printed Material	Web Material (URL)	Other
1.	1.	1. L 12	1. electronics org	1.
2.	2.	2.	2.	2.
3.	3.	3.	3.	3.

Please consult the Aggie Honor System Office for additional information regarding academic misconduct – it is your responsibility to understand what constitutes academic misconduct and to ensure that you do not commit it.

I certify that I have listed above all the sources that I consulted regarding this assignment, and that I have not received nor given any assistance that is contrary to the letter or the spirit of the collaboration guidelines for this assignment.

eCampus Submission Date: 07/16/2020

Printed Name (in lieu of a signature): Quy