

DesignWare VESA DSC Encoder and Decoder IP verview Presentation 70 Synopsys confide hird document, properties the best of t

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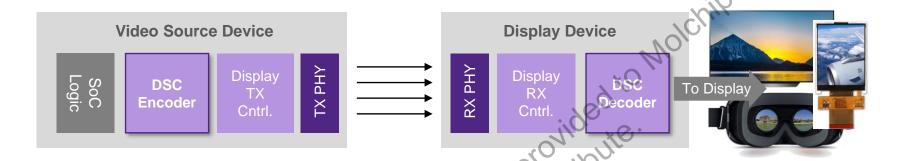
Display Market Trends

Synopsys confidential document provided to Molchip under NDA.



VESA DSC IP Increase Data rates 3x

Through visually lossless and real-time compression

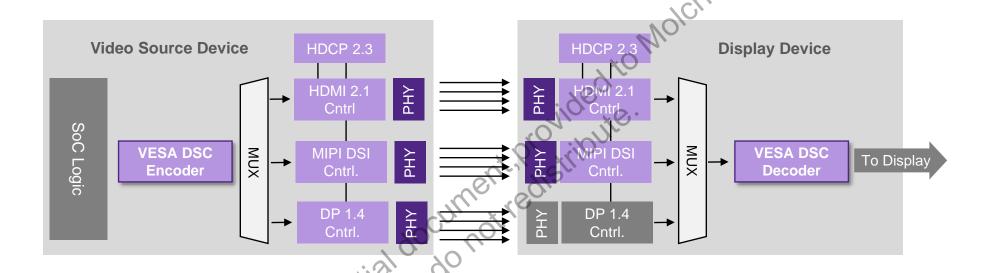


- Today's Consumers demand high definition, rich visual content across wide range of devices.
- Next generation products need to deliver higher resolutions, faster refresh rates
- The Bandwidth demands continue to push the limits of interface standards
- MIPI Alliance, HDMI Forum and VESA are aligned on compression standard: VESA DSC

VESA DSC increases data-rates 3x saving power and SoC resources VESA DSC compressed in real-time and is visually lossless

Complements Synopsys Display Interface Solutions

pre-integrated with HDMI v2.1 MIPI DSI and DisplayPort

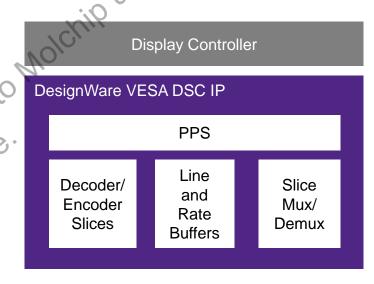


- Synopsys analog IP Synopsys digital IP
 - 3rd party IP

- Offers both VESA DSC 1.1 and 1.2a standards
- Interoperates with proven Synopsys HDMI, MIPI and DisplayPort Solutions
- Increase pixel throughput without need to redesign existing SoC architectures
- Able to share instance across different interfaces to further reduce power and area

VESA DSC Encoder and Decoder Features

- Supports all DSC video formats:
 - RGB, YCbCr, native 4:2:2/4:2:0, simple 4:2:2
- Supports latest interface standards:
 - HDMI 2.1, MIPI DSI, DisplayPort
- Configurable IP delivers low-power and small area
 - Multiple slice decoding: 1, 2, 4,8, 12, 16
 - Precision: 8, 10, 12, 14, 16 bits
 - Selection of coding schemes (MMAP, BP, MPP, ICH)
- Single Port RAM based buffers
- PPS (picture parameter set (PPS) programmable with APB-3 based register interface
- Error reporting for robust auto-recovery



VESA DSC Background

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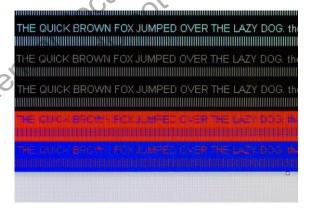
DSC Visually Lossless Compression

Artefacts are not visible to 'normal' observers

- Visually Lossless means that only information that is not visible is removed
- Scientifically tested with observer groups
- DSC keeps luminance part and reduces colors less visible to the human eye
- No Artefacts unlike other "Compression" approaches
 - Chroma Subsampling Out-of-Garmut Artefacts
 - JPEG block coding artifact



VESA DSC 10x amplified error picture (difference between original and decoded)



Chroma Subsampling Out-of-Gamut Artifact for 4:2:0 colored text



JPEG block coding compression artifact

VESA DSC Standard Differences

Synopsys provides DSC 1.1 and DSC 1.2a IP, VDC-M under planning

Features	DSC 1.1	DSC 1.2a	VDC-M 1.1		
Visually lossless compression performance	No.				
30 bit color	3.75:1 (8bpp)	3.75:1 (8bpp)	5:1 (6 bpp)		
24 bit color	3:1 (8bpp)	3:1 (8bpp)	4:1 (6 bpp)		
IC complexity	Low	Low	Medium		
Backward Compatibility	DSC 1.x	DSC 1.x	N/A		
Bits per color support	8/10/12	8/10/12/14/16	8/10/12		
High Dynamic Range ready	CUI Oth	✓	✓		
RGB and YCbCr 4:4:4 native encoding	70//	✓	✓		
YCbCr 4:2:0 and 4:2:2 native encoding	No	✓	✓		
Compliance test guidelines and test scripts	✓	✓	In development		
Adopted Standard	MIPI DSI 1.2	HDMI 2.1	MPI DSI-2 1.1		
557	DSI-2 1.0	VESA DP 1.4a			
"VOA	VESA eDP 1.4b				

Slicing done to reduce clock and power

Total Parallelization for Real-Time Compression

Slicing done to reduce clock and power

Total Parallelization for Real-Time Compression

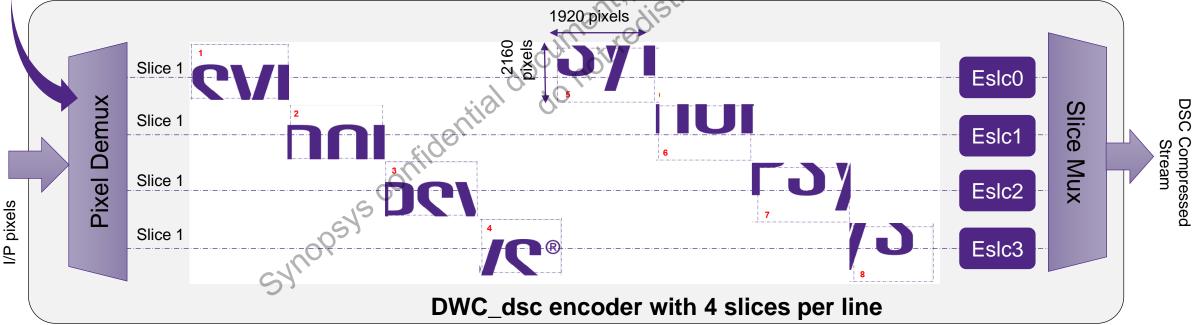
Slicing done to reduce clock and power

Total Parallelization for Real-Time Compression

Slicing done to reduce clock and power

Total Parallelization for Real-Time Compression

Total Parallelization fo 4320 pixels Slice 1 Slice 2 Slice 3 Slice 4 1920 pixels Slice 1 Eslc0



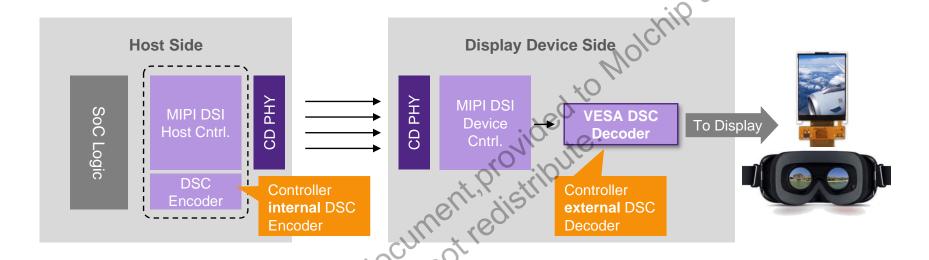
SNPS DSC IP for MIPI DSI and HDMI^{nder}v2.1

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MIPI DSI Saves Power and Resources with VESA DSC

Minimize integration risk by proven MIPI DSI solution



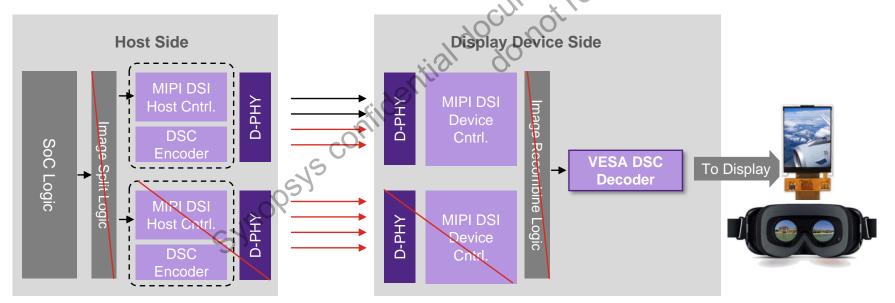
- Host Side offers a DSC Encoder internal to the DSI Host Controller
- Display Side offers the new DSC Encoder IP readily interoperable with the MIPI DSI Device Controller*
- VESA DSC 1.1 reduces bandwidth needs 3x

^{*} See roadmap for interop schedule details

VESA DSC Reduced the number of MIPI DPHY Lanes

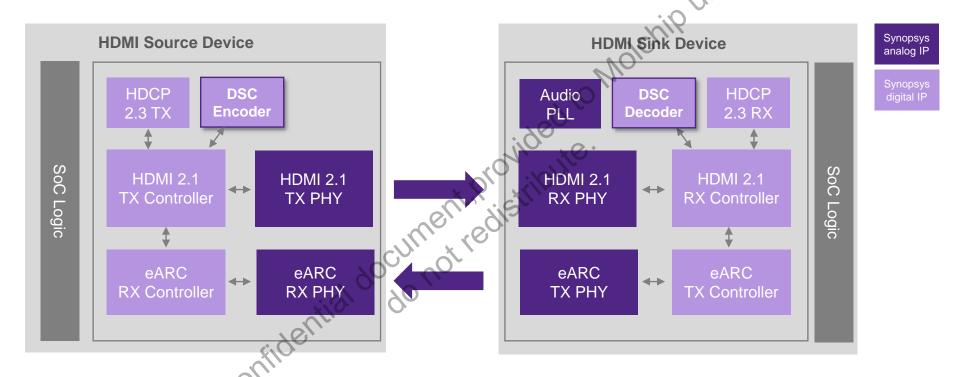
Saving Power, Area and reduce EMI

DPHY 1.2	1chille						
Resolution	FHD (1080x1920)	WQHD (1440x2560)	WQXGZ (1600x2560)	UHD (2160x3840)	WQUXGA (2400x3840)	5K (2880x5120)	8K (4320x8192
Bandwidth	3.58Gbps	6.37Gbps	7.08Gbps	14.33Gbps	15.93Gbps	25.49Gbps	61.16Gbps
No compression	2 lanes	3 lanes	3 lanes	6 or 8 lanes	8 lanes	N/A	N/A
2 x compression	1 lanes	2 lanes	2 lanes	3 lanes	4 lanes	6 or 8 lanes	N/A
3 x compression	1 lane	2 lanes	1 lanes	2 lanes	3 lanes	4 lanes	N/A



HDMI Achieves Higher Refresh and Resolutions with VESA DSC

Minimize integration risk by well integrated HDMI v2.1 solutions



- New DSC Encoder IP readily interoperable with the HDMI RX Solution (Solution contains DSC, TX Cntrl., HDCP 2.3, eARC, Audio PLL, PHYs)
- VESA DSC 1.2 increases pixel bandwidth 3x, thus allows highest refresh (120Hz) and resolutions (beyond 8K)

^{*} See roadmap for interop schedule details



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