Name_____ Student ID □□□□□□□□□□ School_____ Major/Class_____ Seat No._____

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WARNING: MISBEHAVIOR AT EXAM TIME WILL LEAD TO SERIOUS CONSEQUENCE.

SCUT Final Exam

Electric Circuits and Electronics Exam Paper A （2020-2021-1）

Notice: **1. Make sure that you have filled the form on the left side of seal line.**
2. Write your answers on the exam paper.
3. This is a close-book exam.
4. The exam with full score of 100 points lasts 120 minutes.

Question No.	I	II	III	IV	V	VI	VII	VIII	Sum
Score									

INSTRUCTIONS TO CANDIDATES

Using **calculator** is allowed during the examination.

$e \approx 2.72$

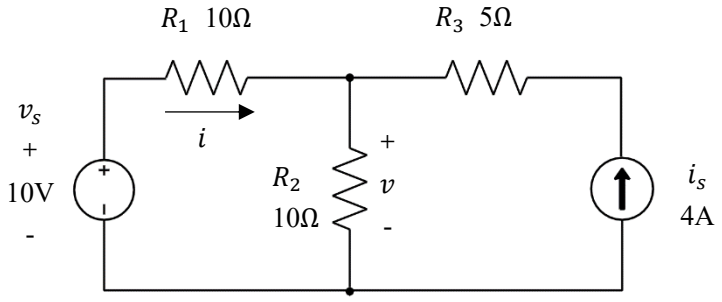
For Bipolar Junction Transistors:

At room temperature, $V_T \cong 0.026\text{V}$

For MOSFETs:

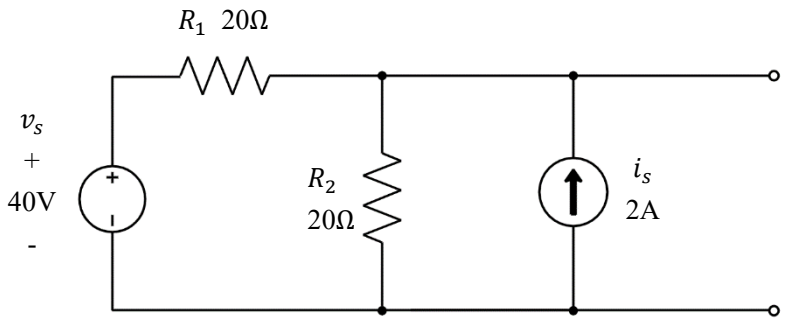
$$K = \left(\frac{W}{L}\right)\frac{KP}{2} \quad \text{and} \quad g_m = 2\sqrt{KI_{\text{DQ}}}$$

I. Consider the circuit shown in the following figure, find the values of v and i. **10**



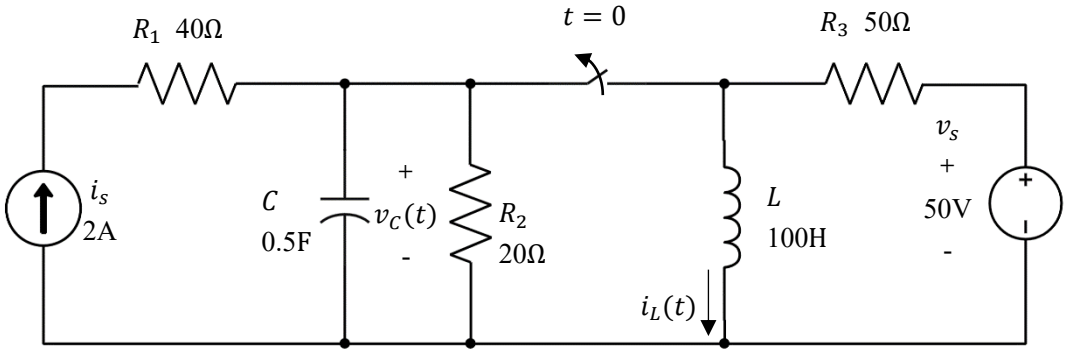
II. Find the Thévenin and Norton equivalent circuit of the following circuit and calculate the maximal output power $P_{\max}$ of the terminal.

10



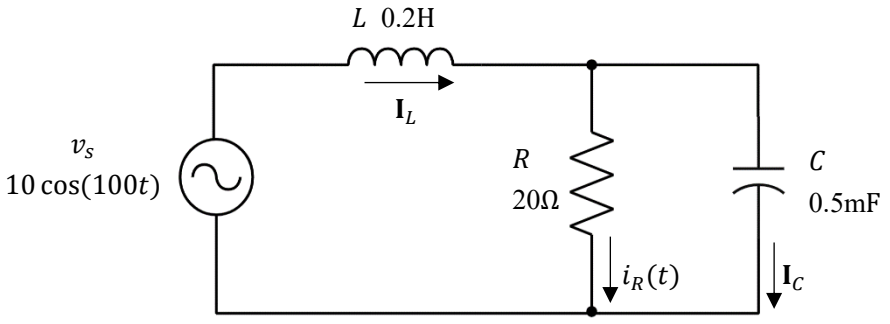
III. The following circuit is operating in steady state with the switch close prior to $t = 0$. Find the expression for $v_C(t)$ when $t < 0$ and $t \geq 0$. Calculate the voltage $i_L(t)$ when $t = 1$s.

10



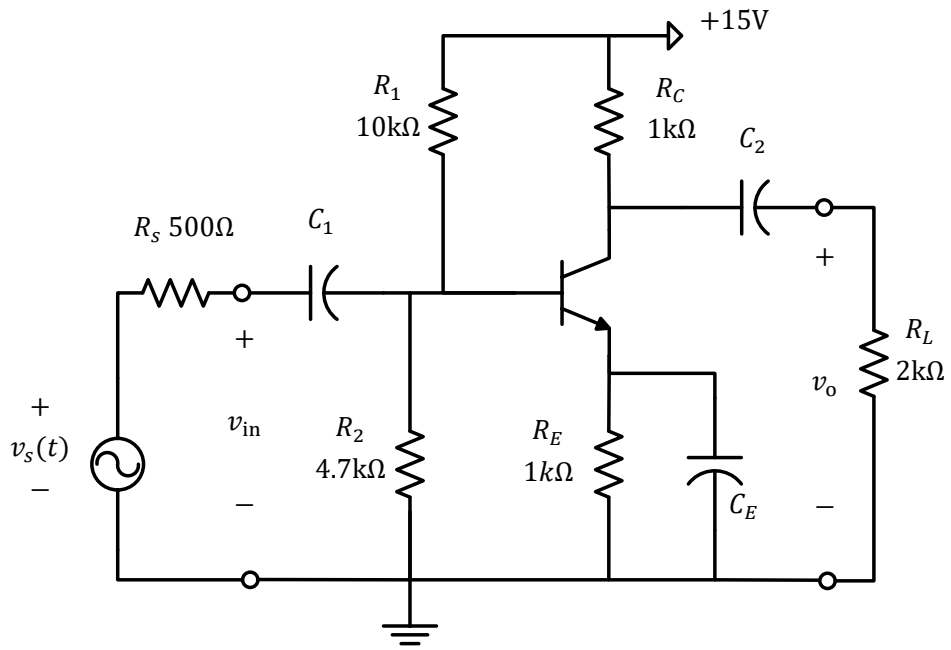
IV. Consider the circuit shown in the following figure. Find the phasors $\mathbf{I}_L$ and $\mathbf{I}_C$, and $i_R(t)$.

10



V. Consider the common-emitter amplifier shown in the following figure.

Total 20



The BJT transistor has $\beta = 300$ and $V_{BEQ} = 0.7V$.

a) Draw the bias circuit to determine the Q point and calculate the values of I_{CQ}, find the value of r_π.

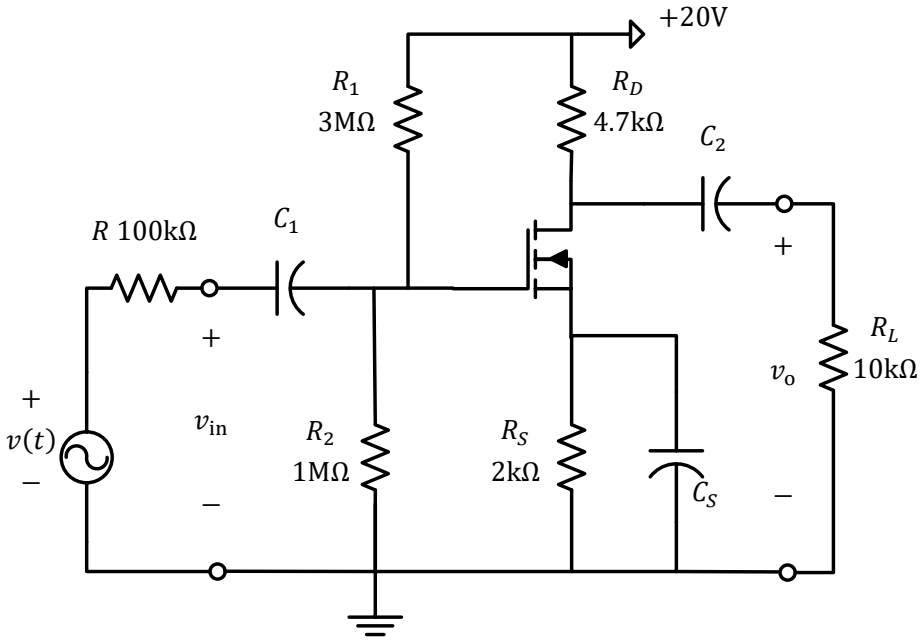
10

b) Draw the small signal equivalent circuit and calculate the voltage gain A_v, input impedance Z_{in}, output impedance Z_o, and power gain G, assuming that the coupling capacitors are short circuits for the ac signal.

10

VI. Consider the common-source amplifier shown in the following figure.

Total 20



The NMOS transistor in the above figure has $KP = 50\mu A/V^2$, $L = 20\mu m$, $W = 400\mu m$, $V_{to} = 2V$, and $r_d = \infty$.

a) Draw the bias circuit to determine the Q point and calculates the values of I_{DQ}, V_{GSQ}, and g_m.

10

b) Draw the small signal equivalent circuit and compute the voltage gain A_v, input impedance Z_{in}, output impedance Z_o, and power gain G, assuming that the coupling capacitors are short circuits for the ac signal.

10

VII. Design a PID controller using Op-amp based on the following equation:

10

$$v_o = 3v_{in}(t) + 5\int_0^t v_{in}(t)dt + 2\frac{dv_{in}(t)}{dt}$$

VIII. Construct a Karnaugh map for the logic function:

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D}$$

Find the minimal sum of product expression, and implement the logic circuit.

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I.

II.

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