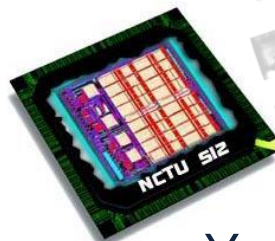


APRII: THINGS TO DO AFTER LAYOUT

NYCU-EE IC LAB FALL 2024



Lecturer: Yen-Ning Tung

Outline

- ✓ **Power Verification**
- ✓ **Bonding Pads Insertion Flow**
- ✓ **Cell-Based Design Flow Review**



Outline

- ✓ **Power Verification**
- ✓ Bonding Pads Insertion Flow
- ✓ Cell-Based Design Flow Review



Power Component

✓ Dynamic Power

✓ Switching Power

- $P = 0.5 * C_L V^2 F * A$,
- C_L : output capacitance loading, V: voltage, F: frequency
- A: average switching activity from VCD or computed
- Charge and discharge the loading capacitive

✓ Internal Power (Short circuit power)

- Both NMOS and PMOS are turned on
- Calculated using *.lib file

✓ Static Power

✓ Leakage Power

- Power consumed by device when no switching
- Calculated using *.lib file

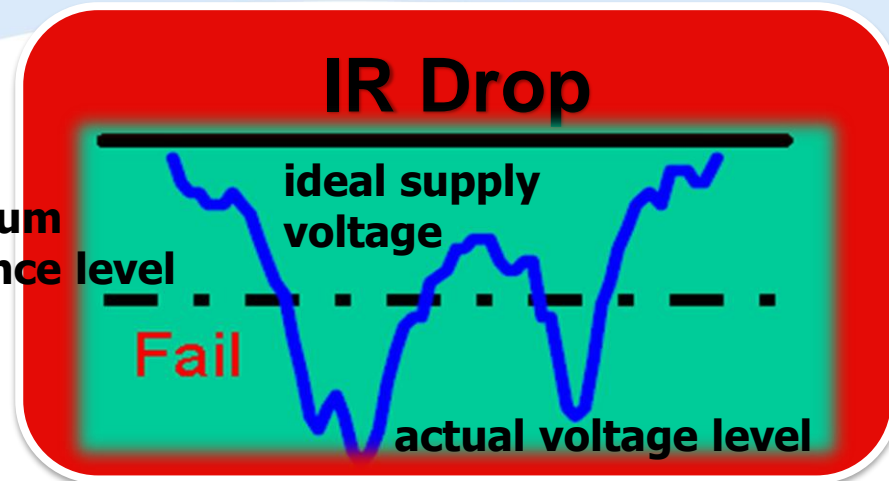


Power Verification - Introduction

✓ IR Drop

- Average or Instantaneous Power Issue

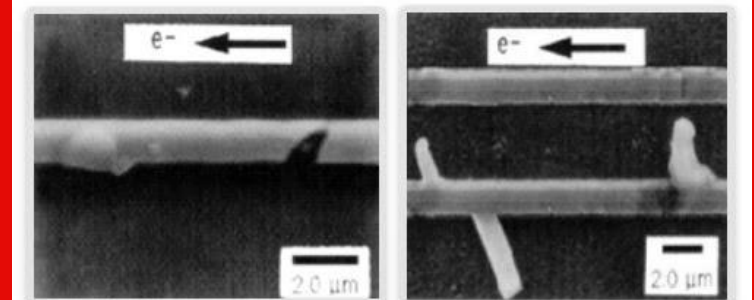
minimum
tolerance level



✓ Electromigration(EM)

- Long Term Power Density Problem

Electromigration(EM)

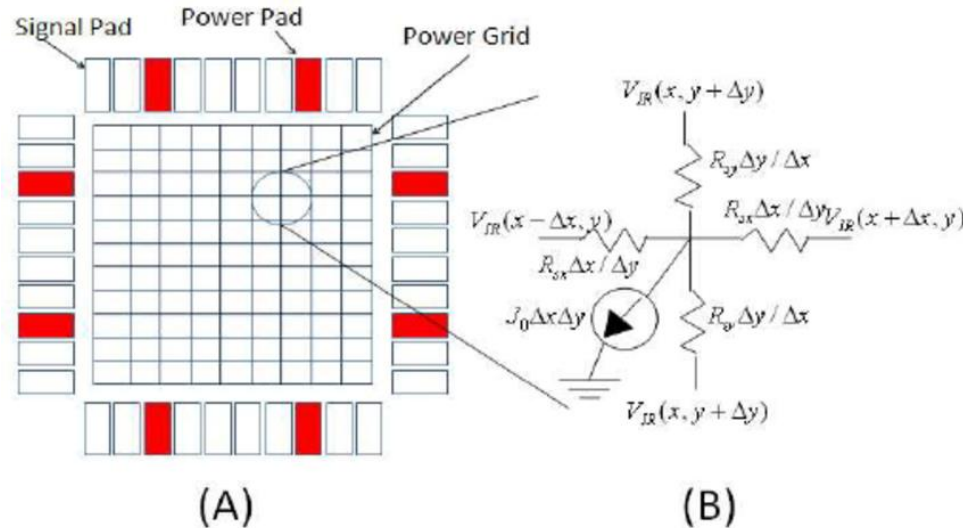


IR Drop (1/3)

✓ Power issue

— IR drop (IRD)

- IR drop is the problem of voltage drop of the power and ground due to high current flowing through the power-ground resistive network
- The drop in supply voltage over the length of the supply line



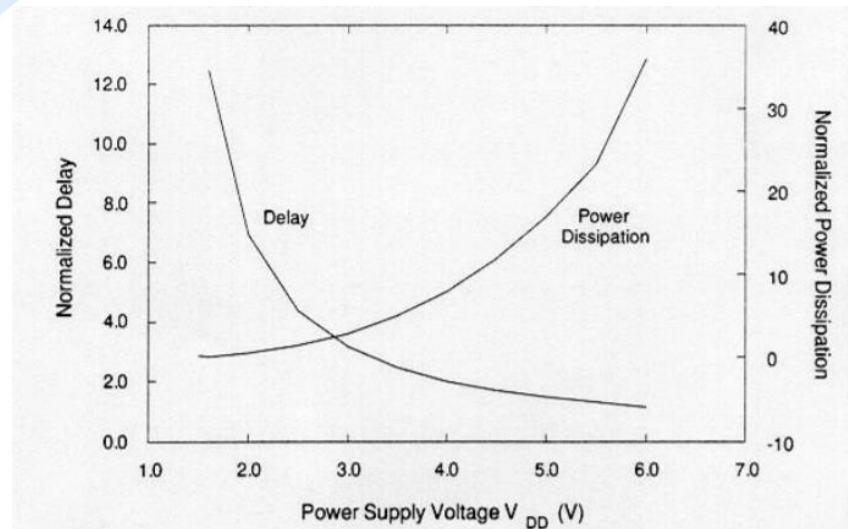
(A) I/O Pad Location and Power Distribution
(B) node model in the grid

IR Drop (2/3)

✓ Power issue

— IR drop (IRD)

- When there are excessive voltage drops in the power network or voltage rises in the ground network, **the device will run at slower speed**



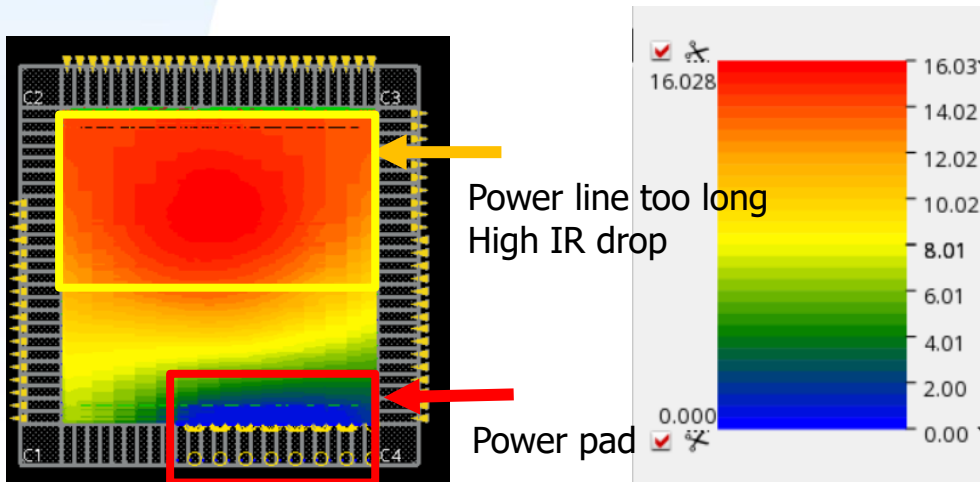
- As the process becoming more and more advanced, the IR drop turns to be an important issue.
- IR drop can cause the chip to fail due to
 - ◆ Performance (circuit running slower than specification)
 - ◆ Functionality problem (setup or hold violations)
 - ◆ Unreliable operation (less noise margin)

Power Verification - Introduction

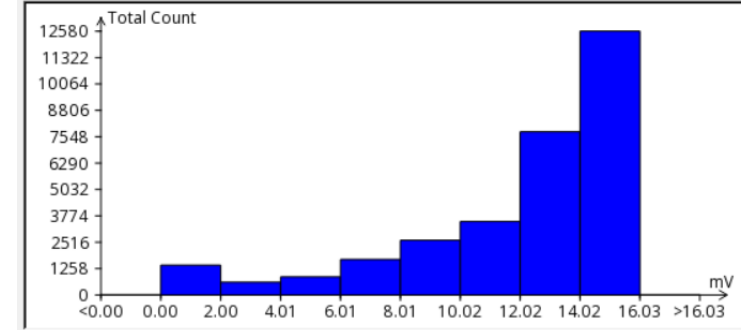
✓ Power issue

— IR drop (IRD)

- Prevention:
 1. Adding stripes to avoid IR drop on cell's power line
 2. Change the position of power pad to avoid long power line
 3. Use square-shaped Chip to avoid long power line
 4. Add decoupling cell



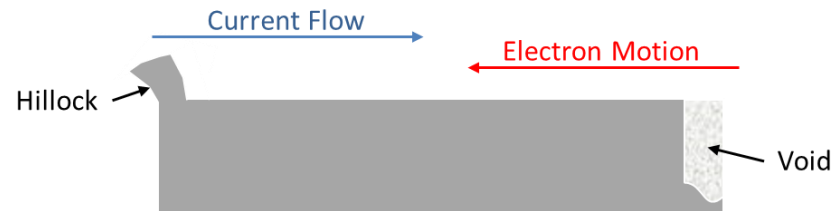
Range	Total Count	Displayed / Scissored
> 16.03 mV	1	1 / 0
16.03 ~ 14.02 mV	12584	12584 / 0
14.02 ~ 12.02 mV	7782	7782 / 0
12.02 ~ 10.02 mV	3503	3503 / 0
10.02 ~ 8.01 mV	2611	2611 / 0
8.01 ~ 6.01 mV	1693	1693 / 0
6.01 ~ 4.01 mV	864	864 / 0
4.01 ~ 2.00 mV	609	609 / 0
2.00 ~ 0.00 mV	1424	1424 / 0
< 0.00 mV	0	0 / 0



Electro-Migration

✓ Electro-Migration (EM)

- EM is the unwanted transport of material due to movement of ions in a conductor, caused by a transfer of momentum from electrons to these ions.
- High-density current in a narrow metal wire may destroy the wire
- Performance Degradation
 - Increase/decrease in wire RC
- Can result in catastrophic failure
 - Open
 - Short
- EM analysis solution
 - Calculates the current on each wire and compares it to foundry EM rules.



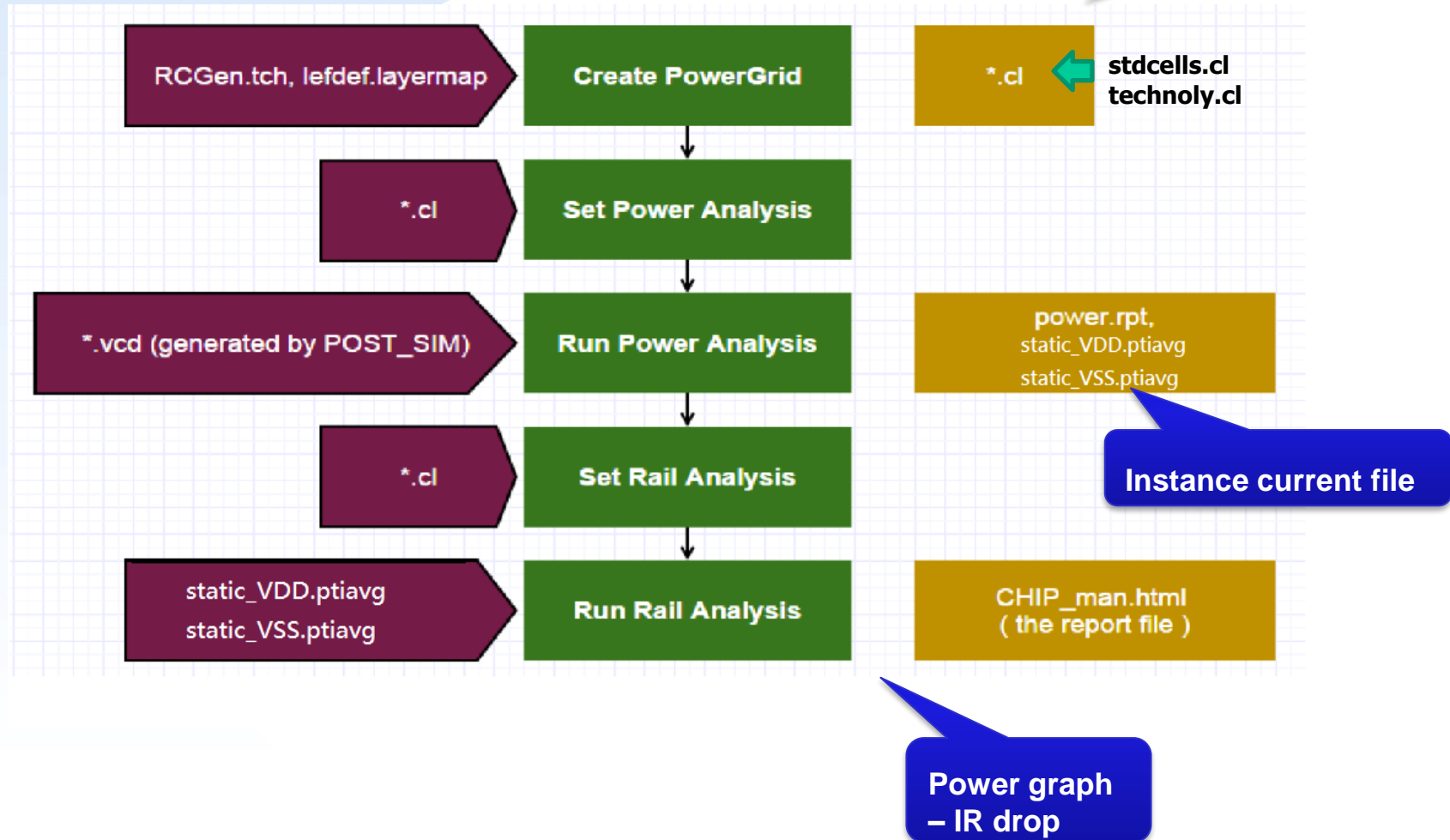
Power Analysis - Method

- ✓ **Vector: simulation waveform result for all gates**
- ✓ **Vector-based**
 - Uses VCD (waveform file)
 - VCD is waveform file, like fsdb
 - Requires:
 - Simulation is possible at the full-chip level
 - Simulation provides sufficient functional coverage of design
 - Vectors include those cause highest power consumption
- ✓ **Vector-independent**
 - Uses TWF (timing window file, generated by Static Timing Analysis)
 - Clock domain, skews, slack, arrival times of each pin.
 - Requires:
 - A good estimation of input switching frequency



Power/Rail Analysis flow

PG library
contains:
Tap location
Tap capacitance
Tap current



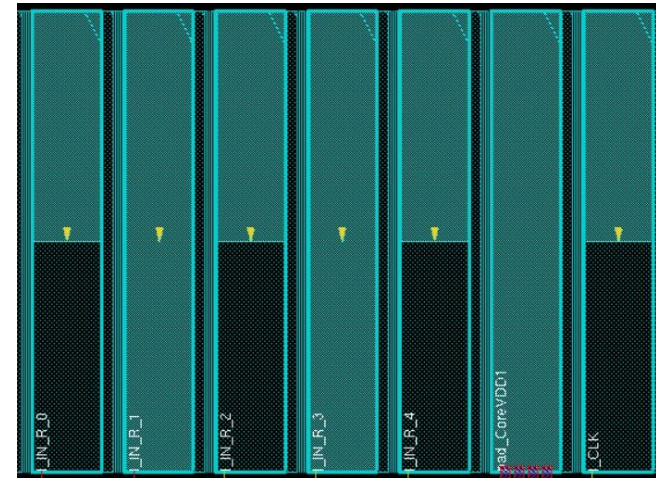
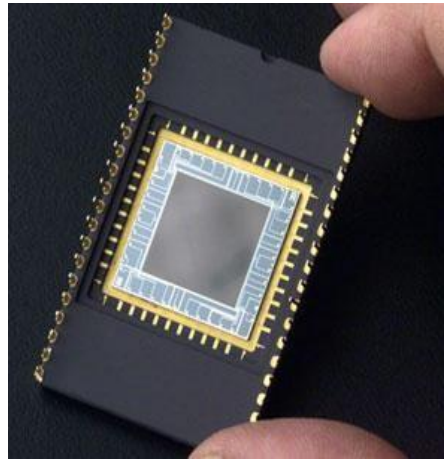
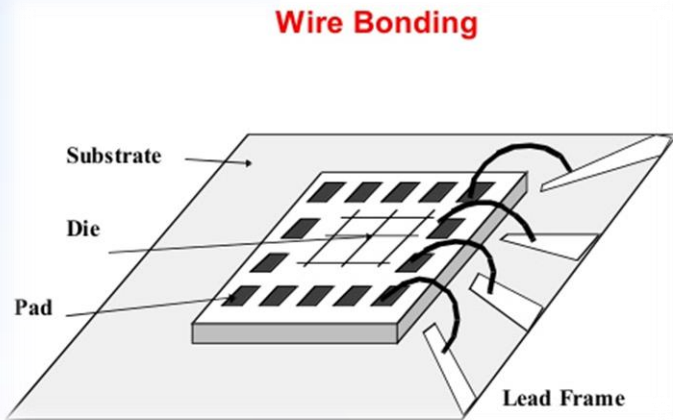
Outline

- ✓ Power Verification
- ✓ **Bonding Pads Insertion Flow**
- ✓ Cell-Based Design Flow Review



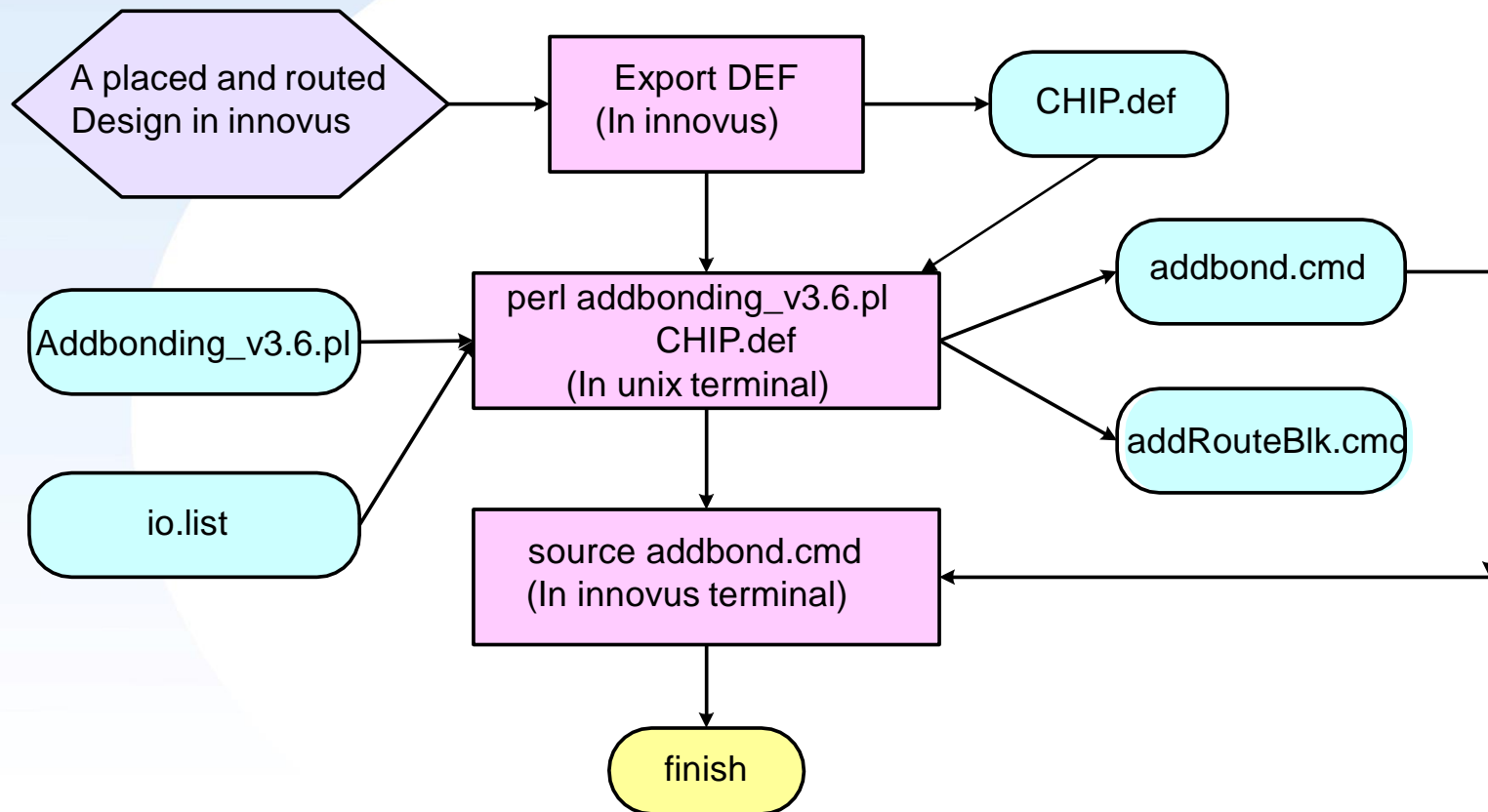
Bonding pads

- A bonding pad is used to connect the circuit on a die to a pin on a packaged chip
- Typically, the bonding pad is made from all the metal layers stacked on top of each other and connected through vias



Bonding pads insertion flow

Flow & Script provided by manufacturer



Outline

- ✓ Power Verification
- ✓ Bonding Pads Insertion Flow
- ✓ **Cell-Based Design Flow Review**
 - LEF Files (.lef)
 - Library Files (.lib)



Data Preparation overview

✓ Library files

- Timing libraries (LIB)
 - fsa0m_a_generic_core_ff1p98vm40c.lib
 - fsa0m_a_generic_core_ss1p62v125c.lib
 - fsa0m_a_t33_generic_io_ff1p98vm40c.lib
 - fsa0m_a_t33_generic_io_ss1p62v125c.lib
- Physical libraries (LEF)
 - fsa0m_a_generic_core.lef
 - fsa0m_a_t33_generic_io.lef
 - FSA0M_A_GENERIC_CORE_ANT_V55.lef
 - FSA0M_A_T33_GENERIC_IO_ANT_V55.lef
 - BONDPAD.lef
- RC extraction
 - u18_Faraday.CapTbl
 - icecaps.tch

- CeltIC libraries
 - u18_ss.cdb
 - u18_ff.cdb
- GDSII layout
 - umc18.gds
 - umc18io3v5v_6lm.gds

✓ Timing constraint files

- Generate timing constraint files from Design Compiler
 - `dc_shell-t> write_sdc CHIP.sdc`

✓ Design netlist files

- Synthesized design netlist
 - `designName_SYN.v`
- Chip design netlist (combine designName_SYN.v & CHIP_SHELL.v)
 - `CHIP_SYN.v`
- IO pad location file
 - `CHIP.io`



Introduction of LEF Files

✓ What is lef ?

- Library Exchange Format (LEF)
- LEF defines the elements of an IC process technology and associated library of cell models.
- LEF file can be divide into two part: technology and physical macros

✓ Technology

- A technology LEF file contains all of the LEF technology information for a design, such as placement and routing design rules, and process information for layers.

✓ Physical Macros

- ✓ – Contains the macro and standard cell information for a design.



Technology LEF file

✓ Process Technology

- Layers
 - Poly
 - Metal
 - Via
- Design rule
 - Net width
 - Net spacing
 - Area
- /*Parasitic
 - Resistance
 - Capacitance*/

```
LAYER met1
TYPE
ROUTING ;
WIDTH 0.240 ;
MAXWIDTH 9.0 ;
AREA 0.1764 ;
THICKNESS 0.528 ;
....
....
END met1
```

```
SPACING
SAMENET met1 met1 0.240 ;
SAMENET met2 met2 0.280
STACK ;
...
END SPACING
```

```
SITE umc6site
SYMMETRY
y ; CLASS
CORE ;
SIZE 0.660 BY 5.040 ;
END umc6site
```

```
[VERSION statement]
[BUSBITCHARS statement]
[DIVIDERCHAR statement]
[UNITS statement]
[MANUFACTURINGGRID statement]
[USEMINSPACING statement]
[CLEARANCEMEASURE statement ;]
[PROPERTYDEFINITIONS statement]
[LAYER (Nonrouting) statement
| LAYER (Routing) statement] ...
[SPACING statement ]
[MAXVIASTACK statement] [VIA
statement] ...
[VIARULE statement] ...
[VIARULE GENERATE statement] ...
[NONDEFAULTRULE statement] ...
[SITE statement] ...
[BEGINEXT statement]
... [END LIBRARY]
```

✓ APR Technology

- Site
- Pitch
- Default direction
- Via rule



Pitch

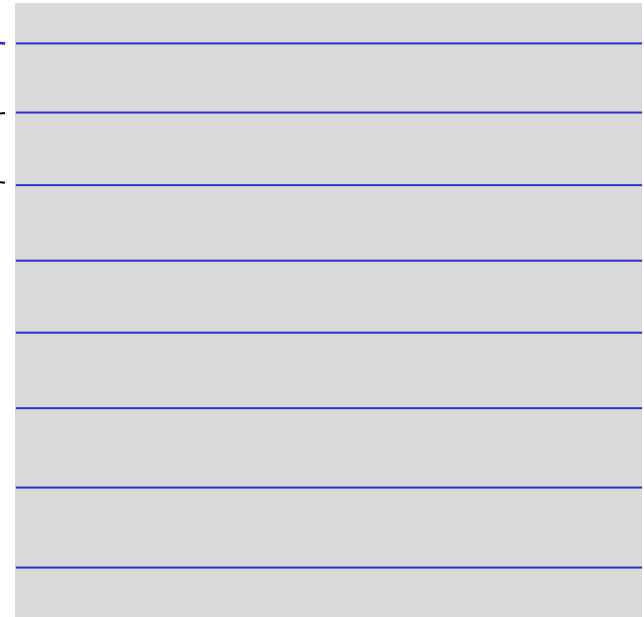
✓ Pitch

- The distance between routing grids
- Reduce routing complexity
- Avoid DRC violation



Routing Grid

pitch



Cell library LEF file

✓ Define physical data for

- Standard cells
- I/O pads
- Memories
- Other hard macros

✓ Describe abstract shape

- A cell library LEF file can include any of the statements as shown in right hand side

```
MACRO
macroName [
CLASS
{ COVER [BUMP]
| RING
| BLOCK [BLACKBOX | SOFT]
| PAD [INPUT | OUTPUT | INOUT | POWER | SPACER | AREAIO]
| CORE [FEEDTHRU | TIEHIGH | TIELOW | SPACER | ANTENNACELL | WELLTAP]
| ENDCAP {PRE | POST | TOPLEFT | TOPRIGHT | BOTTOMLEFT | BOTTOMRIGHT}
} ;]
[FOREIGN foreignCellName [pt [orient]] ;] ...
[ORIGIN pt ;]
[EEQ macroName ;]
[SIZE width BY height ;]
[SYMMETRY {X | Y | R90} ... ;]
[SITE siteName [sitePattern] ;] ...
[PIN statement] ...
[OBS statement] ...
[DENSITY statement] ...
[PROPERTY propName propVal ;] ...
END macroName
```



Introduction of LIB Files

- ✓ The units, operation conditions and template table are defined in the begin of LIB file

```
library (NangateOpenCellLibrary) {  
  /* Documentation Attributes */  
  date      : "Thu 10 Feb 2011, 18:11:58";  
  revision  : "revision 1.0";  
  comment   : "Copyright (c) 2004-2011 Nangate Inc. All Rights Reserved.";  
  
  /* General Attributes */  
  technology      : (cmos);  
  delay_model     : table_lookup;  
  in_place_swap_mode : match_footprint;  
  library_features : (report_delay_calculation,report_power_calculation);  
  
  /* Units Attributes */  
  time_unit      : "1ns";  
  leakage_power_unit : "1nW";  
  voltage_unit    : "1V";  
  current_unit    : "1mA";  
  pulling_resistance_unit : "1kohm";  
  capacitive_load_unit : (1,ff);  
  
  /* Operation Conditions */  
  nom_process      : 1.00;  
  nom_temperature  : 125.00;  
  nom_voltage      : 0.95;  
  
  voltage_map (VDD,0.95);  
  voltage_map (VSS,0.00);  
  
  define(process_corner, operating_conditions, string);  
  operating_conditions (slow) {  
    process_corner : "SlowSlow";  
    process        : 1.00;  
    voltage        : 0.95;  
    temperature    : 125.00;  
    tree_type      : balanced_tree;  
  }  
  default_operating_conditions : slow;  
  
  lu_table_template (Timing_7_7) {  
    variable_1 : input_net_transition;  
    variable_2 : total_output_net_capacitance;  
    index_1 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
    index_2 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
  }  
}
```



Introduction of LIB Files

✓ LIB file contains

- Cell area
- Cell Leakage power
- Rise and fall capacitance of pins
- Timing information
- Internal power

```
/** *****  
Module      : AND2_X1  
Cell Description : Combinational cell (AND2_X1) with drive strength X1  
*****  
  
cell (AND2_X1) {  
  
    drive_strength      : 1;  
  
    area                : 1.064000;  
    pg_pin(VDD) {  
        voltage_name : VDD;  
        pg_type      : primary_power;  
    }  
    pg_pin(VSS) {  
        voltage_name : VSS;  
        pg_type      : primary_ground;  
    }  
  
    cell_leakage_power : 15.154826;  
  
    leakage_power () {  
        when      : "!A1 & !A2";  
        value     : 10.171935;  
    }  
    leakage_power () {  
        when      : "!A1 & A2";  
        value     : 17.208604;  
    }  
    leakage_power () {  
        when      : "A1 & !A2";  
        value     : 12.417207;  
    }  
    leakage_power () {  
        when      : "A1 & A2";  
        value     : 20.821558;  
    }  
  
    pin (A1) {  
  
        direction      : input;  
        related_power_pin : "VDD";  
        related_ground_pin : "VSS";  
        capacitance     : 0.894757;  
        fall_capacitance : 0.830099;  
        rise_capacitance : 0.894757;  
    }  
}
```



Introduction of LIB Files

✓ The timing information in LIB files

- Cell rise and cell fall
- Rise transition and fall transition

```
lu_table_template (Timing_7_7) {  
    variable_1 : input_net_transition;  
    variable_2 : total_output_net_capacitance;  
    index_1 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
    index_2 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
}  
  
cell_rise(Timing_7_7) {  
    index_1 ("0.00231025,0.0112628,0.0426883,0.102700,0.196195,0.327379,0.500000");  
    index_2 ("0.365616,1.893040,3.786090,7.572170,15.144300,30.288700,60.577400");  
    values ("0.0630239,0.0787480,0.0961212,0.129093,0.193632,0.321810,0.577399", \  
            "0.0674459,0.0831711,0.100537,0.133506,0.198055,0.326241,0.581824", \  
            "0.0840800,0.0996979,0.116960,0.149818,0.214346,0.342599,0.598289", \  
            "0.111098,0.127055,0.144257,0.176866,0.241183,0.369419,0.625170", \  
            "0.137221,0.154429,0.171997,0.204249,0.268543,0.396458,0.652147", \  
            "0.158896,0.178441,0.197069,0.229757,0.293570,0.421467,0.676922", \  
            "0.174683,0.196972,0.217621,0.251499,0.315047,0.442340,0.697757");  
}  
  
fall_transition(Timing_7_7) {  
    index_1 ("0.00231025,0.0112628,0.0426883,0.102700,0.196195,0.327379,0.500000");  
    index_2 ("0.365616,1.893040,3.786090,7.572170,15.144300,30.288700,60.577400");  
    values ("0.0142179,0.0179662,0.0220337,0.0295478,0.0439247,0.0728803,0.133234", \  
            "0.0142202,0.0179650,0.0220353,0.0295435,0.0439265,0.0728882,0.133236", \  
            "0.0142401,0.0180012,0.0220653,0.0295620,0.0439313,0.0728830,0.133239", \  
            "0.0152201,0.0186282,0.0225258,0.0298637,0.0441023,0.0729622,0.133254", \  
            "0.0205299,0.0236322,0.0270182,0.0336077,0.0467309,0.0742211,0.133584", \  
            "0.0268061,0.0300308,0.0332223,0.0393239,0.0516523,0.0780366,0.135619", \  
            "0.0337402,0.0373263,0.0406222,0.0464392,0.0579323,0.0828138,0.138569");  
}
```

✓ What will happen if the value is out of range?



Introduction of LIB Files

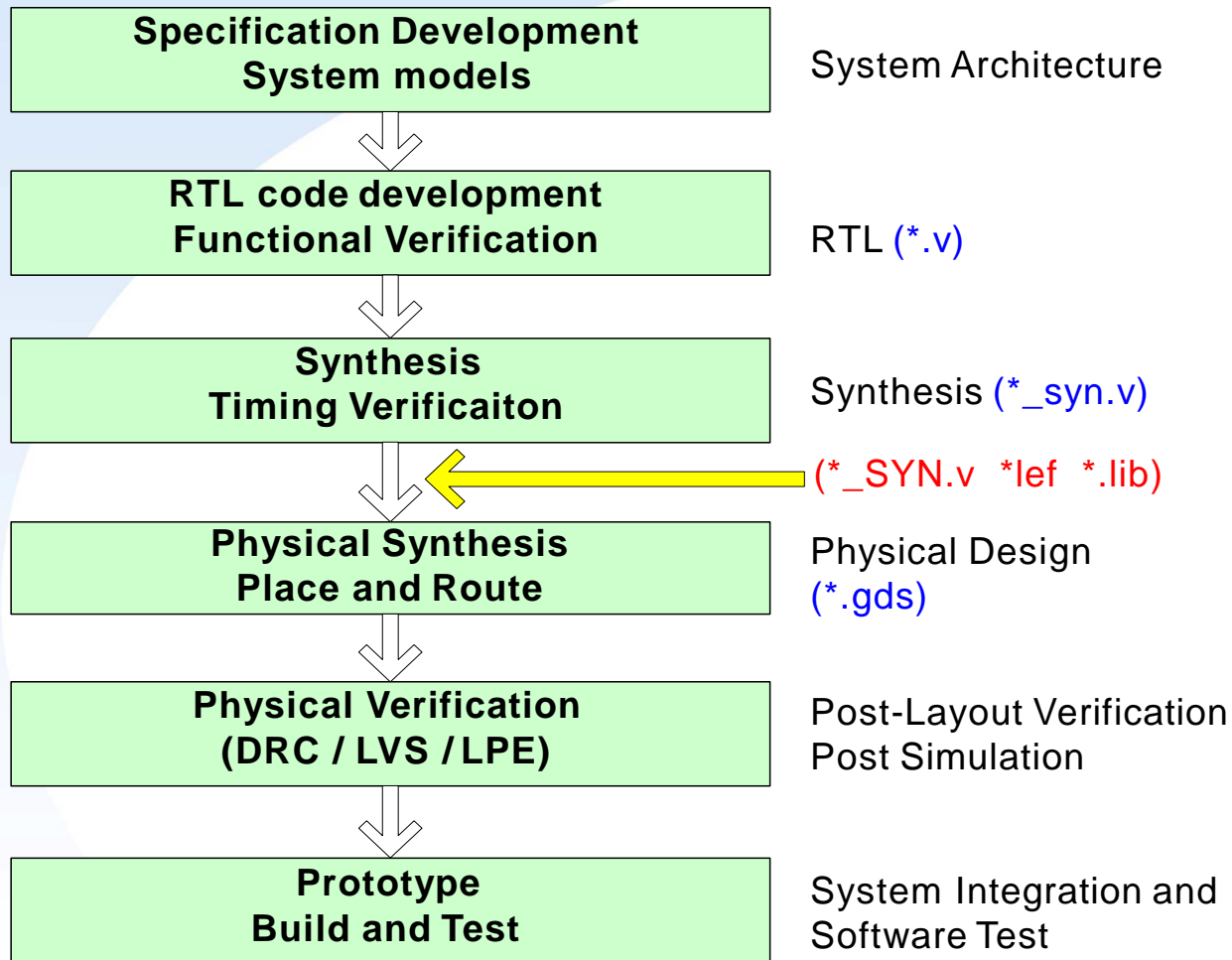
✓ The internal power information in LIB files

- Defined at each input pin
- Fall power and rise power

```
internal_power () {  
    related_pin : "A2";  
    fall_power(Power 7 7) {  
        index_1 ("0.00231025,0.0112628,0.0426883,0.102700,0.196195,0.327379,0.500000");  
        index_2 ("0.365616,3.767000,7.534000,15.068000,30.136000,60.272000,120.544000");  
        values ("4.457832,4.788072,5.028714,5.301675,5.524108,5.672181,5.743632", \  
            "4.446709,4.758343,4.987298,5.263321,5.489568,5.641210,5.704971", \  
            "4.371115,4.709637,4.935650,5.194484,5.422401,5.580039,5.645772", \  
            "4.391769,4.694037,4.926985,5.181429,5.415031,5.571611,5.645876", \  
            "4.493645,4.790255,5.021510,5.280662,5.522565,5.687319,5.762655", \  
            "4.700944,4.900496,5.100309,5.353765,5.684057,5.917852,6.013548", \  
            "5.077164,5.216876,5.371162,5.597479,5.913700,6.180814,6.371565");  
    }  
    rise_power(Power 7 7) {  
        index_1 ("0.00231025,0.0112628,0.0426883,0.102700,0.196195,0.327379,0.500000");  
        index_2 ("0.365616,3.767000,7.534000,15.068000,30.136000,60.272000,120.544000");  
        values ("3.050122,3.245451,3.348436,3.383495,3.410116,3.547264,3.476027", \  
            "3.013344,3.231263,3.325017,3.360157,3.483347,3.508233,3.573011", \  
            "2.986118,3.189128,3.265965,3.330565,3.347222,3.486957,3.419327", \  
            "2.955822,3.140775,3.227351,3.277662,3.243906,3.384560,3.460445", \  
            "3.009854,3.183423,3.252503,3.238903,3.235337,3.371907,3.452974", \  
            "3.163226,3.359162,3.417024,3.391950,3.391603,3.383149,3.467371", \  
            "3.406716,3.630032,3.686185,3.676410,3.630300,3.667160,3.604747");  
    }  
}
```



Cell-based Design Flow



Physical Verification

✓ Physical verification

- Verify DRC and LVS with Calibre
- Fix errors with Virtuoso manually
- Provide GDS2 file to foundry(UMC 、TSMC) for manufacturing



Appendix: Bonding pads insertion steps

- ✓ During the APR flow, save→ DEF→CHIP.def
- ✓ Execute "perl addbonding_v3.6.pl CHIP.def"
- ✓ Back to the Innovus, check the io.list
- ✓ When the APR flow finished, execute "source bondPads.cmd"
- ✓ There will be some cells on the IO PAD

